# STD105N10F7AG

## Automotive-grade N-channel 100 V, 6.8 mΩ typ., 80 A, STripFET™ F7 Power MOSFET in a DPAK package

Datasheet - production data

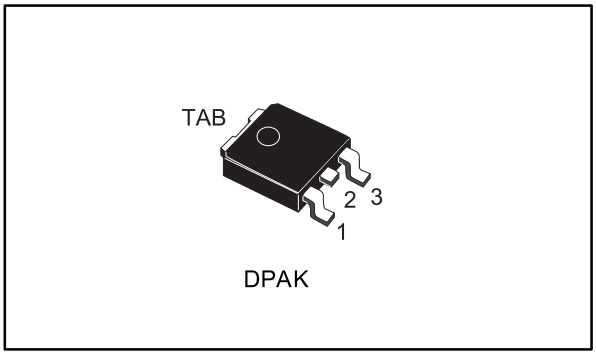
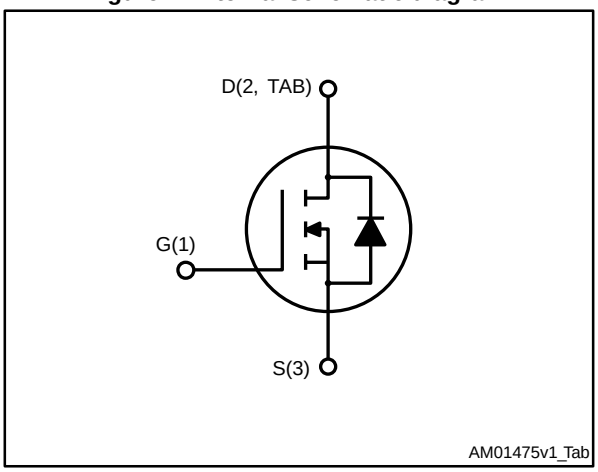



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ | $P_{TOT}$ |
|---|---|---|---|---|
| STD105N10F7AG | 100 V | 8 mΩ | 80 A | 120 W |

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low $C_{rss}/C_{iss}$ ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STD105N10F7AG | 105N10F7 | DPAK | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 100 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 80 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 62 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 320 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 120 | W |
| $T_{stg}$ | Storage temperature range | -55 to 175 | °C |
| $T_J$ | Operation junction temperature range | | |

**Notes:**

(1)Pulse width limited by safe operating area.

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 1.25 | °C/W |
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 50 | |

**Notes:**

(1)When mounted on FR-4 board of 1 inch², 2oz Cu.

**Table 4: Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $E_{AS}$ | Single pulse avalanche energy<br>$T_J$ = 25 °C, L = 3.5 mH, $I_{AS}$ = 15 A, $V_{DD}$ = 50 V, $V_{GS}$ = 10 V | 400 | mJ |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified)

**Table 5: On/Off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS}$ = 0) | $I_D$ = 250 µA | 100 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 100 V | | | 1 | µA |
| | | $V_{DS}$ = 100 V, $T_C$ = 125 °C (1) | | | 100 | µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 20 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$ , $I_D$ = 250 µA | 2.5 | | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$= 40 A | | 6.8 | 8 | mΩ |

**Notes:**

(1)Defined by design, not subject to production test.

**Table 6: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 50 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 4369 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 823 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 36 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 50 V, $I_D$ = 80 A, $V_{GS}$ = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*) | - | 61 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 26 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 13 | - | nC |

**Table 7: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 50 V, $I_D$ = 40 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*) | - | 27 | - | ns |
| $t_r$ | Rise time | | - | 40 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 46 | - | ns |
| $t_f$ | Fall time | | - | 15 | - | ns |

**Table 8: Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 80 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 320 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 80 A, $V_{GS}$ = 0 V | - | | 1.2 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 80 A, di/dt = 100 A/µs<br>$V_{DD}$ = 80 V, $T_j$ = 150 °C | - | 77 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 146 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 4 | | A |

**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.

## 2.1 Electrical characteristics (curves)

**Figure 2: Safe operating area**

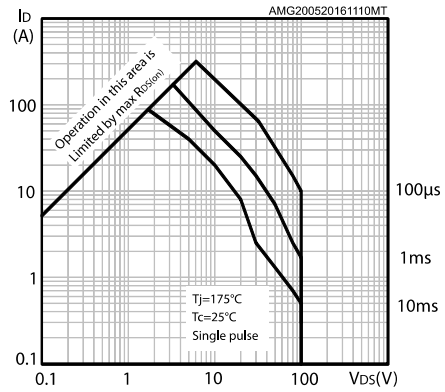



**Figure 3: Thermal impedance**

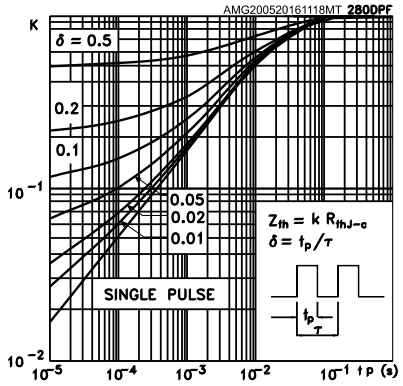



**Figure 4: Output characteristics**

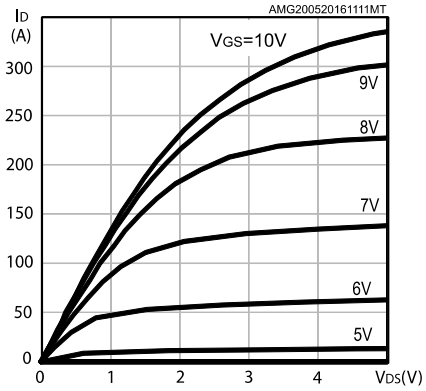



**Figure 5: Transfer characteristics**

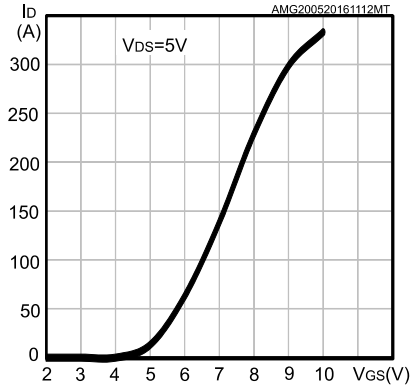



**Figure 6: Normalized $V_{(BR)DSS}$ vs temperature**

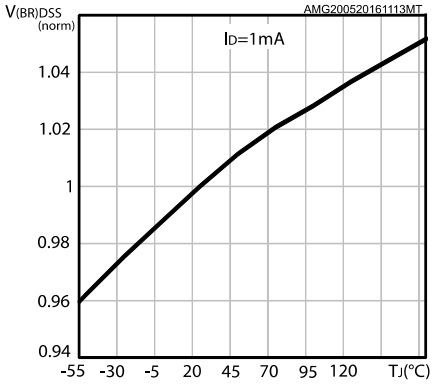



**Figure 7: Static drain-source on-resistance**

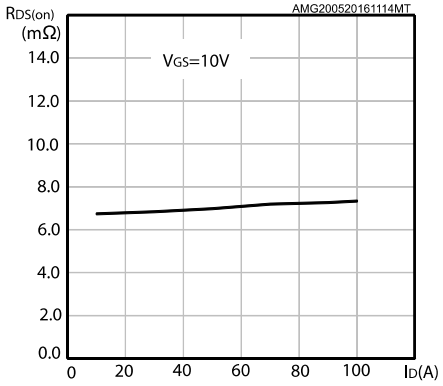


**Figure 8: Gate charge vs gate-source voltage**

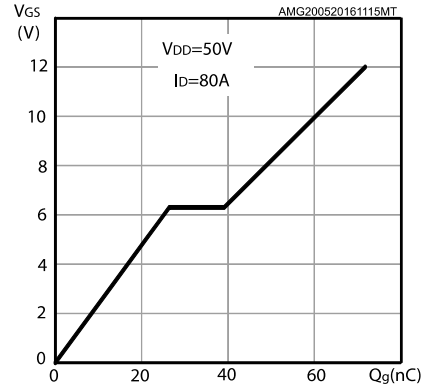



**Figure 9: Capacitance variations**

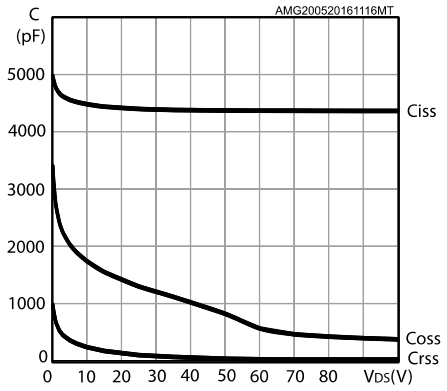



**Figure 10: Normalized gate threshold voltage vs temperature**

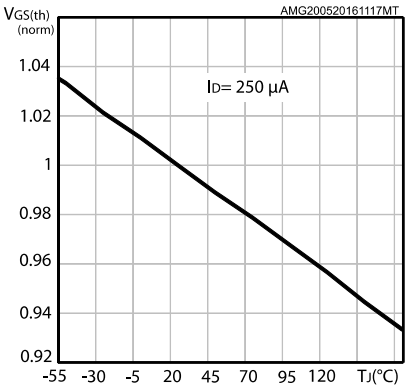



**Figure 11: Normalized on-resistance vs temperature**

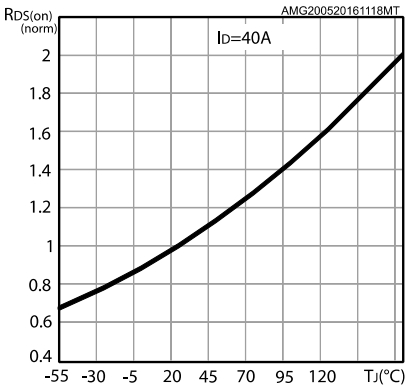
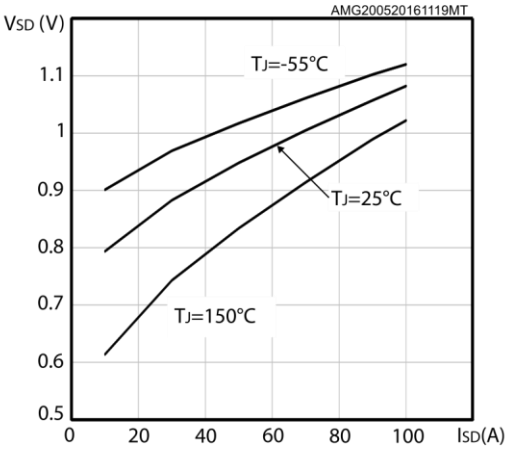



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**

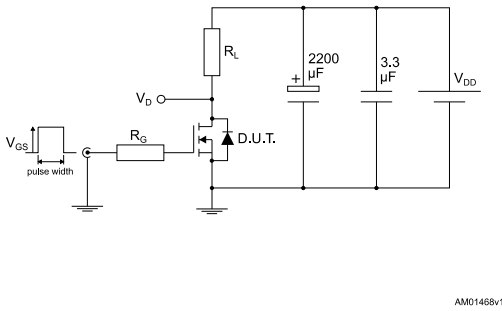



**Figure 14: Test circuit for gate charge behavior**

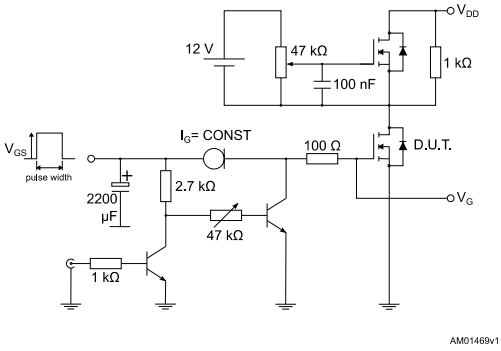



**Figure 15: Test circuit for inductive load switching and diode recovery times**

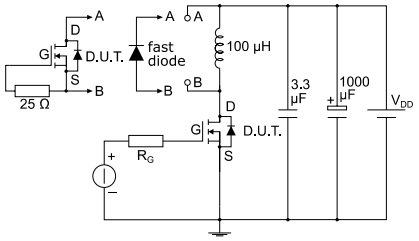



**Figure 16: Unclamped inductive load test circuit**

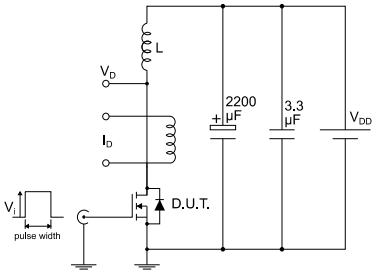



**Figure 17: Unclamped inductive waveform**

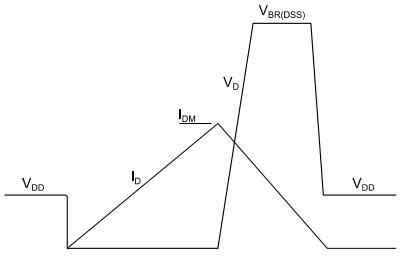
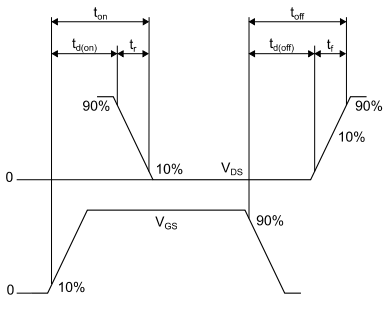



**Figure 18: Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

**Figure 19: DPAK (TO-252) type A2 package outline**

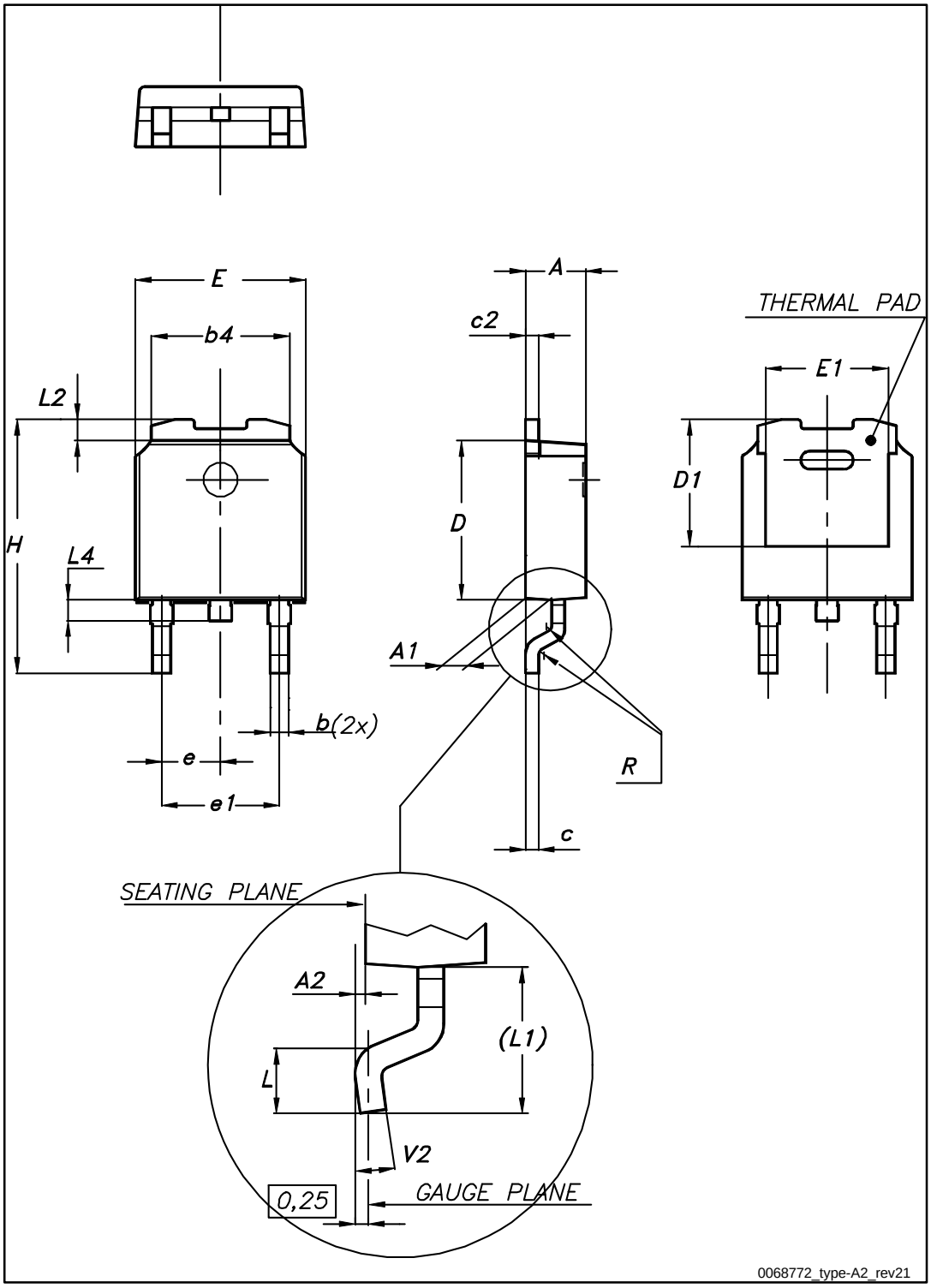
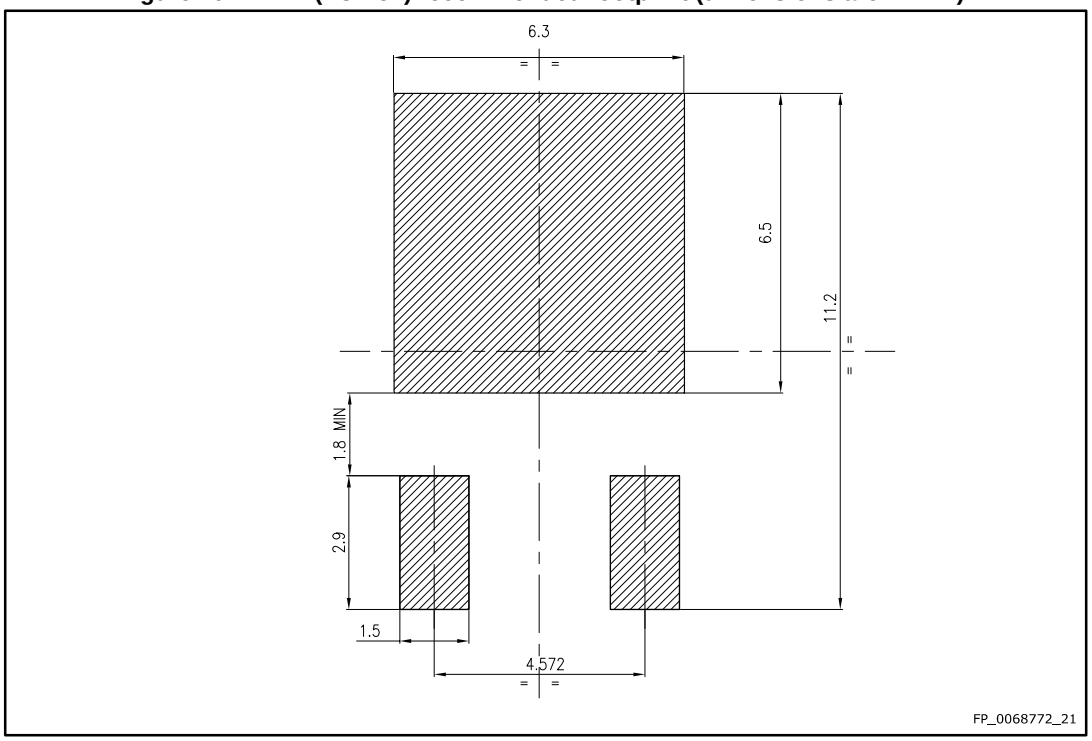


Table 9: DPAK (TO-252) type A2 mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.16 | 2.28 | 2.40 |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

**Figure 20: DPAK (TO-252) recommended footprint (dimensions are in mm)**



# 5 Revision history

Table 10: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 23-Oct-2014 | 1 | First release. |
| 30-Oct-2014 | 2 | Document status promoted from preliminary to production data. |
| 20-May-2016 | 3 | Updated Section 4.1: "DPAK (TO-252) type A2 package information".<br>Minor text changes. |
| 03-Jun-2016 | 4 | Updated title and features in cover page.<br>Updated *Table 5: "On/Off states"*.<br>Minor text changes. |

## IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

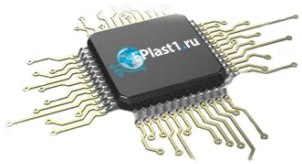
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

**Телефон:** 8 (812) 309 58 32 (многоканальный)
**Факс:** 8 (812) 320-02-42
**Электронная почта:** org@eplast1.ru
**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.