

# **TVP5145PFP**

**NTSC/PAL/SECAM/Component Digital Video  
Decoder With Macrovision™ Detection**

## *Data Manual*

# Contents

| <i>Section</i> | <i>Title</i>                                                              | <i>Page</i> |
|----------------|---------------------------------------------------------------------------|-------------|
| <b>1</b>       | <b>Introduction .....</b>                                                 | <b>1-1</b>  |
| 1.1            | Features .....                                                            | 1-1         |
| 1.2            | Applications .....                                                        | 1-2         |
| 1.3            | Related Products .....                                                    | 1-3         |
| 1.4            | Ordering Information .....                                                | 1-3         |
| 1.5            | Functional Block Diagram .....                                            | 1-4         |
| 1.6            | Terminal Assignments .....                                                | 1-5         |
| 1.7            | Terminal Functions .....                                                  | 1-6         |
| 1.8            | Strapping Terminals Description .....                                     | 1-8         |
| <b>2</b>       | <b>Functional Description .....</b>                                       | <b>2-1</b>  |
| 2.1            | Analog Video Processing and A/D Converters .....                          | 2-1         |
| 2.1.1          | Video Input Selection .....                                               | 2-2         |
| 2.1.2          | Analog Input Clamping and Automatic Gain Control<br>Circuits .....        | 2-2         |
| 2.1.3          | A/D Converters .....                                                      | 2-2         |
| 2.2            | Digital Processing .....                                                  | 2-2         |
| 2.2.1          | Digital Input Selection .....                                             | 2-3         |
| 2.2.2          | Decimation Filter .....                                                   | 2-4         |
| 2.2.3          | Y/C Separation .....                                                      | 2-4         |
| 2.2.3.1        | Color Low-Pass Filter .....                                               | 2-5         |
| 2.2.3.2        | Adaptive Comb Filter .....                                                | 2-6         |
| 2.2.4          | Luminance Processing .....                                                | 2-8         |
| 2.2.5          | Chrominance Processing .....                                              | 2-9         |
| 2.2.6          | SECAM Processing .....                                                    | 2-10        |
| 2.3            | Clock Circuits .....                                                      | 2-12        |
| 2.4            | Genlock Control (GLCO) and Real-Time Control (RTC) .....                  | 2-12        |
| 2.4.1          | GLCO Mode .....                                                           | 2-12        |
| 2.4.2          | RTC Mode .....                                                            | 2-13        |
| 2.5            | Video Output Format .....                                                 | 2-13        |
| 2.5.1          | Sampling Frequencies and Patterns .....                                   | 2-13        |
| 2.5.2          | Video Port 20-/16-Bit 4:2:2 Output Format Timing .....                    | 2-14        |
| 2.5.3          | Video Port 10-/8-Bit 4:2:2 and ITU-R BT.656 Output<br>Format Timing ..... | 2-15        |
| 2.6            | Synchronization Signals .....                                             | 2-15        |
| 2.6.1          | Separate Syncs .....                                                      | 2-15        |
| 2.6.2          | AVID Cropping .....                                                       | 2-17        |
| 2.6.3          | Embedded Syncs .....                                                      | 2-18        |
| 2.7            | Host Interface .....                                                      | 2-19        |

|         |                                                   |      |
|---------|---------------------------------------------------|------|
| 2.7.1   | I2C Host Port Select .....                        | 2-19 |
| 2.7.1.1 | I2C Write Operation .....                         | 2-20 |
| 2.7.1.2 | I2C Read Operation .....                          | 2-20 |
| 2.7.1.3 | Read Phase 1 .....                                | 2-21 |
| 2.7.1.4 | Read Phase 2 .....                                | 2-21 |
| 2.7.1.5 | Microprocessor Start by I2C .....                 | 2-21 |
| 2.7.1.6 | I2C Timing Requirements .....                     | 2-22 |
| 2.7.2   | Parallel Host Interface (PHI) .....               | 2-22 |
| 2.7.2.1 | PHI Register Mapping .....                        | 2-23 |
| 2.7.2.2 | PHI Read/Write Operation .....                    | 2-23 |
| 2.7.2.3 | Latency .....                                     | 2-24 |
| 2.7.2.4 | VBI FIFO .....                                    | 2-24 |
| 2.7.2.5 | Interrupt Status Register A .....                 | 2-24 |
| 2.7.2.6 | Microprocessor Start by PHI .....                 | 2-24 |
| 2.8     | VBI Data Processor .....                          | 2-24 |
| 2.8.1   | VBI FIFO and Ancillary Data in Video Stream ..... | 2-26 |
| 2.9     | Raw Video Data Output .....                       | 2-27 |
| 2.10    | Reset and Initialization .....                    | 2-27 |
| 2.11    | Internal Control Registers .....                  | 2-27 |
| 2.12    | Register Definitions .....                        | 2-30 |
| 2.12.1  | Video Input Source Selection #1 Register .....    | 2-30 |
| 2.12.2  | Analog Channel Controls Register .....            | 2-31 |
| 2.12.3  | Operation Mode Controls Register .....            | 2-32 |
| 2.12.4  | Miscellaneous Control Register .....              | 2-33 |
| 2.12.5  | Color Killer Threshold Control Register .....     | 2-34 |
| 2.12.6  | Luminance Processing Control #1 Register .....    | 2-34 |
| 2.12.7  | Luminance Processing Control #2 Register .....    | 2-35 |
| 2.12.8  | Brightness Control Register .....                 | 2-35 |
| 2.12.9  | Color Saturation Control Register .....           | 2-35 |
| 2.12.10 | Hue Control Register .....                        | 2-35 |
| 2.12.11 | Contrast Control Register .....                   | 2-36 |
| 2.12.12 | Outputs and Data Rates Select Register .....      | 2-36 |
| 2.12.13 | Luminance Control #3 Register .....               | 2-37 |
| 2.12.14 | AVID Start Pixel MSB .....                        | 2-37 |
| 2.12.15 | AVID Start Pixel LSB .....                        | 2-37 |
| 2.12.16 | AVID Stop Pixel MSB .....                         | 2-37 |
| 2.12.17 | AVID Stop Pixel LSB .....                         | 2-38 |
| 2.12.18 | GLCO and RTC Register .....                       | 2-38 |
| 2.12.19 | Horizontal Sync (HSYN) Start Register .....       | 2-38 |
| 2.12.20 | Vertical Blanking Start Register .....            | 2-39 |
| 2.12.21 | Vertical Blanking Stop Register .....             | 2-39 |
| 2.12.22 | Chrominance Control #1 Register .....             | 2-40 |
| 2.12.23 | Chrominance Control #2 Register .....             | 2-41 |
| 2.12.24 | Interrupt Reset Register B .....                  | 2-41 |

|          |                                                |            |
|----------|------------------------------------------------|------------|
| 2.12.25  | Interrupt Enable Register B .....              | 2-42       |
| 2.12.26  | Interrupt Configuration Register B .....       | 2-43       |
| 2.12.27  | Video Input Source Selection #2 Register ..... | 2-43       |
| 2.12.28  | Crystal Frequency Register .....               | 2-44       |
| 2.12.29  | Video Standard Register .....                  | 2-44       |
| 2.12.30  | Microprocessor Start Register .....            | 2-44       |
| 2.12.31  | Major ROM Version Register .....               | 2-44       |
| 2.12.32  | Status Register #1 .....                       | 2-45       |
| 2.12.33  | Status Register #2 .....                       | 2-46       |
| 2.12.34  | Status Register #3 .....                       | 2-46       |
| 2.12.35  | Status Register #4 .....                       | 2-46       |
| 2.12.36  | Interrupt Status Register B .....              | 2-47       |
| 2.12.37  | Interrupt Active Register B .....              | 2-47       |
| 2.12.38  | Minor ROM Version Register .....               | 2-48       |
| 2.12.39  | Status Register #5 .....                       | 2-48       |
| 2.12.40  | Vertical Line Count MSB Register .....         | 2-48       |
| 2.12.41  | Vertical Line Count LSB Register .....         | 2-49       |
| 2.12.42  | Analog Die ID Register .....                   | 2-49       |
| 2.12.43  | Digital Die ID Register .....                  | 2-49       |
| 2.12.44  | Closed Caption Data Registers .....            | 2-49       |
| 2.12.45  | WSS Data Registers .....                       | 2-50       |
| 2.12.46  | VPS Data Registers .....                       | 2-51       |
| 2.12.47  | VITC Data Registers .....                      | 2-51       |
| 2.12.48  | VBI FIFO Read Data Register .....              | 2-51       |
| 2.12.49  | Teletext Filter and Mask Registers .....       | 2-52       |
| 2.12.50  | Teletext Filter Control Register .....         | 2-53       |
| 2.12.51  | Interrupt Status Register A .....              | 2-55       |
| 2.12.52  | Interrupt Enable Register A .....              | 2-56       |
| 2.12.53  | Interrupt Configuration Register A .....       | 2-57       |
| 2.12.54  | VDP Configuration RAM Register .....           | 2-57       |
| 2.12.55  | VDP Status Register .....                      | 2-59       |
| 2.12.56  | FIFO Word Count Register .....                 | 2-59       |
| 2.12.57  | FIFO Interrupt Threshold Register .....        | 2-60       |
| 2.12.58  | FIFO Reset Register .....                      | 2-60       |
| 2.12.59  | Line Number Interrupt Register .....           | 2-60       |
| 2.12.60  | Pixel Alignment Registers .....                | 2-60       |
| 2.12.61  | FIFO Output Control Register .....             | 2-61       |
| 2.12.62  | VDP Clock Register .....                       | 2-61       |
| 2.12.63  | Full Field Enable Register .....               | 2-61       |
| 2.12.64  | Line Mode Registers .....                      | 2-62       |
| 2.12.65  | Full Field Mode Register .....                 | 2-63       |
| <b>3</b> | <b>Electrical Specifications .....</b>         | <b>3-1</b> |
| 3.1      | Absolute Maximum Ratings .....                 | 3-1        |
| 3.2      | Recommended Operating Conditions .....         | 3-1        |

|          |                                            |            |
|----------|--------------------------------------------|------------|
| 3.2.1    | Crystal Specifications .....               | 3-1        |
| 3.3      | Electrical Characteristics .....           | 3-2        |
| 3.3.1    | DC Electrical Characteristics .....        | 3-2        |
| 3.3.2    | Analog Processing and A/D Converters ..... | 3-2        |
| 3.3.3    | Timing .....                               | 3-3        |
| 3.3.3.1  | Clocks, Video Data, Sync Timing .....      | 3-3        |
| 3.3.3.2  | I <sup>2</sup> C Host Port Timing .....    | 3-4        |
| 3.3.3.3  | PHI Host Port Timing (Mode A) .....        | 3-5        |
| 3.3.3.4  | PHI Host Port Timing (Mode B) .....        | 3-6        |
| 3.3.3.5  | PHI Host Port Timing (Mode C) .....        | 3-7        |
| <b>4</b> | <b>Application Information .....</b>       | <b>4-1</b> |
| 4.1      | Application Example .....                  | 4-1        |
| 4.2      | Designing With PowerPAD .....              | 4-2        |
| <b>5</b> | <b>Mechanical Data .....</b>               | <b>5-1</b> |

## List of Illustrations

| <i>Figure</i> | <i>Title</i>                                                                                     | <i>Page</i> |
|---------------|--------------------------------------------------------------------------------------------------|-------------|
| 1–1           | Functional Block Diagram .....                                                                   | 1–4         |
| 2–1           | Analog Video Processors and A/D Converters .....                                                 | 2–1         |
| 2–2           | Digital Video Signal Processing Block Diagram .....                                              | 2–3         |
| 2–3           | Digital Input Multiplexer .....                                                                  | 2–4         |
| 2–4           | Decimation Filter Frequency Response .....                                                       | 2–4         |
| 2–5           | Y/C Separation Block Diagram .....                                                               | 2–5         |
| 2–6           | Color Low-Pass Filter Frequency Response .....                                                   | 2–6         |
| 2–7           | Color Low-Pass Filter With Notch Filter Frequency Response,<br>NTSC Square Pixel Sampling .....  | 2–6         |
| 2–8           | Color Low-Pass Filter With Notch Filter Characteristics,<br>NTSC/PAL ITU-R BT.601 Sampling ..... | 2–6         |
| 2–9           | Color Low-Pass Filter With Notch Filter Characteristics,<br>PAL Square Pixel Sampling .....      | 2–6         |
| 2–10          | Comb Filters Frequency Response .....                                                            | 2–7         |
| 2–11          | Chroma Trap Filter Frequency Response,<br>NTSC Square Pixel Sampling .....                       | 2–7         |
| 2–12          | Chroma Trap Filter Frequency Response,<br>NTSC ITU-R BT.601 Sampling .....                       | 2–7         |
| 2–13          | Chroma Trap Filter Frequency Response,<br>PAL ITU-R BT.601 Sampling .....                        | 2–7         |
| 2–14          | Chroma Trap Filter Frequency Response,<br>PAL Square Pixel Sampling .....                        | 2–8         |
| 2–15          | Luminance Edge-Enhancer Peaking Block Diagram .....                                              | 2–8         |
| 2–16          | Peaking Filter Response, NTSC Square Pixel Sampling .....                                        | 2–9         |
| 2–17          | Peaking Filter Response,<br>NTSC/PAL ITU-R BT.601 Sampling .....                                 | 2–9         |
| 2–18          | Peaking Filter Response, PAL Square Pixel Sampling .....                                         | 2–9         |
| 2–19          | SECAM Data Path .....                                                                            | 2–10        |
| 2–20          | SECAM Filter Frequency Responses and FM Demodulator<br>Characteristic .....                      | 2–11        |
| 2–21          | Reference Clock Configurations .....                                                             | 2–12        |
| 2–22          | GLCO Timing .....                                                                                | 2–13        |
| 2–23          | RTC Timing .....                                                                                 | 2–13        |
| 2–24          | 4:2:2 Sampling .....                                                                             | 2–14        |
| 2–25          | 20-/16-Bit 4:2:2 Output Format .....                                                             | 2–14        |

|      |                                           |      |
|------|-------------------------------------------|------|
| 2-26 | 10-/8-Bit 4:2:2 Output Format .....       | 2-15 |
| 2-27 | Vertical Synchronization Signals .....    | 2-16 |
| 2-28 | Horizontal Synchronization Signals .....  | 2-17 |
| 2-29 | AVID Application .....                    | 2-18 |
| 2-30 | PHI Address Register Map .....            | 2-23 |
| 2-31 | Video Input Source Selection .....        | 2-30 |
| 2-32 | Teletext Filter Function .....            | 2-54 |
| 3-1  | Clocks, Video Data, and Sync Timing ..... | 3-3  |
| 3-2  | I <sup>2</sup> C Host Port Timing .....   | 3-4  |
| 3-3  | PHI Host Port Timing (Mode A) .....       | 3-5  |
| 3-4  | PHI Host Port Timing (Mode B) .....       | 3-6  |
| 3-5  | PHI Host Port Timing (Mode C) .....       | 3-7  |
| 4-1  | Application Example .....                 | 4-1  |

## List of Tables

| <i>Table</i> | <i>Title</i>                                                    | <i>Page</i> |
|--------------|-----------------------------------------------------------------|-------------|
| 1-1          | Terminal Functions .....                                        | 1-6         |
| 1-2          | Strapping Terminals .....                                       | 1-8         |
| 2-1          | Summary of Line Frequencies, Data Rates, and Pixel Counts ..... | 2-14        |
| 2-2          | EAV and SAV Sequence .....                                      | 2-19        |
| 2-3          | Host Port Select .....                                          | 2-19        |
| 2-4          | I <sup>2</sup> C Host Port Terminal Description .....           | 2-19        |
| 2-5          | PHI Host Port Terminal Description .....                        | 2-22        |
| 2-6          | Data Types Supported by the VDP .....                           | 2-25        |
| 2-7          | Ancillary Data Format and Sequence .....                        | 2-26        |
| 2-8          | Reset Sequence .....                                            | 2-27        |
| 2-9          | Registers Summary .....                                         | 2-28        |
| 2-10         | Analog Channel and Video Mode Selection .....                   | 2-31        |
| 2-11         | Digital Output Control .....                                    | 2-33        |
| 2-12         | VBI Configuration RAM .....                                     | 2-58        |

# 1 Introduction

The TVP5145 device is a high-quality, single-chip digital video decoder that converts baseband analog NTSC, PAL, and SECAM video into digital component video. Analog component, composite, and S-video inputs are supported. The TVP5145 device includes two 10-bit oversampling A/D converters. Line-locked sampling is square-pixel or ITU-R BT.601 (27 MHz). The output formats can be 20-/16-bit or 10-/8-bit 4:2:2, or 10-/8-bit ITU-R BT.656 with embedded synchronization. The TVP5145 device utilizes Texas Instruments' patented technology for locking to weak, noisy, or unstable signals, and a chroma frequency control output is generated for synchronizing downstream video encoders.

Complementary three-line or four-line adaptive comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts; a chroma trap filter is also available. Video characteristics including brightness, hue, contrast, and saturation may be programmed using one of four supported host port interfaces: I<sup>2</sup>C and three parallel host interfaces (PHI). The TVP5145 device generates synchronization, blanking, field, lock, and clock signals in addition to digital video outputs.

The TVP5145 device includes methods for advanced vertical blanking interval (VBI) data retrieval. The VBI data processor (VDP) slices, parses, and performs error checking on teletext, closed caption, and other data in several formats. A built-in FIFO stores up to 11 lines of teletext data, and with proper host port synchronization, full-screen teletext retrieval is possible. The TVP5145 device can pass through oversampled raw composite data for host-based software VBI processing.

The TVP5145 device utilizes an internal ROM to contain the program code. Therefore, it does not require microcode download to operate.

The TVP5145 device detects and decodes copy-protected input signals according to the Macrovision™ standard.

The main blocks of the TVP5145 device include:

- Dual A/D converters with analog processors
- Y/C separation by 2D adaptive comb or chroma trap filter
- Chrominance processor
- Luminance processor
- Component processor
- Clock/timing processor and power-down control
- Output formatter
- Host port interface
- VBI data processor
- Macrovision™ 7.1 detection for composite, S-video, and component video

## 1.1 Features

- Accepts NTSC (M, Japan, 4.43), PAL (B, D, G, H, I, M, N, Nc) and SECAM (B, D, G, K, K1, L) composite video, S-video
- Accepts analog component YPbPr video
- Six analog video inputs for up to two component inputs or six composite inputs, or two S-video inputs and two composite inputs
- Two fully differential CMOS analog preprocessing channels with clamping and automatic gain control (AGC) for best S/N performance
- Dual high-speed oversampling 10-bit A/D converters
- Patented architecture for locking to weak, noisy, or unstable signals

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- Single 14.31818-MHz or 27-MHz reference crystal for all standards
- Line-locked clock and sampling
- Automatic detect and switching between NTSC, PAL, and SECAM standards
- Programmable output data rates:
  - 12.2727-MHz square-pixel (NTSC)
  - 14.75-MHz square-pixel (PAL/SECAM)
  - 13.5-MHz ITU-R BT.601 (NTSC, PAL, and SECAM)
- Complementary 4-line (3-H delay) adaptive comb filters for both cross-luminance and cross-chrominance noise reduction
- Subcarrier Genlock/real-time control (RTC) output for synchronizing the color subcarrier of an external encoder
- Active video cropping
- Standard programmable video output formats:
  - 20-/16-bit 4:2:2 YCbCr
  - 10-/8-bit 4:2:2 YCbCr
  - ITU-R BT.656 10-/8-bit 4:2:2 with embedded syncs
- Advanced programmable video output formats:
  - Oversampled raw VBI data during active video
  - Sliced VBI data during vertical blanking or active video
- Multiple VBI data formats supported:
  - World standard teletext (WST), North American broadcast text system (NABTS), closed-caption (CC), and extended data service (XDS)
  - Wide screen signaling (WSS), video program system (VPS), vertical interval time code (VITC), and a custom configuration mode that allows the user to program the VDP for unique VBI data signals
- Macrovision™ copy protection detection
- Programmable host port options including I<sup>2</sup>C and PHI (3 modes)
- Brightness, contrast, saturation, and hue control through host port
- Internal program ROM
- 5-V tolerant digital I/O ports
- 80-terminal TQFP package

## 1.2 Applications

- Digital television
- Digital image processing
- Video conferencing
- Multimedia
- Digital video
- Desktop video

- Video capture
- Video editing
- Professional video applications
- Security applications

### 1.3 Related Products

- TVP5040 NTSC/PAL 2x10 bit Digital Video Decoder With Macrovision, Literature Number SLAS257D
- TVP5031 NTSC/PAL 9-bit Digital Video Decoder With Macrovision, Literature Number SLAS267C
- TVP6000 NTSC/PAL Digital Video Encoder, Literature Number SLAS184

### 1.4 Ordering Information

| $T_A$       | PACKAGED DEVICES                        |
|-------------|-----------------------------------------|
|             | 80-TERMINAL PLASTIC FLAT-PACK PowerPAD™ |
| 0°C to 70°C | TVP5145PFP                              |

PowerPAD is a trademark of Texas Instruments.

1.5 Functional Block Diagram

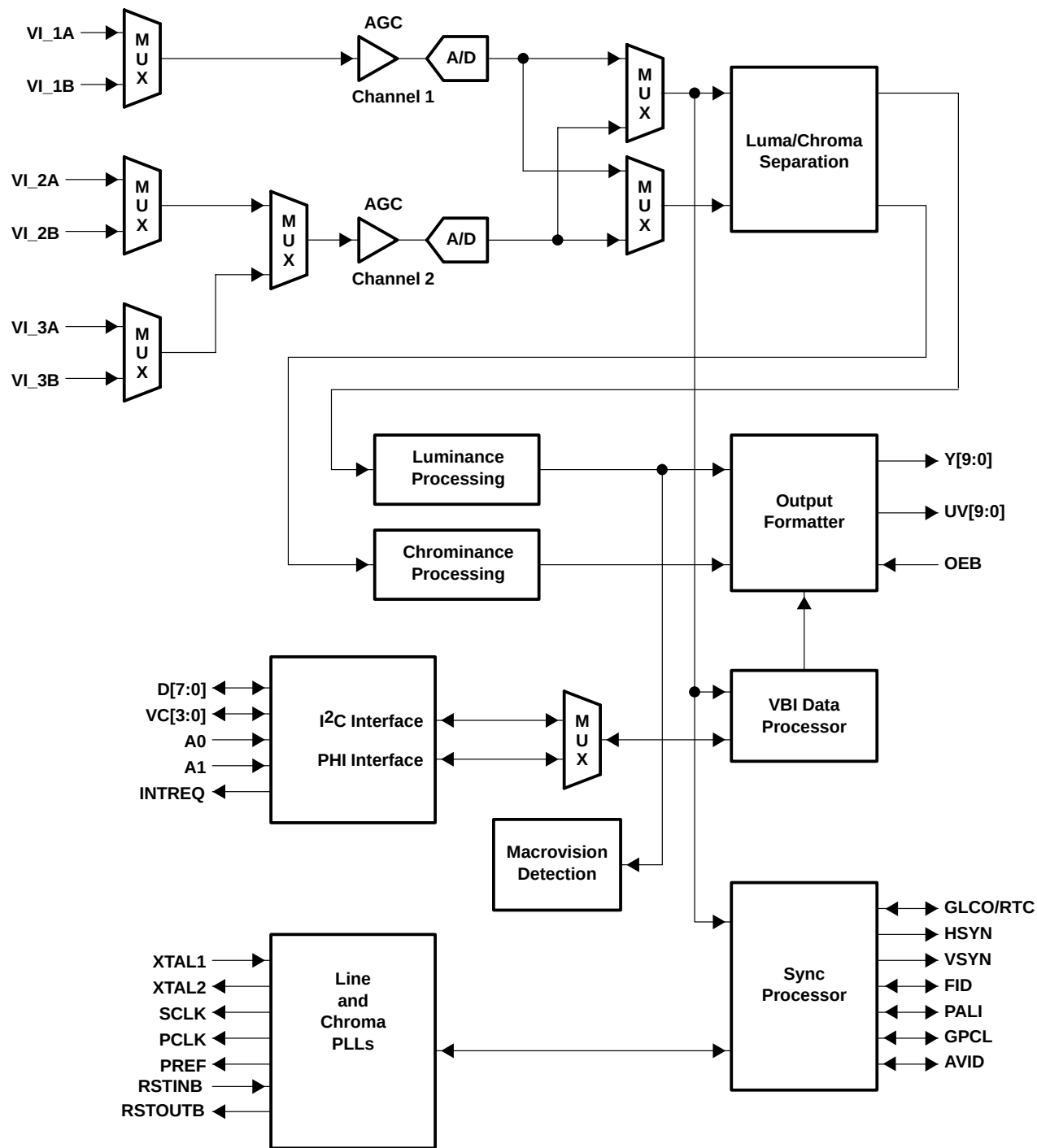
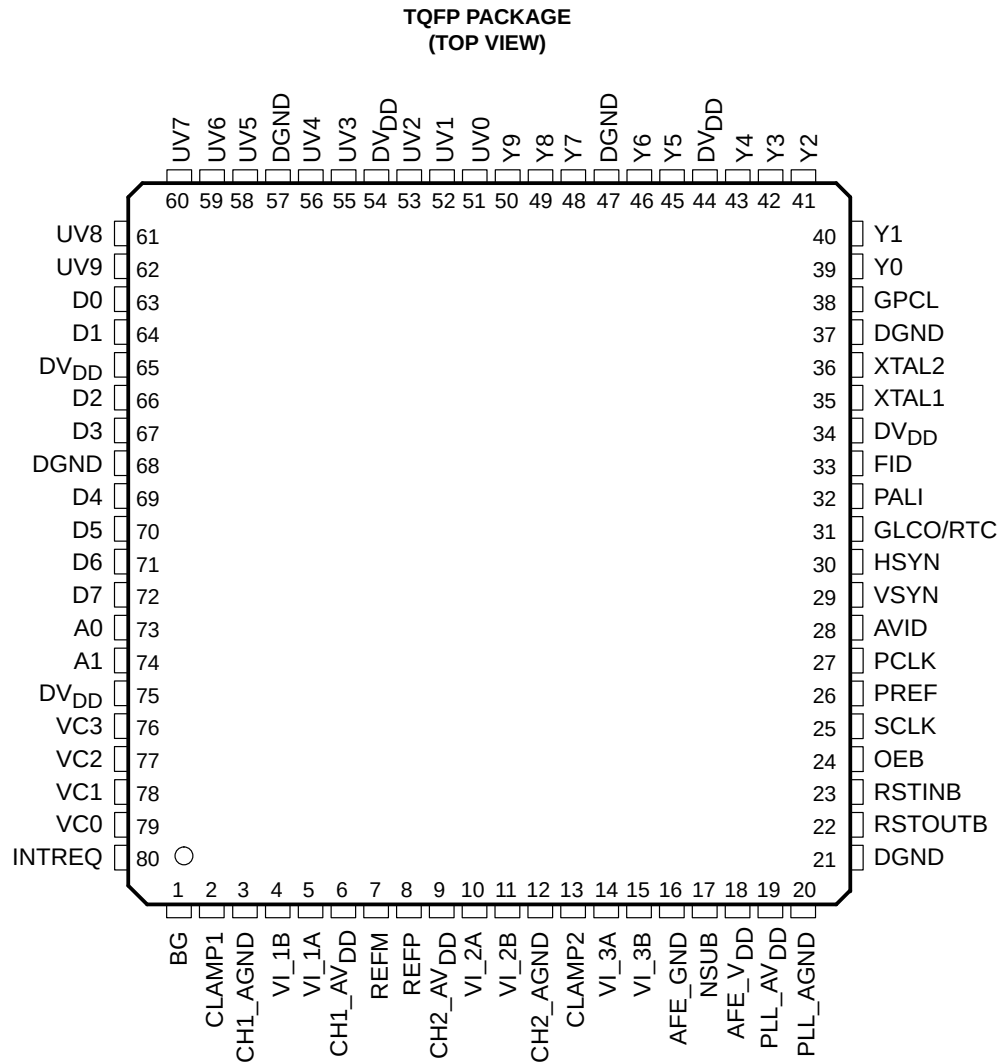


Figure 1–1. Functional Block Diagram

## 1.6 Terminal Assignments



## 1.7 Terminal Functions

**Table 1–1. Terminal Functions**

| TERMINAL             |                                                    | I/O | DESCRIPTION                                                                                                                                                                                                                                                                    |
|----------------------|----------------------------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                 | NUMBER                                             |     |                                                                                                                                                                                                                                                                                |
| Analog Video         |                                                    |     |                                                                                                                                                                                                                                                                                |
| VI_1A                | 5                                                  | I   | Analog video inputs. Up to six composite inputs, two component inputs, two S-video inputs or a combination thereof. The inputs must be ac-coupled. The recommended coupling is 0.1 μF to 1 μF. If inputs are not used, they may be tied to AFE_GND through a 0.1-μF capacitor. |
| VI_1B                | 4                                                  |     |                                                                                                                                                                                                                                                                                |
| VI_2A                | 10                                                 |     |                                                                                                                                                                                                                                                                                |
| VI_2B                | 11                                                 |     |                                                                                                                                                                                                                                                                                |
| VI_3A                | 14                                                 |     |                                                                                                                                                                                                                                                                                |
| VI_3B                | 15                                                 |     |                                                                                                                                                                                                                                                                                |
| Clock Signals        |                                                    |     |                                                                                                                                                                                                                                                                                |
| PCLK                 | 27                                                 | O   | Line-locked pixel clock output. The frequency corresponds to the video standard (see Table 2–1).                                                                                                                                                                               |
| PREF                 | 26                                                 | O   | Line-locked clock phase reference signal output. This signal qualifies clock edges when SCLK clocks data that is changing at the pixel clock rate. It may also be used as a stand-alone pixel clock.                                                                           |
| SCLK                 | 25                                                 | O   | Line-locked system clock output with twice the frequency of the pixel clock (PCLK) (see Table 2–1).                                                                                                                                                                            |
| XTAL1                | 35                                                 | I   | External clock reference input.                                                                                                                                                                                                                                                |
| XTAL2                | 36                                                 | O   | External clock reference output (see Section 2.3, <i>Clock Circuits</i> , for configurations)                                                                                                                                                                                  |
| Digital Video        |                                                    |     |                                                                                                                                                                                                                                                                                |
| UV[9:0] <sup>†</sup> | 62, 61,<br>60, 59,<br>58, 56,<br>55, 53,<br>52, 51 | O   | 10-bit digital chrominance outputs. These terminals may also be configured to output the data from the channel 2 A/D converter. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected.                                                          |
| Y[9:0]               | 50, 49,<br>48, 46,<br>45, 43,<br>42, 41,<br>40, 39 | O   | 10-bit digital luminance outputs, or 10-bit multiplexed luminance and chrominance outputs. These terminals may also be configured to output the data from the channel 1 A/D converter. For the 8-bit mode, the two LSBs are ignored. Unused outputs can be left unconnected.   |
| Host Port-Bus        |                                                    |     |                                                                                                                                                                                                                                                                                |
| A[1:0]               | 74, 73                                             | I   | PHI address port, unused inputs can be left unconnected                                                                                                                                                                                                                        |
| D[7:0]               | 72, 71,<br>70, 69,<br>67, 66,<br>64, 63            | I/O | PHI data port-bits [7:0] (10-kΩ pullup resistors are required for these terminals, if used) Unused outputs can be left unconnected.                                                                                                                                            |
| INTREQ               | 80                                                 | O   | Interrupt request output (10-kΩ pullup resistor is required, if used)                                                                                                                                                                                                          |
| VC0                  | 79                                                 | I/O | PHI mode: Acknowledgement or ready signal<br>I <sup>2</sup> C mode: Serial clock (SCL) (2.2-kΩ pullup resistor is required, if used)                                                                                                                                           |
| VC1                  | 78                                                 | I/O | PHI mode: Read-write or write (RW/W)<br>I <sup>2</sup> C mode: Serial data (SDA) (2.2-kΩ pullup resistor is required, if used)                                                                                                                                                 |
| VC2                  | 77                                                 | I/O | PHI mode: Data strobe or read signal (DS/RD)                                                                                                                                                                                                                                   |
| VC3                  | 76                                                 | I   | PHI mode: Chip select (CS)<br>I <sup>2</sup> C mode: Slave address select (I <sup>2</sup> CA)                                                                                                                                                                                  |

<sup>†</sup> Actual output values are in Cb and Cr color space. Throughout this document, U represents Cb and V represents Cr at the output ports.

**Table 1–1. Terminal Functions (Continued)**

| TERMINAL<br>NAME             | NUMBER                | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------------------|-----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Miscellaneous Signals</b> |                       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| BG                           | 1                     | O   | Connect a 1- $\mu$ F capacitor from this terminal to analog ground. See Figure 2–1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CLAMP1<br>CLAMP2             | 2<br>13               | O   | Clamp voltage outputs. Connect a 0.1- $\mu$ F decoupling capacitor from each terminal to analog ground. See Figure 2–1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| GLCO/RTC                     | 31                    | I/O | This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control from the TVP5145 device. Data is transmitted at the SCLK rate in Genlock mode. In RTC mode, SCLK/4 is used. Additionally, this terminal, in conjunction with PALI and FID, determines the host port mode configuration during initial power up (see Table 2–3).                                                                                                                                                                                                                 |
| GPCL                         | 38                    | I/O | General-purpose control logic. This terminal has three functions: (see Section 2.12.4, <i>Miscellaneous Control</i> )<br>1) General-purpose output. In this mode the state of GPCL is directly programmed via the host port.<br>2) Vertical blank output. In this mode, the GPCL terminal indicates the vertical blanking interval of the output video. The beginning and end times of this signal are programmable via the host port control.<br>3) Sync lock control input. In this mode when GPCL is high, the output clock frequencies and the sync timing are forced to nominal values.                  |
| OEB                          | 24                    | I   | Output enable for Y and UV terminals. Output enable is also controllable via the host port. When this terminal is a logic 1, it forces Y and UV output terminals to high impedance states (active low).                                                                                                                                                                                                                                                                                                                                                                                                       |
| RSTINB                       | 23                    | I   | Reset input, active low                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| RSTOUTB                      | 22                    | O   | Reset output, active low. This is a registered feed through of RSTINB.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>Power Supplies</b>        |                       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| AFE_VDD                      | 18                    |     | Analog supply. Connect to 3.3-V analog supply                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| AFE_GND                      | 16                    |     | Analog ground                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| CH1_AGND<br>CH2_AGND         | 3<br>12               |     | Analog grounds                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CH1_AVDD<br>CH2_AVDD         | 6<br>9                |     | Analog supply. Connect to 3.3-V analog supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| DGND                         | 21, 37, 47,<br>57, 68 |     | Digital grounds                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| DVDD                         | 34, 44, 54,<br>65, 75 |     | Digital supply. Connect to 3.3 V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| NSUB                         | 17                    |     | Substrate ground. Connect to analog ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| PLL_AGND                     | 20                    |     | PLL ground. Connect to analog ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| PLL_AVDD                     | 19                    |     | PLL supply. Connect to 3.3-V analog supply.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| REFM<br>REFP                 | 7<br>8                | O   | A/D reference supply. Connect a 1.0- $\mu$ F capacitor from each terminal to analog ground. Connect a 0.1- $\mu$ F capacitor across REFM and REFP terminals (see Figure 2–1).                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <b>Sync Signals</b>          |                       |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| AVID                         | 28                    | I/O | Active video indicator. This signal is high during the horizontal active time of the video output on the Y and UV terminals.<br><br>This terminal may be placed in a high-impedance state. During reset, AVID is an input, used to program the behavior of Y[9:0], UV[9:0], HSYN, VSYN, AVID, and FID immediately after the completion of reset. If AVID is pulled up during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID will be actively driven after reset. If AVID is pulled down during reset, Y[9:0], UV[9:0], HSYN, VSYN, AVID, PALI, and FID remain in a high-impedance state after reset. |
| FID                          | 33                    | I/O | Odd/even field indicator or vertical lock indicator (VLK). For odd/even indicator, a logic 1 indicates the odd field. For vertical lock indicator, a logic 1 indicates the internal vertical PLL is in a locked state. Additionally, this terminal in conjunction with GLCO and PALI determines the host port configuration during initial power up and reset (see Table 2–3).                                                                                                                                                                                                                                |
| HSYN                         | 30                    | O   | Horizontal sync signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

**Table 1–1. Terminal Functions (Continued)**

| TERMINAL<br>NAME      NUMBER    |    | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------------------|----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Sync Signals (Continued)</b> |    |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| PALI                            | 32 | I/O | PAL line indicator or horizontal lock indicator (HLK).<br><br>For PAL line indicator, a 1 indicates a noninverted line, and a 0 indicates an inverted line.<br>For horizontal lock indicator, a 1 indicates the internal horizontal PLL is in a locked state, and a 0 indicates the internal horizontal PLL is in an unlocked state.<br><br>This terminal is an input terminal during reset and is used in conjunction with GLCO and FID to select the mode of the host interface (see Table 2–3). |
| VSYN                            | 29 | O   | Vertical sync signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

## 1.8 Strapping Terminals Description

All of the following terminals have reset strapping options. The states of these terminals are sampled during reset to configure the TVP5145 device for various modes of operation. These terminals are temporarily turned into inputs during reset and return to their normal operation after reset. Each of the following terminals can be pulled up with a 10-k $\Omega$  resistor to set a 1 to the corresponding bit or be left undriven during reset. The AVID terminal has an internal pulldown resistor (approximately 40 k $\Omega$ ) to pull the terminal low to set a 0.

**Table 1–2. Strapping Terminals**

| TERMINAL<br>NAME      NUMBER |    | DESCRIPTION                                                                                                                                       |
|------------------------------|----|---------------------------------------------------------------------------------------------------------------------------------------------------|
| AVID                         | 28 | Y, U/V output enable (bit 4) and HSYN, VSYN, AVID, FID, and PALI output enable (bit 3) of the miscellaneous control register (see Section 2.12.4) |
| FID                          | 33 | Host interface mode (see Table 2–3)                                                                                                               |
| PALI                         | 32 | Host interface mode (see Table 2–3)                                                                                                               |
| GLCO                         | 31 | Host interface mode (see Table 2–3)                                                                                                               |

† FID, PALI, and GLCO terminals can be pulled down with a 10-k $\Omega$  resistor to set a 0 to the corresponding bit.

## 2 Functional Description

### 2.1 Analog Video Processing and A/D Converters

Figure 2–1 shows a functional diagram of the analog video preprocessors and A/D converters. This block provides the analog interface to all video inputs. It accepts up to six inputs and performs source selection, video clamping, video amplification, analog-to-digital conversion, and fine gain and offset adjustments to center the digitized video signal. In a component mode, three YUV input signals are digitized by two A/D converters applying color multiplexing of UV. Using a single A/D channel for UV chroma avoids gain mismatch between color components.

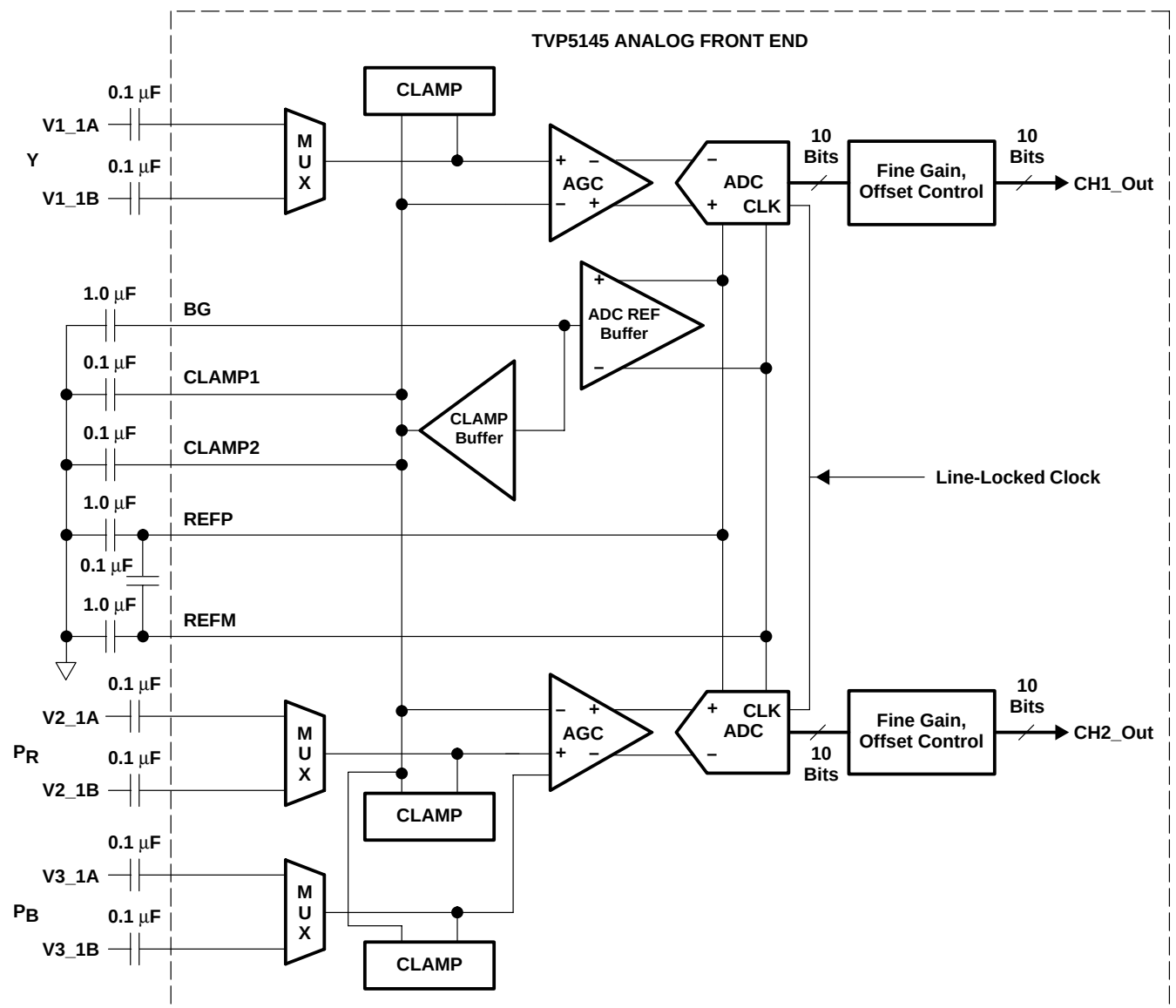


Figure 2–1. Analog Video Processors and A/D Converters



### 2.1.1 Video Input Selection

The TVP5145 device has three analog channels that accept six ac-coupled video inputs. The internal video multiplexers can be configured via the host port. The six analog video inputs may be connected as one of the following:

- Two selectable analog YPbPr component video inputs
- One selectable analog YPbPr component video, one selectable S-video, and one composite video inputs
- Six selectable individual composite video inputs
- Two selectable S-video input and two composite video inputs

The input selection is done by the register setup (see Section 2.12.1, *Video Input Source Selection #1*).

### 2.1.2 Analog Input Clamping and Automatic Gain Control Circuits

An internal clamping circuit restores the ac-coupled video signal to a fixed dc level. The clamping circuit provides line-by-line restoration of the video sync level to a fixed dc reference voltage. Two modes of clamping are provided, coarse and fine. In coarse mode, the most negative portion of the input signal (typically the sync tip) is clamped to a fixed dc level. Fine clamp mode may be enabled to prevent spurious level shifting caused by noise more negative than the sync tip on the input signal. If fine clamp mode is selected, clamping is only enabled during the sync period. External capacitors of 0.1  $\mu$ F on terminals 2 (CLAMP1) and 13 (CLAMP2) are required.

The input video signal amplitude may vary significantly from the nominal level of 1  $V_{P-P}$ . An automatic gain control circuit (AGC) adjusts the signal amplitude to utilize the maximum range of the A/D converter without clipping. The AGC adjusts gain to achieve desired sync amplitude. Some nonstandard video signals contain peak white levels that saturate the A/D converter. In these cases, the AGC automatically cuts back gain to avoid clipping. The AGC has a range of -3 dB to 6 dB.

The fine gain and offset adjustment block precisely controls the sync tip and back porch levels to achieve the best linearity performance.

### 2.1.3 A/D Converters

The TVP5145 device contains two 10-bit oversampling A/D converters that digitize the analog video inputs. A/D converter reference voltages on terminals 8 (REFP) and 7 (REFM) require an external capacitor network for filtering, as shown in Figure 2-1.

## 2.2 Digital Processing

Figure 2-2 is a block diagram of the TVP5145 digital video decoder processing. This block receives digitized video signals from the A/D converters and performs Y/C separation, and Y, U/V signal enhancements. It also generates horizontal and vertical syncs. The Y U/V digital output may be programmed into various formats: 20-/16-bit or 10-/8-bit 4:2:2, and 10-/8-bit ITU-R BT.656 parallel interface standard. This circuit also detects copy-protected material according to the Macrovision specification, and retrieves VBI information. S-video and component video bypass the Y/C separation block.

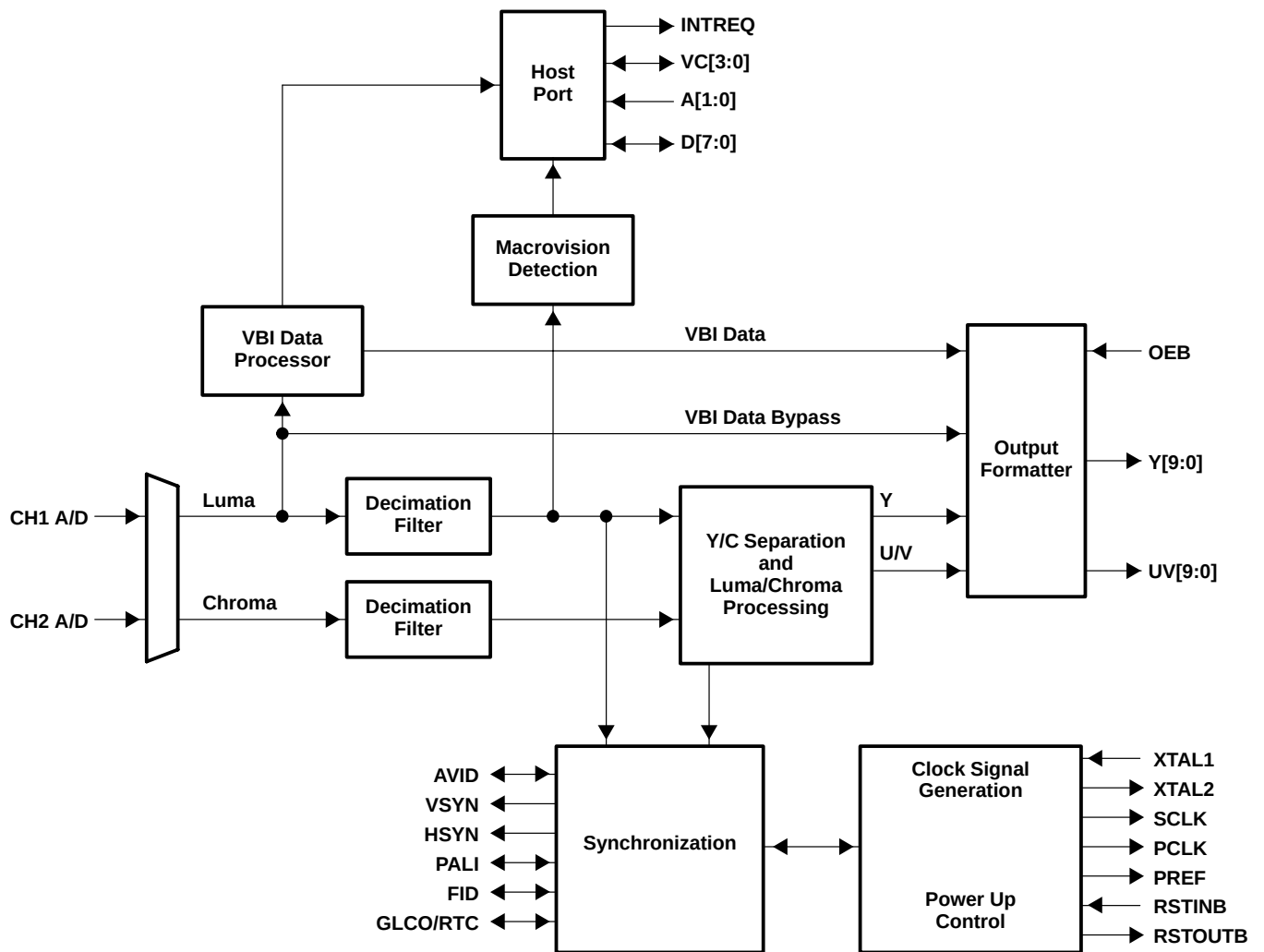


Figure 2-2. Digital Video Signal Processing Block Diagram

### 2.2.1 Digital Input Selection

The digital processing block takes digitized composite, S-video, and component video from two internal A/D converters running at twice the PCLK rate. The data from the A/D converters are appropriately multiplexed as shown in Figure 2-3 for downstream separation and processing of luma and chroma.

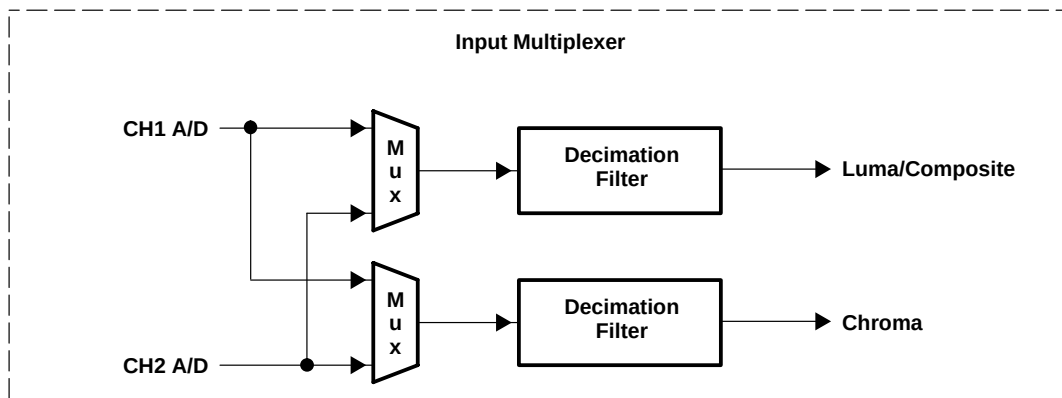


Figure 2–3. Digital Input Multiplexer

## 2.2.2 Decimation Filter

Digitized composite, S-video, or component video at twice the PCLK rate first passes through decimation filters that reduce the data rate from twice the PCLK rate to the PCLK rate. The decimation filter is a half-band filter whose frequency response is shown in Figure 2–4. For applications that can not tolerate any high frequency droop, decimation filters can be bypassed via the host port. Oversampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB. This advantage is lost if the decimation filter is bypassed.

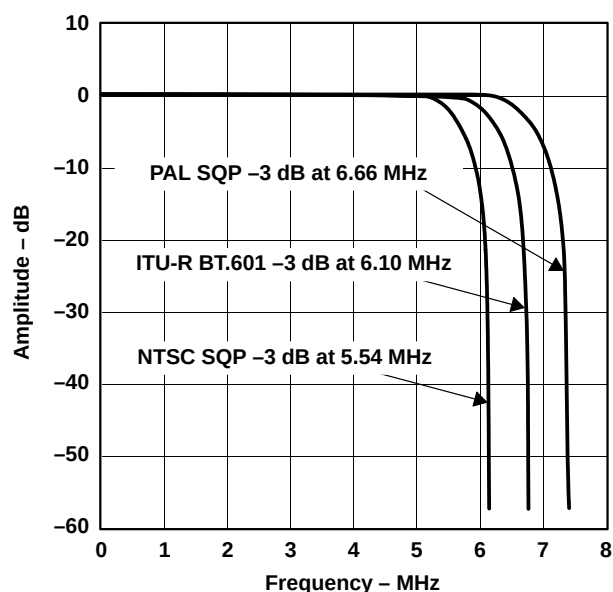


Figure 2–4. Decimation Filter Frequency Response

## 2.2.3 Y/C Separation

Figure 2–5 illustrates the luminance/chrominance (Y/C) separation process in the TVP5145 device. Ten-bit composite video is multiplied by subcarrier signals in the quadrature modulator to generate the color difference signals U and V. U and V are then low-pass filtered. An adaptive 3- or 4-line comb filter separates UV from Y based on the unique property of color phase shift from line to line. Chroma is remodulated through another quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C separation is completely complementary, thus loses no information. However, in some applications, it is desirable to limit the U/V bandwidth. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter

is also available in the luma path. The Y/C separation is bypassed for S-video and component YPbPr video input. Contrast, brightness, hue, and saturation are programmable via the host port.

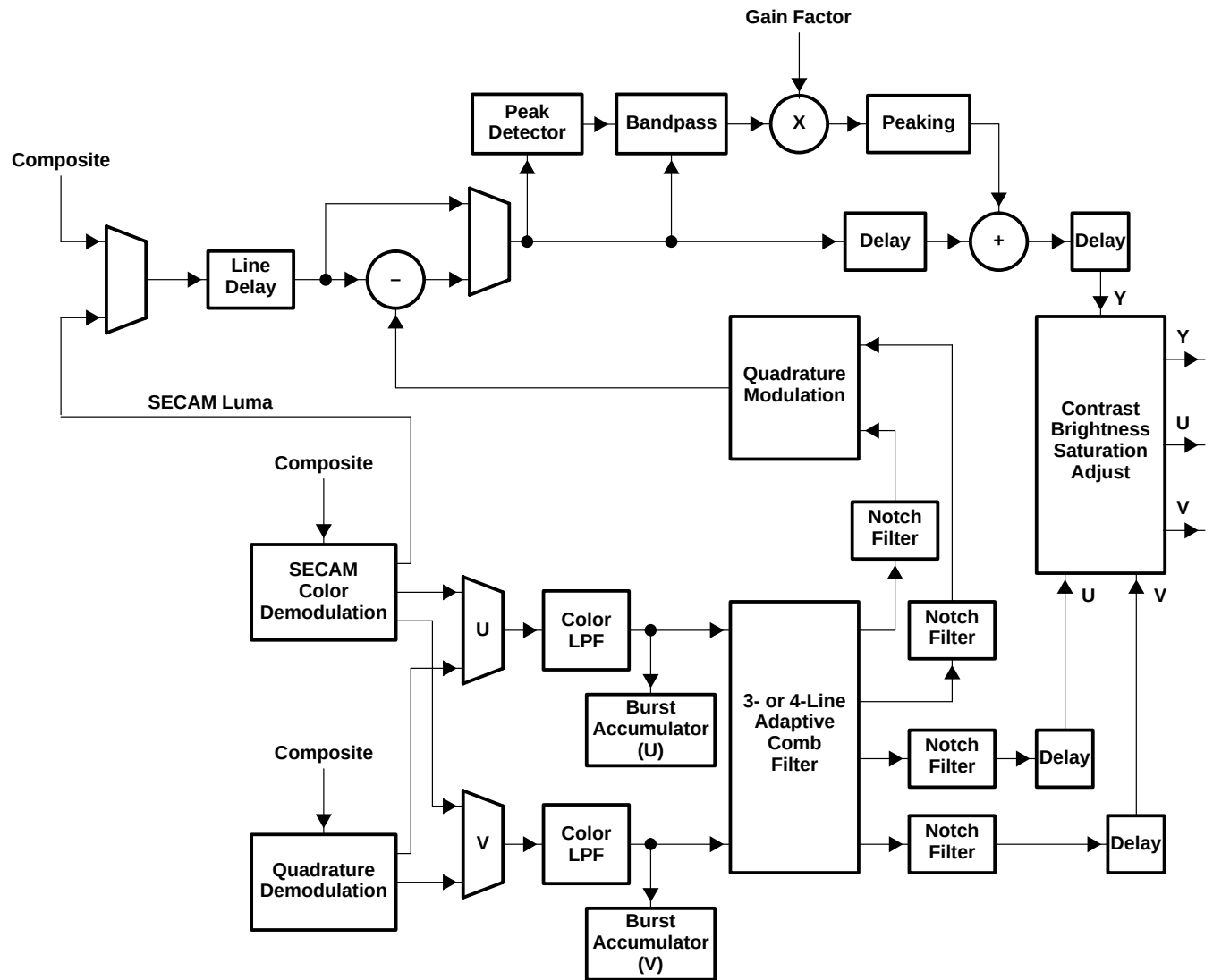


Figure 2-5. Y/C Separation Block Diagram

### 2.2.3.1 Color Low-Pass Filter

High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However, for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. Color low-pass filter bandwidth is programmable via the host port by enabling one of the three notch filters. There are two selectable color low-pass filters for each mode. Figure 2-6 through Figure 2-9 represent the frequency response of the wideband color low-pass filter (default). The detailed -3 dB frequencies of each mode are listed in Section 2.12.23. Please refer to the TVP5040 data manual (Literature Number SLAS257D) for narrow band frequency responses.

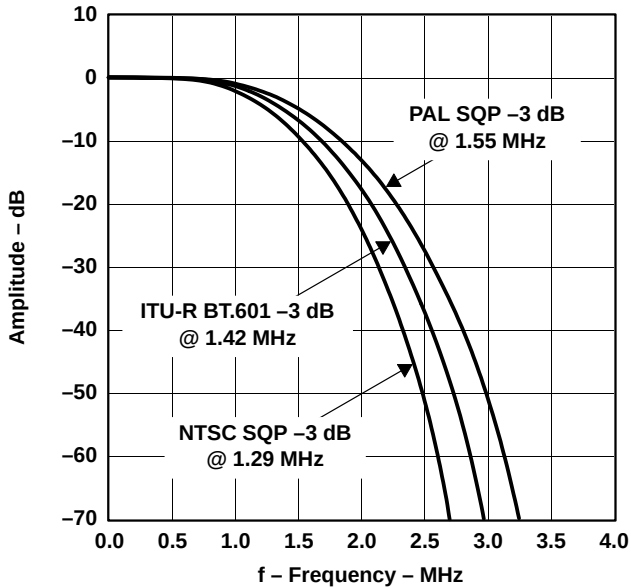


Figure 2-6. Color Low-Pass Filter Frequency Response

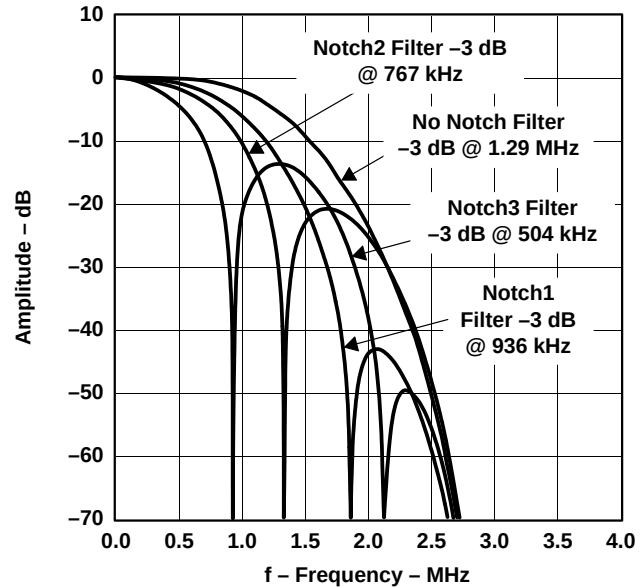


Figure 2-7. Color Low-Pass Filter With Notch Filter Frequency Response, NTSC Square Pixel Sampling

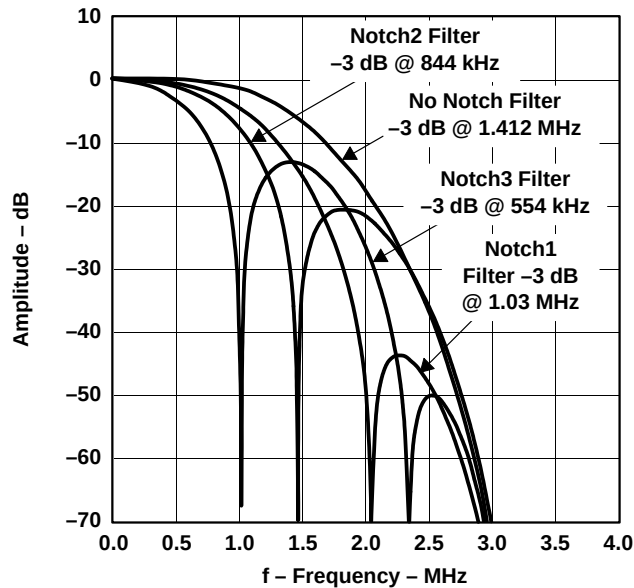


Figure 2-8. Color Low-Pass Filter With Notch Filter Characteristics, NTSC/PAL ITU-R BT.601 Sampling

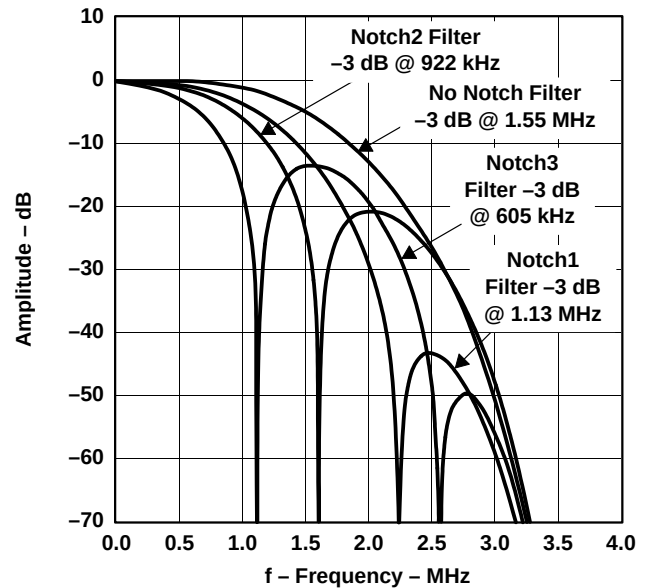


Figure 2-9. Color Low-Pass Filter With Notch Filter Characteristics, PAL Square Pixel Sampling

### 2.2.3.2 Adaptive Comb Filter

Y/C separation may be done using adaptive 4-line (3-H delay), fixed 3-line, fixed 2-line comb filters, or a chroma trap filter. Characteristics of 4-line and 3-line comb filters are shown in Figure 2-10. The filter frequency plots show that both 4-line and 3-line (with filter coefficients  $[1, 3, 3, 1]/8$  and  $[1, 2, 1]/4$ ) comb filters have zeros at  $1/2$  of the horizontal line frequency to separate the interleaved Y/C spectrum in NTSC. The 4-line comb filter has less cross-luma and cross-chroma noise due to slightly sharper filter cutoff. The 4-line comb filter with filter coefficients  $[1, 1, 1, 1]/4$  has

three zeros at  $1/4$ ,  $2/4$ , and  $3/4$  of the horizontal line frequency. This should be used for PAL only because of its  $90^\circ$  U/V phase shifting from line to line. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figure 2–11 through Figure 2–14. TI's patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundaries, and detects and properly handles false colors in high frequency luminance images such as a multiburst pattern or circle pattern. Adaptive comb filtering is the recommended mode of operation. The complete comb filter selection is shown in chrominance control #1 register (see Section 2.12.22).

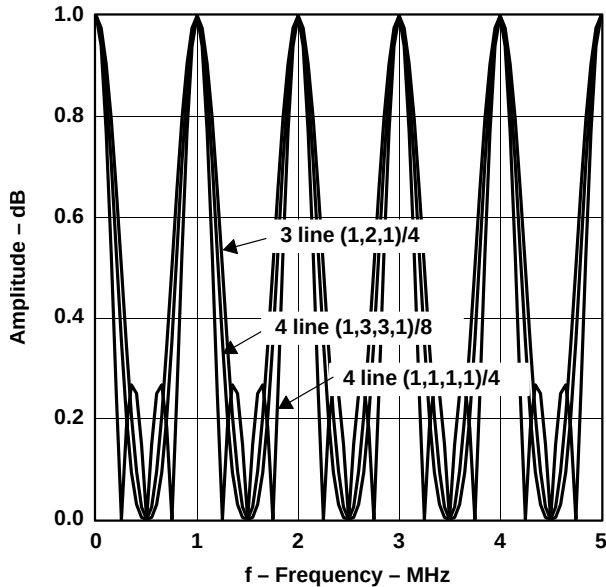


Figure 2–10. Comb Filters Frequency Response

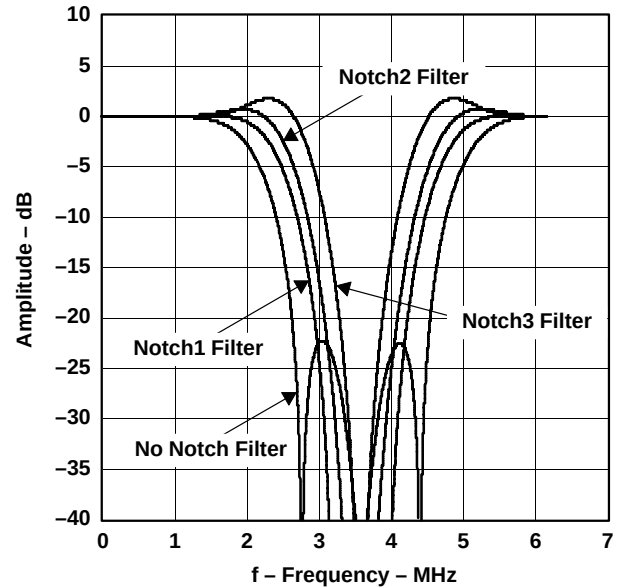


Figure 2–11. Chroma Trap Filter Frequency Response, NTSC Square Pixel Sampling

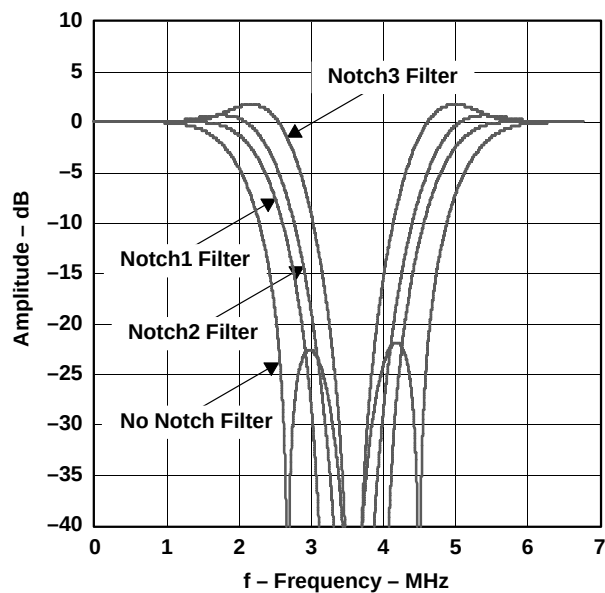


Figure 2–12. Chroma Trap Filter Frequency Response, NTSC ITU-R BT.601 Sampling

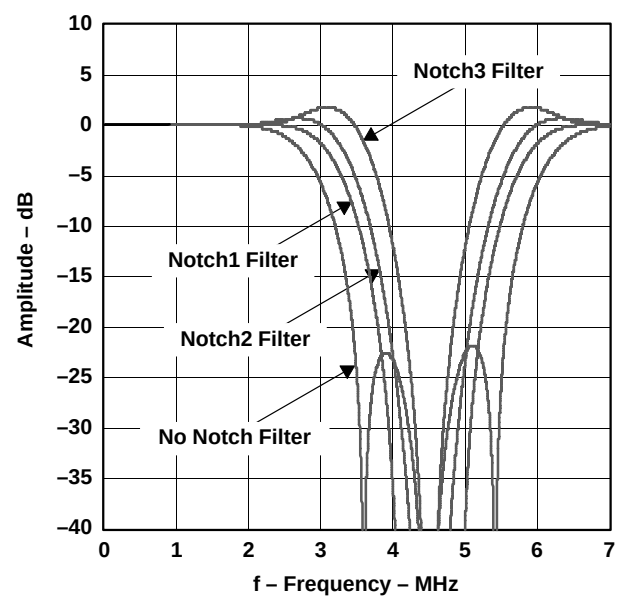


Figure 2–13. Chroma Trap Filter Frequency Response, PAL ITU-R BT.601 Sampling

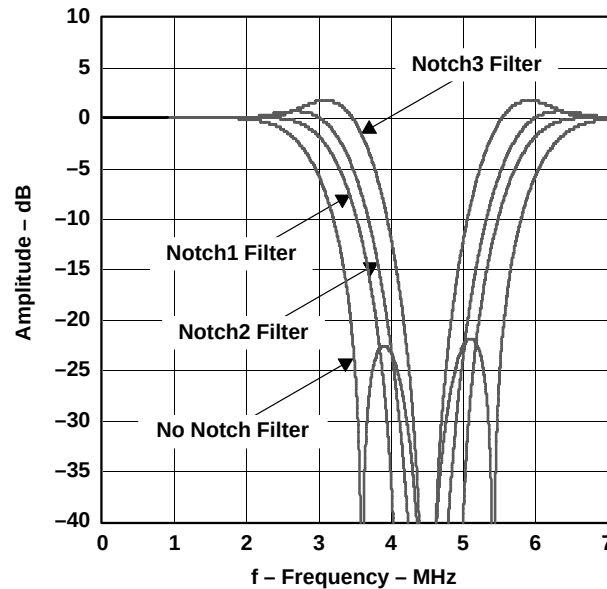


Figure 2-14. Chroma Trap Filter Frequency Response, PAL Square Pixel Sampling

## 2.2.4 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed to the input of a peaking circuit. Figure 2-15 illustrates the basic functions of the luminance data path. In the case of S-video, the luminance signal bypasses the comb filter or chroma trap filter and is fed directly to the circuit. High frequency components of the luminance signal are enhanced by a peaking filter (edge-enhancer). Figure 2-16, Figure 2-17, and Figure 2-18 show the characteristics of the peaking filter at four different gain settings programmable via the host port.

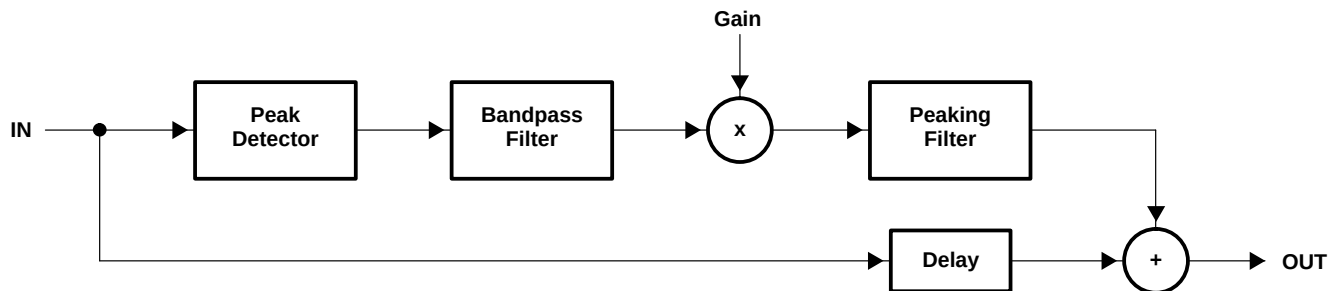


Figure 2-15. Luminance Edge-Enhancer Peaking Block Diagram

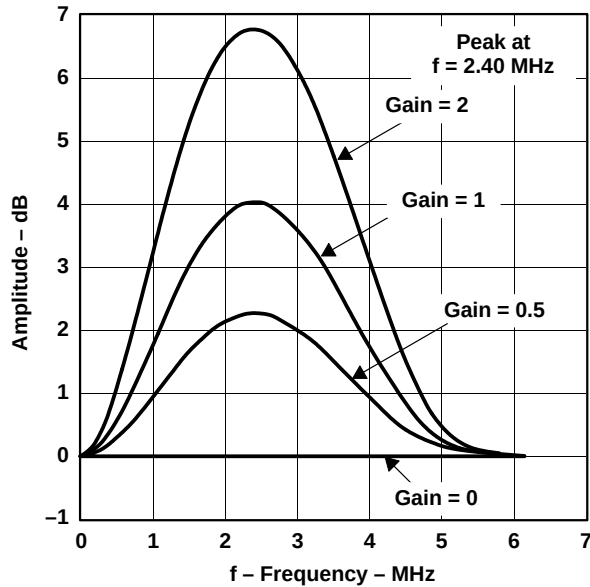


Figure 2-16. Peaking Filter Response, NTSC Square Pixel Sampling

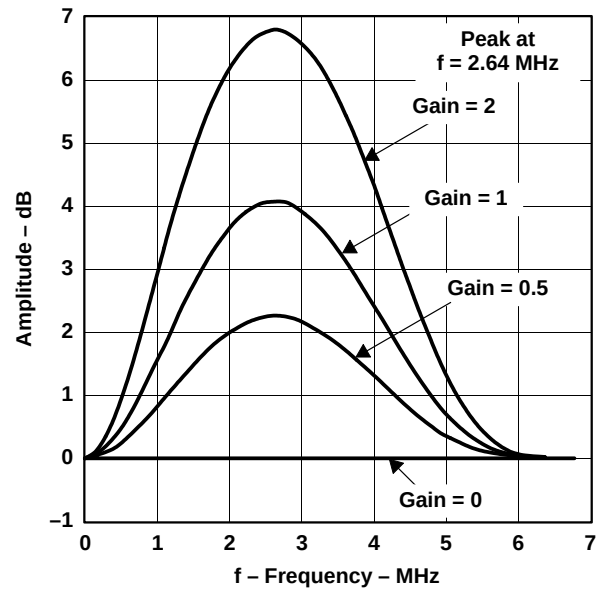


Figure 2-17. Peaking Filter Response, NTSC/PAL ITU-R BT.601 Sampling

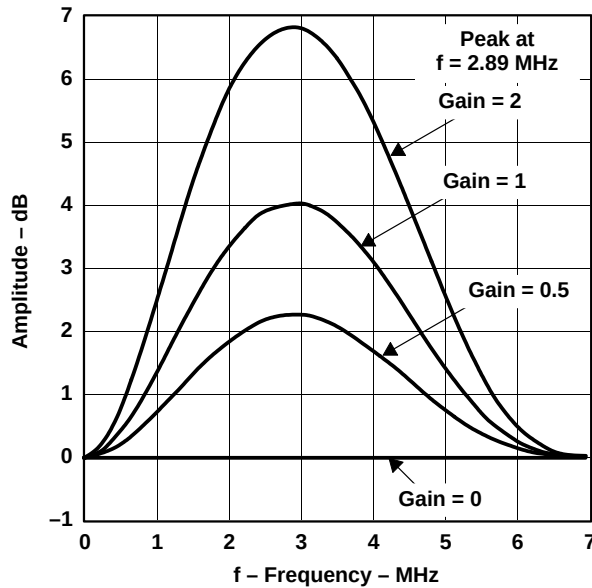


Figure 2-18. Peaking Filter Response, PAL Square Pixel Sampling

## 2.2.5 Chrominance Processing

A quadrature demodulator extracts U and V components from the composite or S-video signal. The U/V signals then pass through the gain control stage for chroma saturation adjustment. A comb filter is applied to both U and V to eliminate cross-chrominance noise. Hue control (not available with YPbPr component inputs) is achieved with phase shift of the demodulator. An automatic color killer circuit is also included in this block. The automatic color killer suppresses the chroma processing when the color burst of the video signal is weak or not present.



## 2.2.6 SECAM Processing

The SECAM standard is similar to PAL except for the modulation of color which is frequency modulation (FM) instead of quadrature amplitude modulation (QAM). The color difference signals Db and Dr are transmitted on an alternating line basis using two different color FM carrier frequencies: 4.25 MHz for Db (blue) and 4.40625 MHz for Dr (red). A line reference signal which is transmitted during the back porch interval identifies the appropriate color signal. Figure 2–19 is a block diagram of the processing data path for SECAM which decodes into YUV. Luma Y is generated by filtering the chroma using a bandpass filter and then subtracting the chroma from the composite input. The delay blocks compensate for delays in the filter and the chroma data path. The filtered chroma is then limited and filtered by a bell filter. The bell filter emphasizes (amplifies) the FM carrier which was deemphasized (attenuated) by the encoder prior to transmission. The bell filter output is then fed to the FM demodulator which outputs a scaled version of UV. These scaled outputs are then converted to UV by the UV conversion block. The line ID block monitors the FM demodulator outputs during the back porch interval so that the Db or Dr line can be identified. The video deemphasis block attenuates the higher frequency components of the inputs which were emphasized (amplified) by the encoder in order to improve SNR. Both the bell and the video deemphasis filters have a nonlinear phase characteristic as required by the SECAM standard ITU-R BT.470. A line delay and two multiplexers demultiplex the UV into separate cosited U and V outputs.

The frequency responses for the SECAM filters and FM demodulator characteristic are shown in Figure 2–20 for the ITU-R BT.601 and square pixel sampling rates.

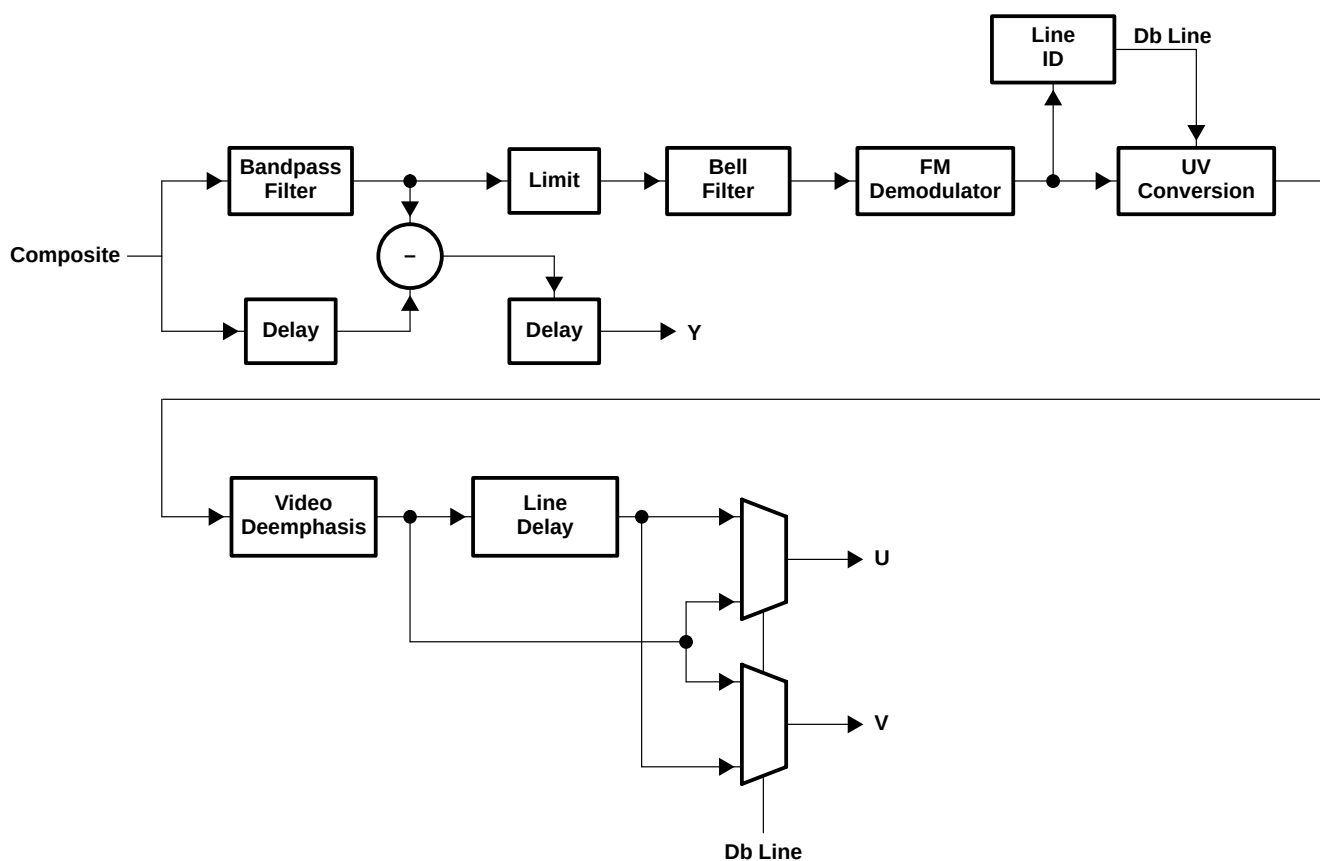
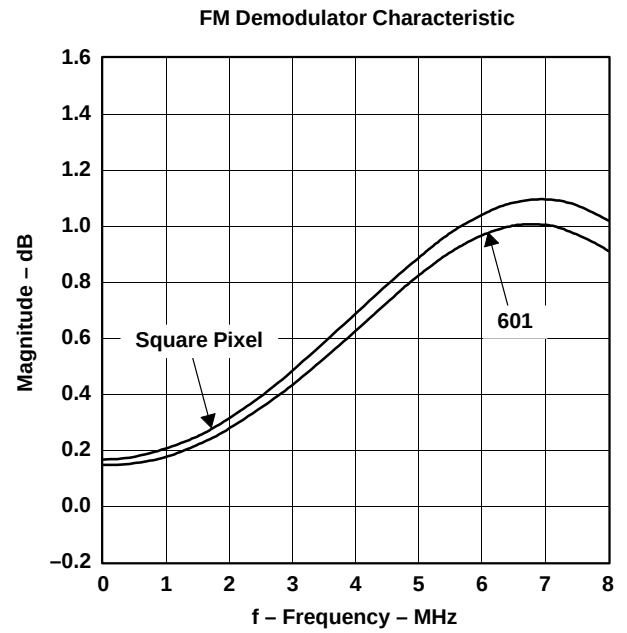
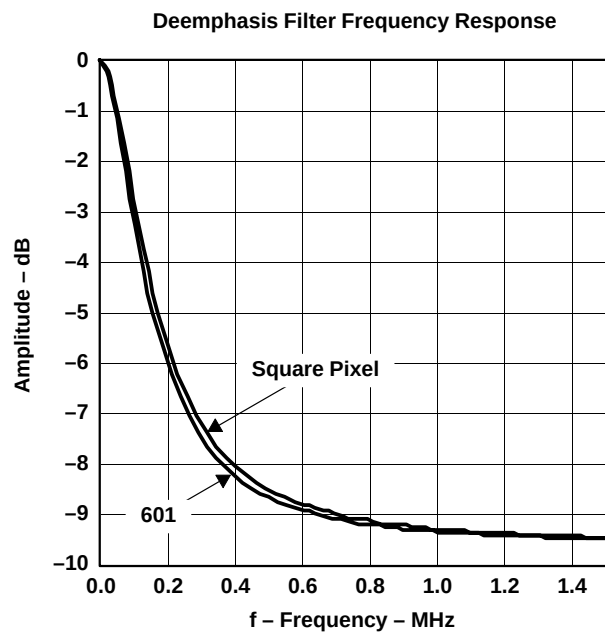
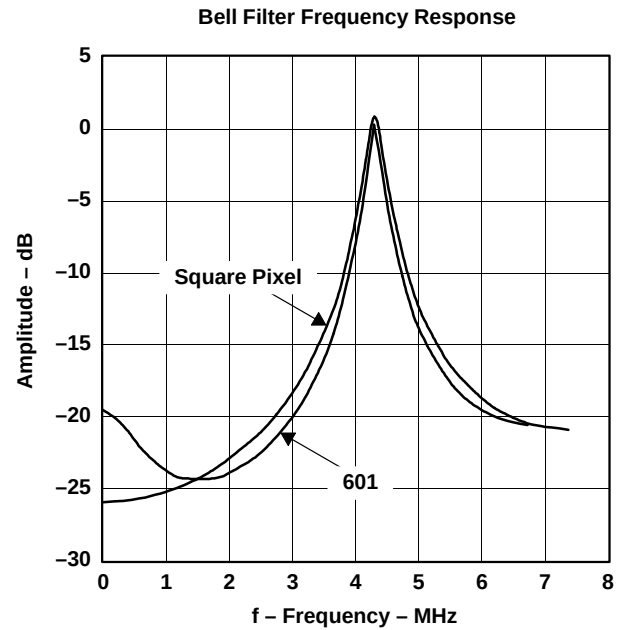
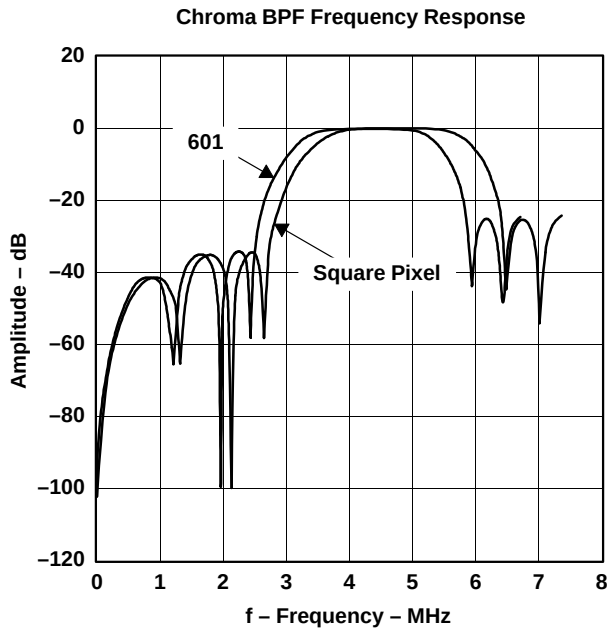


Figure 2–19. SECAM Data Path



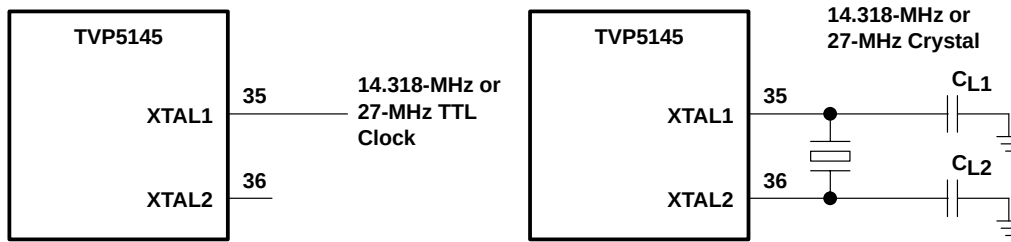
**Figure 2-20. SECAM Filter Frequency Responses and FM Demodulator Characteristic**

## 2.3 Clock Circuits

An internal line-locked phase-locked loop (PLL) generates the system and pixel clocks. A 14.318-MHz or 27-MHz clock is required to drive the PLL. This may be input to the TVP5145 device at the TTL level on terminal 35 (XTAL1), or a crystal of 14.318-MHz or 27-MHz frequency may be connected across terminals 35 and 36 (XTAL2). If a parallel resonant circuit is used as shown in Figure 2–21, then the external capacitors must have the following relationship:

$$C_{L1} = C_{L2} = 2C_L - C_{STRAY},$$

where  $C_{STRAY}$  is the terminal capacitance with respect to ground. Figure 2–21 shows the reference clock configurations.



**Figure 2–21. Reference Clock Configurations**

The TVP5145 device generates three signals PCLK, SCLK, and PREF used for clocking data. PCLK, the pixel clock, can be used for clocking data in the 20-/16-bit 4:2:2 output formats. SCLK is at twice the PCLK frequency and may be used for clocking data in the 10-/8-bit 4:2:2 as well as in ITU-R BT.656 formats. PREF is used as a clock qualifier with SCLK to clock data in the 20-/16-bit 4:2:2 formats, or as an alternate pixel clock.

## 2.4 Genlock Control (GLCO) and Real-Time Control (RTC)

The frequency control word of the internal color subcarrier PLL and the subcarrier phase reset bit are transmitted via terminal 31 (GLCO/RTC). The frequency control word is a 23-bit binary number. The frequency of the PLL can be calculated from the following equation:

$$F_{PLL} = \frac{F_{ctrl}}{2^{23}} \times F_{sclk}$$

where  $F_{PLL}$  is the frequency of the PLL,  $F_{ctrl}$  is the 23-bit PLL frequency control and  $F_{sclk}$  is the frequency of the SCLK. The selection between Genlock and RTC is controlled by the Genlock and RTC register described in Section 2.12.18.

### 2.4.1 GLCO Mode

Figure 2–22 shows the timing diagram of the GLCO mode. The upper 22 bits of the frequency control are used. A write of 1 to bit 4 of the chrominance control register at host port subaddress 1Ah causes the subcarrier PLL phase reset bit to be sent on the next scan line on GLCO. The active low reset bit occurs 7 SCLKs after the transmission of the last bit of PLL frequency control. Upon the transmission of the reset bit, the phase of the TVP5145 internal subcarrier PLL is reset to zero. A genlocking slave device can be connected to the GLCO terminal and uses the information on GLCO to synchronize its internal color phase PLL.

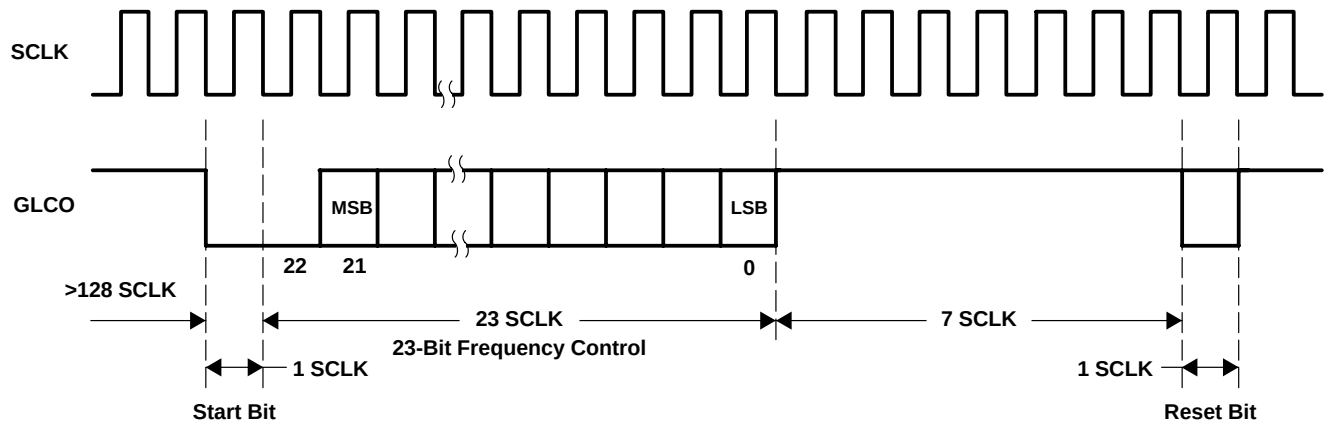


Figure 2-22. GLCO Timing

## 2.4.2 RTC Mode

Figure 2-23 shows the timing diagram of the RTC mode. Clock rate for the RTC mode is 4 times slower than the GLCO clock rate. For PLL frequency control, the upper 22 bits are used. Each frequency control bit is 2 clock cycles long. The active low reset bit occurs 6 CLKs after the transmission of the last bit of PLL frequency control.

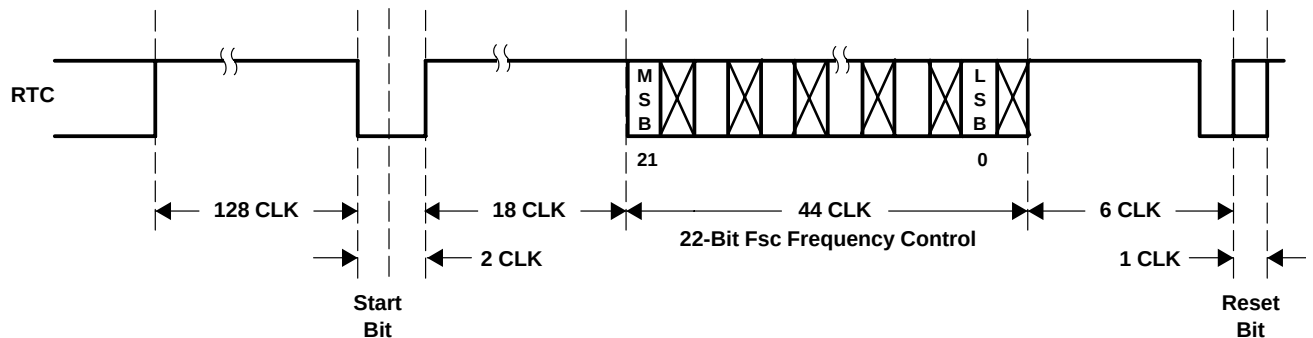


Figure 2-23. RTC Timing

## 2.5 Video Output Format

The TVP5145 device supports both square-pixel and ITU-R BT.601 sampling formats and multiple YCbCr output formats:

- 20-/16-bit 4:2:2
- 10-/8-bit 4:2:2
- 10-/8-bit ITU-R BT.656
- 10-bit digital composite output (raw digital data)

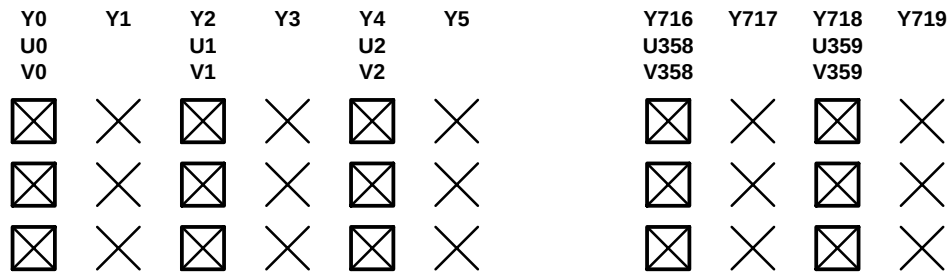
**NOTE:** 16-bit and 8-bit modes use only 8 MSBs of output Y[9:2] and UV[9:2]. Y[1:0] and UV[1:0] are ignored.

### 2.5.1 Sampling Frequencies and Patterns

The sampling frequencies that control the number of pixels per line differ depending on the video format and standards. Table 2-1 shows a summary of the sampling frequencies. The TVP5145 device outputs data in the 4:2:2 sampling pattern (see Figure 2-24). Every second sample is both a luminance and chrominance sample. The remainder are luminance-only samples.

**Table 2–1. Summary of Line Frequencies, Data Rates, and Pixel Counts**

| STANDARDS                           | HORIZONTAL<br>LINE RATE (kHz) | PIXELS PER<br>LINE | ACTIVE PIXELS<br>PER LINE | PCLK<br>FREQUENCY<br>(MHz) | SCLK<br>FREQUENCY<br>(MHz) |
|-------------------------------------|-------------------------------|--------------------|---------------------------|----------------------------|----------------------------|
| NTSC(J, M, 4.43), square-pixel      | 15.73426                      | 780                | 640                       | 12.2727                    | 24.54                      |
| NTSC(J, M, 4.43), ITU-R BT.601      | 15.73426                      | 858                | 720                       | 13.50                      | 27.00                      |
| PAL(B, D, G, H, I, N), square-pixel | 15.625                        | 944                | 768                       | 14.75                      | 29.50                      |
| PAL(B, D, G, H, I, N), ITU-R BT.601 | 15.625                        | 864                | 720                       | 13.50                      | 27.00                      |
| PAL(M), square-pixel                | 15.73426                      | 780                | 640                       | 12.2727                    | 24.54                      |
| PAL(M), ITU-R BT.601                | 15.73426                      | 858                | 720                       | 13.50                      | 27.00                      |
| SECAM, square-pixel                 | 15.625                        | 944                | 768                       | 14.75                      | 29.50                      |
| SECAM, ITU-R BT.601                 | 15.625                        | 864                | 720                       | 13.50                      | 27.00                      |



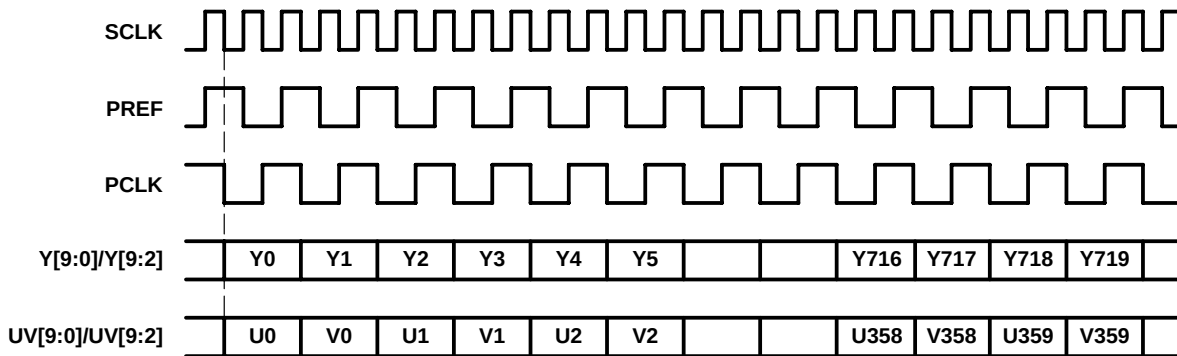
= Luminance-Only Sample  
 = Luminance and Chrominance Sample

Numbering shown is for 13.5-MHz sampling

**Figure 2–24. 4:2:2 Sampling**

## 2.5.2 Video Port 20-/16-Bit 4:2:2 Output Format Timing

**NOTE:**16-bit mode uses only 8 MSBs of output ports.



Numbering shown is for 13.5-MHz sampling

**Figure 2–25. 20-/16-Bit 4:2:2 Output Format**

### 2.5.3 Video Port 10-/8-Bit 4:2:2 and ITU-R BT.656 Output Format Timing

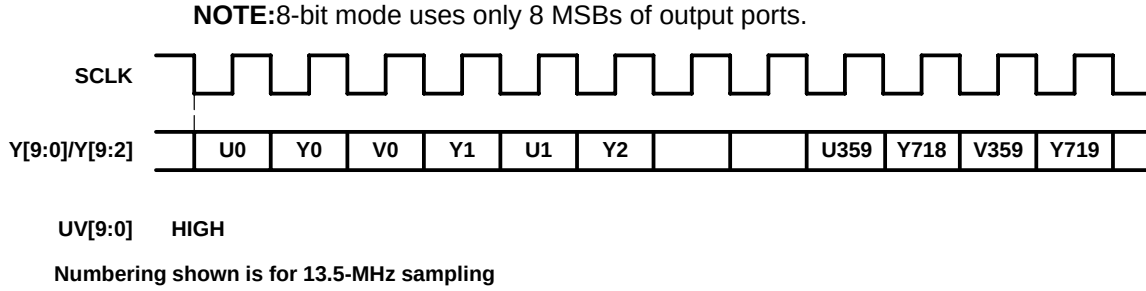
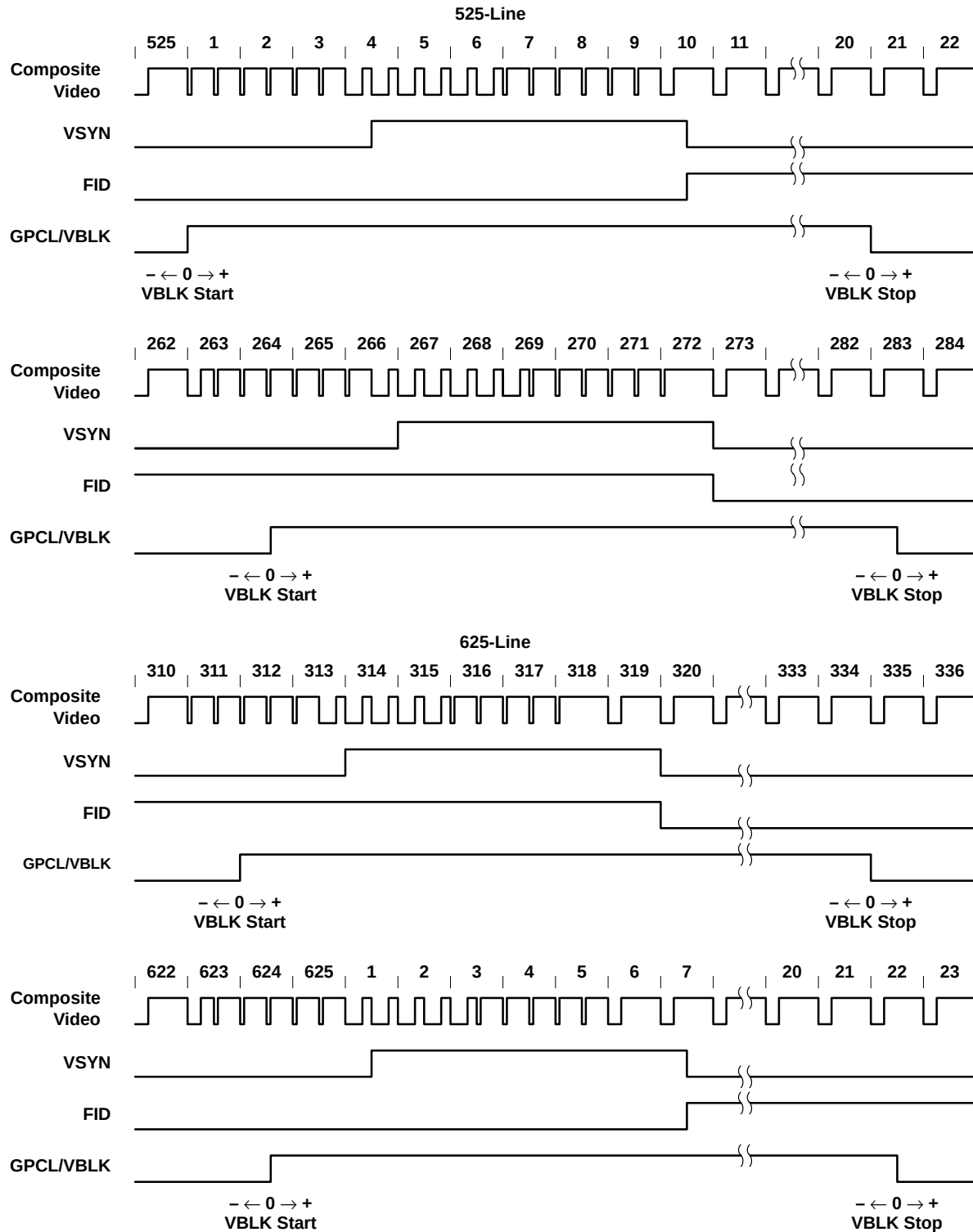


Figure 2–26. 10-/8-Bit 4:2:2 Output Format

## 2.6 Synchronization Signals

### 2.6.1 Separate Syncs

VBLK, HSYN, and AVID are independently software programmable to an SCLK count. This allows any possible alignment to the internal pixel count and line count. The default setting for a 525- and 625-line video output is given as an example below.



- Notes:
1. Line numbering conforms to ITU-R BT470
  2. The VBLK timing shown is valid when VBLK start and stop (registers 18h and 19h) are set to the default value.

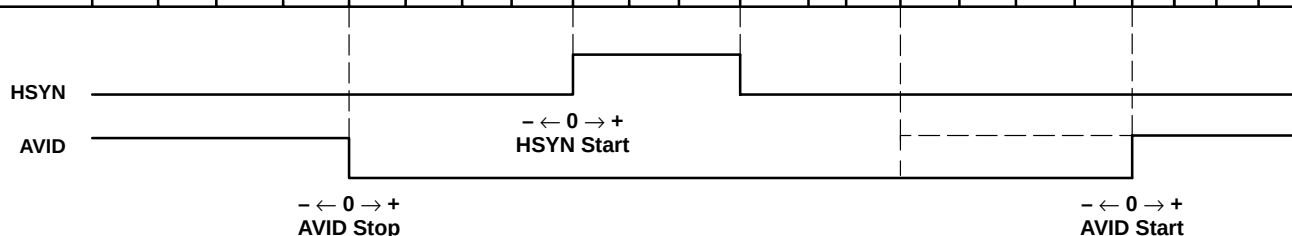
**Figure 2–27. Vertical Synchronization Signals**

10-/8-bit 4:2:2 timing with 2x pixel clock (SCLK) reference. ITU-R BT.656 timing also shown with embedded syncs.

|                    |        |       |        |       |      |      |     |      |      |     |      |      |     |      |      |      |      |      |      |     |      |     |
|--------------------|--------|-------|--------|-------|------|------|-----|------|------|-----|------|------|-----|------|------|------|------|------|------|-----|------|-----|
| NTSC 601           | 1436   | 1437  | 1438   | 1439  | 1440 | 1441 | ... | 1455 | 1456 | ... | 1583 | 1584 | ... | 1711 | 1712 | 1713 | 1714 | 1715 | 0    | 1   | 2    | 3   |
| PAL 601            | 1436   | 1437  | 1438   | 1439  | 1440 | 1441 | ... | 1459 | 1460 | ... | 1587 | 1588 | ... | 1723 | 1724 | 1725 | 1726 | 1727 | 0    | 1   | 2    | 3   |
| ITU 656 Datastream | Cb 359 | Y 718 | Cr 359 | Y 719 | FF   | 00   | ... | 10   | 80   | ... | 10   | 80   | ... | 10   | FF   | 00   | 00   | XX   | Cb 0 | Y 0 | Cr 0 | Y 1 |

|                    |        |       |        |       |      |      |     |      |      |     |      |      |     |      |      |      |      |      |      |     |      |     |
|--------------------|--------|-------|--------|-------|------|------|-----|------|------|-----|------|------|-----|------|------|------|------|------|------|-----|------|-----|
| NTSC sqp           | 1276   | 1277  | 1278   | 1279  | 1280 | 1281 | ... | 1293 | 1294 | ... | 1421 | 1422 | ... | 1555 | 1556 | 1557 | 1558 | 1559 | 0    | 1   | 2    | 3   |
| ITU 656 Datastream | Cb 319 | Y 638 | Cr 319 | Y 639 | FF   | 00   | ... | 10   | 80   | ... | 10   | 80   | ... | 10   | FF   | 00   | 00   | XX   | Cb 0 | Y 0 | Cr 0 | Y 1 |

|                    |        |       |        |       |      |      |     |      |      |     |      |      |     |      |      |      |      |      |      |     |      |     |
|--------------------|--------|-------|--------|-------|------|------|-----|------|------|-----|------|------|-----|------|------|------|------|------|------|-----|------|-----|
| PAL sqp            | 1532   | 1533  | 1534   | 1535  | 1536 | 1537 | ... | 1565 | 1566 | ... | 1693 | 1694 | ... | 1883 | 1884 | 1885 | 1886 | 1887 | 0    | 1   | 2    | 3   |
| ITU 656 Datastream | Cb 383 | Y 766 | Cr 383 | Y 767 | FF   | 00   | ... | 10   | 80   | ... | 10   | 80   | ... | 10   | FF   | 00   | 00   | XX   | Cb 0 | Y 0 | Cr 0 | Y 1 |

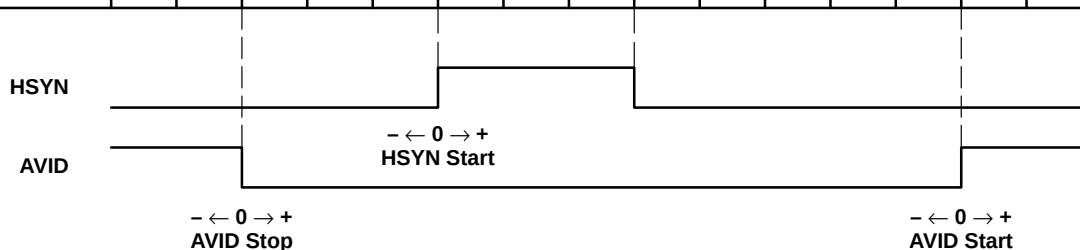


NOTE: AVID rising edge occurs 4 SCLK cycles early when in ITU656 output mode.

(A)

20-/16-bit 4:2:2 timing with 1x pixel clock (PCLK) reference without embedded syncs.

|          |     |     |     |     |     |     |     |     |     |     |     |     |     |   |   |
|----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|---|
| NTSC 601 | 718 | 719 | 720 | ... | 729 | 730 | ... | 793 | 794 | ... | 855 | 856 | 857 | 0 | 1 |
| PAL 601  | 718 | 719 | 720 | ... | 731 | 732 | ... | 795 | 796 | ... | 861 | 862 | 863 | 0 | 1 |
| NTSC sqp | 638 | 639 | 640 | ... | 648 | 649 | ... | 712 | 713 | ... | 777 | 778 | 779 | 0 | 1 |
| PAL sqp  | 766 | 767 | 768 | ... | 784 | 785 | ... | 848 | 849 | ... | 941 | 942 | 943 | 0 | 1 |



(B)

NOTE: The HSYN and AVID timing shown are valid when HSYN start (register 16h), AVID start and stop (registers 11h–14h) are set to the default value.

Figure 2–28. Horizontal Synchronization Signals

## 2.6.2 AVID Cropping

AVID or active video cropping provides a means to decrease bandwidth of the video output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. The horizontal AVID cropping is controlled using registers 11h and 12h for start pixels MSB and LSB, respectively.



Registers 13h and 14h provide access to stop pixels MSB and LSB, respectively. The vertical AVID cropping is controlled using the vertical blanking (VBLK) start and stop registers at addresses 18h and 19h. The effects of VBLK on the video signal is visible on the monitor. This is due to the luma processing during the VBLK period. To disable this effect set bit 4 of register 7h high. This bypasses the luma processing during the vertical blanking period. Figure 2–29 shows an AVID application.

It is important to realize that the video image is not being re-scaled. Instead, a portion of the active video is made unavailable by increasing the horizontal blanking within the AVID pulse and by increasing the vertically blanking within each vertical line.

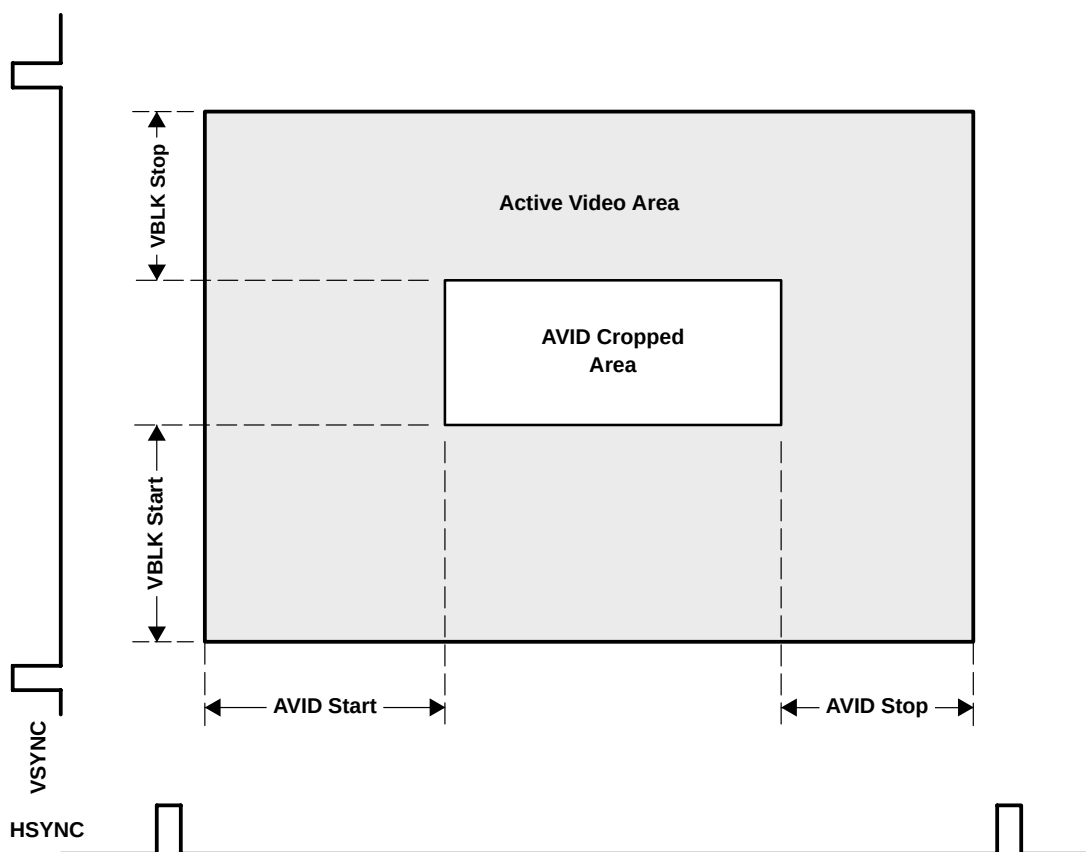


Figure 2–29. AVID Application

### 2.6.3 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the datastream on the rising and falling edges of AVID. These codes contain the V and F bits which also define vertical timing. F and V are software programmable and change after SAV but before EAV, so that the new value always appears on EAV first. Table 2–2 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard.

The P bits are protection bits:

$$P3 = V \text{ xor } H; P2 = F \text{ xor } H; P1 = F \text{ xor } V; P0 = F \text{ xor } V \text{ xor } H$$

**Table 2–2. EAV and SAV Sequence**

|             | 8-BIT DATA |    |    |    |    |    |    |    | 10-BIT DATA |    |
|-------------|------------|----|----|----|----|----|----|----|-------------|----|
|             | D9 (MSB)   | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1          | D0 |
| Preamble    | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1           | 1  |
| Preamble    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  |
| Preamble    | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0           | 0  |
| Status word | 1          | F  | V  | H  | P3 | P2 | P1 | P0 | 0           | 0  |

## 2.7 Host Interface

Communication with the TVP5145 device is via an interface which is configurable at power up and reset to support an I<sup>2</sup>C or PHI bus host. The host interface accesses status and control registers and retrieves sliced VBI data. The host interface also initializes the TVP5145 internal microprocessor. The host port mode is selected by attaching external pullup and pulldown resistors to terminals 31 (GLCO), 32 (PALI), and 33 (FID). The TVP5145 device samples the states of these terminals at power up or at the trailing edge of RSTINB and configures the host port accordingly. Table 2–3 shows the pullup/pulldown combinations required to select each of the host port modes.

**Table 2–3. Host Port Select**

|                  | GLCO | PALI | FID |
|------------------|------|------|-----|
| I <sup>2</sup> C | 0    | 0    | 1   |
| PHI mode A       | 1    | 0    | 1   |
| PHI mode B       | 1    | 1    | 0   |
| PHI mode C       | 1    | 1    | 1   |

NOTE: 1 is pullup and 0 is pulldown.

### 2.7.1 I<sup>2</sup>C Host Port Select

The I<sup>2</sup>C standard consists of two signals, serial input/output data line (VC1) and input clock line (VC0), which carry information between the devices connected to the bus. A third signal (VC3) is used for slave address selection. Although the I<sup>2</sup>C system can be multi-mastered, the TVP5145 device functions as a slave device only.

Both SDA and SCL are lines connected to a positive supply voltage via a 2.2-k $\Omega$  pullup resistor. When the bus is free, both lines are high. The slave address select terminal (VC3) enables the use of two TVP5145 devices tied to the same I<sup>2</sup>C bus. Table 2–4 summarizes the terminal functions of the I<sup>2</sup>C-mode host interface.

**Table 2–4. I<sup>2</sup>C Host Port Terminal Description**

| SIGNAL                  | TYPE             | DESCRIPTION             |
|-------------------------|------------------|-------------------------|
| VC3 (I <sup>2</sup> CA) | I                | Slave address selection |
| VC0 (SCL)               | I                | Input clock line        |
| VC1 (SDA)               | I/O (open drain) | Input/output data line  |

Data transfer rate on the bus is up to 400 kbits/s. The number of interfaces connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the clock. During data transfer, SDA must be held stable high or low during the high period of SCL. A high-to-low transition on the SDA line while the SCL is high indicates an I<sup>2</sup>C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I<sup>2</sup>C stop condition.

Every byte placed on the SDA must be 8 bits long. Each byte must be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the I<sup>2</sup>C master.

### 2.7.1.1 I<sup>2</sup>C Write Operation

Data transfers occur utilizing the following illustrated formats.

An I<sup>2</sup>C master initiates a write operation to the TVP5145 device by generating a start condition followed by the TVP5145 I<sup>2</sup>C address 101110X, the X in the TVP5145 address is 0 when VC3 terminal is tied low and is 1 when VC3 terminal is tied high, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the TVP5145 device, the master presents the subaddress of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The TVP5145 device acknowledges each byte after completion of each transfer. The I<sup>2</sup>C master terminates the write operation by generating a stop condition.

|                                 |          |
|---------------------------------|----------|
| <b>Step 1</b>                   | <b>0</b> |
| I <sup>2</sup> C Start (master) | S        |

|                                           |          |          |          |          |          |          |          |          |
|-------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 2</b>                             | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C General address (master) | 1        | 0        | 1        | 1        | 1        | 0        | X        | 0        |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 3</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                                  |          |          |          |          |          |          |          |          |
|--------------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 4</b>                                    | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Write register address (master) | addr     | addr     | addr     | addr     | addr     | addr     | addr     | addr     |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 5</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                      |          |          |          |          |          |          |          |          |
|--------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 6</b>                        | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Write data (master) | Data     | Data     | Data     | Data     | Data     | Data     | Data     | Data     |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 7<sup>†</sup></b>            | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                |          |
|--------------------------------|----------|
| <b>Step 8</b>                  | <b>0</b> |
| I <sup>2</sup> C Stop (master) | P        |

<sup>†</sup> Repeat steps 6 and 7 until all data have been written.

### 2.7.1.2 I<sup>2</sup>C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I<sup>2</sup>C master initiates a write operation to the TVP5145 device by generating a start condition followed by the TVP5145 I<sup>2</sup>C address 101110X, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the TVP5145 device, the master presents the subaddress of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition. The second phase is the data phase. In this phase, an I<sup>2</sup>C master initiates a read operation to the TVP5145 device by generating a start condition followed by the TVP5145 I<sup>2</sup>C address 101110X, in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the TVP5145 device, the I<sup>2</sup>C master receives one or more bytes of data from the TVP5145 device. The I<sup>2</sup>C master acknowledges the transfer at the end of each byte. After the last data byte desired has been transferred from the TVP5145 device to the master, the master generates a not acknowledge followed by a stop.

### 2.7.1.3 Read Phase 1

|                                 |          |
|---------------------------------|----------|
| <b>Step 1</b>                   | <b>0</b> |
| I <sup>2</sup> C Start (master) | S        |

|                                           |          |          |          |          |          |          |          |          |
|-------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 2</b>                             | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C General address (master) | 1        | 0        | 1        | 1        | 1        | 0        | X        | 0        |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 3</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                                 |          |          |          |          |          |          |          |          |
|-------------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 4</b>                                   | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Read register address (master) | addr     | addr     | addr     | addr     | addr     | addr     | addr     | addr     |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 5</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                |          |
|--------------------------------|----------|
| <b>Step 6</b>                  | <b>0</b> |
| I <sup>2</sup> C Stop (master) | P        |

### 2.7.1.4 Read Phase 2

|                                 |          |
|---------------------------------|----------|
| <b>Step 7</b>                   | <b>0</b> |
| I <sup>2</sup> C Start (master) | S        |

|                                           |          |          |          |          |          |          |          |          |
|-------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 8</b>                             | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C General address (master) | 1        | 0        | 1        | 1        | 1        | 0        | X        | 1        |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 9</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                    |          |          |          |          |          |          |          |          |
|------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 10</b>                     | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Read data (slave) | Data     | Data     | Data     | Data     | Data     | Data     | Data     | Data     |

|                                       |          |
|---------------------------------------|----------|
| <b>Step 11<sup>†</sup></b>            | <b>9</b> |
| I <sup>2</sup> C Acknowledge (master) | A        |

|                                |          |
|--------------------------------|----------|
| <b>Step 12</b>                 | <b>0</b> |
| I <sup>2</sup> C Stop (master) | P        |

<sup>†</sup> Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

### 2.7.1.5 Microprocessor Start by I<sup>2</sup>C

After a hardware reset, the register 7Fh must be written with any data in order to start an operation of the TVP5145 device.

|                                 |          |
|---------------------------------|----------|
| <b>Step 1</b>                   | <b>0</b> |
| I <sup>2</sup> C Start (master) | S        |

|                                           |          |          |          |          |          |          |          |          |
|-------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 2</b>                             | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C General address (master) | 1        | 0        | 1        | 1        | 1        | 0        | X        | 0        |

|                                      |          |
|--------------------------------------|----------|
| <b>Step 3</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                                  |          |          |          |          |          |          |          |          |
|--------------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 4</b>                                    | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Write register address (master) | 0        | 1        | 1        | 1        | 1        | 1        | 1        | 1        |

Write to microprocessor start address = 7Fh

|                                      |          |
|--------------------------------------|----------|
| <b>Step 5</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                      |          |          |          |          |          |          |          |          |
|--------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| <b>Step 6</b>                        | <b>7</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| I <sup>2</sup> C Write data (master) | Data     | Data     | Data     | Data     | Data     | Data     | Data     | Data     |

Any data written to 7Fh starts the TVP5145 device.

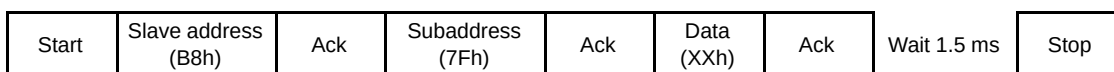
|                                      |          |
|--------------------------------------|----------|
| <b>Step 7</b>                        | <b>9</b> |
| I <sup>2</sup> C Acknowledge (slave) | A        |

|                                |          |
|--------------------------------|----------|
| <b>Step 8</b>                  | <b>0</b> |
| I <sup>2</sup> C Stop (master) | P        |

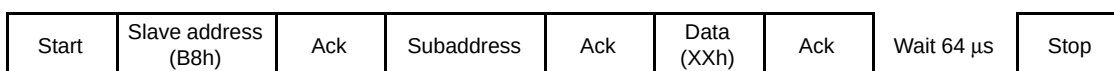
### 2.7.1.6 I<sup>2</sup>C Timing Requirements

The TVP5145 device requires delays in I<sup>2</sup>C accesses to accommodate its internal processor's timing. In accordance with I<sup>2</sup>C specifications, the TVP5145 device holds the I<sup>2</sup>C clock line (SCL) low to indicate the wait period to the I<sup>2</sup>C master. If the I<sup>2</sup>C master is not designed to check for the I<sup>2</sup>C clock line held-low condition, then the maximum delays must always be inserted where required. These delays are of variable length; maximum delays are indicated in the following diagrams:

Microprocessor start register 7Fh



Normal register writing address 00h–8Fh except 7Fh (addresses 90h–FFh do not require delays)



### 2.7.2 Parallel Host Interface (PHI)

Table 2–5 summarizes the terminal functions of the PHI-mode host interface.

**Table 2–5. PHI Host Port Terminal Description**

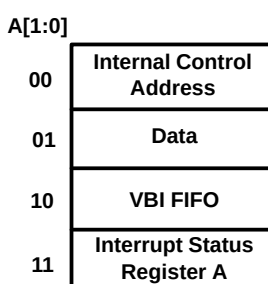
| TVP5145 TERMINAL | PHI SIGNAL NAME                  | TYPE                   | DESCRIPTION                                         |
|------------------|----------------------------------|------------------------|-----------------------------------------------------|
| VC3              | CS                               | I                      | Active low chip select                              |
| VC0              | DTACK—mode A<br>READY—modes B, C | O (see below)          | Data acknowledge—mode A<br>Data ready—modes B and C |
| VC1              | R/W—mode A<br>WR—modes B, C      | I                      | Read/Write—modes A and C<br>Write strobe—mode B     |
| VC2              | DS—mode A<br>RD—mode B           | I                      | Data strobe—mode A<br>Read strobe—mode B            |
| A1:A0            | HA[1:0]                          | I                      | Address bus from host                               |
| D7:D0            | HD[7:0]                          | I/O                    | Input/output data bus from host                     |
| INTREQ           | INTREQ                           | O (nominal open drain) | Interrupt request                                   |

Terminal 80 (INTREQ) is a nominally open drain terminal used to signal interrupts to the host controller. This terminal may be configured as a conventional CMOS I/O buffer (non-open drain) if desired using the interrupt configuration register at subaddress C2h. Contention is possible if multiple devices are connected to the INTREQ signal and it is configured in non-open drain mode.

VC0 (DTACK/READY) is in a high-impedance state when VC3 (CS) is not asserted.

### 2.7.2.1 PHI Register Mapping

The PHI module contains only four registers that are directly accessible to the host (see Figure 2–30). The address register holds an indirect address for internal control register access. When the host accesses the data register, the PHI module reads or writes the internal register selected by the indirect address register. Two other registers are provided for direct access. The FIFO register provides direct access to the VBI FIFO. The other direct access register is the interrupt status register A (C0h). This register contains the state of the interrupt sources.



**Figure 2–30. PHI Address Register Map**

Normally read or write operations require two accesses. To read the VBI FIFO register, set A[1:0] = 10b and perform a read cycle. The FIFO read data will be placed on the D[7:0] bus. To read/write interrupt status register A, set A[1:0] = 11b and perform the read/write cycle. The read/write data will be appropriately multiplexed to/from the external data bus.

### 2.7.2.2 PHI Read/Write Operation

All PHI accesses except for the VBI FIFO and the status/interrupt register require a two-step operation. To access an indirect register the desired internal address must first be written to the address register of the PHI. This is done by setting A[1:0] = 00b and performing a write cycle with D[7:0] = indirect register address. To write to an indirect register, the second step consists of writing the desired data to PHI address A[1:0] = 01b. To read an indirect register, the second step consists of reading the requested data from address 01b.

Read indirect register

| Step 1                 | A1 | A0 | D7                 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|----|----|--------------------|----|----|----|----|----|----|----|
| Write register address | 0  | 0  | Register address   |    |    |    |    |    |    |    |
| Step 2                 | A1 | A0 | D7                 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Read register data     | 0  | 1  | Data from register |    |    |    |    |    |    |    |

Write indirect register

| Step 1                 | A1 | A0 | D7               | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|----|----|------------------|----|----|----|----|----|----|----|
| Write register address | 0  | 0  | Register address |    |    |    |    |    |    |    |
| Step 2                 | A1 | A0 | D7               | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write register data    | 0  | 1  | Data to register |    |    |    |    |    |    |    |

### 2.7.2.3 Latency

PHI accesses to indirect addresses 00h–8Fh require special consideration due to response latencies of up to 64  $\mu$ s for these addresses. Latency occurs between steps 1 and 2 for a read operation, and following step 2 for a write operation. To avoid violating PHI cycle time requirements the host can poll the cycle complete bit in the PHI status register following step 1 for a read or step 2 for a write. Alternatively, the cycle complete enable bit in the interrupt enable register (indirect address C1h) can be set to generate an interrupt for the host when an access has been completed.

PHI accesses to indirect addresses 90h–CFh occur with minimal latency and interrupts will not be generated for the completion of access cycles to these addresses.

### 2.7.2.4 VBI FIFO

The VBI FIFO containing sliced VBI data can be read directly by the PHI host.

| Step 1        | A1 | A0 | D7             | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------|----|----|----------------|----|----|----|----|----|----|----|
| Read VBI FIFO | 1  | 0  | Data from FIFO |    |    |    |    |    |    |    |

### 2.7.2.5 Interrupt Status Register A

Interrupt status register A provides the host with information regarding the source of an interrupt. After an interrupt condition is set, it can be reset by writing a 1 to the appropriate bit in interrupt status register A. Section 2.12.51 contains a description of interrupt status register A.

| Step 1                           | A1 | A0 | D7                                       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----------------------------------|----|----|------------------------------------------|----|----|----|----|----|----|----|
| Access status/interrupt register | 1  | 1  | Data to/from interrupt status register A |    |    |    |    |    |    |    |

### 2.7.2.6 Microprocessor Start by PHI

After hardware reset, the register 7Fh must be written with any data in order to start an operation of the TVP5145 device.

Write indirect register

| Step 1                 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------------------------|----|----|----|----|----|----|----|----|----|----|
| Write register address | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

Write to microprocessor start address = 7Fh

| Step 2              | A1 | A0 | D7               | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------------------|----|----|------------------|----|----|----|----|----|----|----|
| Write register data | 0  | 1  | Data to register |    |    |    |    |    |    |    |

Any data written to 7Fh will start the TVP5145 device.

## 2.8 VBI Data Processor

The TVP5145 VBI data processor (VDP) slices various data services like teletext (WST, NABST), closed caption (CC), wide screen signaling (WSS), VITC, and VPS. These services are acquired by programming the VDP to enable a standard(s) in the vertical blank interval. The results are stored in a FIFO and/or registers. The teletext results are stored in a FIFO only.

Table 2–6 lists a summary of the types of vertical blank interval data supported according to the video standard. It supports both square pixel and ITU–R BT.601 sampling for each standard. The total of 26 standard modes and 2 custom modes are currently supported. One configuration for a standard mode consists of 15 bytes of data plus 1 fill byte. The custom modes are specified by the configuration data (in configuration RAM) when stored in the locations that are designated as custom.

**Table 2–6. Data Types Supported by the VDP**

| LINE MODE<br>REGISTER (D0h–FCh)<br>BITS [3:0] | SAMPLING<br>RATE (0Dh)<br>BIT 7 | NAME              | DESCRIPTION                                         |
|-----------------------------------------------|---------------------------------|-------------------|-----------------------------------------------------|
| 0000b                                         | 0                               | WST SECAM S       | Teletext, SECAM, Square                             |
| 0000b                                         | 1                               | WST SECAM 6       | Teletext, SECAM, ITU–R BT 601                       |
| 0001b                                         | 0                               | WST PAL B S       | Teletext, PAL, System B, Square                     |
| 0001b                                         | 1                               | WST PAL B 6       | Teletext, PAL, System B, ITU–R BT 601               |
| 0010b                                         | 0                               | WST PAL C S       | Teletext, PAL, System C, Square                     |
| 0010b                                         | 1                               | WST PAL C 6       | Teletext, PAL, System C, ITU–R BT 601               |
| 0011b                                         | 0                               | WST, NTSC B S     | Teletext, NTSC, System B, Square                    |
| 0011b                                         | 1                               | WST, NTSC B 6     | Teletext, NTSC, System B, ITU–R BT 601              |
| 0100b                                         | 0                               | NABTS, NTSC C S   | Teletext, NTSC, System C, Square                    |
| 0100b                                         | 1                               | NABTS, NTSC C 6   | Teletext, NTSC, System C, ITU–R BT 601              |
| 0101b                                         | 0                               | NABTS, NTSC D S   | Teletext, NTSC, System D (Japan), Square            |
| 0101b                                         | 1                               | NABTS, NTSC D 6   | Teletext, NTSC, System D (Japan), ITU–R BT 601      |
| 0110b                                         | 0                               | CC, PAL/SECAM S   | Closed Caption PAL/SECAM, Square                    |
| 0110b                                         | 1                               | CC, PAL/SECAM 6   | Closed Caption PAL/SECAM, ITU–R BT 601              |
| 0111b                                         | 0                               | CC, NTSC S        | Closed Caption NTSC, Square                         |
| 0111b                                         | 1                               | CC, NTSC 6        | Closed Caption NTSC, ITU–R BT 601                   |
| 1000b                                         | 0                               | WSS, PAL/SECAM S  | Wide Screen signal, PAL/SECAM, Square               |
| 1000b                                         | 1                               | WSS, PAL/SECAM 6  | Wide Screen signal, PAL/SECAM, ITU–R BT 601         |
| 1001b                                         | 0                               | WSS, NTSC S       | Wide Screen signal, NTSC, Square                    |
| 1001b                                         | 1                               | WSS, NTSC 6       | Wide Screen signal, NTSC, ITU–R BT 601              |
| 1010b                                         | 0                               | VITC, PAL/SECAM S | Vertical Interval timecode, PAL/SECAM, Square       |
| 1010b                                         | 1                               | VITC, PAL/SECAM 6 | Vertical Interval timecode, PAL/SECAM, ITU–R BT 601 |
| 1011b                                         | 0                               | VITC, NTSC S      | Vertical Interval timecode, NTSC, Square            |
| 1011b                                         | 1                               | VITC, NTSC 6      | Vertical Interval timecode, NTSC, ITU–R BT 601      |
| 1100b                                         | 0                               | VPS, PAL S        | Video Program System, PAL, Square                   |
| 1100b                                         | 1                               | VPS, PAL 6        | Video Program System, PAL, ITU–R BT 601             |
| 1101b                                         |                                 | Custom            | Custom                                              |
| 1110b                                         |                                 | Custom            | Custom                                              |
| 1111b                                         | x                               | Active Video      | Active Video/Full Field                             |

At powerup the host interface is required to program the VDP-configuration RAM (VDP-CRAM) contents with the lookup table (see Section 2.12.54). This is done through port address C3h. Each read from or write to this address will auto increment an internal counter to the next RAM location. To access the VDP–CRAM, the line mode registers (D0h–FCh) must be programmed with FFh to avoid a conflict with the microprocessor and the VDP in both writing and reading. Full field mode must also be disabled.

Available VBI lines are from line 6 to line 27 of both field 1 and field 2. Theoretically, each line can be any VBI mode because the VDP processes VBI data on a line-by-line basis. When changing modes, the VDP must allow the current transaction to complete through the delays of the VDP before loading the configuration for the next line into the VDP core. It must also complete loading the configuration before the next line starts processing. The switch pixel number is set through registers CBh and CCh. The default values of CBh and CCh work for all standard modes.

Output data is available either through the VBI-FIFO (B0h) or through dedicated registers at 90h–AFh, both of which are available from the host port.



## 2.8.1 VBI FIFO and Ancillary Data in Video Stream

Sliced VBI data can be output as ancillary data in the video stream in ITU-R BT.656 mode. VBI data is output on the Y[9:2] terminals during the horizontal blanking period following the line from which the data was retrieved. Table 2–7 shows the header format and sequence of the ancillary data inserted into the video stream. This format is also used to store any VBI data into the FIFO. The size of the FIFO is 512 bytes. Therefore, the FIFO can store up to 11 lines of teletext data with the NTSC NABTS standard.

**Table 2–7. Ancillary Data Format and Sequence**

| BYTE NO. | D7 (MSB)           | D6 | D5      | D4         | D3       | D2       | D1                 | D0 (LSB) | DESCRIPTION                |                      |  |
|----------|--------------------|----|---------|------------|----------|----------|--------------------|----------|----------------------------|----------------------|--|
| 0        | 0                  | 0  | 0       | 0          | 0        | 0        | 0                  | 0        | Ancillary data preamble    |                      |  |
| 1        | 1                  | 1  | 1       | 1          | 1        | 1        | 1                  | 1        |                            |                      |  |
| 2        | 1                  | 1  | 1       | 1          | 1        | 1        | 1                  | 1        |                            |                      |  |
| 3        | NEP                | EP | 0       | 1          | 0        | DID2     | DID1               | DID0     | Data ID (DID)              |                      |  |
| 4        | NEP                | EP | F5      | F4         | F3       | F2       | F1                 | F0       | Secondary data ID (SDID)   |                      |  |
| 5        | NEP                | EP | N5      | N4         | N3       | N2       | N1                 | N0       | Number of 32 bit data (NN) |                      |  |
| 6        | Video line # [7:0] |    |         |            |          |          |                    |          | Internal Data ID0 (IDID0)  |                      |  |
| 7        | 0                  | 0  | 0       | Data error | Match #1 | Match #2 | Video line # [9:8] |          | Internal Data ID1 (IDID1)  |                      |  |
| 8        | 1. Data            |    |         |            |          |          |                    |          | Data byte                  | 1 <sup>st</sup> word |  |
| 9        | 2. Data            |    |         |            |          |          |                    |          | Data byte                  |                      |  |
| 10       | 3. Data            |    |         |            |          |          |                    |          | Data byte                  |                      |  |
| 11       | 4. Data            |    |         |            |          |          |                    |          | Data byte                  |                      |  |
| :        | :                  |    |         |            |          |          |                    |          | :                          |                      |  |
|          | m-1. Data          |    |         |            |          |          |                    |          | Data byte                  | N <sup>th</sup> word |  |
|          | m. Data            |    |         |            |          |          |                    |          | Data byte                  |                      |  |
|          | NEP                | EP | CS[5:0] |            |          |          |                    |          | Check sum                  |                      |  |
| 4N+7     | 0                  | 0  | 0       | 0          | 0        | 0        | 0                  | 0        | Fill byte                  |                      |  |

EP: Even parity for D0–D5      NEP: Negated even parity

DID: 91h: Sliced data of VBI lines of first field  
53h: Sliced data of line 24 to end of first field  
55h: Sliced data of VBI lines of second field  
97h: Sliced data of line 24 to end of second field

SDID: This field holds the data format taken from the line mode register of the corresponding line.

NN: Number of Dwords beginning with byte 8 through 4N+7. Note this value is the number of Dwords where each Dword is 4 bytes.

IDID0: Transaction video line number [7:0]

IDID1: Bit 0/1 = Transaction video line number [9:8]  
Bit 2 = Match 2 flag  
Bit 3 = Match 1 flag  
Bit 4 = 1 if an error was detected in the EDC block. 0 if not.

CS: Sum of D0–D7 of DID through last data byte.

Fill byte: Fill bytes make a multiple of 4 bytes from byte 0 to last fill byte. For teletext modes, byte 8 is the sync pattern byte. Byte 9 is '1. Data.'

## 2.9 Raw Video Data Output

The TVP5145 device can output raw A/D video data at twice the sampling rate for external VBI slicing. This is transmitted as an ancillary data block, although a bit differently from the way the sliced VBI data is transmitted in the FIFO format as described in Section 2.8.1. First, the samples are transmitted during the active portion of the line. The ITU-R BT.656 specification requires that a preamble code of 00h FFh FFh ZZh be transmitted where, if ZZh is anything other than 15h, it indicates the presence of ancillary data immediately following the preamble. The TVP5145 device outputs ZZh = 60h. Also, a preamble of 00h FFh FFh 15h must be inserted after the ancillary data to indicate that the remainder of the line is available for the insertion of further ancillary signals.

## 2.10 Reset and Initialization

Reset is initiated at power up or any time terminal 23 (RSTINB) is brought low. Table 2–8 describes the status of the TVP5145 terminals during and immediately after reset.

**Table 2–8. Reset Sequence**

| SIGNAL NAME                                    | DURING RESET                                                                                     | RESET COMPLETED                                                                                         |
|------------------------------------------------|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|
| Y[9:0], UV[9:0], HSYN, VSYN, FID, PALI         | Input                                                                                            | High-impedance if AVID is pulled down during reset.<br>Active output if AVID is pulled up during reset. |
| AVID                                           | Input                                                                                            | High-impedance if AVID is pulled down during reset.<br>Active output if AVID is pulled up during reset. |
| SCLK, PCLK                                     | High-impedance if PREF is pulled down during reset.<br>Active if PREF is pulled up during reset. | Active output                                                                                           |
| PREF                                           | Input                                                                                            | Active output                                                                                           |
| GLCO                                           | Input                                                                                            | Active output                                                                                           |
| VC0                                            | High-impedance                                                                                   | High-impedance                                                                                          |
| D[7:0]                                         | Input                                                                                            | High-impedance                                                                                          |
| A[1:0] in PHI mode                             | Input                                                                                            | Input                                                                                                   |
| RSTINB, SDA, SCL, I <sup>2</sup> CA, OEB, GPCL | Input                                                                                            | Input                                                                                                   |

After hardware reset, the register 7Fh must be written with any data in order to start the operation of the TVP5145 device.

## 2.11 Internal Control Registers

The TVP5145 device is initialized and controlled by a set of internal registers which set all the device operating parameters. Communication between the external controller and the TVP5145 device is through a standard host port. Table 2–9 shows the summary of these registers. The reserved registers must not be written. However, reserved bits in the defined registers must be written with 0s. The detailed programming information of each register is described in the following sections.

**Table 2–9. Registers Summary**

| REGISTER FUNCTION                  | ADDRESS | DEFAULT | R/W |
|------------------------------------|---------|---------|-----|
| Video input source selection #1    | 00h     | 00h     | R/W |
| Analog channel controls            | 01h     | 15h     | R/W |
| Operation mode controls            | 02h     | 00h     | R/W |
| Miscellaneous controls             | 03h     | 19h/01h | R/W |
| Reserved                           | 04h–05h |         |     |
| Color killer threshold control     | 06h     | 00h     | R/W |
| Luminance processing control #1    | 07h     | 00h     | R/W |
| Luminance processing control #2    | 08h     | 00h     | R/W |
| Brightness control                 | 09h     | 80h     | R/W |
| Color saturation control           | 0Ah     | 80h     | R/W |
| Hue control                        | 0Bh     | 00h     | R/W |
| Contrast control                   | 0Ch     | 80h     | R/W |
| Outputs and data rates select      | 0Dh     | 40h     | R/W |
| Luminance processing control #3    | 0Eh     | 00h     | R/W |
| Reserved                           | 0Fh–10h |         |     |
| AVID start pixel MSB               | 11h     | 00h     | R/W |
| AVID start pixel LSB               | 12h     | 00h     | R/W |
| AVID stop pixel MSB                | 13h     | 00h     | R/W |
| AVID stop pixel LSB                | 14h     | 00h     | R/W |
| GLCO/RTC                           | 15h     | 01h     | R/W |
| Horizontal sync start              | 16h     | 80h     | R/W |
| Reserved                           | 17h     |         |     |
| Vertical blanking start            | 18h     | 00h     | R/W |
| Vertical blanking stop             | 19h     | 00h     | R/W |
| Chrominance processing control #1  | 1Ah     | 0Ch     | R/W |
| Chrominance processing control #2  | 1Bh     | 14h     | R/W |
| Interrupt reset register B         | 1Ch     | 00h     | R/W |
| Interrupt enable register B        | 1Dh     | 00h     | R/W |
| Interrupt configuration register B | 1Eh     | 00h     | R/W |
| Reserved                           | 1Fh     |         |     |
| Video input source selection #2    | 20h     | 00h     | R/W |
| Reserved                           | 21h–25h |         |     |
| Crystal frequency                  | 26h     | 00h     | R/W |
| Reserved                           | 27h     |         |     |
| Video standard                     | 28h     | 00h     | R/W |
| Reserved                           | 29h–7Eh |         |     |
| Microprocessor start               | 7Fh     | 00h     | W   |
| Major ROM version                  | 80h     |         | R   |
| Status register #1                 | 81h     |         | R   |
| Status register #2                 | 82h     |         | R   |

R = Read only

W = Write only

R/W = Read and write

**Table 2–9. Registers Summary (Continued)**

| REGISTER FUNCTION                   | ADDRESS  | DEFAULT | R/W |
|-------------------------------------|----------|---------|-----|
| Status register #3                  | 83h      |         | R   |
| Status register #4                  | 84h      |         | R   |
| Interrupt status register B         | 85h      |         | R   |
| Interrupt active register B         | 86h      |         | R   |
| Minor ROM version                   | 87h      |         | R   |
| Status register #5                  | 88h      |         | R   |
| Vertical line count                 | 89h–8Ah  |         | R   |
| Analog die ID                       | 8Bh      |         | R   |
| Digital die ID                      | 8Ch      |         | R   |
| Reserved                            | 8Dh–8Fh  |         |     |
| Closed caption data registers       | 90h–93h  |         | R   |
| WSS data registers                  | 94h–99h  |         | R   |
| VPS data registers                  | 9Ah–A6h  |         | R   |
| VITC data registers                 | A7h–AFh  |         | R   |
| VBI FIFO read data                  | B0h      |         | R   |
| Teletext filter 1                   | B1h–B5h  | 00h     | R/W |
| Teletext filter 2                   | B6h–BAh  | 00h     | R/W |
| Teletext filter control             | BBh      | 00h     | R/W |
| Reserved                            | BC h–BFh |         |     |
| Interrupt status register A         | C0h      | 00h     | R/W |
| Interrupt enable register A         | C1h      | 00h     | R/W |
| Interrupt configuration register A  | C2h      | 04h     | R/W |
| VDP configuration RAM data          | C3h      | 00h     | R/W |
| Configuration RAM address low byte  | C4h      | 00h     | R/W |
| Configuration RAM address high byte | C5h      | 00h     | R/W |
| VDP status register                 | C6h      | 40h     | R/W |
| FIFO word count                     | C7h      |         | R   |
| FIFO interrupt threshold            | C8h      | 80h     | R/W |
| FIFO reset                          | C9h      | 00h     | W   |
| Line number interrupt               | CAh      | 00h     | R/W |
| Pixel alignment register low byte   | CBh      | 59h     | R/W |
| Pixel alignment register high byte  | CCh      | 03h     | R/W |
| FIFO output control                 | CDh      | 01h     | R/W |
| VDP clock                           | CEh      | 00h     | R/W |
| Full field enable                   | CFh      | 00h     | R/W |
| Line mode registers                 | D0h–FBh  | FFh     | R/W |
| Full field mode register            | FCh      | 7Fh     | R/W |
| Reserved                            | FDh–FFh  |         |     |

R = Read only

W = Write only

R/W = Read and write

## 2.12 Register Definitions

### 2.12.1 Video Input Source Selection #1 Register

|         |     |
|---------|-----|
| Address | 00h |
|---------|-----|

| 7        | 6 | 5 | 4 | 3                     | 2              | 1                          | 0                            |
|----------|---|---|---|-----------------------|----------------|----------------------------|------------------------------|
| Reserved |   |   |   | Channel 2,3 selection | Component mode | Channel 1 source selection | Channel 2,3 source selection |

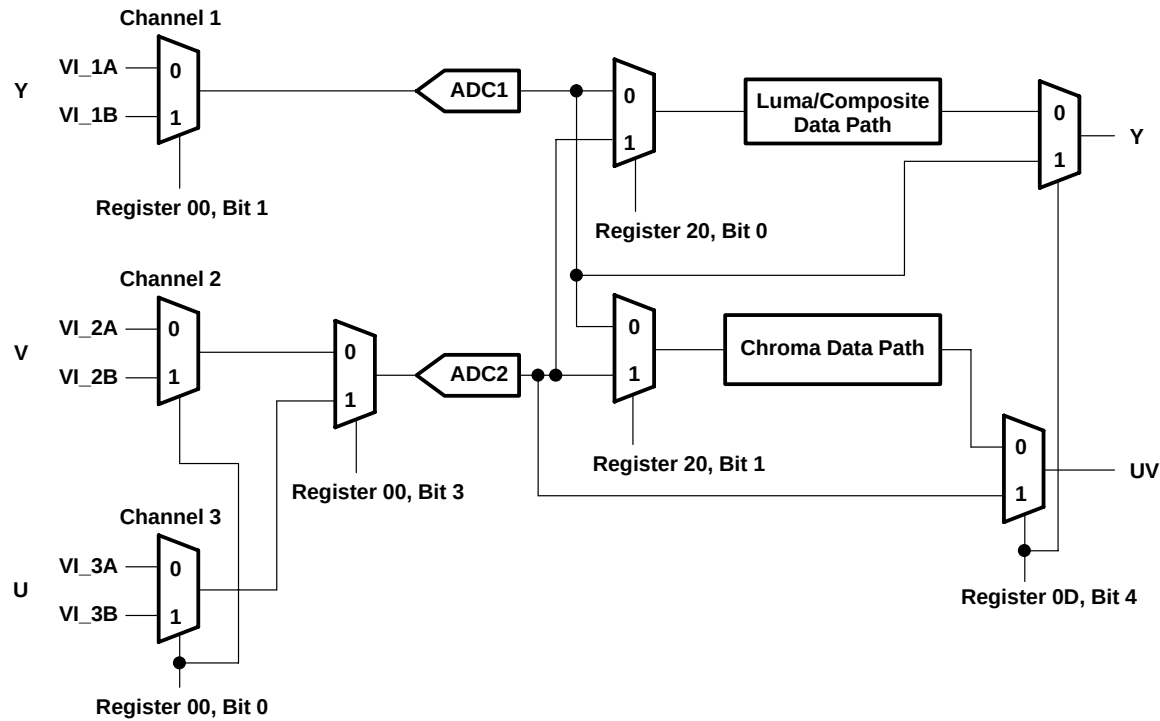


Figure 2–31. Video Input Source Selection

Channels 2,3 selection:

- 0 = Channel 2 selected (default)
- 1 = Channel 3 selected

Component mode:

- 0 = Component mode off (default)
- 1 = Component mode on, Channel 2,3 selection disabled

Channel 1 source selection:

- 0 = VI\_1A selected (default)
- 1 = VI\_1B selected

Channels 2,3 source selection:

- 0 = VI\_2A, VI\_3A selected (default)
- 1 = VI\_2B, VI\_3B selected

**Table 2–10. Analog Channel and Video Mode Selection**

|           | INPUT(S) SELECTED  | ADDRESS 00 |       |       |       | ADDRESS 20 |       |
|-----------|--------------------|------------|-------|-------|-------|------------|-------|
|           |                    | BIT 3      | BIT 2 | BIT 1 | BIT 0 | BIT 1      | BIT 0 |
| Composite | 1A (default)       | X          | 0     | 0     | X     | 0          | 0     |
|           | 1B                 | X          | 0     | 1     | X     | 0          | 0     |
|           | 2A                 | 0          | 0     | X     | 0     | 1          | 1     |
|           | 2B                 | 0          | 0     | X     | 1     | 1          | 1     |
|           | 3A                 | 1          | 0     | X     | 0     | 1          | 1     |
|           | 3B                 | 1          | 0     | X     | 1     | 1          | 1     |
| S-Video   | 1A luma, 2A chroma | 0          | 0     | 0     | 0     | 1          | 0     |
|           | 1A luma, 2B chroma | 0          | 0     | 0     | 1     | 1          | 0     |
|           | 1A luma, 3A chroma | 1          | 0     | 0     | 0     | 1          | 0     |
|           | 1A luma, 3B chroma | 1          | 0     | 0     | 1     | 1          | 0     |
|           | 1B luma, 2A chroma | 0          | 0     | 1     | 0     | 1          | 0     |
|           | 1B luma, 2B chroma | 0          | 0     | 1     | 1     | 1          | 0     |
|           | 1B luma, 3A chroma | 1          | 0     | 1     | 0     | 1          | 0     |
|           | 1B luma, 3B chroma | 1          | 0     | 1     | 1     | 1          | 0     |
|           | 2A luma, 1A chroma | 0          | 0     | 0     | 0     | 0          | 1     |
|           | 2A luma, 1B chroma | 0          | 0     | 1     | 0     | 0          | 1     |
|           | 2B luma, 1A chroma | 0          | 0     | 0     | 1     | 0          | 1     |
|           | 2B luma, 1B chroma | 0          | 0     | 1     | 1     | 0          | 1     |
|           | 3A luma, 1A chroma | 1          | 0     | 0     | 0     | 0          | 1     |
|           | 3A luma, 1B chroma | 1          | 0     | 1     | 0     | 0          | 1     |
|           | 3B luma, 1A chroma | 1          | 0     | 0     | 1     | 0          | 1     |
|           | 3B luma, 1B chroma | 1          | 0     | 1     | 1     | 0          | 1     |
| Component | 1A Y, 2A Pr, 3A Pb | X          | 1     | 0     | 0     | 1          | 0     |
|           | 1B Y, 2B Pr, 3B Pb | X          | 1     | 1     | 1     | 1          | 0     |

### 2.12.2 Analog Channel Controls Register

|         |     |
|---------|-----|
| Address | 01h |
|---------|-----|

| 7        | 6 | 5                                   | 4 | 3                                   | 2 | 1                      | 0 |
|----------|---|-------------------------------------|---|-------------------------------------|---|------------------------|---|
| Reserved |   | Automatic offset control, channel 2 |   | Automatic offset control, channel 1 |   | Automatic gain control |   |

Automatic offset control, channel 2:

- 00 = Reserved
- 01 = Automatic offset enabled (default)
- 10 = Reserved
- 11 = Clamping level frozen to the previously set value

Automatic offset control, channel 1:

- 00 = Reserved
- 01 = Automatic offset enabled (default)
- 10 = Reserved
- 11 = Clamping level frozen to the previously set value

Automatic gain control (AGC):

- 00 = Reserved
- 01 = AGC enabled using luma input as the reference (default)
- 10 = Reserved
- 11 = AGC frozen to the previously set value

### 2.12.3 Operation Mode Controls Register

|         |     |
|---------|-----|
| Address | 02h |
|---------|-----|

| 7        | 6 | 5           | 4 | 3        | 2                           | 1        | 0               |
|----------|---|-------------|---|----------|-----------------------------|----------|-----------------|
| Reserved |   | TV/VCR mode |   | Reserved | Color subcarrier PLL frozen | Reserved | Power down mode |

TV/VCR mode:

- 00 = Automatic, mode determined by the internal detection circuit (default)
- 01 = Reserved
- 10 = VCR (nonstandard video) mode
- 11 = TV (standard video) mode

With automatic detection enabled, unstable or nonstandard syncs on input video will force the device into VCR mode. This turns off the luminance and chrominance comb filters and turns on the chroma trap filter.

Color subcarrier PLL frozen:

- 0 = Color subcarrier PLL increments by the internally generated phase increment. (default)  
GLCO pin outputs the frequency increment
- 1 = Color subcarrier PLL stops incrementing.  
GLCO pin outputs the frozen frequency increment

Power down mode:

- 0 = Normal operation (default)
- 1 = Power down mode. A/Ds are turned off and internal clocks are reduced to minimum.

## 2.12.4 Miscellaneous Control Register

|         |     |
|---------|-----|
| Address | 03h |
|---------|-----|

| 7                        | 6                                    | 5                   | 4                                         | 3        | 2                        | 1                   | 0 |
|--------------------------|--------------------------------------|---------------------|-------------------------------------------|----------|--------------------------|---------------------|---|
| GPCL pin function select | PALI pin and FID pin function select | Y U/V output enable | HSYN, VSYN, AVID, FID, PALI output enable | Reserved | Vertical blanking on/off | Clock output enable |   |

GPCL pin function select:

00 = GPCL is logic 0 output (default)

01 = GPCL is logic 1 output

10 = GPCL is vertical blank output. The vertical blanking on/off bit is used to activate the output.

11 = GPCL is external sync lock control input. All clocks and synchronization signals to assume nominal values. The sync lock control input is active high.

PALI pin and FID pin function select:

0 = PALI outputs PAL indicator signal and pin FID outputs field ID signal (default)

1 = PALI outputs horizontal lock indicator (HLK) and pin FID outputs vertical lock indicator (VLK)

Y U/V output enable:

0 = Y U/V high impedance

1 = Y U/V active

This bit defaults to 0 after reset if terminal 28 (AVID) is pulled down during reset or defaults to 1 if terminal 28 (AVID) is pulled up during reset.

Horizontal sync (HSYN), vertical sync (VSYN), active video indicator (AVID), PALI, and FID output enables:

0 = HSYN, VSYN, AVID, PALI, and FID are high-impedance

1 = HSYN, VSYN, AVID, PALI, and FID are active

This bit defaults to 0 after reset if terminal 28 (AVID) is pulled down during reset or defaults to 1 if terminal 28 (AVID) is pulled up during reset.

Vertical blanking on/off:

0 = Vertical blanking off (default)

1 = Vertical blanking on

Clock output enable:

0 = SCLK and PCLK outputs are high-impedance

1 = SCLK and PCLK outputs are enabled (default)

**Table 2–11. Digital Output Control**

| Terminal 24 (OEB) | Terminal 28 (AVID) | Register 03, Bit 4 (TVPOE) | Register C2, Bit 2 (VDPOE) | YUV Output                 | Notes                                                                                             |
|-------------------|--------------------|----------------------------|----------------------------|----------------------------|---------------------------------------------------------------------------------------------------|
| 1                 | X                  | X                          | X                          | High impedance             | At all times                                                                                      |
| 0                 | 1 during reset     | X                          | X                          | Active after reset         | After reset and before YUV output enable bits are programmed. TVPOE defaults to 1 and VDPOE is 1. |
| 0                 | 0 during reset     | X                          | X                          | High impedance after reset | After reset and before YUV output enable bits are programmed. TVPOE defaults to 0 and VDPOE is 1. |
| 0                 | X                  | 0                          | X                          | High impedance             | After both YUV output enable bits are programmed.                                                 |
| 0                 | X                  | X                          | 0                          | High impedance             | After both YUV output enable bits are programmed.                                                 |
| 0                 | X                  | 1                          | 1                          | Active                     | After both YUV output enable bits are programmed.                                                 |



### 2.12.5 Color Killer Threshold Control Register

|         |     |
|---------|-----|
| Address | 06h |
|---------|-----|

| 7        | 6                      | 5 | 4                      | 3 | 2 | 1 | 0 |
|----------|------------------------|---|------------------------|---|---|---|---|
| Reserved | Automatic color killer |   | Color killer threshold |   |   |   |   |

Automatic color killer:

- 00 = Automatic mode (default)
- 01 = Reserved
- 10 = Color killer enabled, the UV terminals are forced to a zero color state.
- 11 = Color killer disabled

Color killer threshold:

- 11111 = -30 dB
- 10000 = -24 dB
- 00000 = -18 dB (default)

### 2.12.6 Luminance Processing Control #1 Register

|         |     |
|---------|-----|
| Address | 07h |
|---------|-----|

| 7                | 6                    | 5        | 4                                 | 3                                                         | 2 | 1 | 0 |
|------------------|----------------------|----------|-----------------------------------|-----------------------------------------------------------|---|---|---|
| Luma bypass mode | Pedestal not present | Reserved | Luma bypass during vertical blank | Luminance signal delay with respect to chrominance signal |   |   |   |

Luma bypass mode:

- 0 = Input video bypasses the chroma trap and comb filters. Chroma outputs are forced to zero. (default)
- 1 = Input video bypasses the whole luma processing. Raw A/D data is output alternatively as UV data and Y data at SCLK rate. The output data is properly clipped to comply to ITU-R BT.601 coding range. Only valid for 10-bit YUV output format (YUV output format = 100 or 111 at register 0Dh).

Pedestal not present:

- 0 = 7.5 IRE pedestal is present on the analog video input signal (default)
- 1 = Pedestal is not present on the analog video input signal

Luminance bypass enabled during vertical blanking:

- 0 = Disabled (default)
- 1 = Enabled

Luminance bypass will occur for the duration of the vertical blanking as defined by registers 18h and 19h. This feature may be used to prevent distortion of test and data signals present during the vertical blanking interval.

Luma signal delay with respect to chroma signal in pixel clock increments (range -8 to +7 pixel clocks):

- 1111 = -8 pixel clocks delay
- 1011 = -4 pixel clocks delay
- 1000 = -1 pixel clocks delay
- 0000 = 0 pixel clocks delay (default)
- 0011 = 3 pixel clocks delay
- 0111 = 7 pixel clocks delay

### 2.12.7 Luminance Processing Control #2 Register

|         |     |
|---------|-----|
| Address | 08h |
|---------|-----|

|          |                         |          |   |              |   |          |   |
|----------|-------------------------|----------|---|--------------|---|----------|---|
| 7        | 6                       | 5        | 4 | 3            | 2 | 1        | 0 |
| Reserved | Luminance filter select | Reserved |   | Peaking gain |   | Reserved |   |

Luminance filter select:

- 0 = Luminance comb filter enabled (default)
- 1 = Luminance chroma trap filter enabled

Peaking gain:

- 00 = 0 (default)
- 01 = 0.5
- 10 = 1
- 11 = 2

Refer to Figure 2–16, Figure 2–17, and Figure 2–18.

### 2.12.8 Brightness Control Register

|         |     |
|---------|-----|
| Address | 09h |
|---------|-----|

|                    |   |   |   |   |   |   |   |
|--------------------|---|---|---|---|---|---|---|
| 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Brightness control |   |   |   |   |   |   |   |

Brightness control:

- 1111 1111 = 255 (bright)
- 1000 1011 = 139 (ITU-R BT.601 level)
- 1000 0000 = 128 (default)
- 0000 0000 = 0 (dark)

### 2.12.9 Color Saturation Control Register

|         |     |
|---------|-----|
| Address | 0Ah |
|---------|-----|

|                    |   |   |   |   |   |   |   |
|--------------------|---|---|---|---|---|---|---|
| 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Saturation control |   |   |   |   |   |   |   |

Saturation control:

- 1111 1111 = 255 (maximum)
- 1000 0000 = 128 (default)
- 0000 0000 = 0 (no color)

### 2.12.10 Hue Control Register

|         |     |
|---------|-----|
| Address | 0Bh |
|---------|-----|

|             |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|
| 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Hue control |   |   |   |   |   |   |   |

Hue control (does not apply to component video and SECAM):

- 0111 1111 = +180 degrees
- 0000 0000 = 0 degrees (default)
- 1000 0000 = –180 degrees

### 2.12.11 Contrast Control Register

|         |     |
|---------|-----|
| Address | 0Ch |
|---------|-----|

|                  |   |   |   |   |   |   |   |
|------------------|---|---|---|---|---|---|---|
| 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Contrast control |   |   |   |   |   |   |   |

Contrast control:

1111 1111 = 255 (maximum contrast)

1000 0000 = 128 (default)

0000 0000 = 0 (minimum contrast)

### 2.12.12 Outputs and Data Rates Select Register

|         |     |
|---------|-----|
| Address | 0Dh |
|---------|-----|

|               |                       |                |                      |                   |   |   |   |
|---------------|-----------------------|----------------|----------------------|-------------------|---|---|---|
| 7             | 6                     | 5              | 4                    | 3                 | 2 | 1 | 0 |
| Sampling rate | YUV output code range | UV code format | YUV data path bypass | YUV output format |   |   |   |

Sampling rate (changing this bit causes the register settings to be reinitialized):

0 = ITU-R BT.601 sampling rate (default)

1 = Square pixel sampling rate

YUV output code range:

0 = ITU-R BT.601 coding range (Y ranges from 64 to 940. U and V range from 64 to 960)

1 = Extended coding range (Y, U, and V range from 4 to 1016) (default)

UV code format:

0 = Offset binary code (2's complement + 512) (default)

1 = Straight binary code (2's complement)

YUV data path bypass:

00 = Normal operation (default)

01 = Digital composite output pins connected to decimation filter output, decoder function bypassed.  
Both Y and UV buses output data at PCLK rate.

10 = YUV output pins connected to A/D output, decoder function bypassed. Both Y and UV buses  
output data at SCLK rate.

11 = Reserved

YUV output format:

000 = 20-/16-bit 4:2:2 YUV with discrete sync output (default)

001 = Reserved

010 = Reserved

011 = Reserved

100 = 10-/8-bit 4:2:2 UYVYUYVY

101 = Reserved

110 = Reserved

111 = 10-/8-bit ITU-R BT.656 interface with embedded sync output

### 2.12.13 Luminance Control #3 Register

|         |     |
|---------|-----|
| Address | 0Eh |
|---------|-----|

|          |   |   |   |   |   |                    |   |
|----------|---|---|---|---|---|--------------------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1                  | 0 |
| Reserved |   |   |   |   |   | Trap filter select |   |

Trap filter select:

- 00 = No notch (default)
- 01 = Notch 1
- 10 = Notch 2
- 11 = Notch 3

Please refer to Figure 2–11 through Figure 2–14 for the frequency responses of the filters.

### 2.12.14 AVID Start Pixel MSB

|         |     |
|---------|-----|
| Address | 11h |
|---------|-----|

|                      |   |   |   |   |   |   |   |
|----------------------|---|---|---|---|---|---|---|
| 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AVID start pixel MSB |   |   |   |   |   |   |   |

AVID start pixel MSB: The eight MSBs of the 10-bit AVID start pixel. AVID is adjustable with respect to the active video period.

### 2.12.15 AVID Start Pixel LSB

|         |     |
|---------|-----|
| Address | 12h |
|---------|-----|

|          |   |   |   |   |             |                      |   |
|----------|---|---|---|---|-------------|----------------------|---|
| 7        | 6 | 5 | 4 | 3 | 2           | 1                    | 0 |
| Reserved |   |   |   |   | AVID active | AVID start pixel LSB |   |

AVID active:

- 0 = Avid out active in VBLK (default)
- 1 = Avid out inactive in VBLK

AVID start pixel LSB: The two LSBs of the 10-bit AVID start pixel. The TVP5145 device updates the AVID start only when this register is written to.

AVID start pixel:

- 01 1111 1111 = 511
- 00 0000 0001 = 1
- 00 0000 0000 = 0 (default) (see Figure 2–28)
- 11 1111 1111 = –1
- 10 0000 0000 = –512

### 2.12.16 AVID Stop Pixel MSB

|         |     |
|---------|-----|
| Address | 13h |
|---------|-----|

|                     |   |   |   |   |   |   |   |
|---------------------|---|---|---|---|---|---|---|
| 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AVID stop pixel MSB |   |   |   |   |   |   |   |

AVID stop pixel MSB: The eight MSBs of the 10-bit AVID stop pixel.

### 2.12.17 AVID Stop Pixel LSB

|         |     |
|---------|-----|
| Address | 14h |
|---------|-----|

|          |   |   |   |   |   |                     |   |
|----------|---|---|---|---|---|---------------------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1                   | 0 |
| Reserved |   |   |   |   |   | AVID stop pixel LSB |   |

AVID stop pixel LSB: The two LSBs of the 10-bit AVID stop pixel. The TVP5145 device updates the AVID stop only when this register is written to. The number of pixels of active video must be an even number.

AVID stop pixel:

01 1111 1111 = 511  
00 0000 0001 = 1  
00 0000 0000 = 0 (default) (see Figure 2–28)  
11 1111 1111 = –1  
10 0000 0000 = –512

### 2.12.18 GLCO and RTC Register

|         |     |
|---------|-----|
| Address | 15h |
|---------|-----|

|          |   |   |   |   |   |   |           |
|----------|---|---|---|---|---|---|-----------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0         |
| Reserved |   |   |   |   |   |   | GLCO/ RTC |

GLCO/RTC:

0 = GLCO output  
1 = RTC output (default)

Figure 2–22 shows the timing of GLCO and Figure 2–23 shows the timing of RTC.

### 2.12.19 Horizontal Sync (HSYN) Start Register

|         |     |
|---------|-----|
| Address | 16h |
|---------|-----|

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSYN start |   |   |   |   |   |   |   |

HSYN start:

1111 1111 = –127 x 4 pixel clocks  
1111 1110 = –126 x 4 pixel clocks  
1111 1101 = –125 x 4 pixel clocks  
1000 0000 = 0 pixel clocks (default) (see Figure 2–28)  
0111 1111 = 1 x 4 pixel clocks  
0111 1110 = 2 x 4 pixel clocks  
0000 0000 = 128 x 4 pixel clocks

### 2.12.20 Vertical Blanking Start Register

|         |     |
|---------|-----|
| Address | 18h |
|---------|-----|

|                         |   |   |   |   |   |   |   |
|-------------------------|---|---|---|---|---|---|---|
| 7                       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Vertical blanking start |   |   |   |   |   |   |   |

Vertical blanking (VBLK) start:

- 0111 1111 = 127 lines after start of vertical blanking interval
- 0000 0001 = 1 line after start of vertical blanking interval
- 0000 0000 = Same time as start of vertical blanking interval (default) (see Figure 2–27)
- 1000 0001 = 1 line before start of vertical blanking interval
- 1111 1111 = 128 lines before start of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h) and vertical AVID cropping.

### 2.12.21 Vertical Blanking Stop Register

|         |     |
|---------|-----|
| Address | 19h |
|---------|-----|

|                        |   |   |   |   |   |   |   |
|------------------------|---|---|---|---|---|---|---|
| 7                      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Vertical blanking stop |   |   |   |   |   |   |   |

Vertical blanking (VBLK) stop:

- 0111 1111 = 127 lines after stop of vertical blanking interval
- 0000 0001 = 1 line after stop of vertical blanking interval
- 0000 0000 = Same time as stop of vertical blanking interval (default) (see Figure 2–27)
- 1000 0001 = 1 line before stop of vertical blanking interval
- 1111 1111 = 128 lines before stop of vertical blanking interval

Vertical blanking is adjustable with respect to the standard vertical blanking intervals. The setting in this register determines the timing of the GPCL signal when it is configured to output vertical blank (see register 03h). The setting in this register also determines the duration of the luma bypass function (see register 07h) and vertical AVID cropping.

## 2.12.22 Chrominance Control #1 Register

|         |     |
|---------|-----|
| Address | 1Ah |
|---------|-----|

| 7        | 6 | 5 | 4               | 3                                       | 2                              | 1                            | 0 |
|----------|---|---|-----------------|-----------------------------------------|--------------------------------|------------------------------|---|
| Reserved |   |   | Color PLL reset | Chrominance adaptive comb filter enable | Chrominance comb filter enable | Automatic color gain control |   |

Color PLL reset:

- 0 = Color PLL not reset (default)
- 1 = Color PLL reset

Color PLL phase is reset to zero and the color PLL reset bit then immediately returns to zero. When this bit is set, the color PLL reset bit is transmitted on terminal 31 (GLCO) on the next line (NTSC or PAL).

Chrominance adaptive comb filter enable (ACE):

Chrominance comb filter enable (CE):

Chrominance comb filter mode [3:0] (CM[3:0]): Chrominance control #2 register 1Bh, bits 7–4

| ACE            | CE | CM[3] | CM[2]          | CM[1]          | CM[0]          | COMB FILTER SELECTION                                                     |
|----------------|----|-------|----------------|----------------|----------------|---------------------------------------------------------------------------|
| 0              | 0  | X     | X              | X              | X              | Comb filter disabled                                                      |
| 0              | 1  | 0     | 0              | 0              | X              | Fixed 3-line comb filter with (1, 2, 1)/4 coefficients                    |
| 0              | 1  | 0     | 0              | 1              | X              | Fixed 3-line comb filter with (1, 0, 1)/2 coefficients                    |
| 0              | 1  | 1     | 0              | X              | X              | Fixed 2-line comb filter                                                  |
| 0              | 1  | 0     | 1              | 0              | X              | Fixed 4-line (1, 1, 1, 1)/4 comb filter                                   |
| 0              | 1  | 0     | 1              | 1              | X              | Fixed 4-line (1, 3, 3, 1)/8 comb filter                                   |
| 0              | 1  | 1     | 1              | X              | X              | Fixed 2-line comb filter                                                  |
| 1              | X  | X     | 0              | 0              | 0              | Adaptive between 3-line (1, 2, 1)/4 and 2-line comb filter                |
| 1 <sup>†</sup> | X  | X     | 0 <sup>†</sup> | 0 <sup>†</sup> | 1 <sup>†</sup> | Adaptive between 3-line (1, 2, 1)/4 comb filter and no comb filter        |
| 1              | X  | X     | 0              | 1              | 0              | Adaptive between 3-line (1, 0, 1)/2 comb filter and 2-line comb filter    |
| 1              | X  | X     | 0              | 1              | 1              | Adaptive between 3-line (1, 0, 1)/2 comb filter and no comb filter        |
| 1              | X  | X     | 1              | 0              | 0              | Adaptive between 4-line (1, 1, 1, 1)/4 and 2-line comb filter             |
| 1 <sup>‡</sup> | X  | X     | 1 <sup>‡</sup> | 0 <sup>‡</sup> | 1 <sup>‡</sup> | Adaptive between 4-line (1, 1, 1, 1)/4 comb filter and no comb filter     |
| 1              | X  | X     | 1              | 1              | 0              | Adaptive between 4-line (1, 3, 3, 1)/8 comb filter and 2-line comb filter |
| 1              | X  | X     | 1              | 1              | 1              | Adaptive between 4-line (1, 3, 3, 1)/8 comb filter and no comb filter     |

<sup>†</sup> Indicates default settings for NTSC

<sup>‡</sup> Indicates default settings for PAL mode

Automatic color gain control (ACGC):

- 00 = ACGC enabled (default)
- 01 = Reserved
- 10 = ACGC disabled
- 11 = ACGC frozen to the previously set value

### 2.12.23 Chrominance Control #2 Register

|         |     |
|---------|-----|
| Address | 1Bh |
|---------|-----|

|                                    |   |   |   |          |     |                           |   |
|------------------------------------|---|---|---|----------|-----|---------------------------|---|
| 7                                  | 6 | 5 | 4 | 3        | 2   | 1                         | 0 |
| Chrominance comb filter mode [3:0] |   |   |   | Reserved | WCF | Chrominance filter select |   |

Chrominance comb filter mode [3:0] (CM[3:0]): see Section 2.12.22.

Wideband chroma filter (WCF):

- 0 = Disable
- 1 = Enable (default)

Chrominance filter select:

- 00 = No notch (default)
- 01 = Notch 1
- 10 = Notch 2
- 11 = Notch 3

Chrominance output bandwidth (MHz):

| WCF | FILTER SELECT | NTSC ITU-R BT.601 | NTSC SQUARE PIXEL | PAL/SECAM ITU-R BT.601 | PAL/SECAM SQUARE PIXEL |
|-----|---------------|-------------------|-------------------|------------------------|------------------------|
| 0   | 00            | 1.2214            | 1.1102            | 1.2214                 | 1.3340                 |
|     | 01            | 0.8782            | 0.7985            | 0.8782                 | 0.9590                 |
|     | 10            | 0.7297            | 0.6638            | 0.7297                 | 0.7979                 |
|     | 11            | 0.4986            | 0.4533            | 0.4986                 | 0.5449                 |
| 1   | 00            | 1.4170            | 1.2882            | 1.4170                 | 1.5479                 |
|     | 01            | 1.0303            | 0.9362            | 1.0303                 | 1.1260                 |
|     | 10            | 0.8438            | 0.7670            | 0.8438                 | 0.9219                 |
|     | 11            | 0.5537            | 0.5035            | 0.5537                 | 0.6045                 |

Refer to Figure 2–6 through Figure 2–9 for the frequency responses of the filters.

### 2.12.24 Interrupt Reset Register B

|         |     |
|---------|-----|
| Address | 1Ch |
|---------|-----|

|                               |                                  |                     |                          |                                |                          |                        |                      |
|-------------------------------|----------------------------------|---------------------|--------------------------|--------------------------------|--------------------------|------------------------|----------------------|
| 7                             | 6                                | 5                   | 4                        | 3                              | 2                        | 1                      | 0                    |
| Software initialization reset | Macrovision detect changed reset | Command ready reset | Field rate changed reset | Line alternation changed reset | Color lock changed reset | H/V lock changed reset | TV/VCR changed reset |

Software initialization reset:

- 0 = No effect (default)
- 1 = Reset software initialization bit

Macrovision detect changed reset:

- 0 = No effect (default)
- 1 = Reset macrovision detect changed bit

Command ready reset:

- 0 = No effect (default)
- 1 = Reset command ready bit

Field rate changed reset:

- 0 = No effect (default)
- 1 = Reset field rate changed bit



Line alternation changed reset:

- 0 = No effect (default)
- 1 = Reset line alternation changed bit

Color lock changed reset:

- 0 = No effect (default)
- 1 = Reset color lock changed bit

H/V lock changed reset:

- 0 = No effect (default)
- 1 = Reset H/V lock changed bit

TV/VCR changed reset:

- 0 = No effect (default)
- 1 = Reset TV/VCR changed bit

Interrupt reset register B is used by the external processor to reset the interrupt status bits in interrupt status register B. Bits loaded with a 1 allow the corresponding interrupt status bit to reset to 0. Bits loaded with a 0 have no effect on the interrupt status bits.

## 2.12.25 Interrupt Enable Register B

|         |     |
|---------|-----|
| Address | 1Dh |
|---------|-----|

| 7                                       | 6                         | 5                    | 4                 | 3                       | 2                 | 1               | 0             |
|-----------------------------------------|---------------------------|----------------------|-------------------|-------------------------|-------------------|-----------------|---------------|
| Software initialization occurred enable | Macrovision detect enable | Command ready enable | Field rate enable | Line alternation enable | Color lock enable | H/V lock enable | TV/VCR enable |

Software initialization occurred enable:

- 0 = Disabled (default)
- 1 = Enabled

Macrovision detect enable:

- 0 = Disabled (default)
- 1 = Enabled

Command ready enable:

- 0 = Disabled (default)
- 1 = Enabled

Field rate enable:

- 0 = Disabled (default)
- 1 = Enabled

Line alternation enable:

- 0 = Disabled (default)
- 1 = Enabled

Color lock enable:

- 0 = Disabled (default)
- 1 = Enabled

H/V lock enable:

- 0 = Disabled (default)
- 1 = Enabled

TV/VCR enable:

- 0 = Disabled (default)
- 1 = Enabled

Interrupt enable register B is used by the external processor to mask unnecessary interrupt sources for interrupt B. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. Note this register only affects the external pin it does not affect the bits in the interrupt status register. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external pin. To determine if this device is driving the interrupt pin either AND interrupt status register B with interrupt enable register B or check the state of interrupt B in the interrupt B active register.

## 2.12.26 Interrupt Configuration Register B

|         |     |
|---------|-----|
| Address | 1Eh |
|---------|-----|

|          |   |   |   |   |   |   |                      |
|----------|---|---|---|---|---|---|----------------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                    |
| Reserved |   |   |   |   |   |   | Interrupt polarity B |

Interrupt polarity B:

- 0 = Interrupt B is active low (default).
- 1 = Interrupt B is active high.

Interrupt polarity B must be same as interrupt polarity A bit at bit 0 of interrupt configuration register A at address C2h.

Interrupt configuration register B is used to configure the polarity of interrupt B on the external interrupt pin. Note that when the interrupt B is configured for active low, the pin will be driven low when active and high-impedance when inactive (open-collector). Conversely, when the interrupt B is configured for active high, it will be driven high-impedance for active and driven low for inactive.

## 2.12.27 Video Input Source Selection #2 Register

|         |     |
|---------|-----|
| Address | 20h |
|---------|-----|

|          |   |                          |          |   |   |                       |                               |
|----------|---|--------------------------|----------|---|---|-----------------------|-------------------------------|
| 7        | 6 | 5                        | 4        | 3 | 2 | 1                     | 0                             |
| Reserved |   | Decimation filter select | Reserved |   |   | Chroma channel select | Luma/Composite channel select |

Decimation filter select:

- 0 = Selected (default)
- 1 = Bypassed

Chroma channel select:

- 0 = ADC1 selected (default)
- 1 = ADC2 selected

Luma/Composite channel select:

- 0 = ADC1 selected (default)
- 1 = ADC2 selected

See Section 2.12.1, *Video Input Source Selection #1* register, I<sup>2</sup>C address 00h

### 2.12.28 Crystal Frequency Register

|         |     |
|---------|-----|
| Address | 26h |
|---------|-----|

|          |   |   |   |   |   |   |                                  |
|----------|---|---|---|---|---|---|----------------------------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                                |
| Reserved |   |   |   |   |   |   | Crystal/external clock frequency |

Crystal/external clock frequency:

0 = 14.31818 MHz (default)

1 = 27 MHz

### 2.12.29 Video Standard Register

|         |     |
|---------|-----|
| Address | 28h |
|---------|-----|

|          |   |   |   |                |   |   |   |
|----------|---|---|---|----------------|---|---|---|
| 7        | 6 | 5 | 4 | 3              | 2 | 1 | 0 |
| Reserved |   |   |   | Video standard |   |   |   |

Video standard:

0000 = Autoswitch mode (default)  
0001 = (J, M) NTSC square pixel  
0010 = (J, M) NTSC ITU-R BT.601  
0011 = (B, D, G, H, I, N) PAL square pixel  
0100 = (B, D, G, H, I, N) PAL ITU-R BT.601  
0101 = (M) PAL square pixel  
0110 = (M) PAL ITU-R BT.601  
0111 = (Combination-N) PAL square pixel  
1000 = (Combination-N) ITU-R BT.601  
1001 = NTSC 4.43 square pixel  
1010 = NTSC 4.43 ITU\_R BT.601  
1011 = SECAM square pixel  
1100 = SECAM ITU-R BT.601

With the autoswitch code running, the user can force the device to operate in a particular video standard mode and sample rate by writing the appropriate value into this register.

### 2.12.30 Microprocessor Start Register

|         |     |
|---------|-----|
| Address | 7Fh |
|---------|-----|

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|   |   |   |   |   |   |   |   |

A write with any data to this register must be performed to start the microprocessor.

### 2.12.31 Major ROM Version Register

|         |     |
|---------|-----|
| Address | 80h |
|---------|-----|

|                   |   |   |   |   |   |   |   |
|-------------------|---|---|---|---|---|---|---|
| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Major ROM Version |   |   |   |   |   |   |   |

This register contains the major ROM revision number.

## 2.12.32 Status Register #1

|         |     |
|---------|-----|
| Address | 81h |
|---------|-----|

| 7                        | 6                       | 5                 | 4                | 3                            | 2                         | 1                           | 0             |
|--------------------------|-------------------------|-------------------|------------------|------------------------------|---------------------------|-----------------------------|---------------|
| Peak white detect status | Line-alternating status | Field rate status | Lost lock detect | Color subcarrier lock status | Vertical sync lock status | Horizontal sync lock status | TV/VCR status |

Peak white detect status:

- 0 = Peak white is not detected
- 1 = Peak white is detected

Line-alternating status:

- 0 = Nonline alternating
- 1 = Line alternating

Field rate status:

- 0 = 60 Hz
- 1 = 50 Hz

Lost lock detect:

- 0 = No lost lock since status register #1 was last read
- 1 = Lost lock since status register #1 was last read

Color subcarrier lock status:

- 0 = Color subcarrier is not locked
- 1 = Color subcarrier is locked

Vertical sync lock status:

- 0 = Vertical sync is not locked
- 1 = Vertical sync is locked

Horizontal sync lock status:

- 0 = Horizontal sync is not locked
- 1 = Horizontal sync is locked

TV/VCR status:

- 0 = TV
- 1 = VCR

### 2.12.33 Status Register #2

|         |     |
|---------|-----|
| Address | 82h |
|---------|-----|

| 7        | 6                     | 5                   | 4                     | 3                            | 2        | 1                     | 0 |
|----------|-----------------------|---------------------|-----------------------|------------------------------|----------|-----------------------|---|
| Reserved | Weak signal detection | PAL switch polarity | Field sequence status | AGC and offset frozen status | Reserved | Macrovision detection |   |

Weak signal detection:

- 0 = No weak signal
- 1 = Weak signal mode

PAL switch polarity of first line of odd field:

- 0 = PAL switch is 0
- 1 = PAL switch is 1

Field sequence status:

- 0 = Even field
- 1 = Odd field

AGC and offset frozen status:

- 0 = AGC and offset are not frozen
- 1 = AGC and offset are frozen

Macrovision detection:

- 00 = No copy protection
- 01 = AGC pulses/pseudo syncs present
- 10 = AGC pulses/pseudo syncs and 2-line color striping present
- 11 = AGC pulses/pseudo syncs and 4-line color striping present

### 2.12.34 Status Register #3

|         |     |
|---------|-----|
| Address | 83h |
|---------|-----|

| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|---|
| AGC gain |   |   |   |   |   |   |   |

AGC gain:

- 0100 0000 = -3 dB
- 1000 0000 = 0 dB
- 1100 0000 = 3 dB
- 1111 1111 = 6 dB

### 2.12.35 Status Register #4

|         |     |
|---------|-----|
| Address | 84h |
|---------|-----|

| 7                                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------------------|---|---|---|---|---|---|---|
| Subcarrier to horizontal (SCH) phase |   |   |   |   |   |   |   |

SCH (color PLL subcarrier phase at 50% of the falling edge of horizontal sync of line one of odd field; step size 360°/256):

- 0000 0000 = 0.00°
- 0000 0001 = 1.41°
- 0000 0010 = 2.81°
- 1111 1110 = 357.2°
- 1111 1111 = 358.6°

### 2.12.36 Interrupt Status Register B

|         |     |
|---------|-----|
| Address | 85h |
|---------|-----|

| 7                       | 6                          | 5             | 4                  | 3                        | 2                  | 1                | 0              |
|-------------------------|----------------------------|---------------|--------------------|--------------------------|--------------------|------------------|----------------|
| Software initialization | Macrovision detect changed | Command ready | Field rate changed | Line alternation changed | Color lock changed | H/V lock changed | TV/VCR changed |

Software initialization:

- 0 = Software initialization is not ready
- 1 = Software initialization is ready

Macrovision detect changed:

- 0 = Macrovision detect status has not changed
- 1 = Macrovision detect status has changed

Command ready:

- 0 = TVP5145 is not ready to accept a new command
- 1 = TVP5145 is ready to accept a new command

Field rate changed:

- 0 = Field rate has not changed
- 1 = Field rate has changed

Line alternation changed:

- 0 = Line alteration has not changed
- 1 = Line alternation has changed

Color lock changed:

- 0 = Color lock status has not changed
- 1 = Color lock status has changed

H/V lock changed:

- 0 = H/V lock status has not changed
- 1 = H/V lock status has changed

TV/VCR changed:

- 0 = TV/VCR status has not changed
- 1 = TV/VCR status has changed

Interrupt status register B is polled by the external processor to determine the interrupt source for interrupt B. After an interrupt condition is set, it can be reset by writing to interrupt reset register B at subaddress 1Ch with a 1 in the appropriate bit.

### 2.12.37 Interrupt Active Register B

|         |     |
|---------|-----|
| Address | 86h |
|---------|-----|

| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0           |
|----------|---|---|---|---|---|---|-------------|
| Reserved |   |   |   |   |   |   | Interrupt B |

Interrupt B:

- 0 = Interrupt B is not active on the external terminal (default)
- 1 = Interrupt B is active on the external terminal

The interrupt active register B is polled by the external processor to determine if interrupt B is active.

### 2.12.38 Minor ROM Version Register

|         |     |
|---------|-----|
| Address | 87h |
|---------|-----|

|                   |   |   |   |   |   |   |   |
|-------------------|---|---|---|---|---|---|---|
| 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Minor ROM Version |   |   |   |   |   |   |   |

This register contains the minor ROM vision number.

### 2.12.39 Status Register #5

|         |     |
|---------|-----|
| Address | 88h |
|---------|-----|

|                 |          |   |   |                |   |   |               |
|-----------------|----------|---|---|----------------|---|---|---------------|
| 7               | 6        | 5 | 4 | 3              | 2 | 1 | 0             |
| Autoswitch mode | Reserved |   |   | Video standard |   |   | Sampling rate |

This register contains information about the detected video standard and the sampling rate at which the device is currently operating. When autoswitch code is running, this register must be tested to determine which video standard has been detected.

Autoswitch mode:

- 0 = Stand-alone (forced video standard) mode
- 1 = Autoswitch mode

Video standard:

| VIDEO STANDARD [3:1] |       |       | SR    | VIDEO STANDARD                   |
|----------------------|-------|-------|-------|----------------------------------|
| BIT 3                | BIT 2 | BIT 1 | BIT 0 |                                  |
| 0                    | 0     | 0     | 0     | (J, M) NTSC square pixel         |
| 0                    | 0     | 0     | 1     | (J, M) NTSC ITU-R BT.601         |
| 0                    | 0     | 1     | 0     | (B, G, H, I, N) PAL square pixel |
| 0                    | 0     | 1     | 1     | (B, G, H, I, N) PAL ITU-R BT.601 |
| 0                    | 1     | 0     | 0     | (M) PAL square pixel             |
| 0                    | 1     | 0     | 1     | (M) PAL ITU-R BT.601             |
| 0                    | 1     | 1     | 0     | (Combination-N) PAL square pixel |
| 0                    | 1     | 1     | 1     | (Combination-N) ITU-R BT.601     |
| 1                    | 0     | 0     | 0     | NTSC 4.43 square pixel           |
| 1                    | 0     | 0     | 1     | NTSC 4.43 ITU_R BT.601           |
| 1                    | 0     | 1     | 0     | SECAM square pixel               |
| 1                    | 0     | 1     | 1     | SECAM ITU-R BT.601               |

Sampling rate (SR):

- 0 = Square pixel
- 1 = ITU-R BT.601

### 2.12.40 Vertical Line Count MSB Register

|         |     |
|---------|-----|
| Address | 89h |
|---------|-----|

|          |   |   |   |   |   |                         |   |
|----------|---|---|---|---|---|-------------------------|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1                       | 0 |
| Reserved |   |   |   |   |   | Vertical line count MSB |   |

Vertical line count MSB:

Vertical line count bits [9:8]

### 2.12.41 Vertical Line Count LSB Register

|         |     |
|---------|-----|
| Address | 8Ah |
|---------|-----|

|                         |   |   |   |   |   |   |   |
|-------------------------|---|---|---|---|---|---|---|
| 7                       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Vertical line count LSB |   |   |   |   |   |   |   |

Vertical line count LSB:

Vertical line count bits[7:0]

The registers 89h and 8Ah can be read and combined to extract the current vertical line count. This can be used with nonstandard video signals such as a VCR in fast-forward or rewind mode to synchronize downstream video circuitry.

### 2.12.42 Analog Die ID Register

|         |     |
|---------|-----|
| Address | 8Bh |
|---------|-----|

|               |   |   |   |   |   |   |   |
|---------------|---|---|---|---|---|---|---|
| 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Analog die ID |   |   |   |   |   |   |   |

This register identifies the analog die ID.

### 2.12.43 Digital Die ID Register

|         |     |
|---------|-----|
| Address | 8Ch |
|---------|-----|

|                |   |   |   |   |   |   |   |
|----------------|---|---|---|---|---|---|---|
| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Digital die ID |   |   |   |   |   |   |   |

This register identifies the digital die ID.

### 2.12.44 Closed Caption Data Registers

|         |         |
|---------|---------|
| Address | 90h–93h |
|---------|---------|

| Address | 7                             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------------------------|---|---|---|---|---|---|---|
| 90h     | Closed caption field 1 byte 1 |   |   |   |   |   |   |   |
| 91h     | Closed caption field 1 byte 2 |   |   |   |   |   |   |   |
| 92h     | Closed caption field 2 byte 1 |   |   |   |   |   |   |   |
| 93h     | Closed caption field 2 byte 2 |   |   |   |   |   |   |   |

These registers contain the closed caption data arranged in bytes per field.



## 2.12.45 WSS Data Registers

|         |         |
|---------|---------|
| Address | 94h–99h |
|---------|---------|

### NTSC

| ADDRESS | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   | BYTE               |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|--------------------|
| 94h     |     |     | b5  | b4  | b3  | b2  | b1  | b0  | WSS field 1 byte 1 |
| 95h     | b13 | b12 | b11 | b10 | b9  | b8  | b7  | b6  | WSS field 1 byte 2 |
| 96h     |     |     | b19 | b18 | b17 | b16 | b15 | b14 | WSS field 1 byte 3 |
| 97h     |     |     | b5  | b4  | b3  | b2  | b1  | b0  | WSS field 2 byte 1 |
| 98h     | b13 | b12 | b11 | b10 | b9  | b8  | b7  | b6  | WSS field 2 byte 2 |
| 99h     |     |     | b19 | b18 | b17 | b16 | b15 | b14 | WSS field 2 byte 3 |

These registers contain the wide screen signaling (WSS) data for NTSC.

- Bits 0–1 represent word 0, aspect ratio
- Bits 2–5 represent word 1, header code for word 2
- Bits 6–13 represent word 2, copy control
- Bits 14–19 represent word 3, CRC

### PAL/SECAM

| ADDRESS | 7        | 6  | 5   | 4   | 3   | 2   | 1  | 0  | BYTE               |
|---------|----------|----|-----|-----|-----|-----|----|----|--------------------|
| 94h     | b7       | b6 | b5  | b4  | b3  | b2  | b1 | b0 | WSS field 1 byte 1 |
| 95h     |          |    | b13 | b12 | b11 | b10 | b9 | b8 | WSS field 1 byte 2 |
| 96h     | b7       | b6 | b5  | b4  | b3  | b2  | b1 | b0 | WSS field 2 byte 1 |
| 97h     |          |    | b13 | b12 | b11 | b10 | b9 | b8 | WSS field 2 byte 2 |
| 98h     | Reserved |    |     |     |     |     |    |    |                    |
| 99h     | Reserved |    |     |     |     |     |    |    |                    |

PAL/SECAM:

- Bits 0–3 represent group 1, aspect ratio
- Bits 4–7 represent group 2, enhanced services
- Bits 8–10 represent group 3, subtitles
- Bits 11–13 represent group 4, others

## 2.12.46 VPS Data Registers

|         |         |
|---------|---------|
| Address | 9Ah–A6h |
|---------|---------|

| ADDRESS | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|---|---|---|---|---|---|---|
| 9Ah     | VPS byte 1  |   |   |   |   |   |   |   |
| 9Bh     | VPS byte 2  |   |   |   |   |   |   |   |
| 9Ch     | VPS byte 3  |   |   |   |   |   |   |   |
| 9Dh     | VPS byte 4  |   |   |   |   |   |   |   |
| 9Eh     | VPS byte 5  |   |   |   |   |   |   |   |
| 9Fh     | VPS byte 6  |   |   |   |   |   |   |   |
| A0h     | VPS byte 7  |   |   |   |   |   |   |   |
| A1h     | VPS byte 8  |   |   |   |   |   |   |   |
| A2h     | VPS byte 9  |   |   |   |   |   |   |   |
| A3h     | VPS byte 10 |   |   |   |   |   |   |   |
| A4h     | VPS byte 11 |   |   |   |   |   |   |   |
| A5h     | VPS byte 12 |   |   |   |   |   |   |   |
| A6h     | VPS byte 13 |   |   |   |   |   |   |   |

These registers contain the entire VPS data line except the clock run-in code or the start code.

## 2.12.47 VITC Data Registers

|         |         |
|---------|---------|
| Address | A7h–AFh |
|---------|---------|

| ADDRESS | 7                           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------------------|---|---|---|---|---|---|---|
| A7h     | VITC byte 1, frame byte 1   |   |   |   |   |   |   |   |
| A8h     | VITC byte 2, frame byte 2   |   |   |   |   |   |   |   |
| A9h     | VITC byte 3, seconds byte 1 |   |   |   |   |   |   |   |
| AAh     | VITC byte 4, seconds byte 2 |   |   |   |   |   |   |   |
| ABh     | VITC byte 5, minutes byte 1 |   |   |   |   |   |   |   |
| ACh     | VITC byte 6, minutes byte 2 |   |   |   |   |   |   |   |
| ADh     | VITC byte 7, hour byte 1    |   |   |   |   |   |   |   |
| A Eh    | VITC byte 8, hour byte 2    |   |   |   |   |   |   |   |
| AFh     | VITC byte 9, CRC            |   |   |   |   |   |   |   |

These registers contain the VITC data.

## 2.12.48 VBI FIFO Read Data Register

|         |     |
|---------|-----|
| Address | B0h |
|---------|-----|

| 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|
| FIFO read data |   |   |   |   |   |   |   |

This address is provided to access VBI data in the FIFO through the host port. All forms of teletext data come directly from the FIFO, while all other forms of VBI data can be programmed to come from registers or from the FIFO. Current status of the FIFO can be found at address C6h and the number of bytes in the FIFO is located at address C7h. If the host port is to be used to read data from the FIFO, the output formatter must be disabled at address CDh bit 0. The format used for the VBI FIFO is shown in Section 2.8.1.

## 2.12.49 Teletext Filter and Mask Registers

|         |         |
|---------|---------|
| Address | B1h–BAh |
|---------|---------|

| ADDRESS | 7               | 6 | 5 | 4 | 3                  | 2 | 1 | 0 |
|---------|-----------------|---|---|---|--------------------|---|---|---|
| B1h     | Filter 1 Mask 1 |   |   |   | Filter 1 Pattern 1 |   |   |   |
| B2h     | Filter 1 Mask 2 |   |   |   | Filter 1 Pattern 2 |   |   |   |
| B3h     | Filter 1 Mask 3 |   |   |   | Filter 1 Pattern 3 |   |   |   |
| B4h     | Filter 1 Mask 4 |   |   |   | Filter 1 Pattern 4 |   |   |   |
| B5h     | Filter 1 Mask 5 |   |   |   | Filter 1 Pattern 5 |   |   |   |
| B6h     | Filter 2 Mask 1 |   |   |   | Filter 2 Pattern 1 |   |   |   |
| B7h     | Filter 2 Mask 2 |   |   |   | Filter 2 Pattern 2 |   |   |   |
| B8h     | Filter 2 Mask 3 |   |   |   | Filter 2 Pattern 3 |   |   |   |
| B9h     | Filter 2 Mask 4 |   |   |   | Filter 2 Pattern 4 |   |   |   |
| BAh     | Filter 2 Mask 5 |   |   |   | Filter 2 Pattern 5 |   |   |   |

For an NABTS system, the packet prefix consists of five bytes. Each byte contains four data bits (D[3:0]) interlaced with four Hamming protection bits (H[3:0]):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D[3]  | H[3]  | D[2]  | H[2]  | D[1]  | H[1]  | D[0]  | H[0]  |

Only data portion D[3:0] from each byte is applied to a teletext filter function with corresponding pattern bits P[3:0] and mask bits M[3:0]. Hamming protection bits are ignored by the filter.

For WST system (PAL or NTSC), the packet prefix consists of two bytes. The two bytes contain three bits of magazine number (M[2:0]) and five bits of row address (R[4:0]), interlaced with eight Hamming protection bits H[7:0]:

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R[0]  | H[3]  | M[2]  | H[2]  | M[1]  | H[1]  | M[0]  | H[0]  |
| R[4]  | H[7]  | R[3]  | H[6]  | R[2]  | H[5]  | R[1]  | H[4]  |

The mask bits enable filtering using the corresponding bit in the pattern register. For example, a 1 in the LSB of mask 1 means that the filter module must compare the LSB of nibble 1 in the pattern register to the first data bit on the transaction. If these match, a true result is returned. A 0 in a bit of mask 1 means that the filter module must ignore that data bit of the transaction. If all 0s are programmed in the mask bits, the filter matches all patterns returning a true result (default 00h).

Figure 2–32 shows the filter functions using data D[3:0], pattern P[3:0], and mask M[3:0].

Pattern and mask for each byte and filter are referred as <1,2><P,M><1,2,3,4,5> where:

- <1,2> identifies the filter 1 or 2
- <P,M> identifies the pattern or mask
- <1,2,3,4,5> identifies the byte number

### 2.12.50 Teletext Filter Control Register

|         |     |
|---------|-----|
| Address | BBh |
|---------|-----|

| 7        | 6 | 5 | 4            | 3 | 2    | 1                   | 0                   |
|----------|---|---|--------------|---|------|---------------------|---------------------|
| Reserved |   |   | Filter logic |   | Mode | TTX filter 2 enable | TTX filter 1 enable |

Filter logic: allows different logic to be applied when combining the decision of filter 1 and filter 2 as follows:

- 00 = NOR (Default)
- 01 = NAND
- 10 = OR
- 11 = AND

Mode:

- 0 = Teletext WST PAL mode B (2 header bytes) (default)
- 1 = Teletext NABTS NTSC mode C (5 header bytes) 1

TTX filter 2 enable:

- 0 = Disabled (default)
- 1 = Enabled

TTX filter 1 enable:

- 0 = Disabled (default)
- 1 = Enabled

If the filter matches or if the filter mask is all 0s, then a true result is returned. Figure 2–32 also shows the filter logic selection and filter enables.

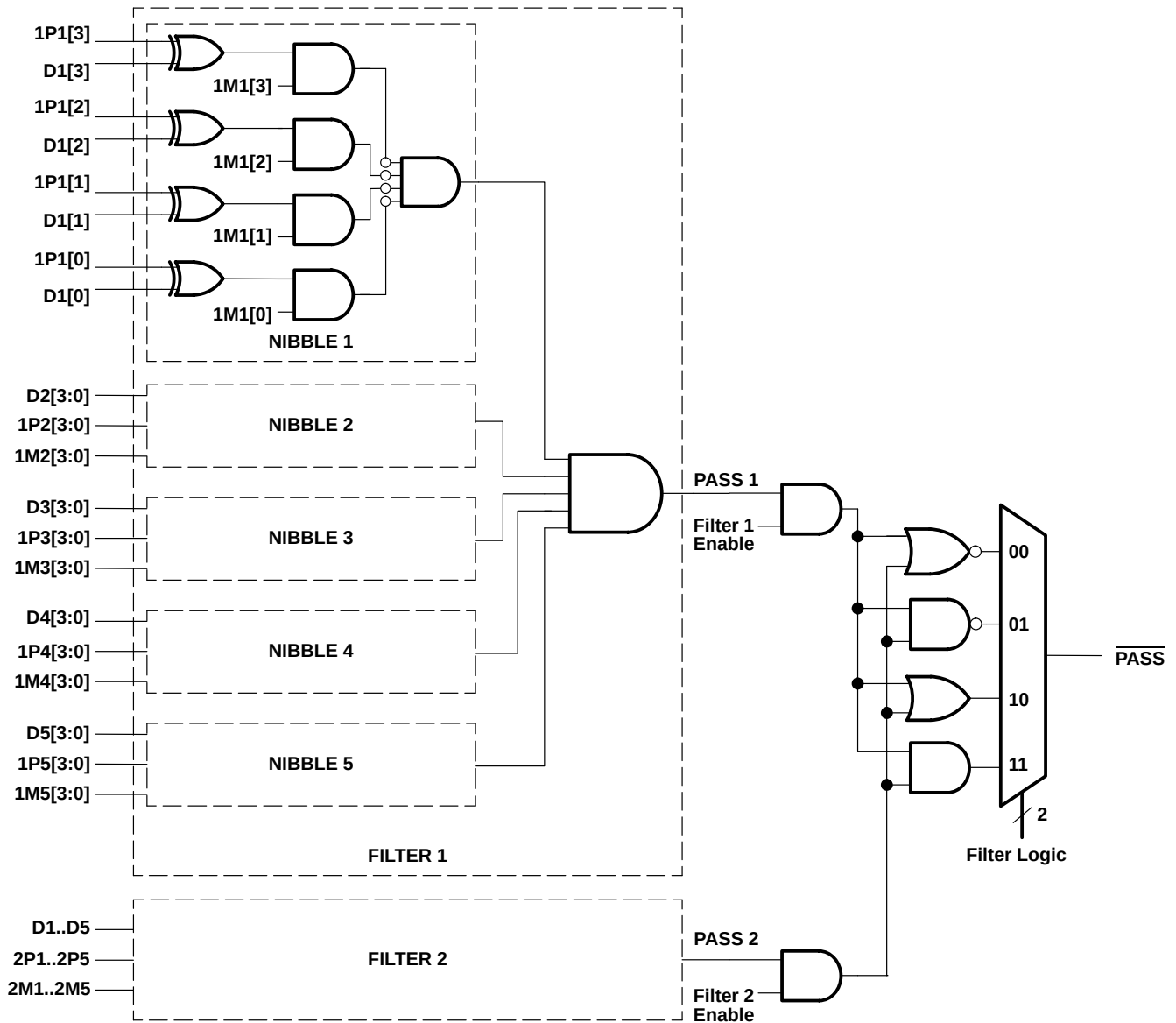


Figure 2-32. Teletext Filter Function

### 2.12.51 Interrupt Status Register A

|         |     |
|---------|-----|
| Address | C0h |
|---------|-----|

| 7                    | 6              | 5                        | 4                   | 3        | 2                        | 1              | 0              |
|----------------------|----------------|--------------------------|---------------------|----------|--------------------------|----------------|----------------|
| Lock state interrupt | Lock interrupt | Cycle complete interrupt | Bus error interrupt | Reserved | FIFO threshold interrupt | Line interrupt | Data interrupt |

The interrupt status register A can be polled by the host processor to determine the source of an interrupt. After an interrupt condition is set it can be reset by writing to this register with a 1 in the appropriate bit(s).

Lock state interrupt:

- 0 = TVP5145 not locked to video signal
- 1 = TVP5145 locked to video signal

Lock interrupt:

- 0 = A transition has not occurred on the lock signal
- 1 = A transition has occurred on the lock signal

Cycle complete interrupt:

- 0 = Read or write cycle in progress
- 1 = Read or write cycle complete

Bus error interrupt:

- 0 = No bus error
- 1 = PHI interface detected an illegal access

FIFO threshold interrupt:

- 0 = The amount of data in the FIFO has not yet crossed the threshold programmed at address C8h.
- 1 = The amount of data in the FIFO has crossed the threshold programmed at address C8h.

Line interrupt:

- 0 = The video line number has not yet been reached.
- 1 = The video line number programmed in address CAh has occurred.

Data interrupt:

- 0 = No data is available
- 1 = VBI data is available either in the FIFO or in the VBI data registers.

## 2.12.52 Interrupt Enable Register A

|         |     |
|---------|-----|
| Address | C1h |
|---------|-----|

| 7        | 6                     | 5                               | 4                          | 3        | 2                               | 1                     | 0                     |
|----------|-----------------------|---------------------------------|----------------------------|----------|---------------------------------|-----------------------|-----------------------|
| Reserved | Lock interrupt enable | Cycle complete interrupt enable | Bus error interrupt enable | Reserved | FIFO threshold interrupt enable | Line interrupt enable | Data interrupt enable |

The interrupt enable register A is used by the host processor to mask unnecessary interrupt sources. Bits loaded with a 1 allow the corresponding interrupt condition to generate an interrupt on the external pin. Conversely, bits loaded with a 0 mask the corresponding interrupt condition from generating an interrupt on the external pin. Note this register only affects the interrupt on the external terminal, it does not affect the bits in interrupt status register A. A given condition can set the appropriate bit in the status register and not cause an interrupt on the external terminal. To determine if this device is driving the interrupt terminal either perform a logical AND of interrupt status register A with interrupt enable register A, or check the state of the interrupt A bit in the interrupt configuration register at address C2h.

Lock interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

Cycle complete interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

Bus error interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

FIFO threshold interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

Line interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

Data interrupt enable:

- 0 = Disabled (default)
- 1 = Enabled

### 2.12.53 Interrupt Configuration Register A

|         |     |
|---------|-----|
| Address | C2h |
|---------|-----|

|          |   |   |   |   |            |             |                      |
|----------|---|---|---|---|------------|-------------|----------------------|
| 7        | 6 | 5 | 4 | 3 | 2          | 1           | 0                    |
| Reserved |   |   |   |   | YUV enable | Interrupt A | Interrupt polarity A |

YUV enable:

- 0 = YUV pins are high-impedance
- 1 = YUV pins are active if other conditions are met (default)

Interrupt A (read-only):

- 0 = Interrupt A is not active on the external pin (default)
- 1 = Interrupt A is active on the external pin

Interrupt polarity A:

- 0 = Interrupt A is active low (default)
- 1 = Interrupt A is active high

Note that when the interrupt A is configured as active low, the terminal is driven low when active and high-impedance when inactive (open drain). Conversely, when the terminal is configured as active high, it is driven high-impedance when active and driven low when inactive.

### 2.12.54 VDP Configuration RAM Register

|         |         |
|---------|---------|
| Address | C3h–C5h |
|---------|---------|

|         |                    |   |   |   |   |   |   |               |
|---------|--------------------|---|---|---|---|---|---|---------------|
| Address | 7                  | 6 | 5 | 4 | 3 | 2 | 1 | 0             |
| C3h     | Configuration data |   |   |   |   |   |   |               |
| C4h     | RAM address (7:0)  |   |   |   |   |   |   |               |
| C5h     | Reserved           |   |   |   |   |   |   | RAM address 8 |

The configuration RAM data is provided to initialize the VDP with initial constants. The configuration RAM is 512 bytes total organized as 32 different configurations of 16 bytes each. The first 26 configurations are defined for the current VBI standards. An additional 2 configurations can be used as a custom programmed mode for unique standards.

Address C3h is used to read or write to the RAM. The RAM internal address counter is automatically incremented with each transaction. Addresses C5h and C4h make up a 9-bit address to load the internal address counter with a specific start address. This can be used to write a subset of the RAM for only those standards of interest. Registers D0h–FBh must all be programmed with FFh, before writing or reading the configuration RAM. Full field mode (CFh) must be disabled as well.

The suggested RAM contents are shown below. All values are hexadecimal.



**Table 2–12. VBI Configuration RAM**

| Index             | Address | 0            | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B | C | D | E  | F |
|-------------------|---------|--------------|----|----|----|----|----|----|----|----|----|----|---|---|---|----|---|
| WST SECAM S       | 000     | AA           | AA | FF | FF | E7 | 2E | 20 | 26 | E6 | 75 | 0D | 0 | 0 | 0 | 10 | 0 |
| WST SECAM 6       | 010     | AA           | AA | FF | FF | E7 | 2E | 20 | 26 | E6 | B4 | 0E | 0 | 0 | 0 | 10 | 0 |
| WST PAL B S       | 020     | AA           | AA | FF | FF | 27 | 2E | 20 | 2B | A6 | 0D | 0F | 0 | 0 | 0 | 10 | 0 |
| WST PAL B 6       | 030     | AA           | AA | FF | FF | 27 | 2E | 20 | 2B | A6 | 72 | 10 | 0 | 0 | 0 | 10 | 0 |
| WST PAL C S       | 040     | AA           | AA | FF | FF | E7 | 2E | 20 | 22 | A6 | 71 | 0C | 0 | 0 | 0 | 10 | 0 |
| WST PAL C 6       | 050     | AA           | AA | FF | FF | E7 | 2E | 20 | 22 | A6 | 98 | 0D | 0 | 0 | 0 | 10 | 0 |
| WST NTSC S        | 060     | AA           | AA | FF | FF | 27 | 2E | 20 | 23 | 69 | EF | 0E | 0 | 0 | 0 | 10 | 0 |
| WST NTSC 6        | 070     | AA           | AA | FF | FF | 27 | 2E | 20 | 23 | 69 | 93 | 0D | 0 | 0 | 0 | 10 | 0 |
| NABTS, NTSC S     | 080     | AA           | AA | FF | FF | E7 | 2E | 20 | 22 | 69 | EF | 0E | 0 | 0 | 0 | 15 | 0 |
| NABTS, NTSC 6     | 090     | AA           | AA | FF | FF | E7 | 2E | 20 | 22 | 69 | 93 | 0D | 0 | 0 | 0 | 15 | 0 |
| NABTS, NTSC-J S   | 0A0     | AA           | AA | FF | FF | A7 | 2E | 20 | 23 | 69 | EF | 0E | 0 | 0 | 0 | 10 | 0 |
| NABTS, NTSC-J 6   | 0B0     | AA           | AA | FF | FF | A7 | 2E | 20 | 23 | 69 | 93 | 0D | 0 | 0 | 0 | 10 | 0 |
| CC, PAL/SECAM S   | 0C0     | AA           | 2A | FF | 3F | 04 | 51 | 6E | 02 | A6 | AE | 08 | 0 | 0 | 0 | 27 | 0 |
| CC, PAL/SECAM 6   | 0D0     | AA           | 2A | FF | 3F | 04 | 51 | 6E | 02 | A6 | 7B | 09 | 0 | 0 | 0 | 27 | 0 |
| CC, NTSC S        | 0E0     | AA           | 2A | FF | 3F | 04 | 51 | 6E | 02 | 69 | 82 | 0A | 0 | 0 | 0 | 27 | 0 |
| CC, NTSC 6        | 0F0     | AA           | 2A | FF | 3F | 04 | 51 | 6E | 02 | 69 | 8C | 09 | 0 | 0 | 0 | 27 | 0 |
| WSS, PAL/SECAM S  | 100     | 5B           | 55 | C5 | FF | 0  | 71 | 6E | 42 | A6 | 77 | 0E | 0 | 0 | 0 | 3A | 0 |
| WSS, PAL/SECAM 6  | 110     | 5B           | 55 | C5 | FF | 0  | 71 | 6E | 42 | A6 | CD | 0F | 0 | 0 | 0 | 3A | 0 |
| WSS, NTSC S       | 120     | 38           | 00 | 3F | 00 | 0  | 71 | 6E | 43 | 69 | 55 | 09 | 0 | 0 | 0 | 39 | 0 |
| WSS, NTSC C       | 130     | 38           | 00 | 3F | 00 | 0  | 71 | 6E | 43 | 69 | 7C | 08 | 0 | 0 | 0 | 39 | 0 |
| VITC, PAL/SECAM S | 140     | 0            | 0  | 0  | 0  | 0  | 8F | 6D | 49 | A6 | CC | 07 | 0 | 0 | 0 | 4C | 0 |
| VITC, PAL/SECAM 6 | 150     | 0            | 0  | 0  | 0  | 0  | 8F | 6D | 49 | A6 | 85 | 08 | 0 | 0 | 0 | 4C | 0 |
| VITC, NTSC S      | 160     | 0            | 0  | 0  | 0  | 0  | 8F | 6D | 49 | 69 | 70 | 09 | 0 | 0 | 0 | 4C | 0 |
| VITC, NTSC 6      | 170     | 0            | 0  | 0  | 0  | 0  | 8F | 6D | 49 | 69 | 94 | 08 | 0 | 0 | 0 | 4C | 0 |
| VPS, PAL S        | 180     | AA           | AA | FF | FF | BA | CE | 2B | 0D | A6 | D9 | 0A | 0 | 0 | 0 | 60 | 0 |
| VPS, PAL 6        | 190     | AA           | AA | FF | FF | BA | CE | 2B | 0D | A6 | DA | 0B | 0 | 0 | 0 | 60 | 0 |
| Custom            | 1A0     | Programmable |    |    |    |    |    |    |    |    |    |    |   |   |   |    |   |
| Custom            | 1B0     | Programmable |    |    |    |    |    |    |    |    |    |    |   |   |   |    |   |

### 2.12.55 VDP Status Register

|         |     |
|---------|-----|
| Address | C6h |
|---------|-----|

| 7               | 6          | 5             | 4                    | 3                    | 2             | 1             | 0              |
|-----------------|------------|---------------|----------------------|----------------------|---------------|---------------|----------------|
| FIFO full error | FIFO empty | TTX available | CC field 1 available | CC field 2 available | WSS available | VPS available | VITC available |

The VDP status register indicates whether data is available in either the FIFO or data registers, and status information about the FIFO. Reading data from the corresponding register does not clear the status flags automatically. These flags are only reset by writing a 1 to the respective bit. However, bit 6 is updated automatically.

FIFO full error:

- 0 = No FIFO full error
- 1 = FIFO was full during write to FIFO

The FIFO full error flag is set when the current line of VBI data can not enter the FIFO. For example, if the FIFO has only 10 bytes left and teletext is the current VBI line, the FIFO full error flag is set, but no data is written because the entire teletext line will not fit. However, if the next VBI line is closed caption requiring only 2 bytes of data plus the header, this goes into the FIFO. Even if the full error flag is set.

FIFO empty:

- 0 = FIFO is not empty
- 1 = FIFO is empty

TTX available:

- 0 = Teletext data is not available
- 1 = Teletext data is available

CC field 1 available:

- 0 = Closed caption data from field 1 is not available
- 1 = Closed caption data from field 1 is available

CC field 2 available:

- 0 = Closed caption data from field 2 is not available
- 1 = Closed caption data from field 2 is available

WSS available:

- 0 = WSS data is not available
- 1 = WSS data is available

VPS available:

- 0 = VPS data is not available
- 1 = VPS data is available

VITC available:

- 0 = VITC data is not available
- 1 = VITC data is available

### 2.12.56 FIFO Word Count Register

|         |     |
|---------|-----|
| Address | C7h |
|---------|-----|

| 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---|---|---|---|---|---|---|
| Number of words |   |   |   |   |   |   |   |

This register provides the number of words in the FIFO. Note: 1 word equals 2 bytes.

### 2.12.57 FIFO Interrupt Threshold Register

|         |     |
|---------|-----|
| Address | C8h |
|---------|-----|

|                 |   |   |   |   |   |   |   |
|-----------------|---|---|---|---|---|---|---|
| 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Number of words |   |   |   |   |   |   |   |

This register is programmed to trigger an interrupt when the number of words in the FIFO exceeds this value (default 80h). This interrupt must be enabled at address C1h. Note: 1 word equals 2 bytes.

### 2.12.58 FIFO Reset Register

|         |     |
|---------|-----|
| Address | C9h |
|---------|-----|

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Any data |   |   |   |   |   |   |   |

Writing any data to this register resets the FIFO.

### 2.12.59 Line Number Interrupt Register

|         |     |
|---------|-----|
| Address | CAh |
|---------|-----|

|                |                |             |   |   |   |   |   |
|----------------|----------------|-------------|---|---|---|---|---|
| 7              | 6              | 5           | 4 | 3 | 2 | 1 | 0 |
| Field 1 enable | Field 2 enable | Line number |   |   |   |   |   |

This register is programmed to trigger an interrupt when the video line number matches this value in bits 5:0. This interrupt must be enabled at address C1h. Note, the value of 0 or 1 does not generate an interrupt.

Field 1 enable:

- 0 = Disabled (default)
- 1 = Enabled

Field 2 enable:

- 0 = Disabled (default)
- 1 = Enabled

Line number: (default 00h)

### 2.12.60 Pixel Alignment Registers

|         |         |
|---------|---------|
| Address | CBh–CCh |
|---------|---------|

|         |                    |   |   |   |   |   |                    |   |
|---------|--------------------|---|---|---|---|---|--------------------|---|
| Address | 7                  | 6 | 5 | 4 | 3 | 2 | 1                  | 0 |
| CBh     | Switch pixel [7:0] |   |   |   |   |   |                    |   |
| CCh     | Reserved           |   |   |   |   |   | Switch pixel [9:8] |   |

These registers form a 10-bit horizontal pixel position from the falling edge of sync, where the VDP controller will initiate the program from one line standard to the next line standard. For example, the previous line of teletext to the next line of closed caption. This value must be set so that the switch occurs after the previous transaction has cleared the delay in the VDP, but early enough to allow the new values to be programmed before the current settings are required.

The default value is 0x359 and has been tested with every standard supported here. A new value will only be needed if a custom standard is in use.

### 2.12.61 FIFO Output Control Register

|         |     |
|---------|-----|
| Address | CDh |
|---------|-----|

|          |   |   |   |   |   |   |                    |
|----------|---|---|---|---|---|---|--------------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                  |
| Reserved |   |   |   |   |   |   | Host access enable |

This register is programmed to allow the host port access to the FIFO or allowing all VDP data to go out the video port.

Host access enable:

- 0 = Output FIFO data to the video output Y[9:2]
- 1 = Allow host port access to the FIFO data (default)

### 2.12.62 VDP Clock Register

|         |     |
|---------|-----|
| Address | CEh |
|---------|-----|

|          |   |   |   |   |   |   |                |
|----------|---|---|---|---|---|---|----------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0              |
| Reserved |   |   |   |   |   |   | Clock standard |

Clock standard:

- 0 = Square pixel clock mode (default)
- 1 = ITU-R BT.601 clock mode

### 2.12.63 Full Field Enable Register

|         |     |
|---------|-----|
| Address | CFh |
|---------|-----|

|          |   |   |   |   |   |   |                   |
|----------|---|---|---|---|---|---|-------------------|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0                 |
| Reserved |   |   |   |   |   |   | Full field enable |

This register enables the full field mode. In this mode, all lines outside the vertical blank area and all lines in the line mode registers programmed with FFh will be sliced with the definition of register FCh. Values other than FFh in the line mode registers allow a different slice mode for that particular line.

Full field enable:

- 0 = Disable full field mode (default)
- 1 = Enable full field mode

## 2.12.64 Line Mode Registers

|         |         |
|---------|---------|
| Address | D0h–FBh |
|---------|---------|

| ADDRESS | 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------------|---|---|---|---|---|---|---|
| D0h     | Line 6 Field 1  |   |   |   |   |   |   |   |
| D1h     | Line 6 Field 2  |   |   |   |   |   |   |   |
| D2h     | Line 7 Field 1  |   |   |   |   |   |   |   |
| D3h     | Line 7 Field 2  |   |   |   |   |   |   |   |
| D4h     | Line 8 Field 1  |   |   |   |   |   |   |   |
| D5h     | Line 8 Field 2  |   |   |   |   |   |   |   |
| D6h     | Line 9 Field 1  |   |   |   |   |   |   |   |
| D7h     | Line 9 Field 2  |   |   |   |   |   |   |   |
| D8h     | Line 10 Field 1 |   |   |   |   |   |   |   |
| D9h     | Line 10 Field 2 |   |   |   |   |   |   |   |
| DAh     | Line 11 Field 1 |   |   |   |   |   |   |   |
| DBh     | Line 11 Field 2 |   |   |   |   |   |   |   |
| DCh     | Line 12 Field 1 |   |   |   |   |   |   |   |
| DDh     | Line 12 Field 2 |   |   |   |   |   |   |   |
| DEh     | Line 13 Field 1 |   |   |   |   |   |   |   |
| DFh     | Line 13 Field 2 |   |   |   |   |   |   |   |
| E0h     | Line 14 Field 1 |   |   |   |   |   |   |   |
| E1h     | Line 14 Field 2 |   |   |   |   |   |   |   |
| E2h     | Line 15 Field 1 |   |   |   |   |   |   |   |
| E3h     | Line 15 Field 2 |   |   |   |   |   |   |   |
| E4h     | Line 16 Field 1 |   |   |   |   |   |   |   |
| E5h     | Line 16 Field 2 |   |   |   |   |   |   |   |
| E6h     | Line 17 Field 1 |   |   |   |   |   |   |   |
| E7h     | Line 17 Field 2 |   |   |   |   |   |   |   |
| E8h     | Line 18 Field 1 |   |   |   |   |   |   |   |
| E9h     | Line 18 Field 2 |   |   |   |   |   |   |   |
| EAh     | Line 19 Field 1 |   |   |   |   |   |   |   |
| EBh     | Line 19 Field 2 |   |   |   |   |   |   |   |
| ECh     | Line 20 Field 1 |   |   |   |   |   |   |   |
| EDh     | Line 20 Field 2 |   |   |   |   |   |   |   |
| EEh     | Line 21 Field 1 |   |   |   |   |   |   |   |
| EFh     | Line 21 Field 2 |   |   |   |   |   |   |   |
| F0h     | Line 22 Field 1 |   |   |   |   |   |   |   |
| F1h     | Line 22 Field 2 |   |   |   |   |   |   |   |
| F2h     | Line 23 Field 1 |   |   |   |   |   |   |   |
| F3h     | Line 23 Field 2 |   |   |   |   |   |   |   |
| F4h     | Line 24 Field 1 |   |   |   |   |   |   |   |
| F5h     | Line 24 Field 2 |   |   |   |   |   |   |   |
| F6h     | Line 25 Field 1 |   |   |   |   |   |   |   |
| F7h     | Line 25 Field 2 |   |   |   |   |   |   |   |
| F8h     | Line 26 Field 1 |   |   |   |   |   |   |   |
| F9h     | Line 26 Field 2 |   |   |   |   |   |   |   |
| FAh     | Line 27 Field 1 |   |   |   |   |   |   |   |
| FBh     | Line 27 Field 2 |   |   |   |   |   |   |   |

These registers program the specific VBI standard at a specific line in the video field.

Bit 7:

- 0 = Disable filtering of null bytes in closed caption modes
- 1 = Enable filtering of null bytes in closed caption modes (default)

In teletext modes, bit 7 enables the data filter function for that particular line. If it is set to 0, the data filter passes all data on that line.

Bit 6:

- 0 = Send VBI data to registers only.
- 1 = Send VBI data to FIFO and the registers. Teletext data only goes to FIFO. (default)

Bit 5:

- 0 = Allow VBI data with errors in the FIFO
- 1 = Do not allow VBI data with errors in the FIFO (default)

Bit 4:

- 0 = Do not enable error detection and correction
- 1 = Enable error detection and correction (when bits [3:0] = 0 to 5 only) (default)

Bits [3:0]:

- 0000 = WST SECAM
- 0001 = WST PAL B
- 0010 = WST PAL C
- 0011 = WST NTSC
- 0100 = NABTS NTSC
- 0101 = NABTS NTSC-Japan
- 0110 = CC PAL/SECAM
- 0111 = CC NTSC
- 1000 = WSS PAL/SECAM
- 1001 = WSS NTSC
- 1010 = VITC PAL/SECAM
- 1011 = VITC NTSC
- 1100 = VPS PAL
- 1101 = Custom 1
- 1110 = Custom 2
- 1111 = Active video (default)

A value of FFh in the line mode registers is required for any line to be sliced as part of the full field mode.

## 2.12.65 Full Field Mode Register

|         |     |
|---------|-----|
| Address | FCh |
|---------|-----|

|                 |   |   |   |   |   |   |   |
|-----------------|---|---|---|---|---|---|---|
| 7               | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Full field mode |   |   |   |   |   |   |   |

This register programs the specific VBI standard for full field mode. It can be any VBI standard. Individual line settings take priority over the full field register. This allows each VBI line to be programmed independently but have the remaining lines in full field mode. The full field mode register has the same definitions as the line mode registers (default 7Fh).



## 3 Electrical Specifications

### 3.1 Absolute Maximum Ratings<sup>†</sup>

|                                                            |                                   |
|------------------------------------------------------------|-----------------------------------|
| Digital power supply voltage, DV <sub>DD</sub>             | −0.3 V to 3.6 V                   |
| Analog power supply voltage, AV <sub>DD</sub> <sup>‡</sup> | −0.5 V to 3.6 V                   |
| Digital input voltage, V <sub>I</sub>                      | −0.3 V to DV <sub>DD</sub> +0.3 V |
| Operating free-air temperature, T <sub>A</sub>             | 0°C to 70°C                       |
| Storage temperature, T <sub>stg</sub>                      | −65°C to 150°C                    |

<sup>†</sup> Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup> AFE\_V<sub>DD</sub>, CH1\_AV<sub>DD</sub>, CH2\_AV<sub>DD</sub>, PLL\_AV<sub>DD</sub>

### 3.2 Recommended Operating Conditions

|                                                                                             | MIN | NOM | MAX  | UNIT |
|---------------------------------------------------------------------------------------------|-----|-----|------|------|
| DV <sub>DD</sub> Digital supply voltage                                                     | 3.0 | 3.3 | 3.6  | V    |
| AV <sub>DD</sub> Analog supply voltage                                                      | 3.1 | 3.3 | 3.5  | V    |
| V <sub>I(P-P)</sub> Analog input voltage (ac-coupling necessary)                            | 0.5 | 1.0 | 1.41 | V    |
| V <sub>IH</sub> Digital input voltage high                                                  | 2   |     |      | V    |
| V <sub>IL</sub> Digital input voltage low                                                   |     |     | 0.8  | V    |
| V <sub>IH</sub> (I <sup>2</sup> C) Input voltage high, VC0 and VC1 in I <sup>2</sup> C mode | 2.3 |     |      | V    |
| V <sub>IL</sub> (I <sup>2</sup> C) Input voltage low, VC0 and VC1 in I <sup>2</sup> C mode  |     |     | 1.0  | V    |
| I <sub>OH</sub> Output current, V <sub>out</sub> = 2.4 V                                    | −4  | −8  |      | mA   |
| I <sub>OL</sub> Output current, V <sub>out</sub> = 0.4 V                                    | 6   | 8   |      | mA   |
| T <sub>A</sub> Operating free-air temperature                                               | 0   |     | 70   | °C   |

#### 3.2.1 Crystal Specifications

| CRYSTAL/CLOCK SPECIFICATIONS | MIN | NOM         | MAX | UNIT |
|------------------------------|-----|-------------|-----|------|
| Frequency                    |     | 14.31818/27 |     | MHz  |
| Frequency tolerance          |     |             | ±50 | ppm  |



### 3.3 Electrical Characteristics

$DV_{DD} = 3.3\text{ V}$ ,  $AV_{DD} = 3.3\text{ V}$

For minimum/maximum values:  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ , and for typical values:  $T_A = 25^\circ\text{C}$

#### 3.3.1 DC Electrical Characteristics

| PARAMETER                           |                        | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------|-----------------|-----|-----|-----|------|
| I <sub>DD(D)</sub>                  | Digital supply current | S-video         | 140 |     |     | mA   |
|                                     |                        | CVBS            | 140 |     |     | mA   |
| I <sub>DD(A)</sub>                  | Analog supply current  | S-video         | 110 |     |     | mA   |
|                                     |                        | CVBS            | 65  |     |     | mA   |
| Total power dissipation             |                        | S-video         | 825 |     |     | mW   |
|                                     |                        | CVBS            | 680 |     |     | mW   |
| Total power dissipation (powerdown) |                        |                 | 200 |     |     | mW   |
| I <sub>lkg</sub>                    | Input leakage current  |                 | 10  |     |     | μA   |
| C <sub>i</sub>                      | Input capacitance      | By design       | 8   |     |     | pF   |
| V <sub>OH</sub>                     | Output voltage high    |                 | 2.4 |     |     | V    |
| V <sub>OL</sub>                     | Output voltage low     |                 | 0.4 |     |     | V    |

NOTE 1: Measured with a load of 10 k $\Omega$  in parallel to 15 pF.

#### 3.3.2 Analog Processing and A/D Converters

| PARAMETER                                    |  | TEST CONDITIONS                         | MIN  | TYP  | MAX  | UNIT       |
|----------------------------------------------|--|-----------------------------------------|------|------|------|------------|
| $Z_i$ Input impedance, analog video inputs   |  | By design                               | 200  |      |      | k $\Omega$ |
| $C_i$ Input capacitance, analog video inputs |  | By design                               |      |      | 10   | pF         |
| $V_i(pp)$ Input voltage range                |  | $C_{coupling} = 0.1\text{ }\mu\text{F}$ | 0.50 | 1.0  | 1.41 | V          |
| $\Delta G$ Gain control range                |  |                                         | -3   |      | 6    | dB         |
| DNL DC differential nonlinearity             |  | AFE only                                |      | 0.75 | 1.0  | LSB        |
| INL DC integral nonlinearity                 |  | AFE only                                |      | 1    | 2.5  | LSB        |
| $F_r$ Frequency response                     |  | Multiburst (60 IRE)                     | -0.9 |      | -3   | dB         |
| XTALK Crosstalk                              |  | 6 MHz                                   |      |      | -50  | dB         |
| SNR Signal-to-noise ratio                    |  | 1 MHz, 1.0 V <sub>p-p</sub>             |      | 54   |      | dB         |
| NS Noise spectrum                            |  | Luma ramp (100 kHz to full, tilt-null)  |      | -58  |      | dB         |
| DP Differential phase                        |  | Modulated ramp                          |      | 0.5  |      | °          |
| DG Differential gain                         |  | Modulated ramp                          |      | 1.5% |      |            |

### 3.3.3 Timing

#### 3.3.3.1 Clocks, Video Data, Sync Timing

| PARAMETER             |                                                                    | TEST CONDITIONS<br>(see NOTE 2) | MIN | TYP | MAX | UNIT |
|-----------------------|--------------------------------------------------------------------|---------------------------------|-----|-----|-----|------|
| Duty cycle PCLK, SCLK |                                                                    |                                 | 40% | 50% | 60% |      |
| t <sub>1</sub>        | Rise time SCLK                                                     | 10% to 90%                      |     | 3   |     | ns   |
| t <sub>2</sub>        | Fall time SCLK                                                     | 90% to 10%                      |     | 2   |     | ns   |
| t <sub>3</sub>        | Delay time, SCLK falling edge to PCLK                              | See Note 3                      | -2  |     | 3   | ns   |
| t <sub>4</sub>        | Delay time, SCLK rising edge to PREF                               |                                 |     |     | 5   | ns   |
| t <sub>5</sub>        | Fall time PCLK                                                     | 90% to 10%                      |     | 2   |     | ns   |
| t <sub>6</sub>        | Rise time PCLK                                                     | 10% to 90%                      |     | 3   |     | ns   |
| t <sub>7</sub>        | Delay time, SCLK falling edge to digital outputs except PCLK, PREF | See Note 3                      | -2  |     | 10  | ns   |

NOTES: 2. C<sub>L</sub> = 50 pF  
3. SCLK falling edge may occur up to 2 ns after PREF, Y, UV output transitions.

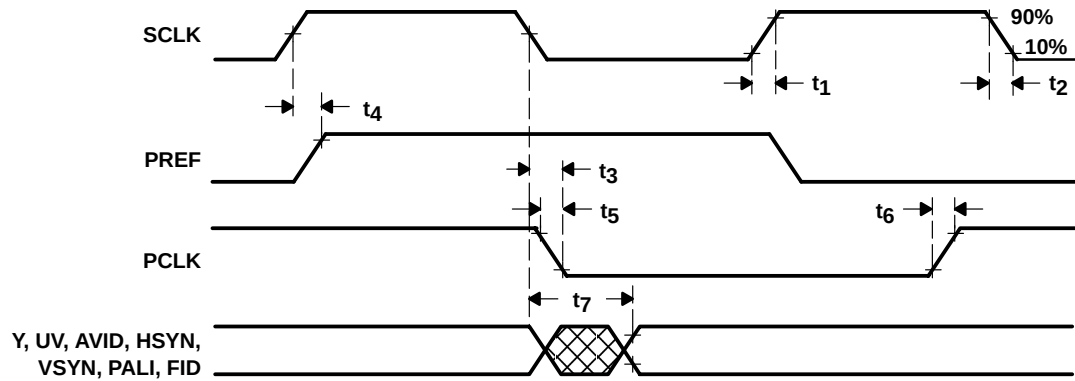


Figure 3-1. Clocks, Video Data, and Sync Timing

3.3.3.2 I<sup>2</sup>C Host Port Timing

| PARAMETER                   |                                             | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|---------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>1</sub>              | Bus free time between STOP and START        |                 | 1.3 |     |     | μs   |
| t <sub>2</sub>              | Data hold time                              |                 | 0   |     | 0.9 | μs   |
| t <sub>3</sub>              | Data setup time                             |                 | 100 |     |     | ns   |
| t <sub>4</sub>              | Setup time for a (repeated) START condition |                 | 0.6 |     |     | μs   |
| t <sub>5</sub>              | Setup time for a STOP condition             |                 | 0.6 |     |     | ns   |
| t <sub>6</sub>              | Hold time (repeated) START condition        |                 | 0.6 |     |     | μs   |
| t <sub>7</sub>              | Rise time VC1(SDA) and VC0(SCL) signal      |                 |     |     | 250 | ns   |
| t <sub>8</sub>              | Fall time VC1(SDA) and VC0(SCL) signal      |                 |     |     | 250 | ns   |
| C <sub>b</sub>              | Capacitive load for each bus line           |                 |     |     | 400 | pF   |
| f <sub>I<sup>2</sup>C</sub> | I <sup>2</sup> C clock frequency            |                 |     |     | 400 | kHz  |

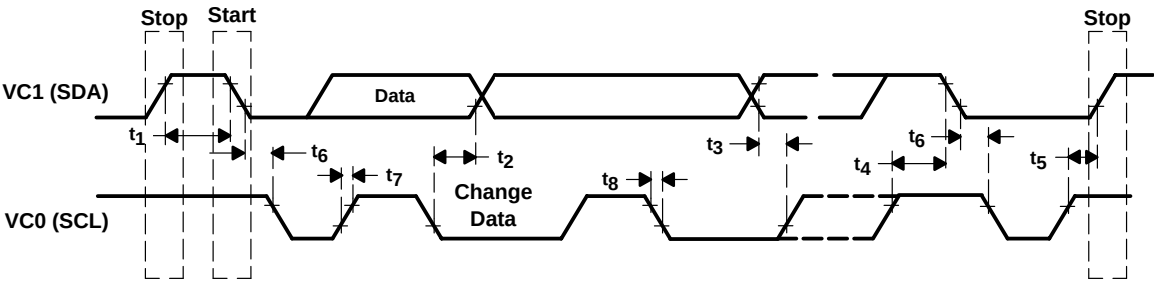


Figure 3–2. I<sup>2</sup>C Host Port Timing

### 3.3.3.3 PHI Host Port Timing (Mode A)

|                | PARAMETER                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|-------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>1</sub> | A[1:0], D[0:7], VC1 setup until VC2 low   |                 | 5   |     |     | ns   |
| t <sub>2</sub> | A[1:0], D[0:7], VC1 hold after VC2 high   |                 | 5   |     |     | ns   |
| t <sub>3</sub> | Delay VC0 low after VC2 low               |                 | 0   |     |     | ns   |
| t <sub>4</sub> | Delay VC2 high after VC0 low              |                 | 5   |     |     | ns   |
| t <sub>5</sub> | Delay VC0 high after VC2 high             |                 | 0   |     |     | ns   |
| t <sub>6</sub> | Delay VC2 low (next cycle) after VC0 high |                 | 5   |     |     | ns   |
| t <sub>7</sub> | (Read cycle) D[7:0] setup until VC0 low   |                 | 10  |     |     | ns   |
| t <sub>8</sub> | (Read cycle) D[7:0] hold after VC2 high   |                 | 0   |     |     | ns   |

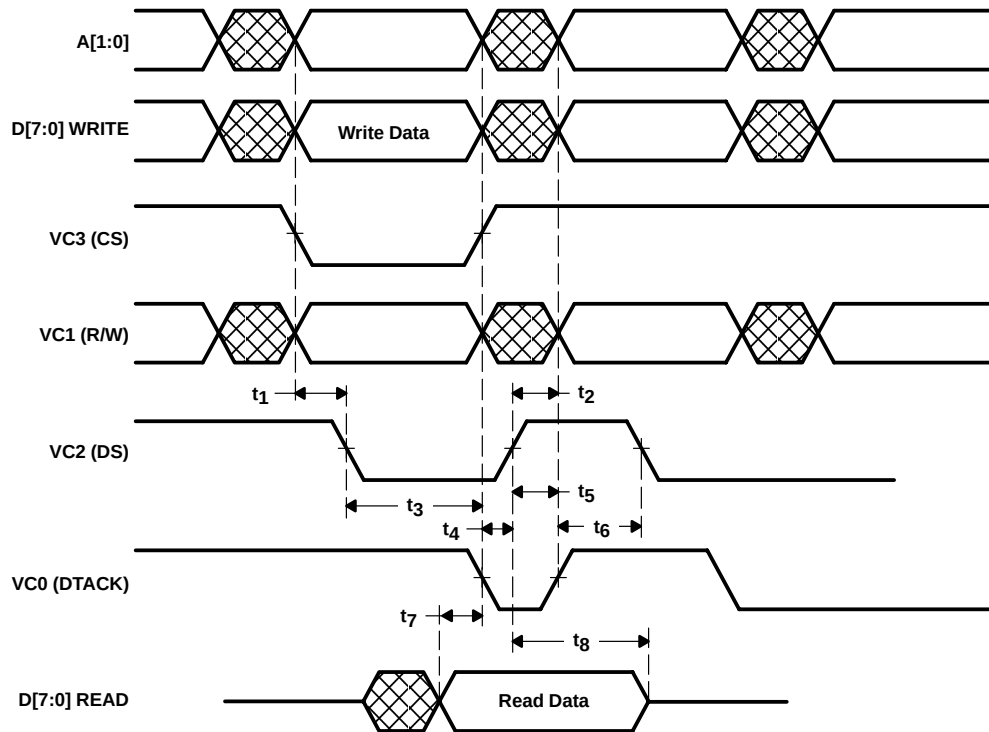


Figure 3–3. PHI Host Port Timing (Mode A)

### 3.3.3.4 PHI Host Port Timing (Mode B)

|                 | PARAMETER                                | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>1</sub>  | A[1:0], VC3 setup until VC1 or VC2 low   |                 | 10  |     |     | ns   |
| t <sub>2</sub>  | A[1:0], VC3 hold after VC1 or VC2 high   |                 | 10  |     |     | ns   |
| t <sub>3</sub>  | Delay VC0 low after VC1 or VC2 low       |                 |     |     | 28  | ns   |
| t <sub>4</sub>  | D[7:0] setup until VC1 low               |                 | 5   |     |     | ns   |
| t <sub>5</sub>  | D[7:0] hold after VC1 high               |                 | 10  |     |     | ns   |
| t <sub>6</sub>  | VC0 low pulse width                      |                 | 10  |     |     | ns   |
| t <sub>7</sub>  | VC1 high until any command active        |                 | 80  |     |     | ns   |
| t <sub>8</sub>  | VC1, VC2 command pulse width             |                 | 40  |     |     | ns   |
| t <sub>9</sub>  | (Read cycle) D[7:0] setup until VC0 high |                 | 0   |     |     | ns   |
| t <sub>10</sub> | (Read cycle) D[7:0] hold after VC2 high  |                 | 0   |     |     | ns   |
| t <sub>11</sub> | Delay VC1 or VC2 high after VC0 high     |                 | 0   |     |     | ns   |

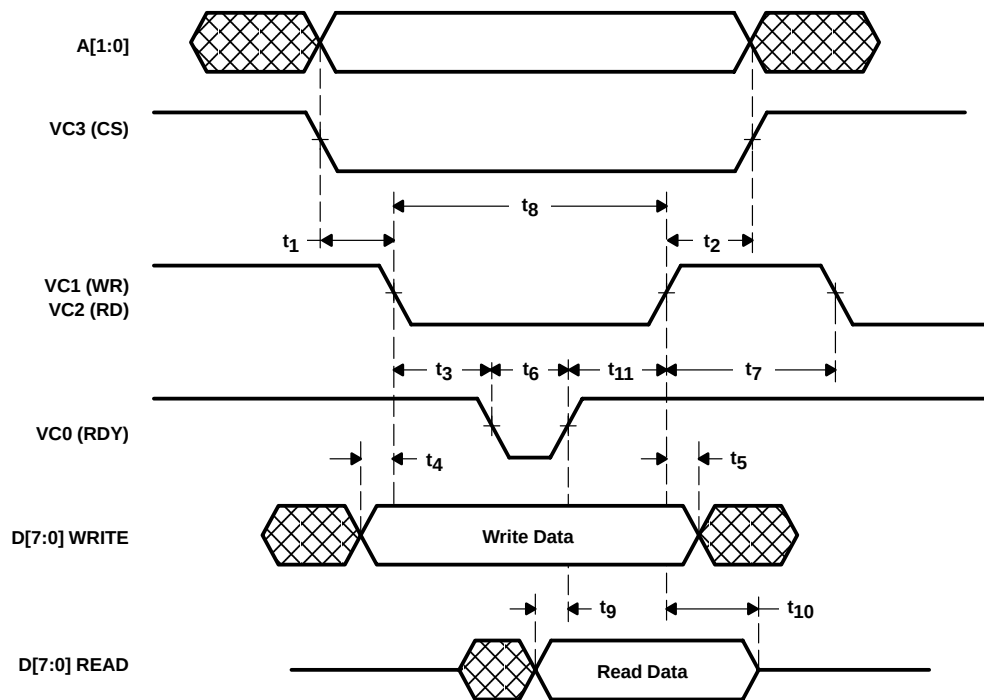


Figure 3–4. PHI Host Port Timing (Mode B)

### 3.3.3.5 PHI Host Port Timing (Mode C)

|                | PARAMETER                                    | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|----------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>1</sub> | A[1:0], D[7:0], VC1, VC3 setup until VC2 low |                 | 5   |     |     | ns   |
| t <sub>2</sub> | A[1:0], D[7:0], VC1, VC3 hold after VC2 high |                 | 0   |     |     | ns   |
| t <sub>3</sub> | Delay VC0 low after VC2 low                  |                 | 2   |     |     | ns   |
| t <sub>4</sub> | (Read cycle) D[7:0] setup until VC0 high     |                 | 20  |     |     | ns   |
| t <sub>5</sub> | (Read cycle) D[7:0] hold after VC0 high      |                 | 0   |     |     | ns   |

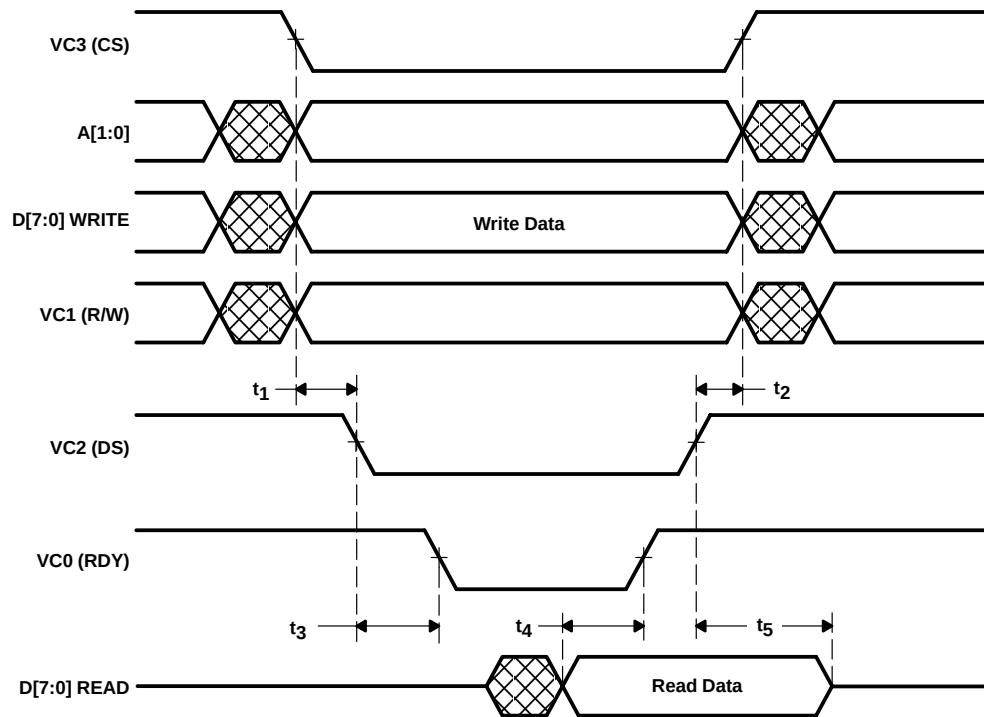


Figure 3–5. PHI Host Port Timing (Mode C)



## 4 Application Information

### 4.1 Application Example

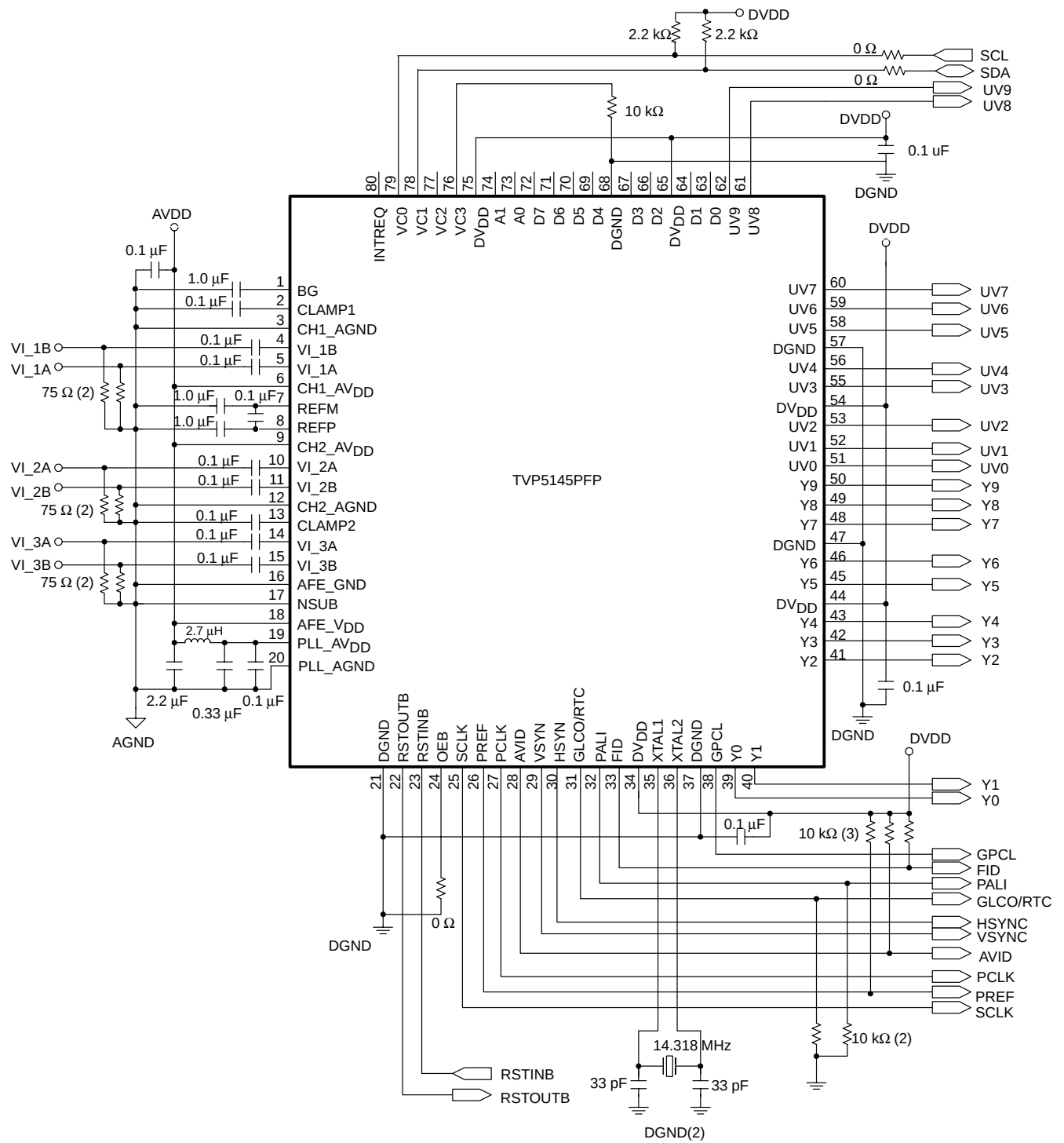


Figure 4–1. Application Example



## 4.2 Designing With PowerPAD™

The TVP5145 device is housed in a high-performance, thermally enhanced, 80-pin PowerPAD package (TI package designator: 80PFP). Use of the PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing the PowerPAD PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD of connection etches or vias under the package. The recommended option, however, is not to run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 80-terminal PFP PowerPAD package is 8 mm x 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: <http://www.ti.com>

For the TVP5145 device, this thermal land must be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size must be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TVP5145PFP       | NRND                  | HTQFP        | PFP             | 80   | 96          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-3-260C-168 HR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

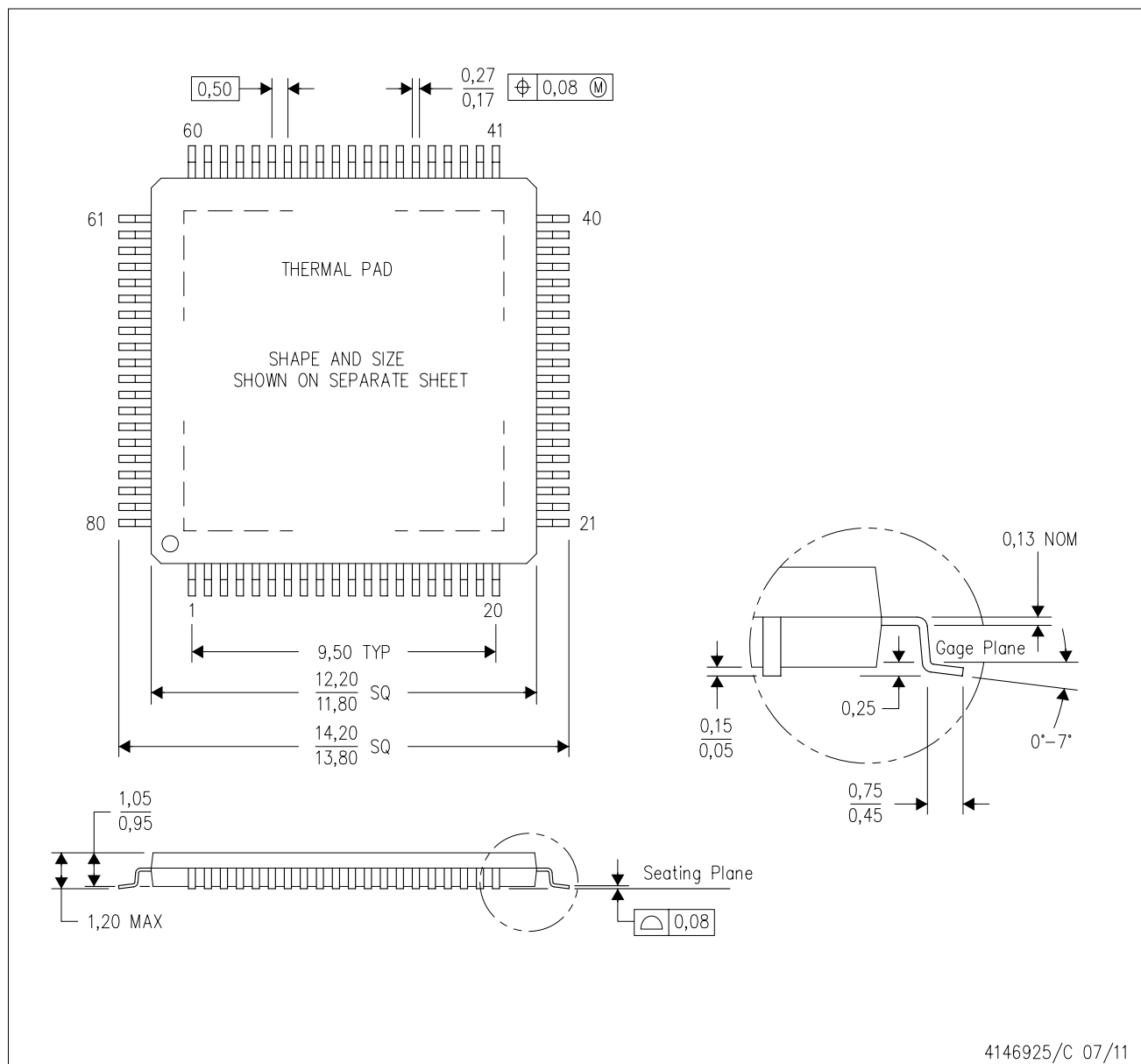
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## THERMAL PAD MECHANICAL DATA

PFP (S-PQFP-G80)

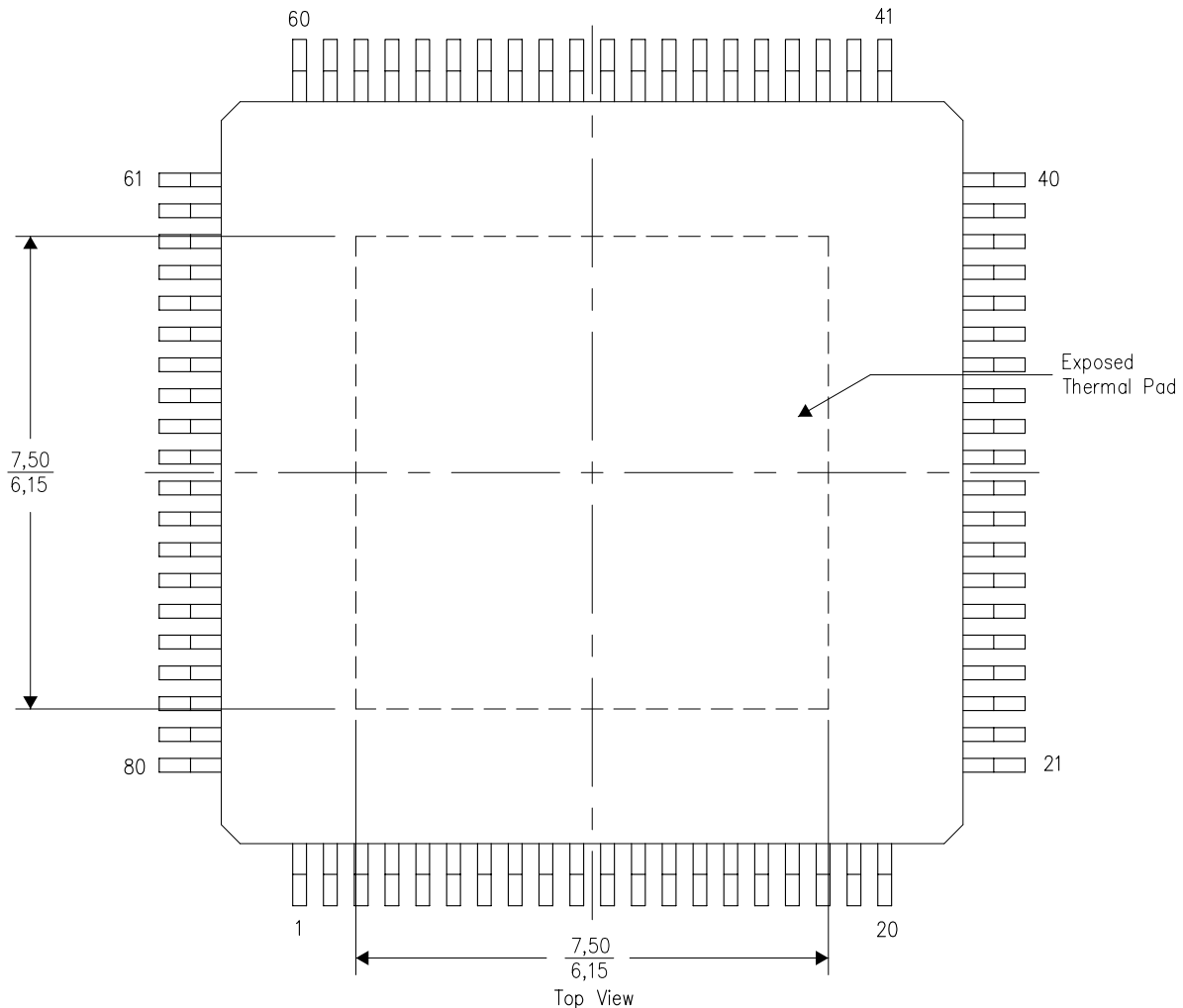
PowerPAD™ PLASTIC QUAD FLATPACK

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



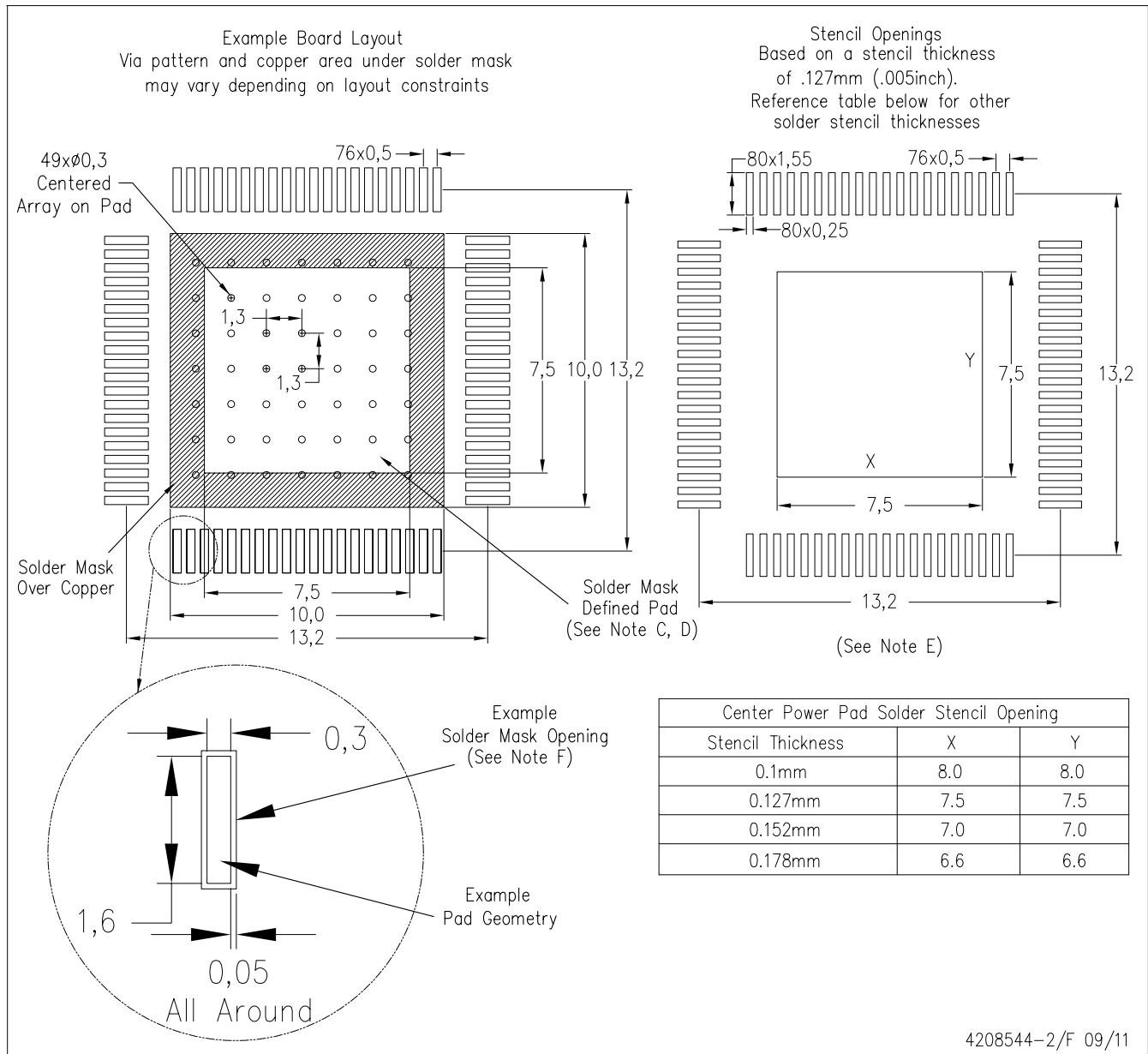
4206327-2/N 09/11

NOTE: A. All linear dimensions are in millimeters

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PFP (S-PQFP-G80)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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