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FAIRCHILD

SEMICONDUCTOR®

FDG6335N 20V N-Channel PowerTrench[®] MOSFET

General Description

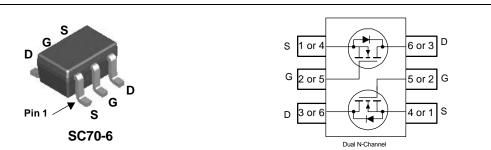
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low $R_{DS(ON)}$ and gate charge (Q_G) in a small package.

Applications

- DC/DC converter
- Power management
- Loadswitch

Features

- $\mbox{ or } A, \mbox{ 20 V}. \qquad R_{DS(ON)} = 300 \mbox{ m} \Omega \ @ \ V_{GS} = 4.5 \ V \\ R_{DS(ON)} = 400 \mbox{ m} \Omega \ @ \ V_{GS} = 2.5 \ V \\ \label{eq:DS(ON)}$
- Low gate charge (1.1 nC typical)
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$
- Compact industry standard SC70-6 surface mount package



The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

Absolute Maximum Ratings T_{A=25°C} unless otherwise noted

Symbol	Parameter			Ratings	Units	
V _{DSS}	Drain-Source Voltage			20	V	
V _{GSS}	Gate-Source Voltage			± 12		
I _D	Drain Current – Continuous		(Note 1)	0.7	А	
	– Pulsed			2.1		
PD	Power Dissi	pation for Single Operation	(Note 1)	0.3	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C	
. 3, . 310	- - J - J - J		9			
	I Charact	5	5			
Therma	I Charact	5		415	°C/W	
Therma _{R₀JA} Packag	I Charact	teristics sistance, Junction-to-Ambie g and Ordering Ir	ent (Note 1)	-	°C/W	
Therma R _{eJA}	I Charact	sistance, Junction-to-Ambie	ent (Note 1)	415 Tape width	°C/W	

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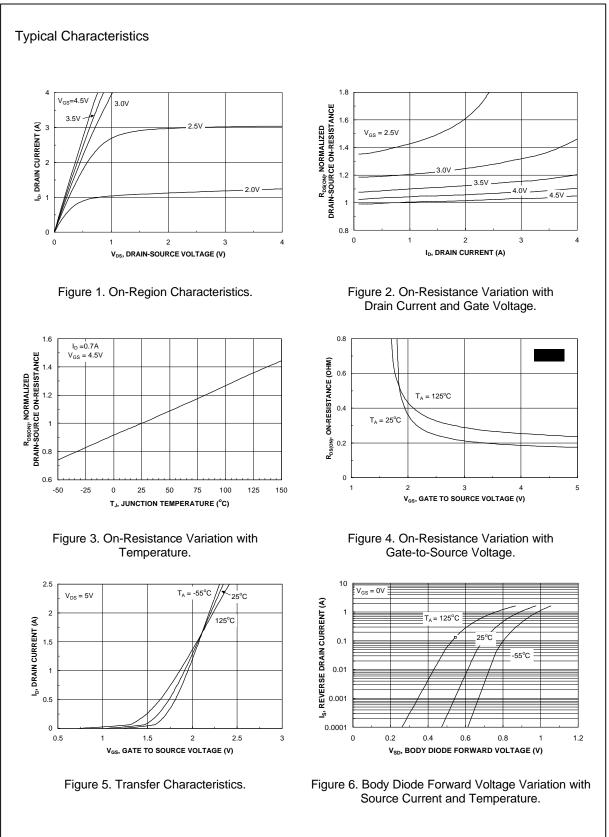
FDG6335N

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					•
BV _{DSS} Drain–Source Breakdown Voltage		$V_{GS}=0~V, \qquad I_D=250~\mu A$	20			V
<u>ΔBVdss</u> ΔTj	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
I _{GSSF}	Gate–Body Leakage, Forward $V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Chara	acteristics (Note 2)				•	
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, \qquad I_D = 250 \ \mu A$	0.6	1.1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_{J}}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C		-2.8		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS}=4.5 \ V, I_{D}=0.7 \ A \\ V_{GS}=2.5 \ V, I_{D}=0.6 \ A \\ V_{GS}=4.5 \ V, I_{D}=0.7 \ A, \ T_{J}{=}125^{\circ}C \end{array} $		180 293 247	300 400 442	mΩ
I _{D(on)}	On–State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$	1			Α
g fs	Forward Transconductance	$V_{\text{DS}} = 5 \text{ V}, \qquad I_{\text{D}} = 0.7 \text{ A}$		2.8		S
Dynamic	Characteristics				•	
C _{iss}	Input Capacitance			113		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		34		pF
C _{rss}	Reverse Transfer Capacitance			16		pF
Switching	Characteristics (Note 2)					
d(on)	Turn-On Delay Time	$V_{DD} = 10 \text{ V}, \qquad I_D = 1 \text{ A},$		5	10	ns
tr	Turn–On Rise Time	V_{GS} = 4.5 V, R_{GEN} = 6 Ω		7	15	ns
t _{d(off)}	Turn–Off Delay Time			9	18	ns
li i	Turn–Off Fall Time			1.5	3	ns
Q _g	Total Gate Charge	$V_{DS} = 10 \text{ V}, I_D = 0.7 \text{ A},$		1.1	1.4	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = 4.5 V$		0.24		nC
Q _{gd}	Gate-Drain Charge			0.3		nC
Drain-Sc	ource Diode Characteristics	and Maximum Ratings				
ls	Maximum Continuous Drain-Sour	0			0.25	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \ V, \qquad I_S = 0.25 \ A \ (Note 2)$		0.74	1.2	V

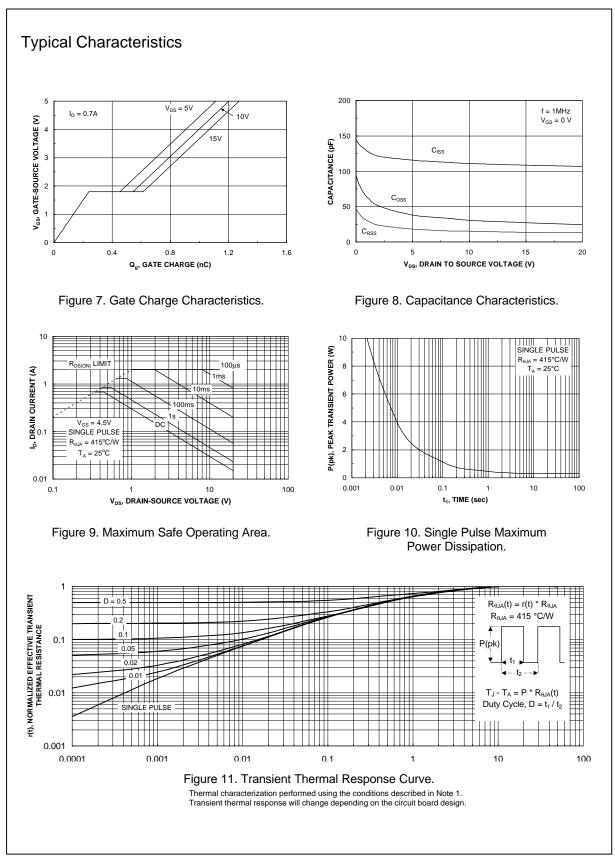
the drain pins. R_{BJC} is guaranteed by design while R_{BJA} is determined by the user's board design. $R_{BJA} = 415^{\circ}C/W$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

FDG6335N Rev C (W)



FDG6335N



FDG6335N

FDG6335N Rev C (W)

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