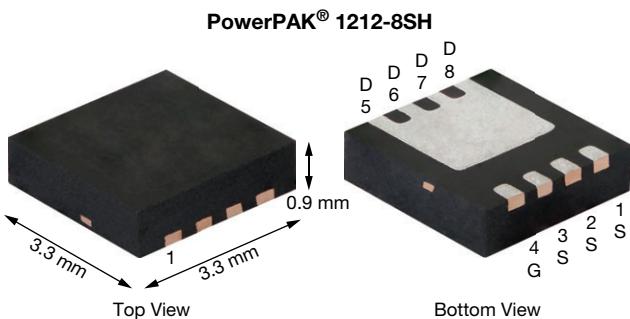


P-Channel 30 V (D-S) MOSFET



FEATURES

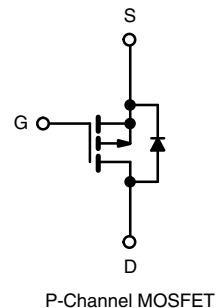
- TrenchFET® power MOSFET
- Low thermal resistance PowerPAK® package with small size
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load switch
- Adapter switch
- Notebook PC



PRODUCT SUMMARY

V_{DS} (V)	-30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -10$ V	0.0114
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5$ V	0.0200
Q_g typ. (nC)	24.6
I_D (A) ^{e, f}	-35
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH129DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-30	
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	-35 ^e	A
	$T_C = 70$ °C		
	$T_A = 25$ °C		
	$T_A = 70$ °C		
Pulsed drain current	I_{DM}	-60	
Continuous source-drain diode current	$T_C = 25$ °C	-35 ^e	
	$T_A = 25$ °C	-3.2 ^{a, b}	
Avalanche current	I_{AS}	-25	
Single pulse avalanche energy	E_{AS}	31.25	mJ
Maximum power dissipation	$T_C = 25$ °C	52.1	
	$T_C = 70$ °C	3.3	W
	$T_A = 25$ °C	3.8 ^{a, b}	
	$T_A = 70$ °C	2.4 ^{a, b}	
Operating junction and storage temperature range	T_J, T_{stg}	-50 to +150	
Soldering recommendations (peak temperature) ^{c, d}		260	°C

Notes

- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?773257). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Package limited
- Based on $T_C = 25$ °C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient a, b	$t \leq 10 \text{ s}$	R_{thJA}	26	33	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.9	2.4	°C/W

Notes

- a. Surface mounted on 1" x 1" FR4 board
b. Maximum under steady state conditions is 81 °C/W

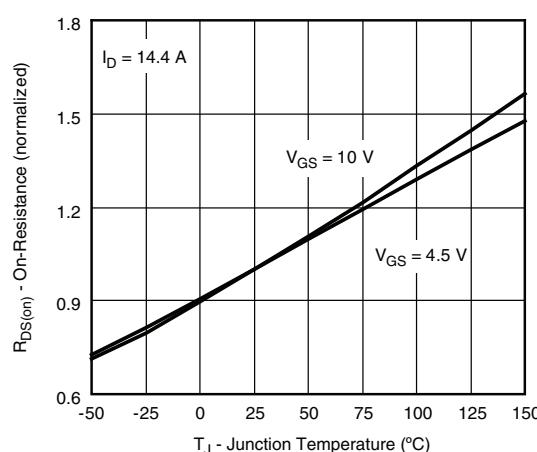
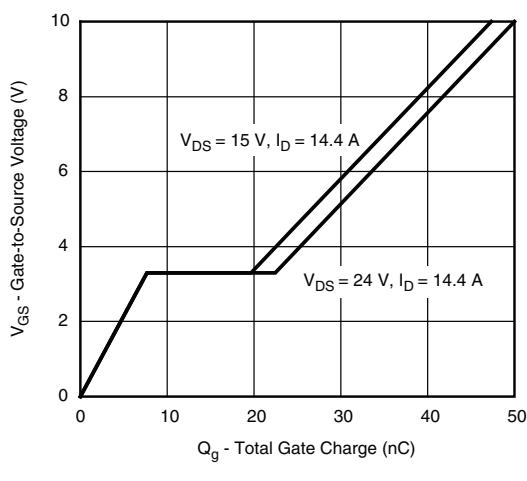
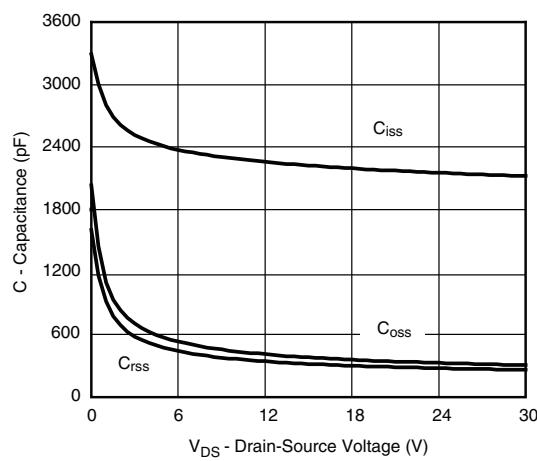
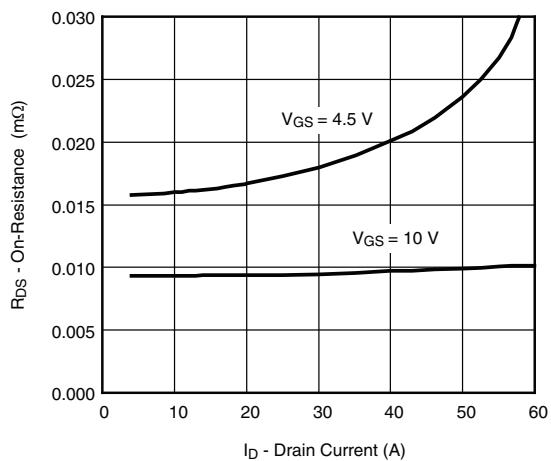
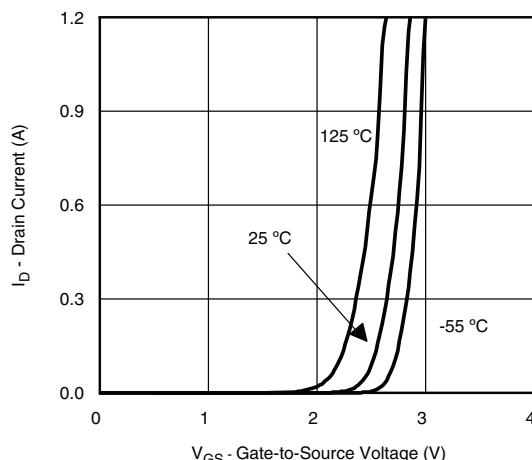
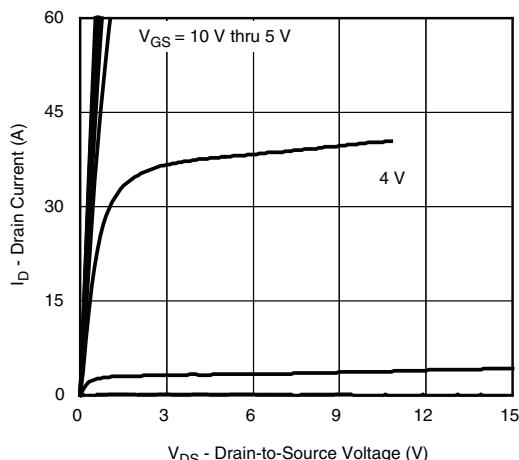
SPECIFICATIONS ($T_J = 25 \text{ °C}$, unless otherwise noted)

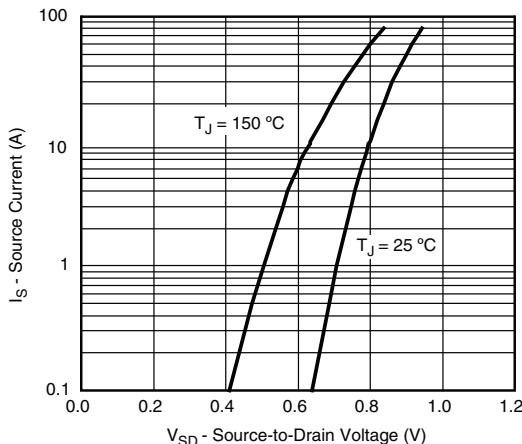
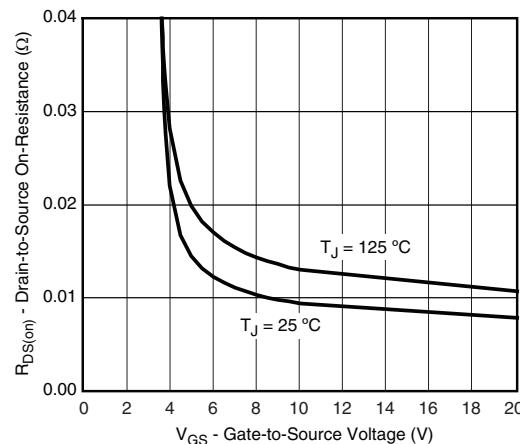
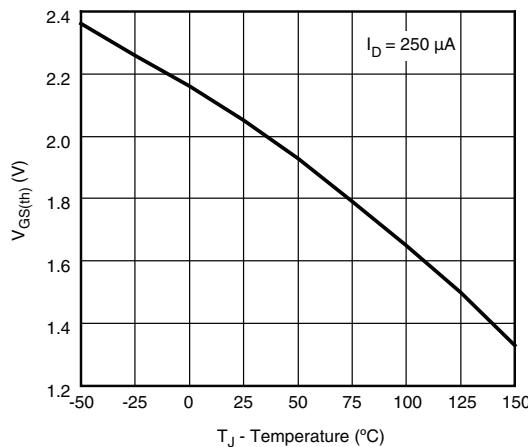
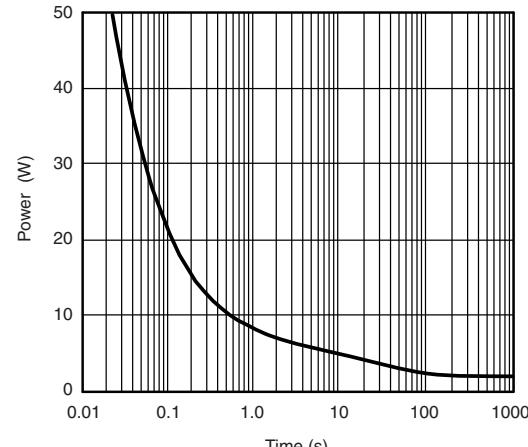
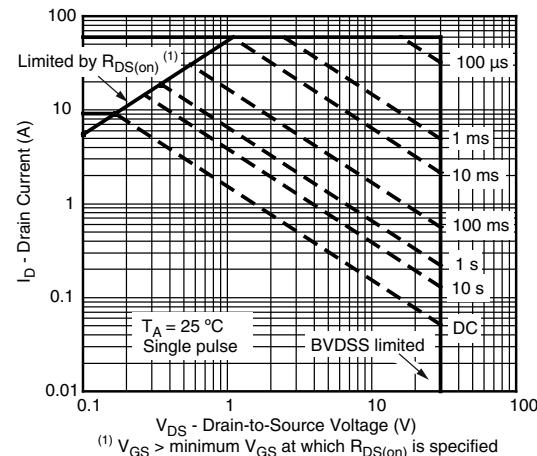
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-30	-	-	V	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250 \mu\text{A}$	-	-20	-	mV/°C	
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	5	-		
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1.5	-	-2.8	V	
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μA	
		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55 \text{ °C}$	-	-	-10		
On-state drain current ^a	$I_{D(\text{on})}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -10 \text{ V}$	-20	-	-	A	
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = -10 \text{ V}, I_D = -14.4 \text{ A}$	-	0.0095	0.0114	Ω	
		$V_{GS} = -4.5 \text{ V}, I_D = -11.5 \text{ A}$	-	0.0160	0.0200		
Forward transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -14.4 \text{ A}$	-	37	-	S	
Dynamic ^b							
Input capacitance	C_{iss}	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2230	3345	pF	
Output capacitance	C_{oss}		-	385	578		
Reverse transfer capacitance	C_{rss}		-	322	-		
Total gate charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -14.4 \text{ A}$	-	47.5	71	nC	
Gate-source charge	Q_{gs}		-	24.6	37		
Gate-drain charge	Q_{gd}		-	7.7	-		
Gate resistance	R_g		-	12	-		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 1.5 \Omega$ $I_D \equiv -10 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	0.4	1.8	3.6	Ω
Rise time	t_r		-	50	75	ns	
Turn-off delay time	$t_{d(off)}$		-	43	65		
Fall time	t_f		-	30	45		
Turn-on delay time	$t_{d(on)}$		-	14	21		
Rise time	t_r		-	14	21		
Turn-off delay time	$t_{d(off)}$		-	9	18		
Fall time	t_f		-	36	54		
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25 \text{ °C}$	-	-	-35 ^e	A	
Pulse diode forward current ^a	I_{SM}		-	-	-60		
Body diode voltage	V_{SD}	$I_F = -10 \text{ A}$	-	-0.8	-1.2	V	
Body diode reverse recovery time	t_{rr}	$I_F = -10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, T_J = 25 \text{ °C}$	-	31	47	ns	
Body diode reverse recovery charge	Q_{rr}		-	30	45	nC	
Reverse recovery fall time	t_a		-	15	-	ns	
Reverse recovery rise time	t_b		-	16	-		

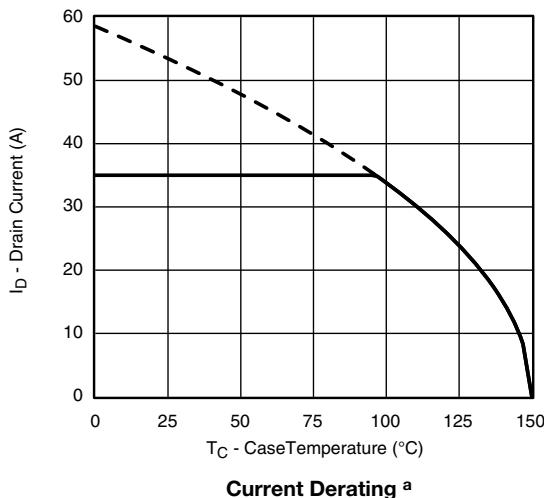
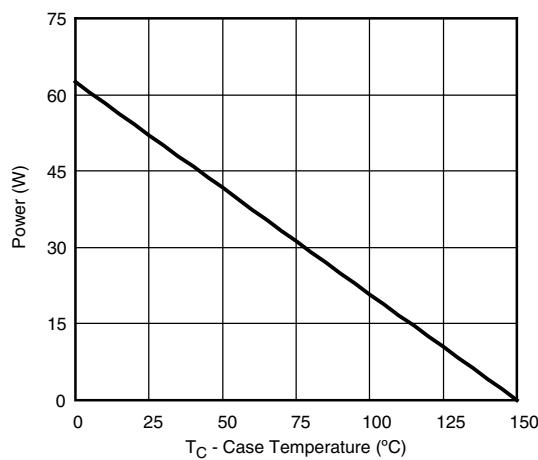
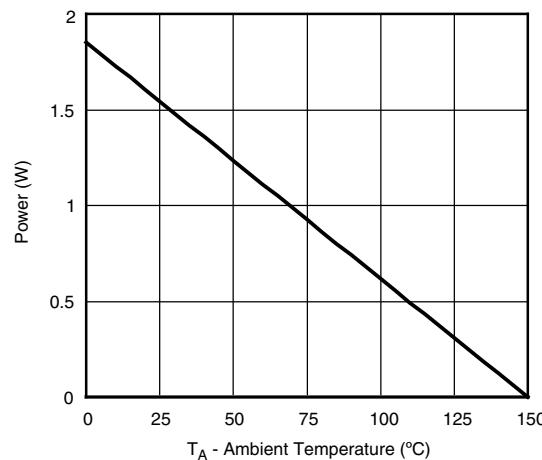
Notes

- a. Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$
b. Guaranteed by design, not subject to production testing

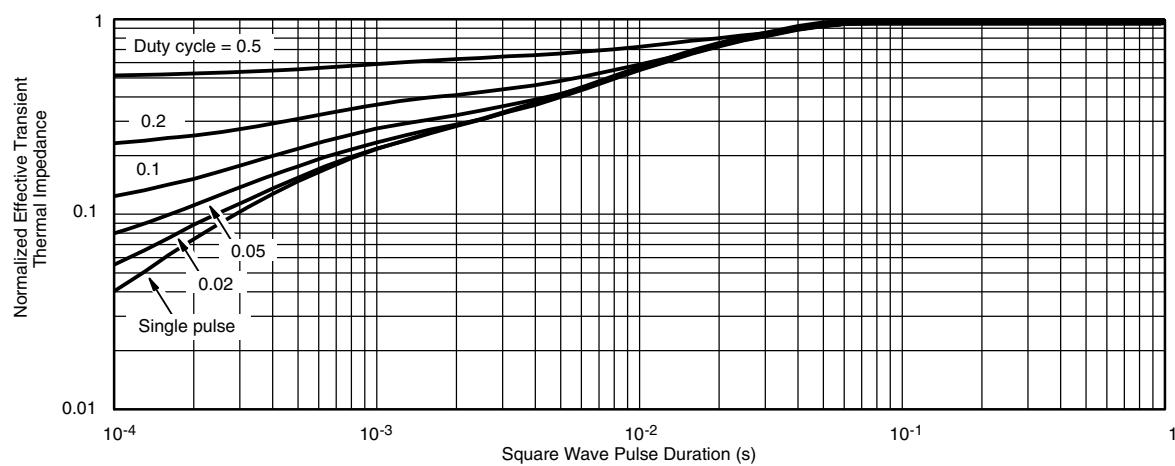
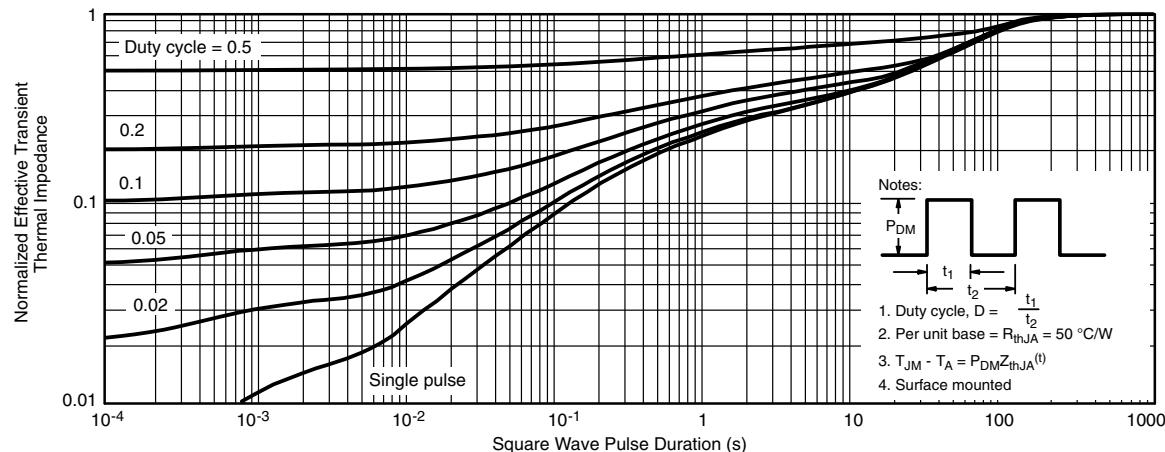
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

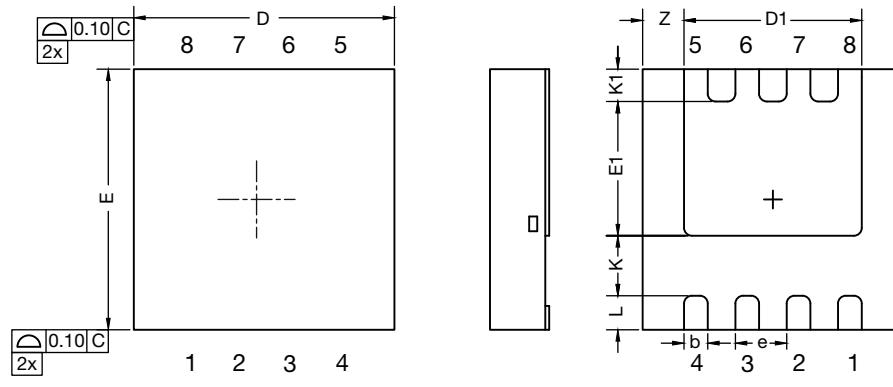
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

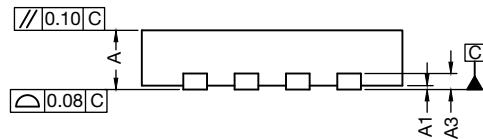
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75903.

PowerPAK® 1212-SWLH



Backside view



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.30 BSC			0.012 BSC		
D	3.30 BSC			0.130 BSC		
D1	2.15	2.25	2.35	0.084	0.088	0.092
E	3.30 BSC			0.130 BSC		
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 BSC			0.026 BSC		
K	0.76 typ.			0.030 typ.		
K1	0.41 typ.			0.016 typ.		
L	0.43 BSC			0.017 BSC		
Z	0.525 typ.			0.021 typ.		

ECN: C18-0001-Rev. A, 15-Jan-18

DWG: 6062



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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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