

MC14069UB

Hex Inverter

The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Triple Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|-------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

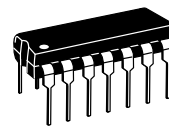
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



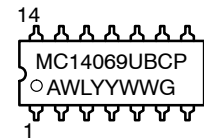
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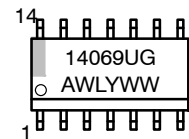
MARKING DIAGRAMS



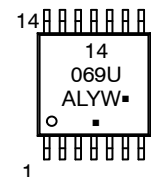
PDIP-14
P SUFFIX
CASE 646



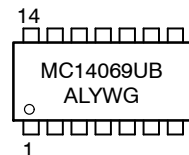
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOEIAJ-14
F SUFFIX
CASE 965



A = Assembly Location

WL, L = Wafer Lot

YY, Y = Year

WW, W = Work Week

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14069UB

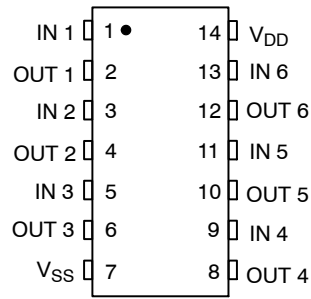


Figure 1. Pin Assignment

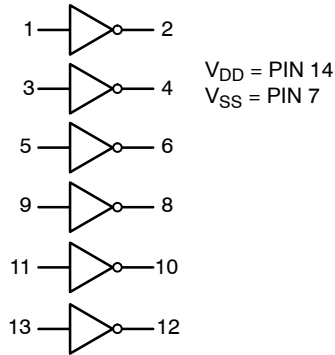
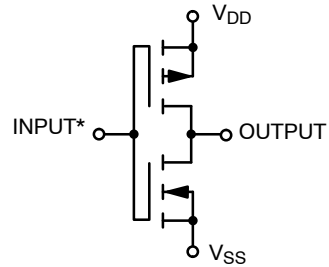


Figure 3. Logic Diagram



*Double diode protection on all inputs not shown
(1/6 of circuit shown)

Figure 2. Circuit Schematic

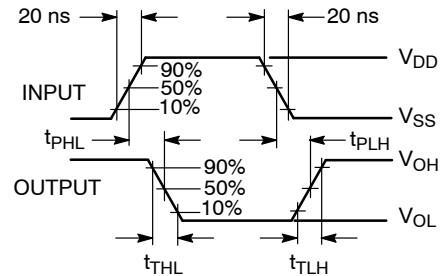
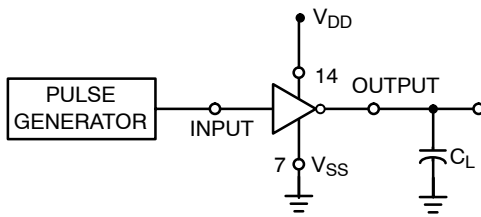


Figure 4. Switching Time Test Circuit and Waveforms

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|------------------------|-----------------------------------|
| MC14069UBCPG | PDIP-14 (Pb-Free) | 500 Units / Tape & Ammunition Box |
| MC14069UBDG | SOIC-14 (Pb-Free) | 55 Units / Rail |
| MC14069UBDR2G | SOIC-14 (Pb-Free) | 2500 Units / Tape & Reel |
| MC14069UBDTR2G | TSSOP-14* | 2500 Units / Tape & Reel |
| MC14069UBFELG | SOEIAJ-14 (Pb-Free) | 2000 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V_{DD} Vdc | - 55°C | | 25°C | | | 125°C | | Unit |
|---|--|-----------------|--|-----------|-------|--------------------|-----------|-------|-----------|-----------------|
| | | | Min | Max | Min | Typ ⁽²⁾ | Max | Min | Max | |
| Output Voltage $V_{in} = V_{DD}$ $V_{in} = 0$ | "0" Level V_{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | "1" Level V_{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | |
| | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | |
| | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | |
| Input Voltage $(V_O = 4.5 \text{ Vdc})$ $(V_O = 9.0 \text{ Vdc})$ $(V_O = 13.5 \text{ Vdc})$ $(V_O = 0.5 \text{ Vdc})$ $(V_O = 1.0 \text{ Vdc})$ $(V_O = 1.5 \text{ Vdc})$ | "0" Level V_{IL} | 5.0 | - | 1.0 | - | 2.25 | 1.0 | - | 1.0 | Vdc |
| | | 10 | - | 2.0 | - | 4.50 | 2.0 | - | 2.0 | |
| | | 15 | - | 2.5 | - | 6.75 | 2.5 | - | 2.5 | |
| | "1" Level V_{IH} | 5.0 | 4.0 | - | 4.0 | 2.75 | - | 4.0 | - | |
| | | 10 | 8.0 | - | 8.0 | 5.50 | - | 8.0 | - | |
| | | 15 | 12.5 | - | 12.5 | 8.25 | - | 12.5 | - | |
| Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$ $(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$ | Source I_{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | |
| | Sink I_{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | |
| 15 | | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | | |
| Input Current | I_{in} | 15 | - | ± 0.1 | - | ± 0.00001 | ± 0.1 | - | ± 1.0 | μAdc |
| Input Capacitance $(V_{in} = 0)$ | C_{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF |
| Quiescent Current (Per Package) | I_{DD} | 5.0 | - | 0.25 | - | 0.0005 | 0.25 | - | 7.5 | μAdc |
| | | 10 | - | 0.5 | - | 0.0010 | 0.5 | - | 15 | |
| | | 15 | - | 1.0 | - | 0.0015 | 1.0 | - | 30 | |
| Total Supply Current ^{(3) (4)} (Dynamic plus Quiescent, Per Gate) ($C_L = 50 \text{ pF}$) | I_T | 5.0 | $I_T = (0.3 \mu\text{A/kHz}) f + I_{DD}/6$ | | | | | | | μAdc |
| 10 | $I_T = (0.6 \mu\text{A/kHz}) f + I_{DD}/6$ | | | | | | | | | |
| 15 | $I_T = (0.9 \mu\text{A/kHz}) f + I_{DD}/6$ | | | | | | | | | |
| Output Rise and Fall Times ⁽³⁾ $(C_L = 50 \text{ pF})$ $t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH}, t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH}, t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$ | $t_{TLH},$ t_{THL} | 5.0 | - | - | - | 100 | 200 | - | - | ns |
| | | 10 | - | - | - | 50 | 100 | - | - | |
| | | 15 | - | - | - | 40 | 80 | - | - | |
| | | 15 | - | - | - | 40 | 80 | - | - | |
| Propagation Delay Times ⁽³⁾ $(C_L = 50 \text{ pF})$ $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 22 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 17 \text{ ns}$ | $t_{PLH},$ t_{PHL} | 5.0 | - | - | - | 65 | 125 | - | - | ns |
| | | 10 | - | - | - | 40 | 75 | - | - | |
| | | 15 | - | - | - | 30 | 55 | - | - | |
| | | 15 | - | - | - | 30 | 55 | - | - | |

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

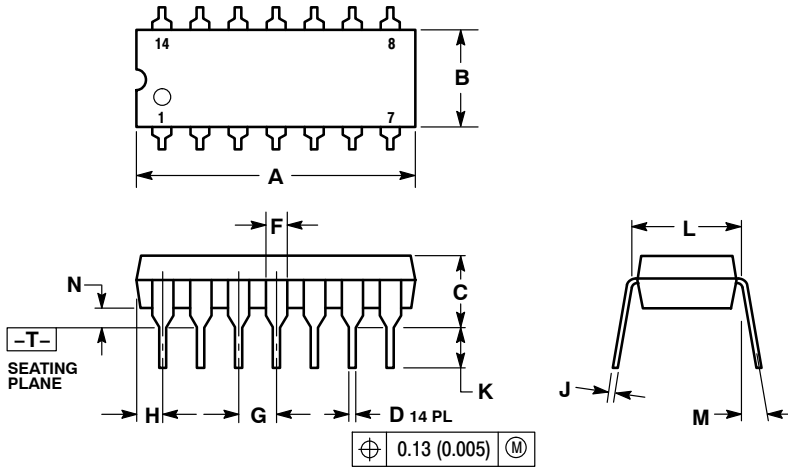
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

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PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

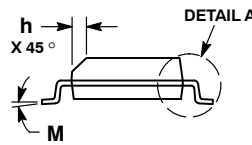
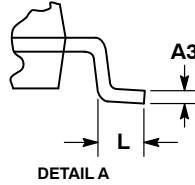
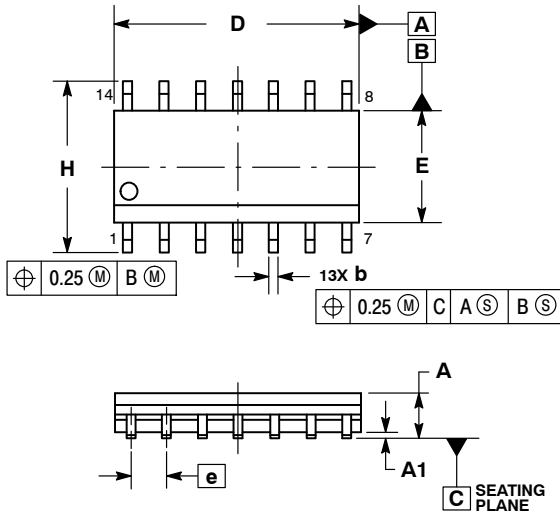
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

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PACKAGE DIMENSIONS

SOIC-14 NB
CASE 751A-03
ISSUE K

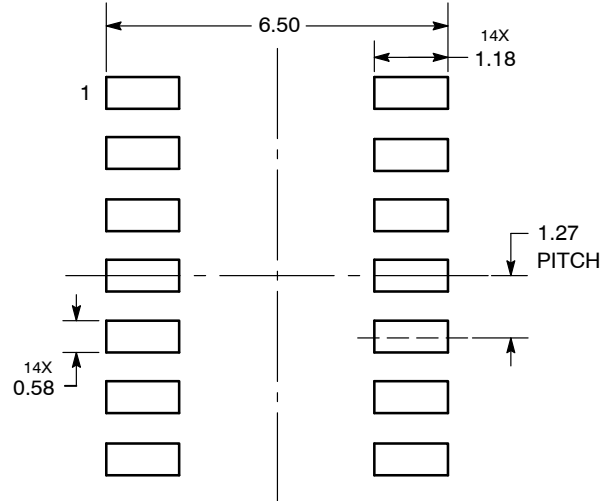


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



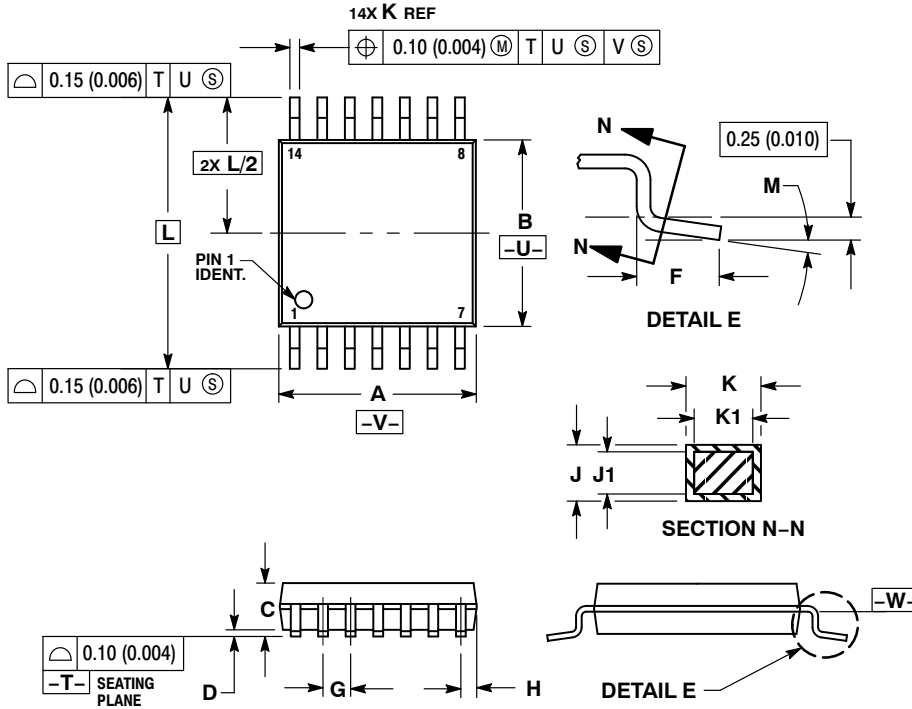
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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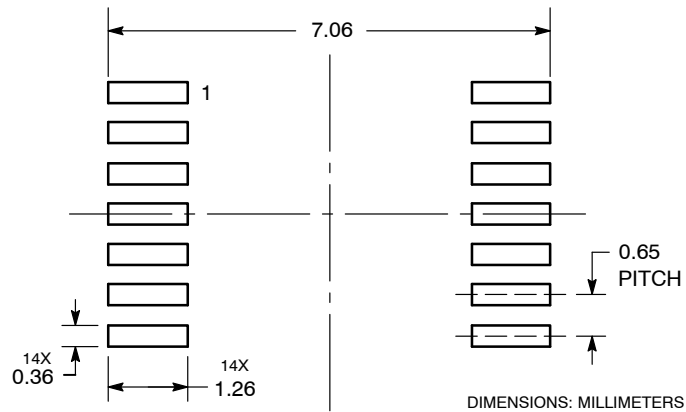
PACKAGE DIMENSIONS

TSSOP-14
CASE 948G-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT*

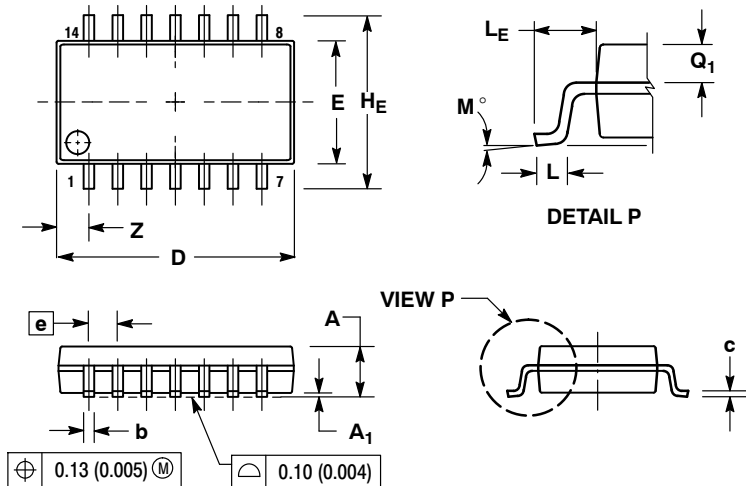


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14069UB

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| HE | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| LE | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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