

### FEATURES

- Guaranteed  $\overline{\text{RESET}}$  valid with  $V_{CC} = 1 \text{ V}$
- 190  $\mu\text{A}$  quiescent current
- Precision supply voltage monitor
  - 4.65 V (ADM705/ADM707)
  - 4.40 V (ADM706/ADM708)
- 200 ms reset pulse width
- Debounce TTL/CMOS manual reset input ( $\overline{\text{MR}}$ )
- Independent watchdog timer (ADM705/ADM706)
- 1.60 sec timeout (ADM705/ADM706)
- Active high reset output (ADM707/ADM708)
- Voltage monitor for power fail or low battery warning
- Superior upgrade for MAX705 to MAX708

### APPLICATIONS

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Critical microprocessor supply monitoring

### GENERAL DESCRIPTION

The ADM705/ADM706/ADM707/ADM708 microprocessor supervisory circuits are suitable for monitoring 5 V power supplies/batteries and microprocessor activity.

The ADM705/ADM706 provide power-supply monitoring circuitry that generate a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with  $V_{CC}$  as low as 1 V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.60 sec.

In addition, there is a 1.25 V threshold detector to warn of power failures, to detect low battery conditions, or to monitor an additional power supply. An active low, debounced manual reset input ( $\overline{\text{MR}}$ ) is also included.

### FUNCTIONAL BLOCK DIAGRAMS



Figure 1. ADM705/ADM706



Figure 2. ADM707/ADM708

The ADM705 and ADM706 are identical except for the reset threshold monitor levels, which are 4.65 V and 4.40 V, respectively.

The ADM707 and ADM708 provide a similar functionality to the ADM705 and ADM706 and only differ in that a watchdog timer function is not available. Instead, an active high reset output (RESET) is available as well as the active low reset output ( $\overline{\text{RESET}}$ ). The ADM707 and ADM708 are identical except for the reset threshold monitor levels, which are 4.65 V and 4.40 V, respectively.

All devices are available in narrow 8-lead PDIP and 8-lead SOIC packages.

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## REVISION HISTORY

### 1/16—Rev. G to Rev. H

Changes to Table 3.....	5
Changes to Power Fail Comparator Section and Figure 15 .....	8
Changes to Figure 16.....	9
Changes to Figure 18 and Figure 20.....	10
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

### 3/08—Rev. F to Rev. G

Changes to Applications .....	1
Changes to Table 2.....	4
Changes to Figure 9.....	6
Changes to Figure 10, Figure 11, and Figure 12 .....	7
Changes to Figure 14.....	8
Changes to Ordering Guide .....	12

### 2/07—Rev. E to Rev. F

Updated Format.....	Universal
Changes to Watchdog Timeout Period.....	3
Replaced Pin Configurations and Function Descriptions Section..	5

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### 7/06—Rev. D to Rev. E

Added RM-8 (MSOP) Package.....	Universal
Changes to Table 2.....	4
Updated Outline Dimensions.....	12
Changes to Ordering Guide .....	12

### 11/05—Rev. C to Rev. D

Updated Format.....	Universal
Deleted Figure 2.....	4
Updated Outline Dimensions.....	11
Changes to Ordering Guide .....	12

### 8/02—Rev. B to Rev. C

Removed RM-8 ( $\mu$ SOIC) Package.....	Universal
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## SPECIFICATIONS

$V_{CC} = 4.75\text{ V to }5.5\text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
$V_{CC}$ Operating Voltage Range	1.0		5.5	V	
Supply Current		190	250	$\mu\text{A}$	
LOGIC OUTPUT					
Reset Threshold	4.5	4.65	4.75	V	ADM705/ADM707
	4.25	4.40	4.50	V	ADM706/ADM708
Reset Threshold Hysteresis		40		mV	
RESET PULSE WIDTH	160	200	280	ms	
RESET OUTPUT VOLTAGE					
	$V_{CC} - 1.5$		0.4	V	$I_{SOURCE} = 800\ \mu\text{A}$
			0.3	V	$I_{SINK} = 3.2\ \text{mA}$
			0.3	V	$V_{CC} = 1\ \text{V}$ , $I_{SINK} = 50\ \mu\text{A}$
			0.3	V	$V_{CC} = 1.2\ \text{V}$ , $I_{SINK} = 100\ \mu\text{A}$
RESET OUTPUT VOLTAGE					
	$V_{CC} - 1.5$		0.4	V	ADM707/ADM708, $I_{SOURCE} = 800\ \mu\text{A}$
			0.4	V	ADM707/ADM708, $I_{SINK} = 1.2\ \text{mA}$
WATCHDOG TIMEOUT PERIOD ( $t_{WD}$ )					
WDI Pulse Width ( $t_{WP}$ )	1.00	1.60	2.25	sec	$V_{IL} = 0.4\ \text{V}$ , $V_{IH} = V_{CC} \times 0.8$ , $WDI = V_{CC}$
WATCHDOG INPUT					
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current					
	–150	50	150	$\mu\text{A}$	WDI = 0 V
		–50		$\mu\text{A}$	WDI = 0 V
WDO OUTPUT VOLTAGE					
	$V_{CC} - 1.5$		0.4	V	$I_{SOURCE} = 800\ \mu\text{A}$
			0.4	V	$I_{SINK} = 1.2\ \text{mA}$
MANUAL RESET INPUT					
$\overline{\text{MR}}$ Pull-Up Current	100	250	600	$\mu\text{A}$	$\overline{\text{MR}} = 0\ \text{V}$
$\overline{\text{MR}}$ Pulse Width	150			ns	
MR INPUT THRESHOLD					
Logic Low			0.8	V	
Logic High	2.0			V	
$\overline{\text{MR}}$ TO RESET OUTPUT DELAY					
			250	ns	
POWER FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	
PFI Input Current	–25	+0.01	+25	nA	
PFO OUTPUT VOLTAGE					
	$V_{CC} - 1.5$		0.4	V	$I_{SOURCE} = 800\ \mu\text{A}$
			0.4	V	$I_{SINK} = 3.2\ \text{mA}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Rating
$V_{CC}$	-0.3 V to +6 V
All Other Inputs	-0.3 V to $V_{CC} + 0.3$ V
Input Current	
$V_{CC}$	20 mA
GND	20 mA
Digital Output Current	20 mA
Power Dissipation, N-8 PDIP	727 mW
$\theta_{JA}$ Thermal Impedance	135°C/W
Power Dissipation, R-8 SOIC	470 mW
$\theta_{JA}$ Thermal Impedance	110°C/W
Power Dissipation, RM-8 MSOP	900 mW
$\theta_{JA}$ Thermal Impedance	206°C/W
Operating Temperature Range	
Industrial (Version A)	-40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Storage Temperature Range	-65°C to +150°C
ESD Rating	>4.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

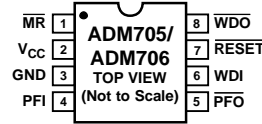


Figure 3. ADM705/ADM706 PDIP/SOIC Pin Configuration

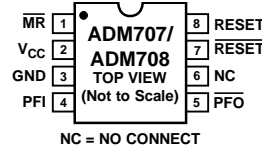


Figure 4. ADM707/ADM708 PDIP/SOIC Pin Configuration

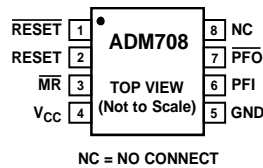


Figure 5. ADM708 MSOP Pin Configuration

Table 3. Pin Function Descriptions

Mnemonic	Pin Number			Description
	ADM705/ ADM706 (PDIP, SOIC)	ADM707/ ADM708 (PDIP, SOIC)	ADM708 (MSOP)	
MR	1	1	3	Manual Reset Input. When this pin is taken below 0.8 V, a reset is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch as it is internally debounced. An internal 250 $\mu$ A pull-up current holds the input high when floating.
V <sub>CC</sub>	2	2	4	5 V Power Supply Input. Place a 0.1 $\mu$ F decoupling capacitor between the V <sub>CC</sub> and GND pins.
GND	3	3	5	0 V Ground Reference for All Signals.
PFI	4	4	6	Power Fail Input. PFI is the noninverting input to the power fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI must be connected to GND.
$\overline{PFO}$	5	5	7	Power Fail Output. $\overline{PFO}$ is the output from the power fail comparator. It goes low when PFI is less than 1.25 V.
WDI	6	Not applicable	Not applicable	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output (WDO) goes low. The timer resets with each transition at the WDI input. Either a high to low or a low to high transition clears the counter. The internal timer is also cleared whenever reset is asserted. The watchdog timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	Not applicable	6	8	No Connect.
$\overline{RESET}$	7	7	1	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It can be triggered either by V <sub>CC</sub> being below the reset threshold or by a low signal on the manual reset input (MR). $\overline{RESET}$ remains low whenever V <sub>CC</sub> is below the reset threshold (4.65 V in ADM705/ADM707, 4.40 V in ADM706/ADM708). It remains low for 200 ms after V <sub>CC</sub> goes above the reset threshold or MR goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to MR.
$\overline{WDO}$	8	Not applicable	Not applicable	Watchdog Output. $\overline{WDO}$ remains low until the watchdog timer is cleared. $\overline{WDO}$ also goes low during low line conditions. Whenever V <sub>CC</sub> is below the reset threshold, $\overline{WDO}$ goes low if the internal $\overline{WDO}$ remains low. As soon as V <sub>CC</sub> goes above the reset threshold, $\overline{WDO}$ goes high.
RESET	Not applicable	8	2	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$ .

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 6.  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

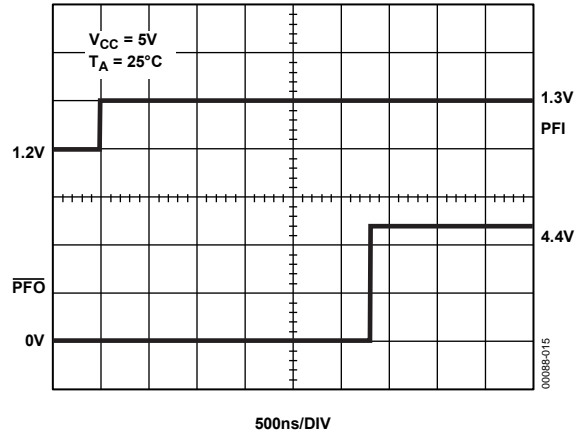


Figure 9. PFI Comparator Deassertion Response Time



Figure 7. ADM707/ADM708  $\overline{\text{RESET}}$  Output Voltage vs. Supply Voltage

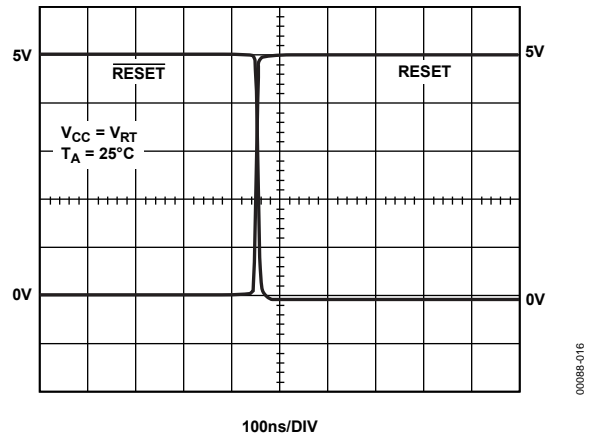


Figure 10.  $\overline{\text{RESET}}$ ,  $\overline{\text{RESET}}$  Assertion

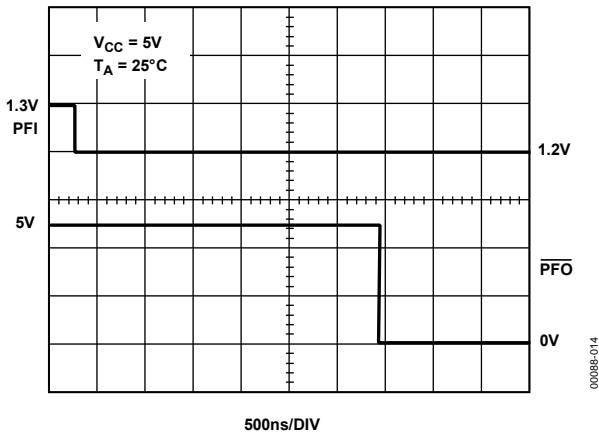


Figure 8. PFI Comparator Assertion Response Time

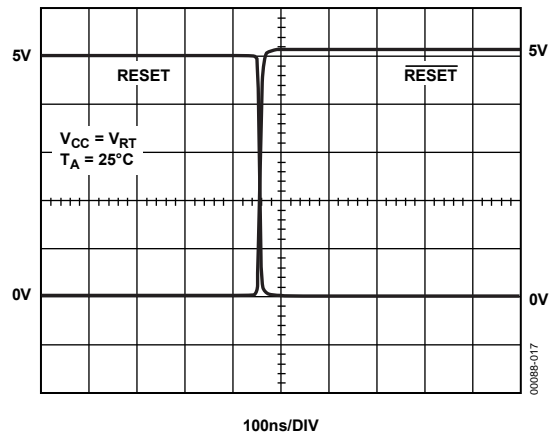


Figure 11.  $\overline{\text{RESET}}$ ,  $\overline{\text{RESET}}$  Deassertion



Figure 12. ADM705/ADM707  $\overline{RESET}$  Response Time

## CIRCUIT INFORMATION

### POWER FAIL RESET OUTPUT

$\overline{\text{RESET}}$  is an active low output that provides a reset signal to the microprocessor whenever the  $V_{CC}$  input is below the reset threshold. An internal timer holds  $\overline{\text{RESET}}$  low for 200 ms after the voltage on  $V_{CC}$  rises above the threshold. This functions as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. The  $\overline{\text{RESET}}$  output is guaranteed to remain valid (low) with  $V_{CC}$  as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply voltage ramps up.

In addition to  $\overline{\text{RESET}}$ , an active high RESET output is also available on the ADM707/ADM708. This is the complement of  $\overline{\text{RESET}}$  and is useful for processors requiring an active high reset signal.

### MANUAL RESET

The manual reset input ( $\overline{\text{MR}}$ ) allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typically). The  $\overline{\text{MR}}$  input is TTL-/CMOS-compatible, so it can also be driven by any logic reset output.



Figure 13.  $\overline{\text{RESET}}$ ,  $\overline{\text{MR}}$ , and  $\overline{\text{WDO}}$  Timing

### WATCHDOG TIMER (ADM705/ADM706)

The watchdog timer circuit can monitor the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor toggles the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.60 sec), then the watchdog output ( $\overline{\text{WDO}}$ ) goes low. The  $\overline{\text{WDO}}$  can be connected to a nonmaskable interrupt (NMI) on the processor; therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine then rectifies the problem.

If a  $\overline{\text{RESET}}$  signal is required when a timeout occurs, the  $\overline{\text{WDO}}$  must connect to the manual reset input ( $\overline{\text{MR}}$ ).

The watchdog timer is cleared by either a high to low or a low to high transition on WDI. It is also cleared by  $\overline{\text{RESET}}$  going low; therefore, the watchdog timeout period begins after  $\overline{\text{RESET}}$  goes high.

When  $V_{CC}$  falls below the reset threshold,  $\overline{\text{WDO}}$  is forced low, whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by  $\overline{\text{RESET}}$  going low.

The watchdog monitor can be deactivated by floating the WDI. The  $\overline{\text{WDO}}$  can then be used as a low line output because it goes low only when  $V_{CC}$  falls below the reset threshold.

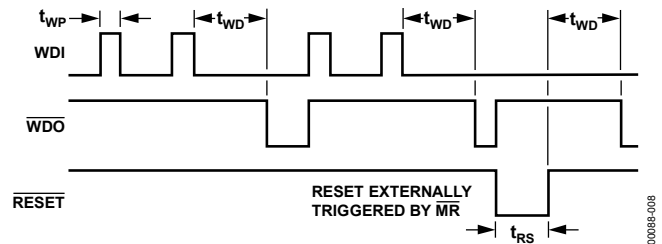


Figure 14. Watchdog Timing

### POWER FAIL COMPARATOR

The power fail comparator is an independent comparator that can monitor the input power supply. The comparator inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input can monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ( $\overline{\text{PFO}}$ ) goes low, indicating a power failure. For early warning of power failure, the comparator monitors the preregulator input by choosing an appropriate resistive divider network. The  $\overline{\text{PFO}}$  output can interrupt the processor so a shutdown procedure is implemented before power is lost.

As the voltage on the PFI pin is limited to  $V_{CC} + 0.3$  V, it is recommended to connect the PFI pin with a Schottky diode to the  $\overline{\text{RESET}}$  pin as shown in Figure 15. This helps clamping the PFI pin voltage during device power up and operation.



Figure 15. Power Fail Comparator



**Adding Hysteresis to the Power Fail Comparator**

For increased noise immunity, hysteresis can be added to the power fail comparator. Because the comparator circuit is noninverting, hysteresis can be added by connecting a resistor between the PFO output and the PFI input as shown in Figure 16.



Figure 16. Adding Hysteresis to the Power Fail Comparator

When  $\overline{PFO}$  is low, Resistor R3 sinks current from the summing junction at the PFI pin. When  $\overline{PFO}$  is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity can be achieved by connecting a capacitor between PFI and GND. The equations calculate the hysteresis are as follows:

$$V_H = 1.25 \left[ 1 + \left( \frac{R2 + R3}{R2 \times R3} \right) R1 \right]$$

$$V_L = 1.25 + R1 \left( \frac{1.25}{R2} - \frac{V_{CC} - 1.25}{R3} \right)$$

$$V_{MID} = 1.25 \left( \frac{R1 + R2}{R2} \right)$$

**VALID RESET BELOW 1 V  $V_{CC}$**

The ADM705/ADM706/ADM707/ADM708 are guaranteed to provide a valid reset level with  $V_{CC}$  as low as 1 V (see the Typical Performance Characteristics section). As  $V_{CC}$  drops below 1 V, the internal transistor does not have sufficient drive to hold the voltage RESET at 0 V. A pull-down resistor can connect externally, as shown in Figure 17, to hold the line low if required.



Figure 17. RESET Valid Below 1 V

### APPLICATIONS INFORMATION

A typical application circuit is shown in Figure 18. The unregulated dc input supply is monitored using PFI via the resistive divider network. Resistor R1 and Resistor R2 must be selected so when the supply voltage drops below the desired level (such as 8 V), the voltage on PFI drops below the 1.25 V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input provides additional time to execute an orderly shutdown procedure before power is lost.



Figure 18. Typical Application Circuit

Microprocessor activity is monitored using WDI. This is driven using an output line from the processor. The software routines toggle this line at least once every 1.60 seconds. If a problem occurs and this line is not toggled, WDO goes low and a nonmaskable interrupt is generated. This interrupt routine can clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, WDO must connect to MR as shown in Figure 19.

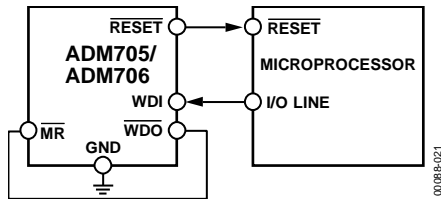


Figure 19. RESET From WDO

### MONITORING ADDITIONAL SUPPLY LEVELS

It is possible to use the power fail comparator to monitor a second supply as shown in Figure 20. The two sensing resistors, R1 and R2, are selected so the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. PFO can connect to MR so a reset is generated when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.



Figure 20. Monitoring 5 V and an Additional Supply, Vx

### MICROPROCESSOR WITH BIDIRECTIONAL RESET

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor must be inserted between the ADM705/ADM706/ADM707/ADM708 RESET output pin and the microprocessor RESET pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, it must be buffered, as shown in Figure 21.

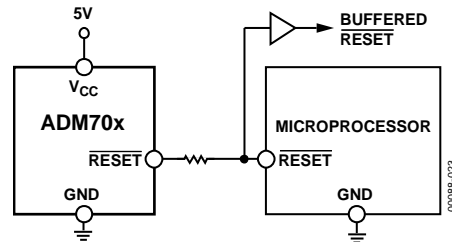


Figure 21. Bidirectional Input/Output RESET

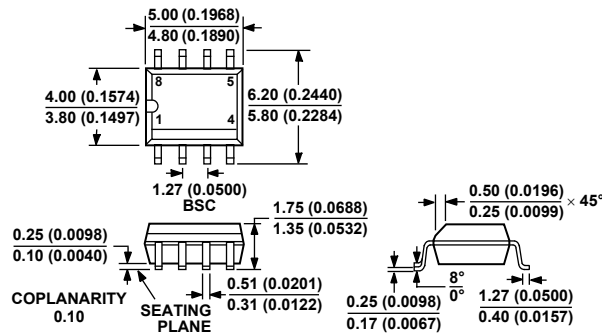
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 22. 8-Lead Plastic Dual-in-Line Package [PDIP] Narrow Body (N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 8-Lead Standard Small Outline Package [SOIC\_N] (R-8)

Dimensions shown in millimeters and (inches)





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