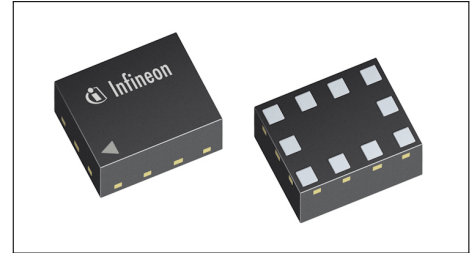


BGSA141MN10

Low Resistance Antenna Aperture Switch

Features

- Designed for high-linearity antenna aperture switching and RF tuning applications
- Multiple selectable switch configurations: SP4T/SP3T/SPDT/SPST
- Ultra low R_{ON} resistance of $1.0\ \Omega$ at each port in ON state
- Low C_{OFF} capacitance of 270 fF at each port in OFF state
- High max RF voltage OFF state handling
- Low harmonic generation
- MIPI RFFE control interface
- Hardware Pin swapping function to select 2 USID addresses
- Supply voltage range: 2.3 to 3.6 V
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm
- RoHS and WEEE compliant package



1.1 x 1.5 mm²

Application

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Block diagram

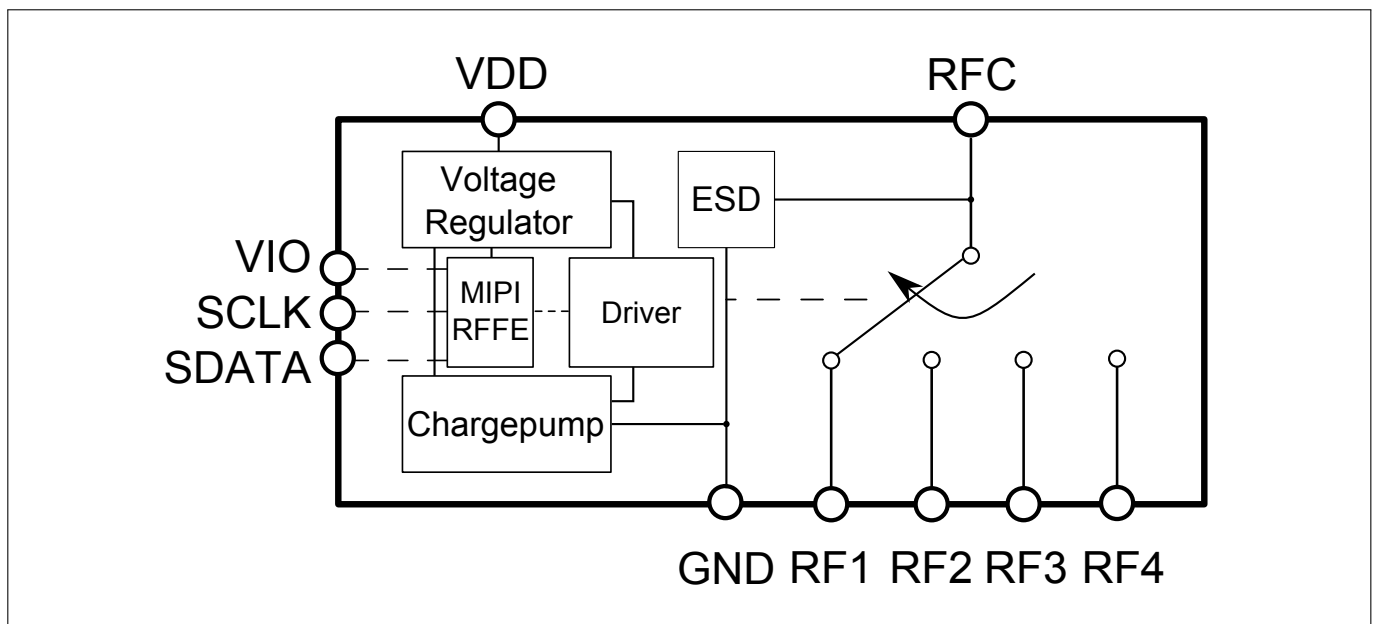


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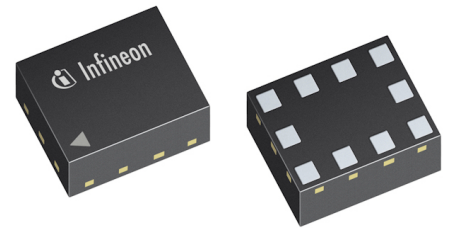
BGSA141MN10

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Description

The BGSA141MN10 is a versatile Single-Pole Quad Throw (SP4T) / Single Pole Triple Throw (SP3T) / Single Pole Double Throw (SPDT) and Single Pole Single Throw (SPST) RF antenna aperture switch optimized for low C_{off} as well as low R_{on} enabling applications up to 4.0 GHz. Including a RFFE digital control interface, this switch offers the possibility to adopt a SP4T, SP3T, SPDT along with SPST topology for a better flexibility in RF Front-End designs.

The BGSA141MN10 includes 4 ultra-low R_{on} ports making it ideal for antenna aperture switching and switchable capacitors of high values. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

BGSA141MN10 empower its users with a smart USID selection feature. Default USID is 0b1100 when data signal is routed to pin 5 and clock signal to pin 6. Default USID is 0b1101 when data signal is routed to pin 6 and clock signal to pin 5. This Infineon patented feature allows to drive 2 identical BGSA141MN10 parts with the same MIPI RFFE bus opening higher degree of flexibility and freedom in the PCB design.

| Product Name | Marking | Package |
|--------------|---------|-----------|
| BGSA141MN10 | M5 | TSNP-10-3 |

Maximum Ratings

2 Maximum Ratings

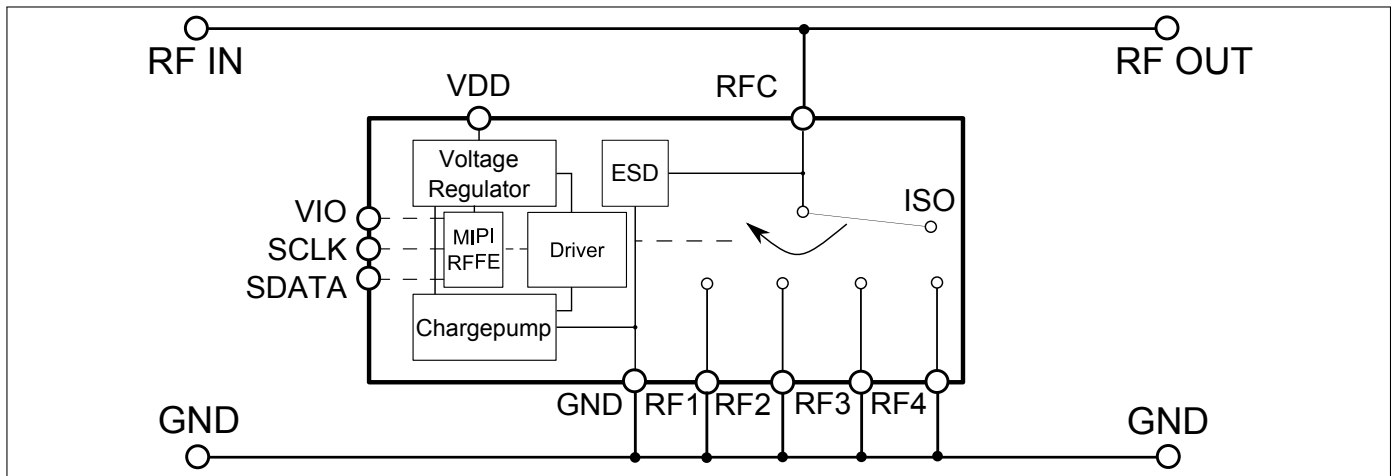


Figure 1: RF operating voltage measurement configuration

Table 1: Maximum Ratings, Table I at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---------------|--------|------|---------|------------------|--|
| | | Min. | Typ. | Max. | | |
| Frequency Range | f | 0.1 | – | – | GHz | ¹⁾ |
| Supply voltage ²⁾ | V_{DD} | -0.5 | – | 6 | V | only for infrequent and short duration time periods |
| Storage temperature range | T_{STG} | -55 | – | 150 | $^\circ\text{C}$ | – |
| RF input power | P_{RF_max} | – | – | 39 | dBm | Pulsed RF input duty cycle of 25 % and 4620 μs in ON-state, measured per 3GPP TS 45.005 |
| RF voltage | V_{RF_max} | – | – | 44 | V | Short term peaks (1 μs in 0.1% duty cycle), exceeding typical linearity, Ron and Coff parameters, in Isolation mode, test condition schematic in Fig. 1 |
| ESD capability, CDM ³⁾ | V_{ESDCDM} | -1 | – | +1 | kV | |
| ESD capability, HBM ⁴⁾ | V_{ESDHBM} | – | – | Class1B | - | |
| ESD capability, system level (RFC port) ⁵⁾ | V_{ESDANT} | -8 | – | +8 | kV | RFC vs system GND, with 27 nH shunt inductor |
| Junction temperature | T_j | – | – | 125 | $^\circ\text{C}$ | – |

¹⁾ Switch has a lowpass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.

²⁾ Note: Consider potential ripple voltages on top of V_{DD} . Including RF ripple, V_{DD} must not exceed the maximum ratings: $V_{DD} = V_{DC} + V_{Ripple}$.

³⁾ Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

⁴⁾ Human Body Model ANSI/ESDA/JEDEC JS-001 ($R = 1,5\text{ k}\Omega$, $C = 100\text{ pF}$).

⁵⁾ IEC 61000-4-2 ($R = 330\ \Omega$, $C = 150\text{ pF}$), contact discharge.

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Low Resistance Antenna Aperture Switch

Maximum Ratings

Table 2: Maximum Ratings, Table II at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------------|--------|------|-------------------------------|------|------------------------------------|
| | | Min. | Typ. | Max. | | |
| Maximum DC-voltage on RF-Ports and RF-Ground | V_{RFDC} | 0 | – | 0 | V | No DC voltages allowed on RF-Ports |
| RFFE Supply Voltage | V_{IO} | -0.5 | – | 3.6 | V | – |
| RFFE Control Voltage Levels | V_{SCLK} , V_{SDATA} | -0.7 | – | $V_{IO}+0.7$ (max. 3.6) | V | – |

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

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Low Resistance Antenna Aperture Switch

DC Characteristics

3 DC Characteristics

Table 3: DC Characteristics at $T_A = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|------------|--------------------|------|--------------------|---------------|---------------------------|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | V_{DD} | 2.3 | 2.8 | 3.6 | V | – |
| Supply Current | I_{DD} | – | 80 | 150 | μA | Normal Mode |
| | | – | 0.1 | 2 | μA | Low Power or Default Mode |
| RFFE supply voltage | V_{IO} | 1.65 | 1.8 | 1.95 | V | – |
| RFFE input high voltage ¹ | V_{IH} | $0.7 \cdot V_{IO}$ | – | V_{IO} | V | – |
| RFFE input low voltage ¹ | V_{IL} | 0 | – | $0.3 \cdot V_{IO}$ | V | – |
| RFFE output high voltage ¹ | V_{OH} | $0.8 \cdot V_{IO}$ | – | V_{IO} | V | – |
| RFFE output low voltage ¹ | V_{OL} | 0 | – | $0.2 \cdot V_{IO}$ | V | – |
| RFFE control input capacitance | C_{Ctrl} | – | – | 2 | pF | – |
| RFFE supply current | I_{VIO} | – | 15 | 25 | μA | Idle State |

¹SCLK and SDATA

BGSA141MN10

Low Resistance Antenna Aperture Switch

RF Small Signal Parameters

4 RF Small Signal Parameters

Table 4: Parametric specifications using SP4T configuration

| Parameter | Symbol | Values | | | Unit | STATE / Notes |
|--|------------------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Frequency range | f | 0.1 | | 4.0 | GHz | |
| RF1, RF2, RF3 or RF4 to RFc ON resistance | $R_{ON_{SP4T}}$ | – | 1.0 | | Ω | $V_{DD} = 2.3 - 3.6 V$, $T_A = -40^\circ C... + 85^\circ C$, $Z_0 = 50 \Omega$ |
| RF1, RF2, RF3 or RF4 to RFc OFF capacitance | $C_{OFF_{SP4T}}$ | – | 270 | | fF | |

Table 5: Parametric specifications using SP3T configuration

| Parameter | Symbol | Values | | | Unit | STATE / Notes |
|--|---------------------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Frequency range | f | 0.1 | | 4.0 | GHz | |
| RF1 RF2 or RF3 RF4 to RFc ¹⁾ ON resistance | $R_{ON_{SP3T(1)}}$ | – | 0.5 | | Ω | $V_{DD} = 2.3 - 3.6 V$, $T_A = -40^\circ C... + 85^\circ C$, $Z_0 = 50 \Omega$ |
| RF1 RF2 or RF3 RF4 to RFc ¹⁾ OFF capacitance | $C_{OFF_{SP3T(1)}}$ | – | 540 | | fF | |
| RF1, RF2, RF3 or RF4 to RFc ON resistance | $R_{ON_{SP3T(2)}}$ | – | 1.0 | | Ω | |
| RF1, RF2, RF3 or RF4 to RFc OFF capacitance | $C_{OFF_{SP3T(2)}}$ | – | 270 | | fF | |

¹⁾RF1 and RF2 or RF3 and RF4 connected together on PCB

Table 6: Parametric specifications using SPDT configuration

| Parameter | Symbol | Values | | | Unit | STATE / Notes |
|---|------------------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Frequency range | f | 0.1 | | 4.0 | GHz | |
| RF1 RF2 and RF3 RF4 to RFc ¹⁾ ON resistance | $R_{ON_{SPDT}}$ | – | 0.5 | | Ω | $V_{DD} = 2.3 - 3.6 V$, $T_A = -40^\circ C... + 85^\circ C$, $Z_0 = 50 \Omega$ |
| RF1 RF2 and RF3 RF4 to RFc ¹⁾ OFF capacitance | $C_{OFF_{SPDT}}$ | – | 540 | | fF | |

¹⁾RF1 and RF2, RF3 and RF4 connected together on PCB

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Low Resistance Antenna Aperture Switch

RF Small Signal Parameters

Table 7: Parametric specifications using SPST configuration

| Parameter | Symbol | Values | | | Unit | STATE / Notes |
|--|---------------|--------|------|------|----------|---|
| | | Min. | Typ. | Max. | | |
| Frequency range | f | 0.1 | | 4.0 | GHz | |
| RF1 RF2 RF3 RF4 to RFc ¹⁾ ON resistance | R_{ONSPST} | – | 0.25 | | Ω | $V_{DD} = 2.3 - 3.6 V$, $T_A = -40\text{ }^\circ\text{C} \dots +85\text{ }^\circ\text{C}$, $Z_0 = 50\ \Omega$ |
| RF1 RF2 RF3 RF4 to RFc ¹⁾ OFF capacitance | $C_{OFFSPST}$ | – | 1.08 | | pF | |

¹⁾RF1, RF2, RF3, RF4 connected together on PCB

Table 8: RF electrical parameters

Insertion Loss: RF1 to RFc, RF2 to RFc, RF3 to RFc or RF4 to RFc (SP4T mode) ^(1,2)

| Parameter | Symbol | Values | | | Unit | STATE / Notes |
|-----------------|-------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| 698 - 960 MHz | IL_{SP4T} | 0.1 | 0.25 | 0.4 | dB | $V_{DD} = 2.3 - 3.6 V$, $Z_0 = 50\ \Omega$, $T_A = -40\text{ }^\circ\text{C} \dots +85\text{ }^\circ\text{C}$ |
| 1710 - 1980 MHz | | 0.35 | 0.55 | 0.7 | dB | |
| 1981 - 2169 MHz | | 0.45 | 0.65 | 1.0 | dB | |
| 2170 - 2690 MHz | | 0.5 | 0.80 | 1.2 | dB | |

Return Loss: RF1, RF2, RF3 or RF4 ^(1,2,3)

| | | | | | | |
|-----------------|-------------|----|----|---|----|--|
| 698 - 960 MHz | RL_{SP4T} | 16 | 21 | – | dB | $V_{DD} = 2.3 - 3.6 V$, $Z_0 = 50\ \Omega$, $T_A = -40\text{ }^\circ\text{C} \dots +85\text{ }^\circ\text{C}$ |
| 1710 - 2690 MHz | | 12 | 14 | – | dB | |

Isolation: RF1 to RFc, RF2 to RFc, RF3 to RFc or RF4 to RFc (SP4T mode) ^(1,2,3)

| | | | | | | |
|-----------------|--------------|----|----|---|----|--|
| 698 - 960 MHz | ISO_{SP4T} | 21 | 25 | – | dB | $V_{DD} = 2.3 - 3.6 V$, $Z_0 = 50\ \Omega$, $T_A = -40\text{ }^\circ\text{C} \dots +85\text{ }^\circ\text{C}$ |
| 1710 - 1980 MHz | | 15 | 18 | – | dB | |
| 1981 - 2169 MHz | | 14 | 17 | – | dB | |
| 2170 - 2690 MHz | | 13 | 16 | – | dB | |

Isolation: RFc to RFx (Isolation mode) ^(1,2,3)

| | | | | | | |
|-----------------|------------|----|----|---|----|--|
| 698 - 960 MHz | ISO_{ON} | 17 | 20 | – | dB | $V_{DD} = 2.3 - 3.6 V$, $Z_0 = 50\ \Omega$, $T_A = -40\text{ }^\circ\text{C} \dots +85\text{ }^\circ\text{C}$ |
| 1710 - 1980 MHz | | 12 | 14 | – | dB | |
| 1981 - 2169 MHz | | 11 | 13 | – | dB | |
| 2170 - 2690 MHz | | 10 | 13 | – | dB | |

Switching Time

| | | | | | | |
|------------------------|-----------|-----|----|----|---------------|--|
| MIPI to RF Time | t_{INT} | 0.5 | 5 | 6 | μs | 50 % last SCLK falling edge to 90 % RF value settled, Fig. 2 |
| Power Up Settling Time | t_{PUS} | – | 10 | 25 | μs | After power down mode, Fig. 3 |

¹⁾ Valid for all RF power levels, no compression behavior

²⁾ On application board without any matching components

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Low Resistance Antenna Aperture Switch

RF Small Signal Parameters

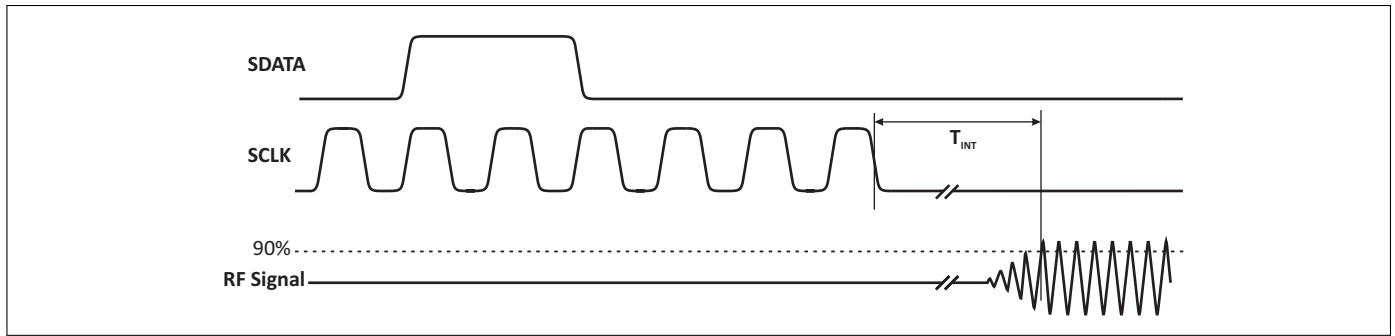


Figure 2: MIPI to RF Time

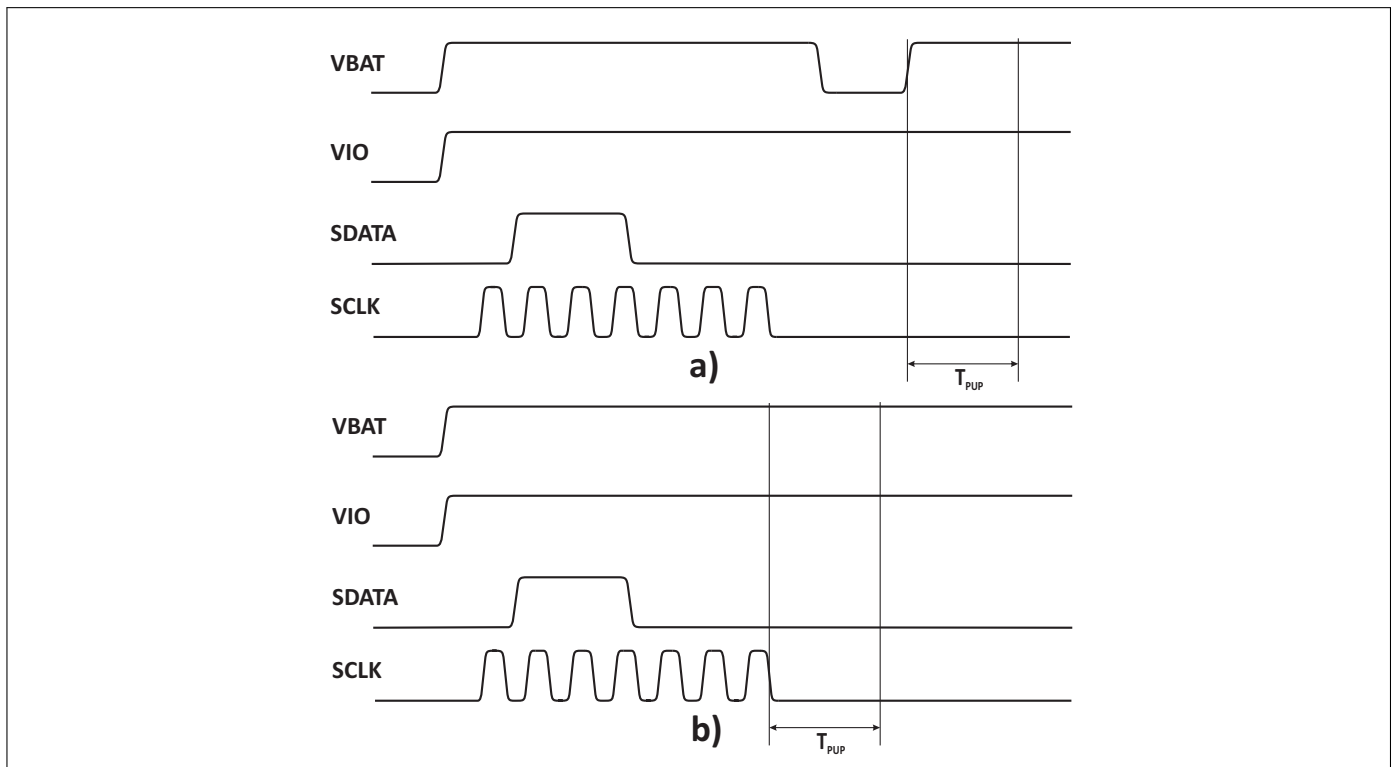


Figure 3: Power-Up Settling Time Definition

Power-Up Settling Time Definition: **a)** when the device is already in Active Mode. **b)** when changing from Low Power Mode to Active Mode.

After Power-Up of VIO the device is set to Low Power Mode. An additional MIPI instruction is necessary to set the switch to Active Mode. This case is covered by **b)**.

5 RF large signal parameters

Table 9: RF large signal specifications

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| RF operating voltage | V_{RF_peak} | – | – | 36 | V | In isolation Mode. Test conditions schematic in Fig. 1 |
| Harmonic Generation up to 12.75 GHz^(1,2,3) | | | | | | |
| All RF Ports Second Order Harmonics | P_{H2} | – | -105 | – | dBc | 25 dBm, $f_0 = 786$ MHz |
| All RF Ports Third Order Harmonics | P_{H3} | – | -115 | – | dBc | 25 dBm, $f_0 = 786$ MHz |
| All RF Ports Second Order Harmonics | P_{H2} | – | -93 | – | dBc | 33 dBm, $f_0 = 824$ MHz |
| All RF Ports Third Order Harmonics | P_{H3} | – | -94 | – | dBc | 33 dBm, $f_0 = 824$ MHz |
| All RF Ports Higher Order Harmonics | $P_{Hx,x>3}$ | – | – | -105 | dBc | 25 dBm |
| Intermodulation Distortion IMD2^(1,2,3) | | | | | | |
| IIP2, low | IIP2,l | – | 110 | – | dBm | IIP2 conditions, Tab. 10 |
| IIP2, high | IIP2,h | – | 120 | – | dBm | |
| Intermodulation Distortion IMD3^(1,2,3) | | | | | | |
| IIP3 | IIP3 | – | 75 | – | dBm | IIP3 conditions, Tab. 11 |
| SV LTE Intermodulation^(1,2,3) | | | | | | |
| IIP3,SVLTE | IIP3,SV | – | 75 | – | dBm | SV-LTE conditions, Tab. 12 |

¹⁾ Terminating Port Impedance: $Z_0 = 50 \Omega$

²⁾ Supply Voltage: $V_{DD} = 2.3 - 3.6$ V

³⁾ On application board without any matching components

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RF large signal parameters

Table 10: IIP2 conditions table

| Band | In-Band Frequency [MHz] | Blocker Frequency 1 [MHz] | Blocker Power 1 [dBm] | Blocker Frequency 2 [MHz] | Blocker Power 2 [dBm] |
|-------------|-------------------------|---------------------------|-----------------------|---------------------------|-----------------------|
| Band 1 Low | 2140 | 1950 | 20 | 190 | -15 |
| Band 1 High | 2140 | 1950 | 20 | 4090 | -15 |
| Band 5 Low | 881.5 | 836.5 | 20 | 45 | -15 |
| Band 5 High | 881.5 | 836.5 | 20 | 1718 | -15 |

Table 11: IIP3 conditions table

| Band | In-Band Frequency [MHz] | Blocker Frequency 1 [MHz] | Blocker Power 1 [dBm] | Blocker Frequency 2 [MHz] | Blocker Power 2 [dBm] |
|--------|-------------------------|---------------------------|-----------------------|---------------------------|-----------------------|
| Band 1 | 2140 | 1950 | 20 | 1760 | -15 |
| Band 5 | 881.5 | 836.5 | 20 | 791.5 | -15 |

Table 12: SV-LTE conditions table

| Band | In-Band Frequency [MHz] | Blocker Frequency 1 [MHz] | Blocker Power 1 [dBm] | Blocker Frequency 2 [MHz] | Blocker Power 2 [dBm] |
|---------|-------------------------|---------------------------|-----------------------|---------------------------|-----------------------|
| Band 5 | 872 | 827 | 23 | 872 | 14 |
| Band 13 | 747 | 786 | 23 | 747 | 14 |
| Band 20 | 878 | 833 | 23 | 2544 | 14 |

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MIPI RFFE Specification

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

Table 13: MIPI Features

| Feature | Supported | Comment |
|--|-----------|--|
| Register write command sequence | Yes | |
| Register read command sequence | Yes | |
| Extended register write command sequence | No | Up to 4 Bytes |
| Extended register read command sequence | No | Up to 4 Bytes |
| Register 0 write command sequence | Yes | |
| Trigger function | Yes | Trigger assignment to each control register is supported |
| Programmable USID | Yes | 3 register command sequence and extended register command sequence |
| Status Register | Yes | Register for debugging |
| Reset | Yes | By VIO, Power Mode and RFFE_STATUS |
| Group SID | Yes | |
| USID_Sel pin | Yes | External pin for changing USID: 1: Pin 5=SDATA and Pin 6=SCLK → 1100, 2: Pin 5=SCLK and Pin 6=SDATA → 1101 |
| Full speed write | Yes | |
| Half speed read | Yes | |
| Full speed read | Yes | |

Table 14: Startup Behavior

| Feature | State | Comment |
|------------------|-----------|---|
| Power status | LOW POWER | The chip is in low power mode after startup |
| Trigger function | ENABLED | Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register. |

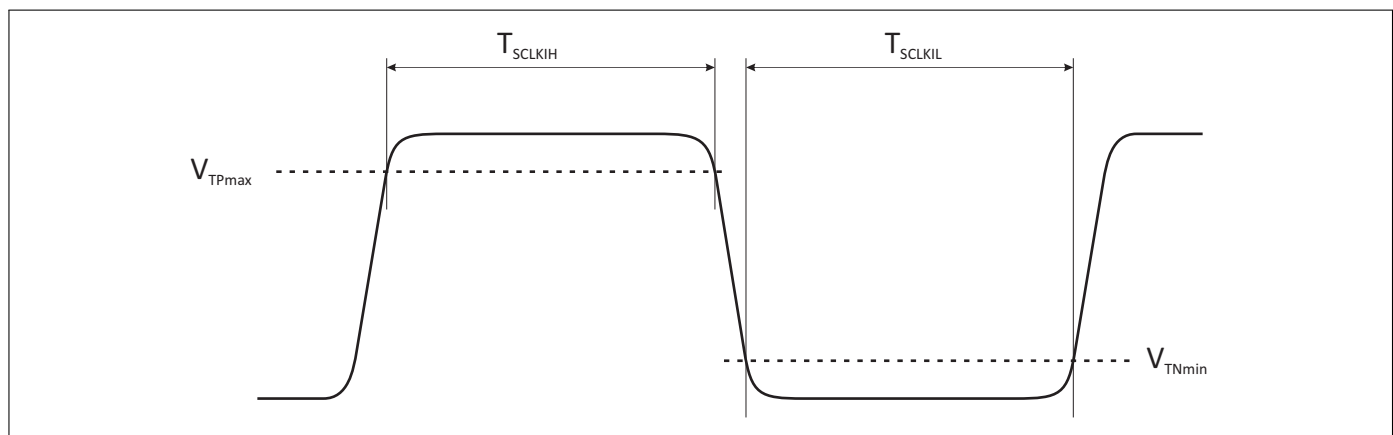


Figure 4: Received clock signal constraints

Table 15: MIPI RFFE Operating Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------|-----------|--------|------|-------|---------|------------------------|
| | | Min. | Typ. | Max. | | |
| SCLK Frequency | FSCLK | 0.032 | - | 26 | MHz | Full speed |
| | | 0.032 | - | 13 | MHz | Half speed |
| SCLK Period | TSCLK | 0.038 | - | 32 | μ s | Full speed |
| | | 0.077 | - | 32 | μ s | Half speed |
| SCLK Low Period | TSCLKIL | 11.25 | - | - | ns | Full speed, see Fig. 4 |
| | | 24 | - | - | ns | Half speed, see Fig. 4 |
| SCLK High Period | TSCLKIH | 11.25 | - | - | ns | Full speed, see Fig. 4 |
| | | 24 | - | - | ns | Half speed, see Fig. 4 |
| SDATA Setup Time | TS | 1 | - | - | ns | Full speed, see Fig. 5 |
| | | 2 | - | - | ns | Half speed, see Fig. 5 |
| SDATA Hold Time | TH | 5 | - | - | ns | Full speed, see Fig. 5 |
| | | 5 | - | - | ns | Half speed, see Fig. 5 |
| SDATA Release Time | TSDATAZ | - | - | 10 | ns | Full speed, see Fig. 6 |
| | | - | - | 18 | ns | Half speed, see Fig. 6 |
| Time for Data Output | TD | - | - | 10.25 | ns | Full speed, see Fig. 7 |
| | | - | - | 22 | ns | Half speed, see Fig. 7 |
| SDATA Rise/Fall Time | TSDATAOTR | 2.1 | - | 6.5 | ns | Full speed, see Fig. 7 |
| | | 2.1 | - | 10 | ns | Half speed, see Fig. 7 |
| VIO Rise Time | TVIO-R | 10 | - | 450 | μ s | See Fig. 8 |
| VIO Reset Time | TVIO-RST | 10 | - | - | μ s | See Fig. 8 |
| Reset Delay Time | TSIGOL | 0.12 | - | - | μ s | See Fig. 8 |

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MIPI RFFE Specification

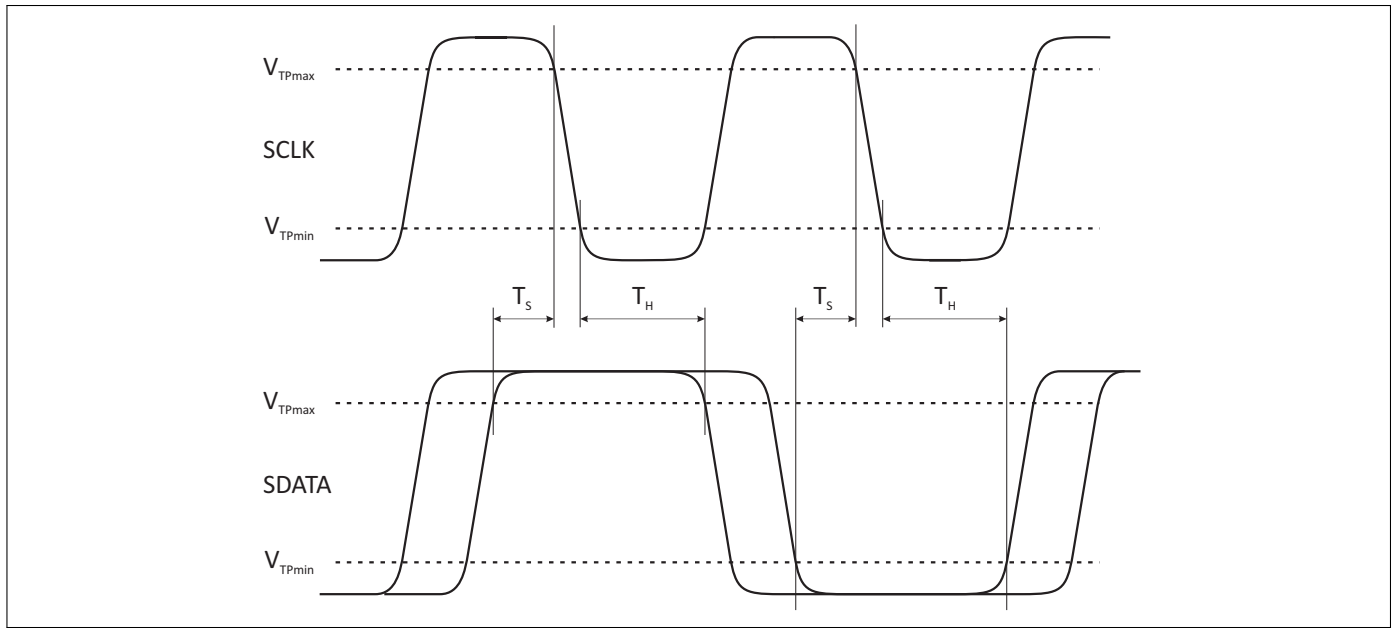


Figure 5: Bus active data receiver timing requirements

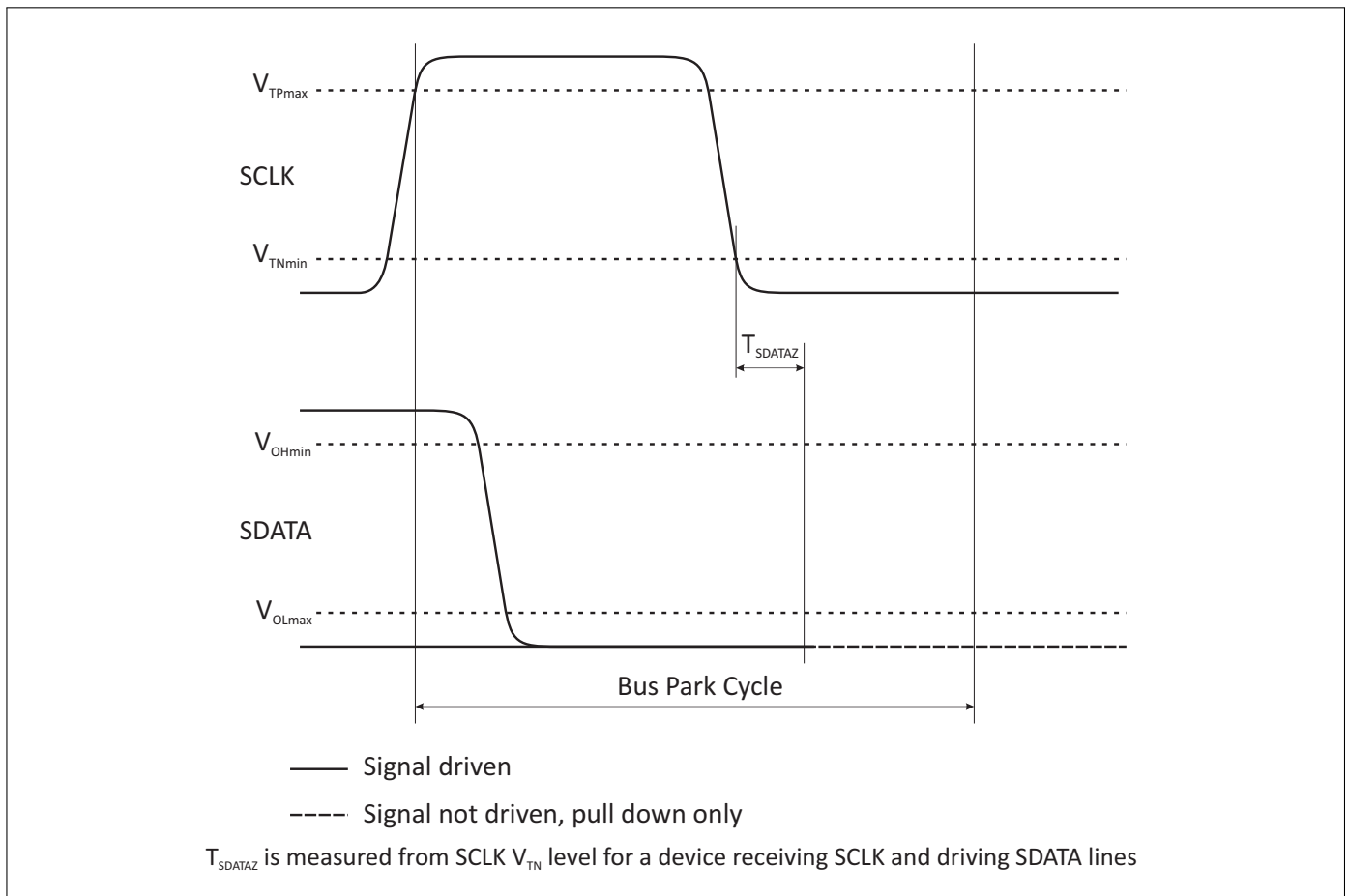


Figure 6: Bus park cycle timing

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MIPI RFFE Specification

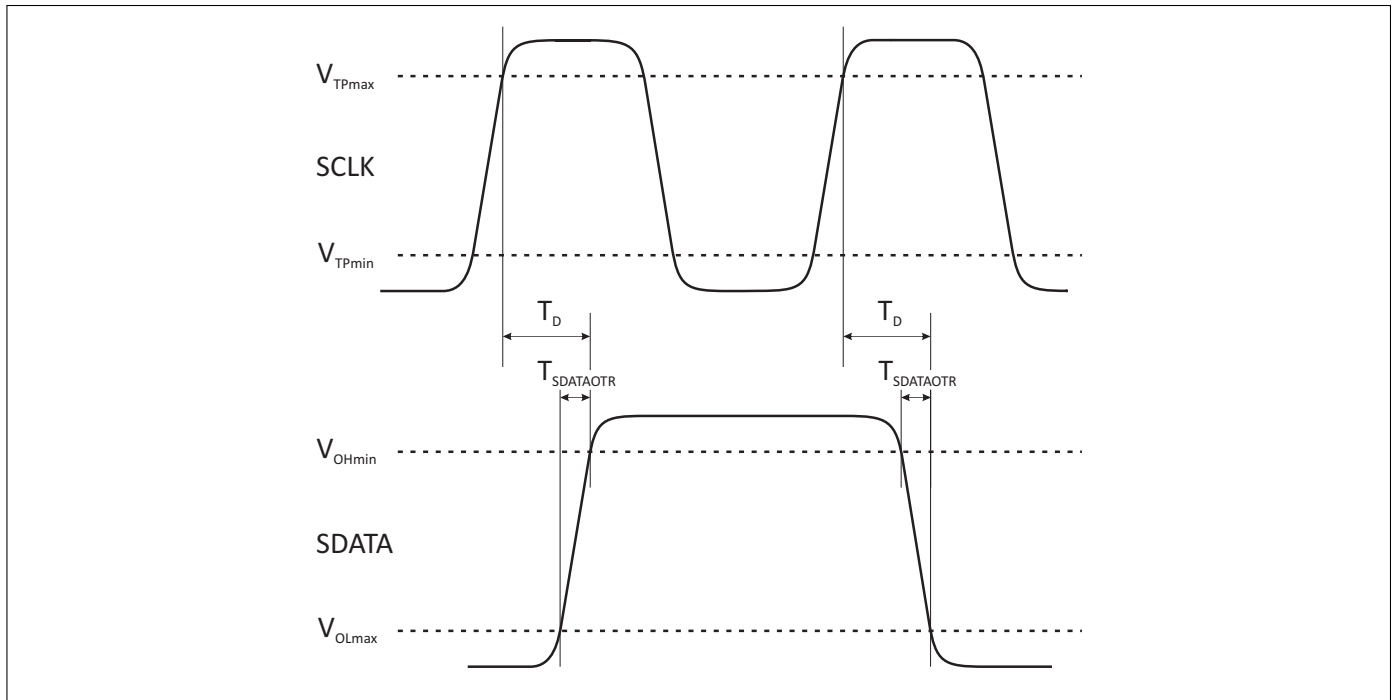


Figure 7: Bus active data transmission timing specification

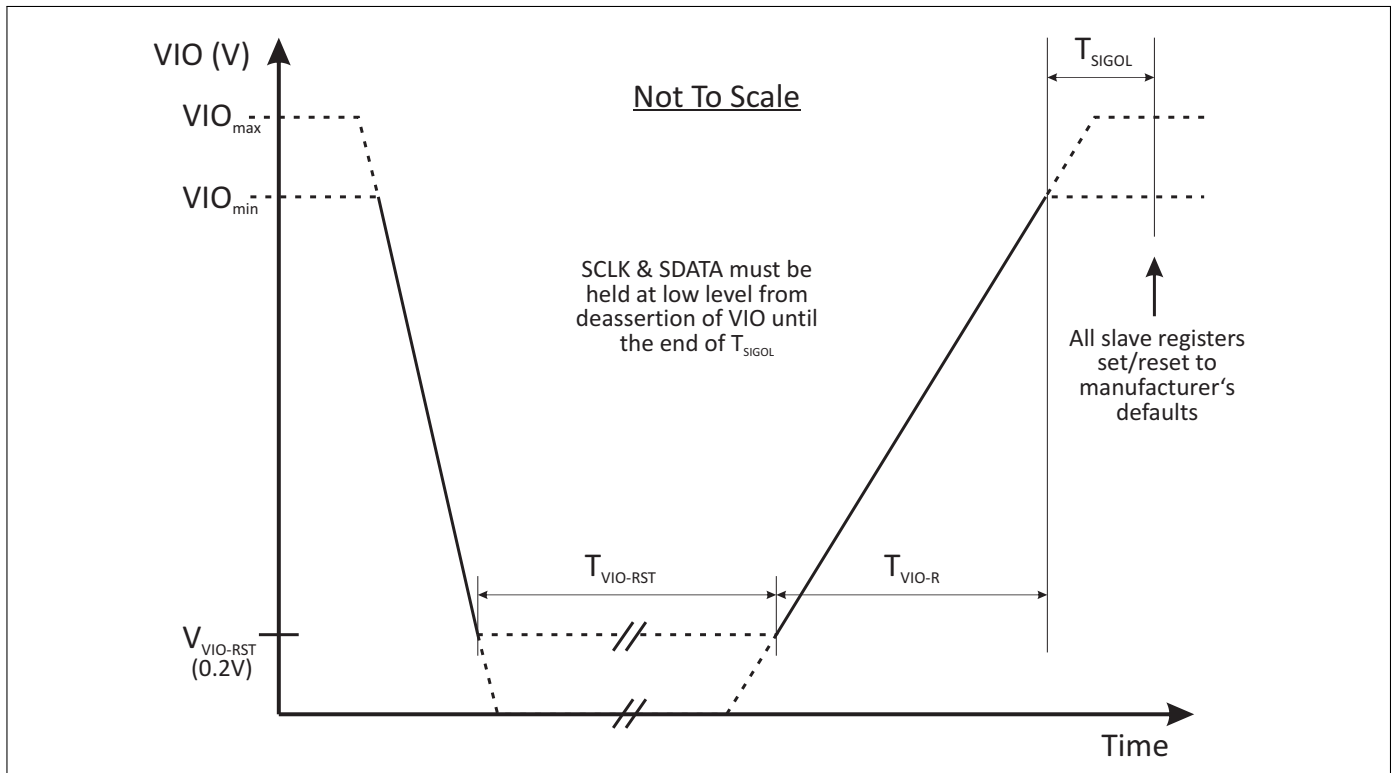


Figure 8: Requirements for VIO-initiated reset

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MIPI RFFE Specification

Table 16: Register Mapping

| Register Address | Register Name | Data Bits | Function | Description | Default | Broadcast_ID Support | Trigger Support | R/W |
|------------------|-----------------------|-----------|--------------------------|---|-------------|---|-----------------|-----|
| 0x0000 | REGISTER_0 | 7:0 | MODE_CTRL | RF Switch Control | 00000000 | No | Yes | R/W |
| 0x001D | PRODUCT_ID | 7:0 | PRODUCT_ID | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. | 00011100 | No | No | R |
| 0x001E | MANUFACTURER_ID | 7:0 | MANUFACTURER_ID [7:0] | This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. | 00011010 | No | No | R |
| 0x001C | PM_TRIG | 7:6 | PWR_MODE | 00: Normal operation 01: Default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved | 10 | Yes | No | R/W |
| | | 5 | TRIGGER_MASK_2 | If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register. | 0 | No | | |
| | | 4 | TRIGGER_MASK_1 | If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register. | 0 | No | | |
| | | 3 | TRIGGER_MASK_0 | If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register. | 0 | No | | |
| | | 2 | TRIGGER_2 | A write of a one to this bit loads trigger 2's registers. | 0 | Yes | | |
| | | 1 | TRIGGER_1 | A write of a one to this bit loads trigger 1's registers. | 0 | Yes | | |
| | | 0 | TRIGGER_0 | A write of a one to this bit loads trigger 0's registers. | 0 | Yes | | |
| | | 0x001F | MAN_USID | 7:6 | SPARE | These are read-only bits that are reserved and yield a value of 0b00 at readback. | 00 | |
| 5:4 | MANUFACTURER_ID [9:8] | | | These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. | 01 | | | |
| 3:0 | USID | | | Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. | See Tab. 13 | | | |
| 0x001A | RFFE_STATUS | 7 | SOFTWARE RESET | 0: Normal operation 1: Software reset | 0 | No | No | R/W |
| | | 6 | COMMAND_FRAME_PARITY_ERR | Command sequence received with parity error - discard command. | 0 | No | No | R |
| | | 5 | COMMAND_LENGTH_ERR | Command length error | 0 | | | |
| | | 4 | ADDRESS_FRAME_PARITY_ERR | Address frame parity error = 1 | 0 | | | |
| | | 3 | DATA_FRAME_PARITY_ERR | Data frame with parity error | 0 | | | |
| | | 2 | READ_UNUSED_REG | Read command to an invalid address | 0 | | | |
| | | 1 | WRITE_UNUSED_REG | Write command to an invalid address | 0 | | | |
| | | 0 | BID_GID_ERR | Read command with a BROADCAST_ID or GROUP_SID | 0 | | | |
| 0x001B | GROUP_SID | 7:4 | RESERVED | | 0000 | No | No | R/W |
| | | 3:0 | GROUP_SID | Group slave ID | 0000 | | | |

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MIPI RFFE Specification

Table 17: Switch MIPI Control Combinations (truth table)

| State | Mode | REGISTER_0 – Switch control register | | | | | | | |
|-------|-----------------------|--------------------------------------|----|----|----|----|----|----|----|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | Isolation mode (open) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | RF1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | RF2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | RF3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | RF4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 5 | RF1 RF2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 6 | RF1 RF3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 7 | RF1 RF4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 8 | RF2 RF3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 9 | RF2 RF4 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 10 | RF3 RF4 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 11 | RF1 RF2 RF3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 12 | RF1 RF2 RF4 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 13 | RF1 RF3 RF4 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 14 | RF2 RF3 RF4 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 15 | RF1 RF2 RF3 RF4 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 16 | RFC short to GND | x | 1 | x | x | x | x | x | x |

Application Information

7 Application Information

Pin Configuration and Function

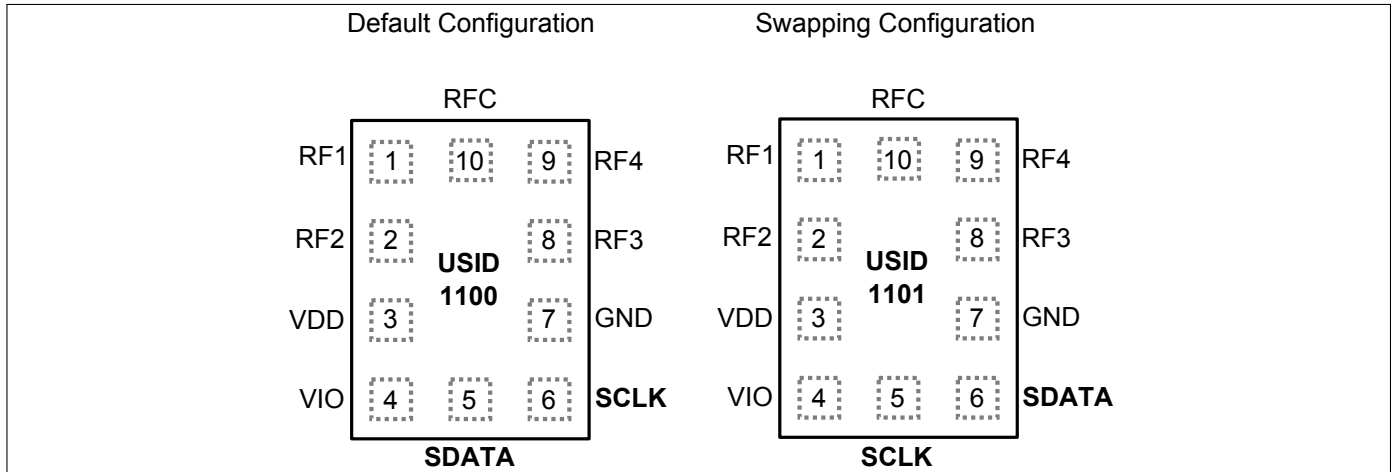


Figure 9: BGSA141MN10 Pin Configuration - USID 1100 and USID 1101 (top view)

Table 18: Pin Definition and Function USID 1100

| Pin No. | Name | Function |
|---------|-------|-------------------|
| 1 | RF1 | RF1 port |
| 2 | RF2 | RF2 port |
| 3 | VDD | Power Supply |
| 4 | VIO | RFFE Power Supply |
| 5 | SDATA | MIPI RFFE DATA |
| 6 | SCLK | MIPI RFFE CLOCK |
| 7 | GND | Ground |
| 8 | RF3 | RF3 port |
| 9 | RF4 | RF port |
| 10 | RFC | Common RF port |

Table 19: Pin Definition and Function - USID 1101

| Pin No. | Name | Function |
|---------|-------|-------------------|
| 1 | RF1 | RF1 port |
| 2 | RF2 | RF2 port |
| 3 | VDD | Power Supply |
| 4 | VIO | RFFE Power Supply |
| 5 | SCLK | MIPI RFFE CLOCK |
| 6 | SDATA | MIPI RFFE DATA |
| 7 | GND | Ground |
| 8 | RF3 | RF3 port |
| 9 | RF4 | RF port |
| 10 | RFC | Common RF port |

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Package Information

8 Package Information

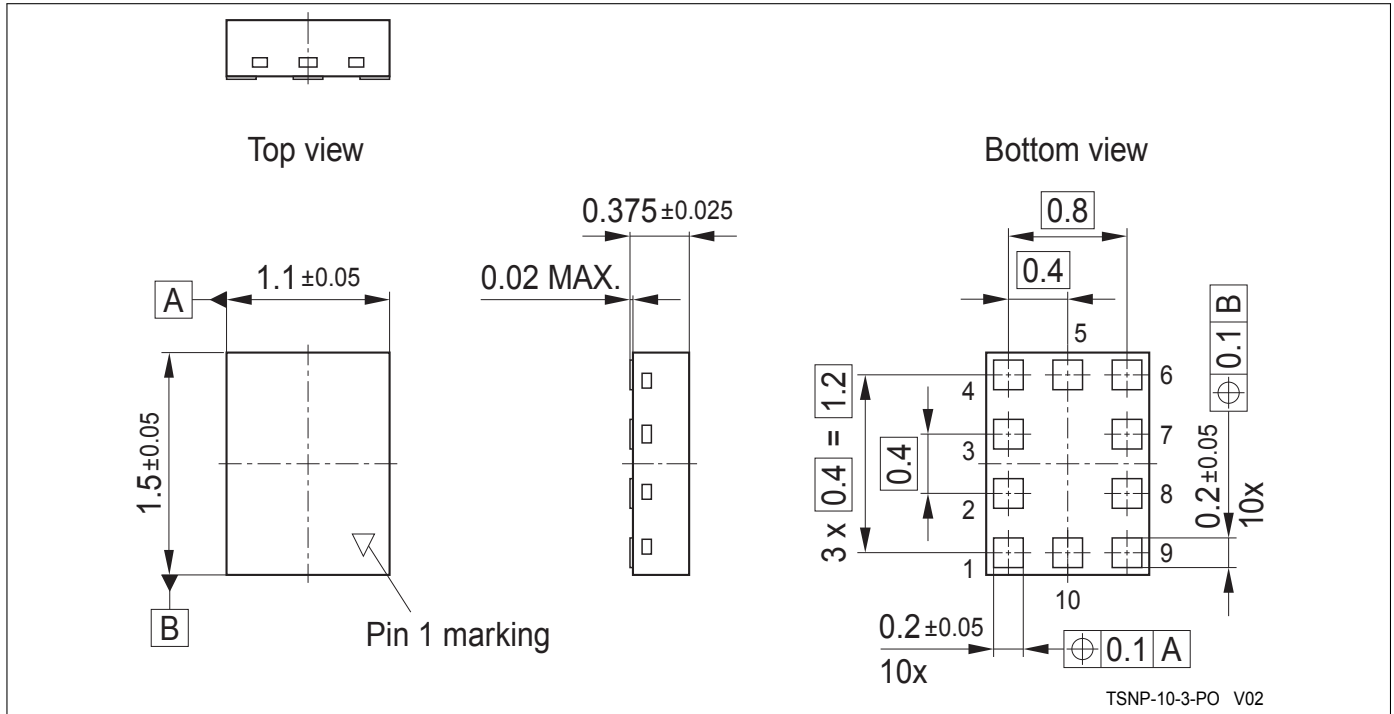


Figure 10: TSNP-10-3 Package Outline (top, side and bottom views)

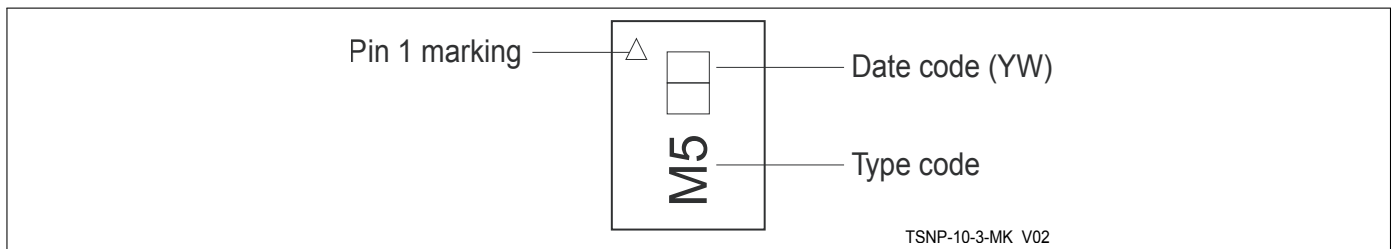


Figure 11: Marking Specification (top view): Date code digits Y and W defined in Table 20/21

Table 20: Year date code marking - digit "Y"

| Year | "Y" | Year | "Y" | Year | "Y" |
|------|-----|------|-----|------|-----|
| 2000 | 0 | 2010 | 0 | 2020 | 0 |
| 2001 | 1 | 2011 | 1 | 2021 | 1 |
| 2002 | 2 | 2012 | 2 | 2022 | 2 |
| 2003 | 3 | 2013 | 3 | 2023 | 3 |
| 2004 | 4 | 2014 | 4 | 2024 | 4 |
| 2005 | 5 | 2015 | 5 | 2025 | 5 |
| 2006 | 6 | 2016 | 6 | 2026 | 6 |
| 2007 | 7 | 2017 | 7 | 2027 | 7 |
| 2008 | 8 | 2018 | 8 | 2028 | 8 |
| 2009 | 9 | 2019 | 9 | 2029 | 9 |

Table 21: Week date code marking - digit "W"

| Week | "W" | Week | "W" | Week | "W" | Week | "W" | Week | "W" |
|------|-----|------|-----|------|-----|------|-----|------|-----|
| 1 | A | 12 | N | 23 | 4 | 34 | h | 45 | v |
| 2 | B | 13 | P | 24 | 5 | 35 | j | 46 | x |
| 3 | C | 14 | Q | 25 | 6 | 36 | k | 47 | y |
| 4 | D | 15 | R | 26 | 7 | 37 | l | 48 | z |
| 5 | E | 16 | S | 27 | a | 38 | n | 49 | 8 |
| 6 | F | 17 | T | 28 | b | 39 | p | 50 | 9 |
| 7 | G | 18 | U | 29 | c | 40 | q | 51 | 2 |
| 8 | H | 19 | V | 30 | d | 41 | r | 52 | 3 |
| 9 | J | 20 | W | 31 | e | 42 | s | | |
| 10 | K | 21 | Y | 32 | f | 43 | t | | |
| 11 | L | 22 | Z | 33 | g | 44 | u | | |

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Package Information

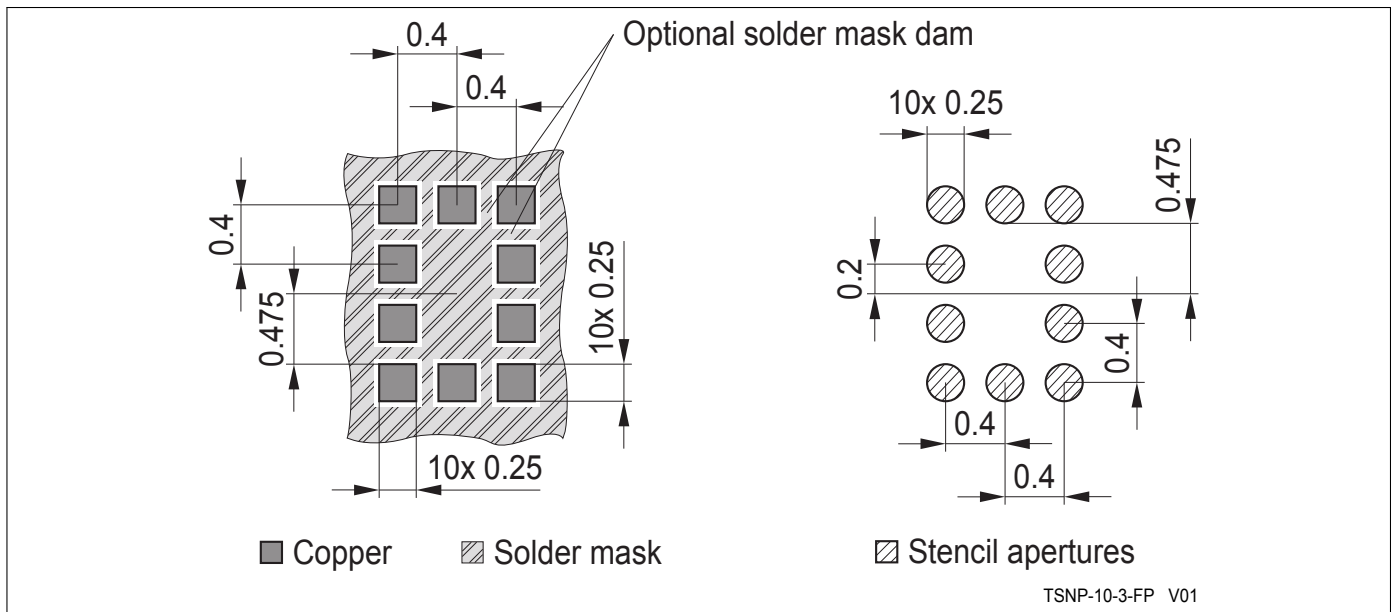


Figure 12: Footprint Recommendation

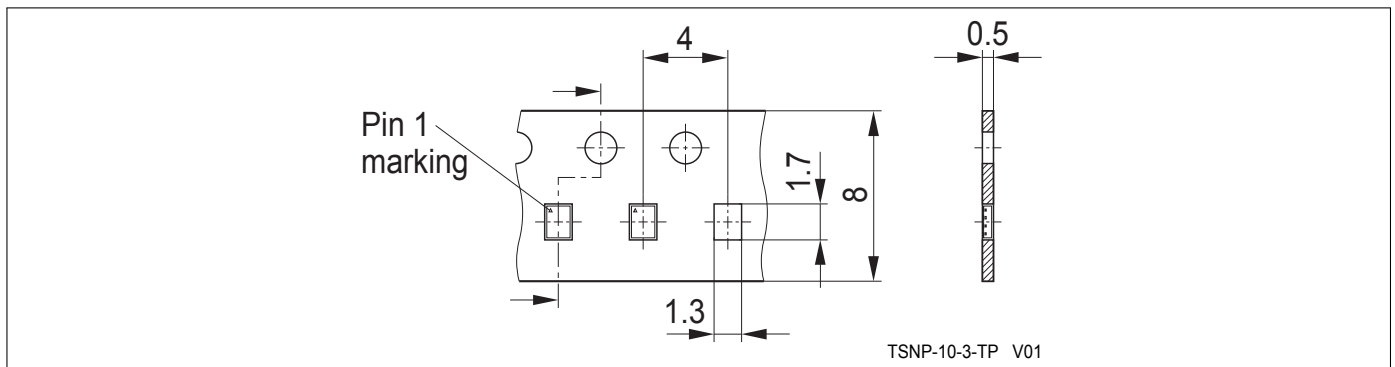


Figure 13: TSNP-10-3 Carrier Tape

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Revision History

| Page or Item | Subjects (major changes since previous revision) |
|---------------------------------|--|
| Revision 2.0, 2017-06-12 | |
| | Release as final version |
| | |

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