ZL30244, ZL30245

Dual-Channel Any-to-Any Clock Multiplier and Frequency Synthesizer ICs

Product Brief

September 2015

Features

- **Two Independent APLL Channels**
- **Four Input Clocks Per Channel**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency from 9.72MHz to 1250MHz (9.72MHz to 300MHz for CMOS)
  - Clock selection by pin or register control
- **Low-Jitter Fractional-N APLL and 3 Outputs Per Channel**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Easy-to-configure, encapsulated design requires no external VCXO or loop filter components
  - Each output has independent dividers
  - Output jitter as low as 0.16ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from external (ZL30244) or internal (ZL30245) EEPROM; up to four configs, pin-selectable
  - SPI or I^2C processor Interface
  - Numerically controlled oscillator mode
  - Spread-spectrum modulation mode
  - Space-saving 5x10mm LGA package
  - Easy-to-use evaluation software

Ordering Information

ZL30244 LFG7	64 Pin LGA	Trays
ZL30244 LFF7	64 Pin LGA	Tape and Reel
ZL30245 LFG7	64 Pin LGA	Trays
ZL30245 LFF7	64 Pin LGA	Tape and Reel

Ni Au

Package size: 5 x 10 mm

-40°C to +85°C

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

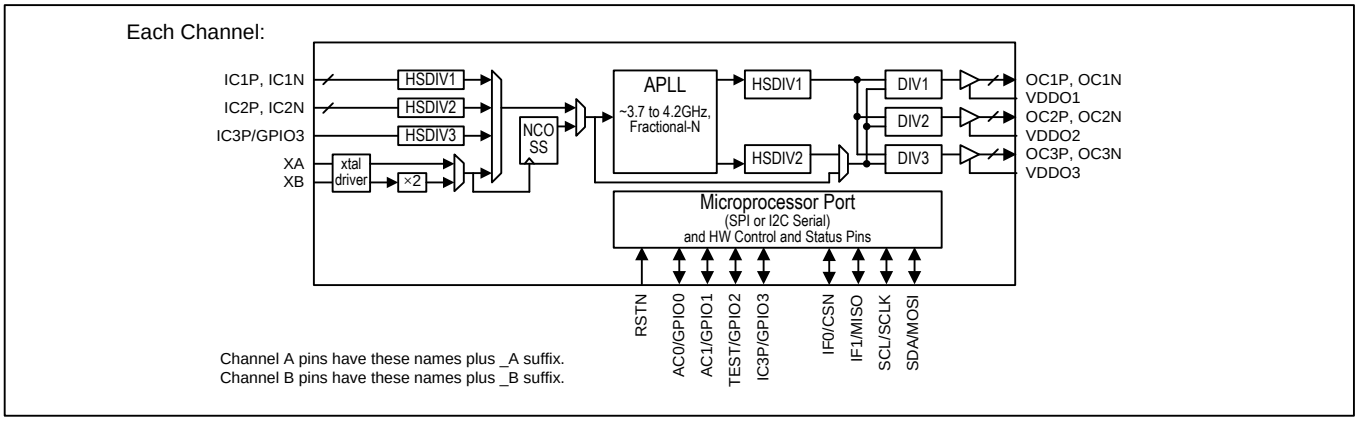

Figure 1 - Functional Block Diagram

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1. Application Examples

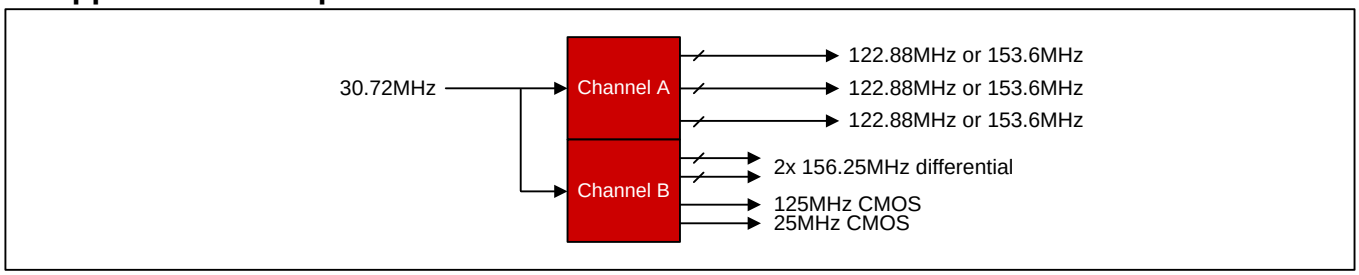


Figure 2 – Base Station Clock Multiplication and Ethernet Frequency Synthesis

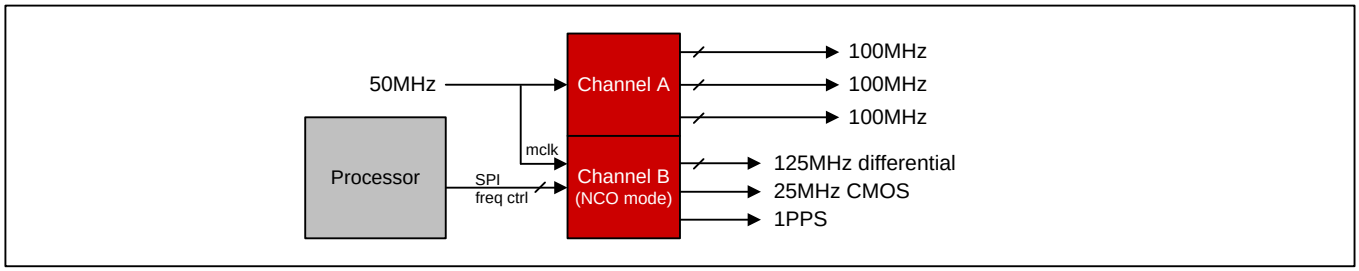


Figure 3 - PCI Express Clock Synthesis and NCO for IEEE1588 Slave Clock

2. Detailed Features

2.1 Input Clock Features

- Four input clocks per channel: one crystal/CMOS, two differential/CMOS, one single-ended/CMOS
- Input clocks can be any frequency from 9.72MHz up to 1250MHz (differential) or 300MHz (CMOS)

2.2 APLL Features

- APLL with very high-resolution fractional (i.e. non-integer) multiplication per channel
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers per channel (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.3 Output Clock Features

- Three low-jitter output clocks per channel
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter as low as 0.16ps RMS (12kHz to 20MHz integration band)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (example: OC3P 125MHz, OC3N 25MHz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks (PCIe gen. 1, 2 and 3)
- Sophisticated output-to-output phase alignment (among outputs in the same channel)
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.4 General Features

- SPI or I^2C serial microprocessor interface per channel

- Automatic self-configuration at power-up from external (ZL30244) or internal (ZL30245) EEPROM memory; pin control to specify one of four stored configurations
- Each channel can be configured for numerically controlled oscillator (NCO) mode, which allows system software to steer frequency with resolution better than 0.01ppb
- Each channel can be configured for pread-spectrum modulation mode (meets PCI Express requirements)
- Four general-purpose I/O pins per channel, each with many possible status and control options
- Each channel's reference clock can be fundamental-mode crystal, low-cost XO or clock signal from elsewhere in the system

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30244 or ZL30245 quick and easy
- Generates configuration scripts to be stored in external (ZL30244) or internal (ZL30245) EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30244 or ZL30245 evaluation board

3. Pin Diagram

The device is packaged in a 5x10mm 64-pin LGA package.

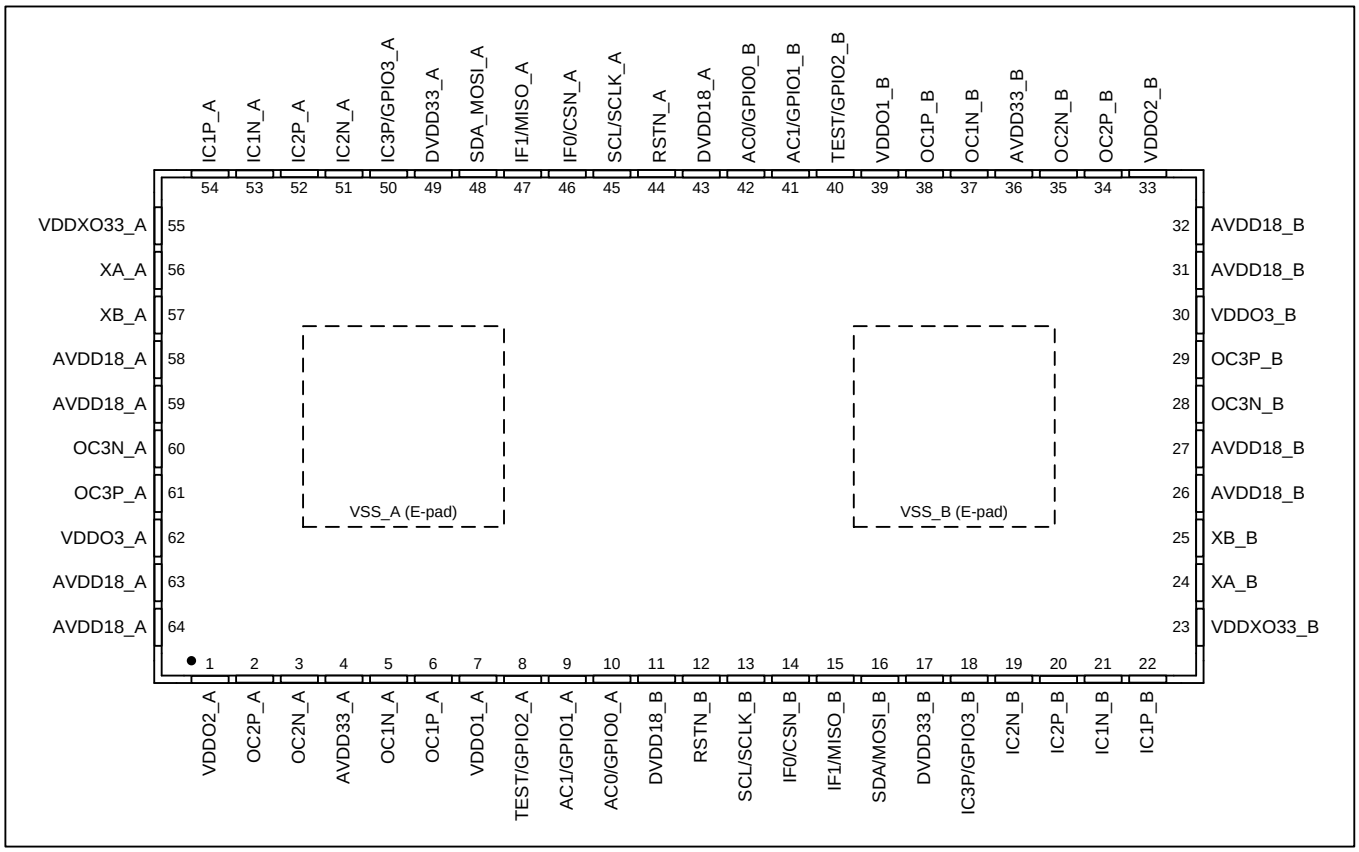
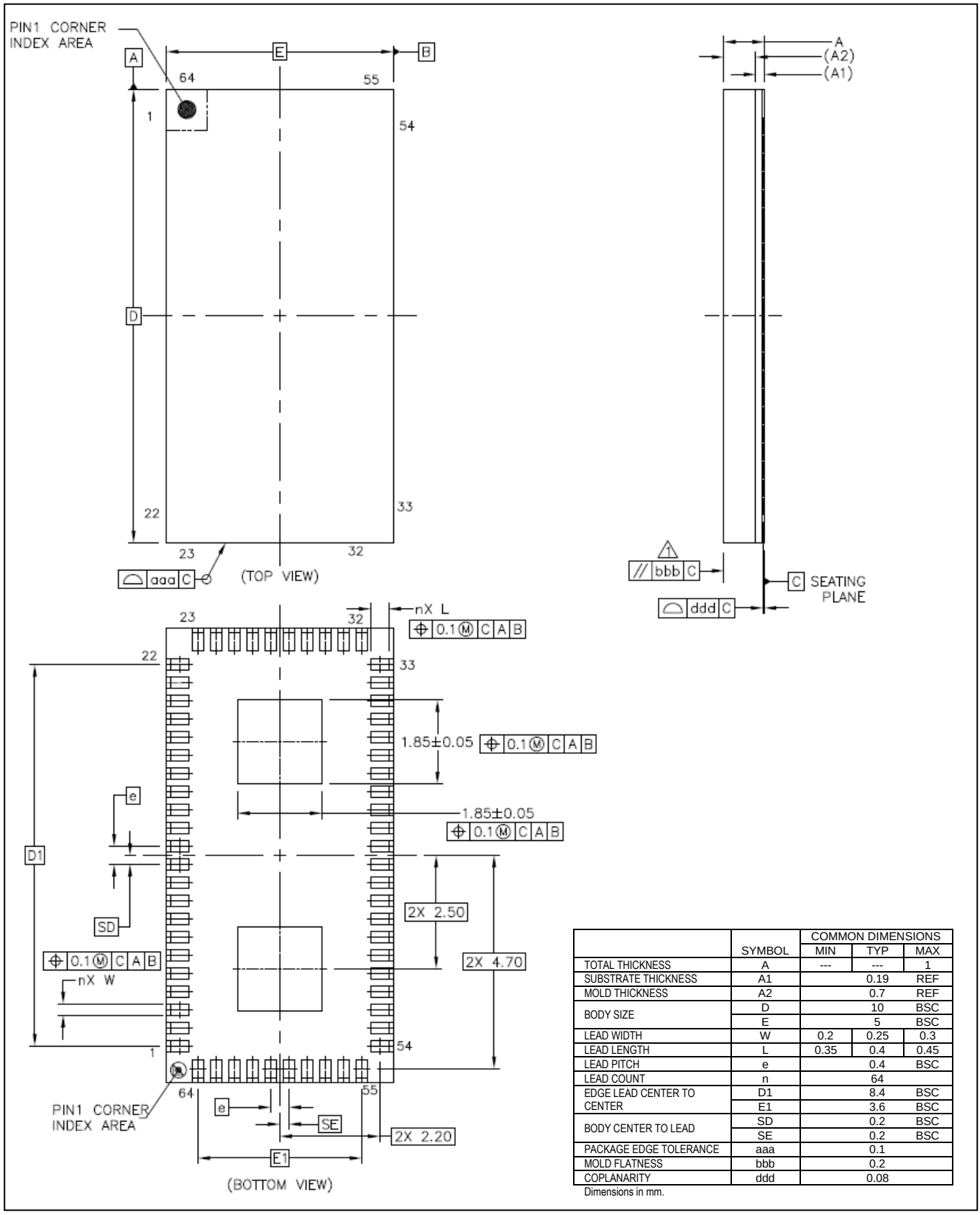


Figure 4 - Pin Diagram

4. Mechanical Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN	TYP	MAX
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.19	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		10	BSC
	E		5	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		64	
EDGE LEAD CENTER TO CENTER	D1		8.4	BSC
	E1		3.6	BSC
BODY CENTER TO LEAD	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	

Dimensions in mm.

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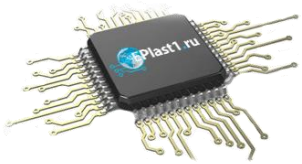
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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