PRELIMINARY

CY7C10612G
CY7C10612GE

16-Mbit (1 M × 16) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active power
  - I_{CC} = 90 mA typical
- Low CMOS standby power
  - I_{SB2} = 20 mA typical
- Operating voltages of 3.3 ± 0.3 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 54-pin TSOP II package

Functional Description

The CY7C10612G and CY7C10612GE are high performance CMOS fast static RAM devices with embedded ECC. both device are offered in single chip enable option. The CY7C10612GE device includes an error indication pin that signals an error-detection and correction event during a read cycle.

To write to the device, take Chip Enables ($\overline{CE}$) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 14 for a complete description of Read and Write modes.

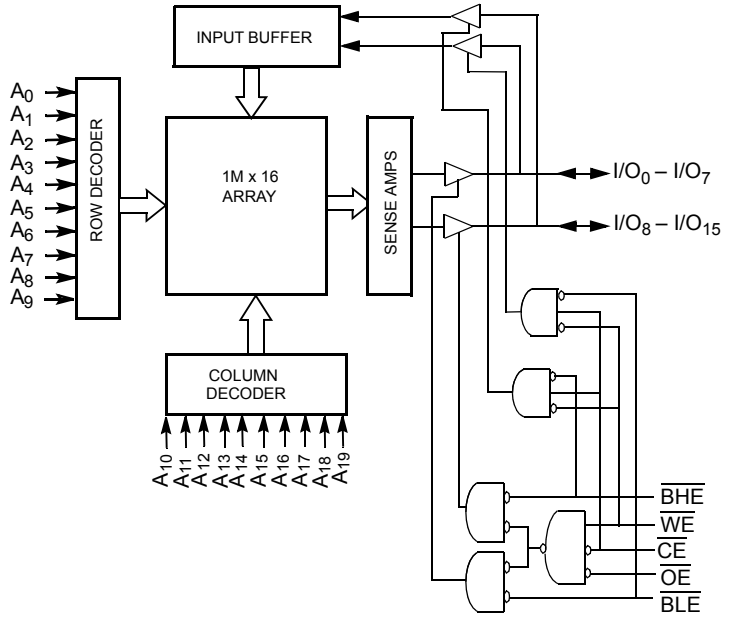
The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

On the CY7C10612GE devices the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = high). See the Truth Table on page 14 for a complete description of read and write modes.

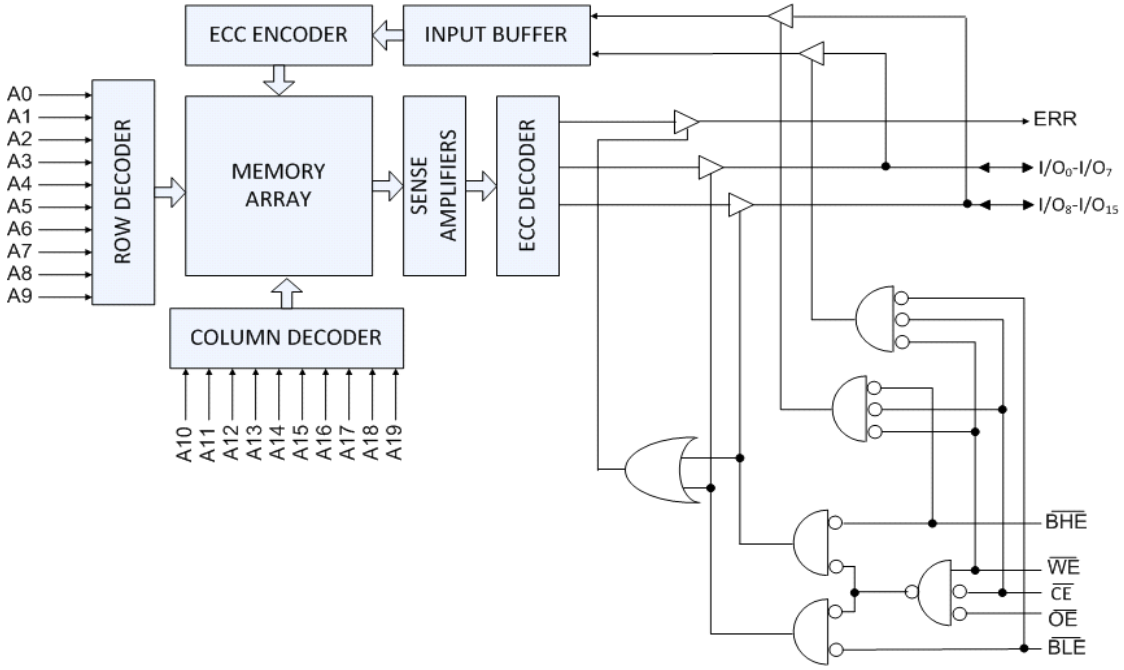
The CY7C10612G and CY7C10612GE are available in a 54-pin TSOP II package.

For a complete list of related documentation, click here.

Logic Block Diagram – CY7C10612G



Logic Block Diagram – CY7C10612GE



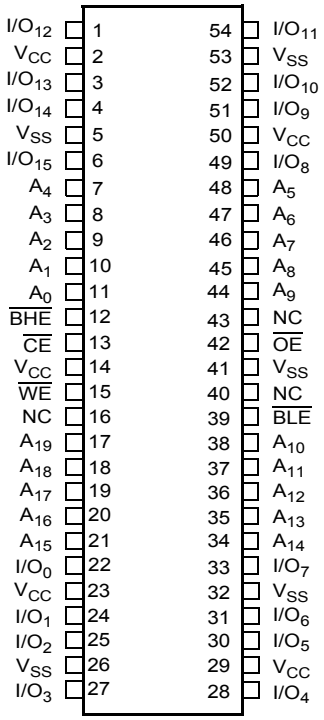
Contents

Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	110	mA
Maximum CMOS Standby Current	30	mA

Pin Configurations

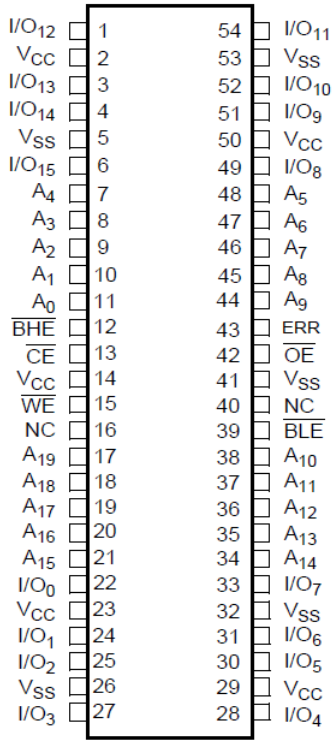
Figure 1. 54-pin TSOP II Pinout (Top View) [1]
CY7C10612G



Note
1. NC pins are not connected on the die.

Pin Configurations (continued)

Figure 2. 54-pin TSOP II Pinout with ERR (Top View) [2, 3]
CY7C10612GE



Note
2. NC pins are not connected on the die.
3. ERR is an Output pin. If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND [4] ..... –0.5 V to V_{CC} + 0.5 V

DC Voltage Applied to Outputs in High Z State [4] ..... –0.5 V to V_{CC} + 0.5 V

DC Input Voltage [4] ..... –0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		10 ns			Unit
				Min	Typ[5]	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.2	–	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8 mA		–	–	0.4	
V_{IH}[4]	Input HIGH Voltage	–		2.0	–	V_{CC} + 0.3	
V_{IL}[4]	Input LOW Voltage	–		–0.3	–	0.8	
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	
I_{CC}	Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 100 MHz	–	90.0	110.0	mA
			f = 66.7 MHz	–	70.0	80.0	
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} [5], V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	–	40.0	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2 V [5], V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0		–	20.0	30.0	

Notes

4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 2 ns.
5. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for a V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for a V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Capacitance

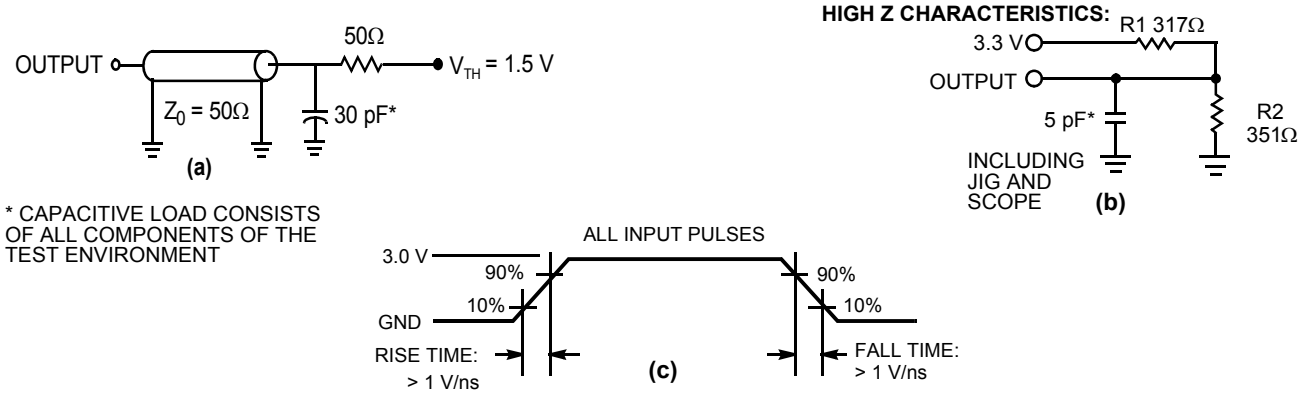
Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF
C_{OUT}	I/O Capacitance			

Thermal Resistance

Parameter [6]	Description	Test Conditions	54-pin TSOP II	Unit
Θ_{JA}	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	°C/W
Θ_{JC}	Thermal Resistance (junction to case)		21.58	

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [7]



Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Full-device AC operation assumes a 100-µs ramp time from 0 to V_{CC} (min) and 100-µs wait time after V_{CC} stabilizes to its operational value.

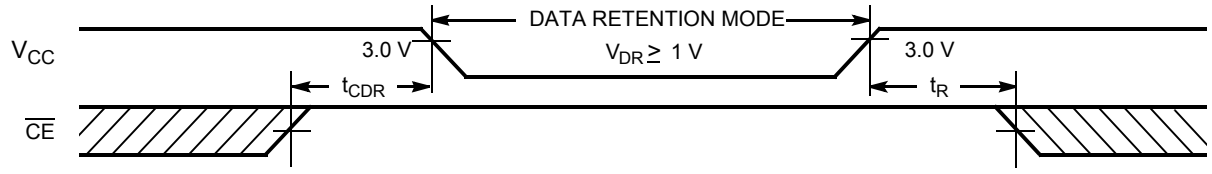
Data Retention Characteristics

Over the Operating Range –45 °C to 85 °C

Parameter	Description	Conditions	Min	Typ [8]	Max	Unit
V_{DR}	V_{CC} for Data Retention	–	1.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	30.0	mA
t_{CDR} [9]	Chip Deselect to Data Retention Time	–	0.0	–	–	ns
t_R [9, 10]	Operation Recovery Time	–	10.0	–	–	

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
9. This parameter is guaranteed by design and is not tested.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

AC Switching Characteristics

Over the Operating Range

Parameter [11]	Description	-10		Unit
		Min	Max	
Read Cycle				
t_{POWER}	V_{CC} to the first access [12]	100.0	–	µs
t_{RC}	Read cycle time	10.0	–	ns
t_{AA}	Address to data valid	–	10.0	
t_{OHA}	Data hold from address change	3.0	–	
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10.0	
t_{DOE}	$\overline{OE}$ LOW to data valid	–	5.0	
t_{LZOE}	$\overline{OE}$ LOW to low Z [13, 14, 15]	0.0	–	
t_{HZOE}	$\overline{OE}$ HIGH to high Z [13, 14, 15]	–	5.0	
t_{LZCE}	$\overline{CE}$ LOW to low Z [13, 14, 15]	3.0	–	
t_{HZCE}	$\overline{CE}$ HIGH to high Z [13, 14, 15]	–	5.0	
t_{PU}	$\overline{CE}$ LOW to power-up [16]	0.0	–	
t_{PD}	$\overline{CE}$ HIGH to power-down [16]	–	10.0	
t_{DBE}	Byte enable to data valid	–	5.0	
t_{LZBE}	Byte enable to low Z	1.0	–	
t_{HZBE}	Byte disable to high Z	–	6.0	
Write Cycle [17, 18]				
t_{WC}	Write cycle time	10.0	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7.0	–	
t_{AW}	Address setup to write end	7.0	–	
t_{HA}	Address hold from write end	0.0	–	
t_{SA}	Address setup to write start	0.0	–	
t_{PWE}	$\overline{WE}$ pulse width	7.0	–	
t_{SD}	Data setup to write end	5.0	–	
t_{HD}	Data hold from write end	0.0	–	
t_{LZWE}	$\overline{WE}$ HIGH to low Z [13, 14, 15]	3.0	–	
t_{HZWE}	$\overline{WE}$ LOW to high Z [13, 14, 15]	–	5.0	
t_{BW}	Byte enable to end of write	7.0	–	

Notes

11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 3 on page 7, unless specified otherwise.
12. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
13. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} , t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured ±200 mV from steady state voltage.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. Tested initially and after any design or process changes that may affect these parameters.
16. These parameters are guaranteed by design and are not tested.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. Chip enable must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612G [19, 20]

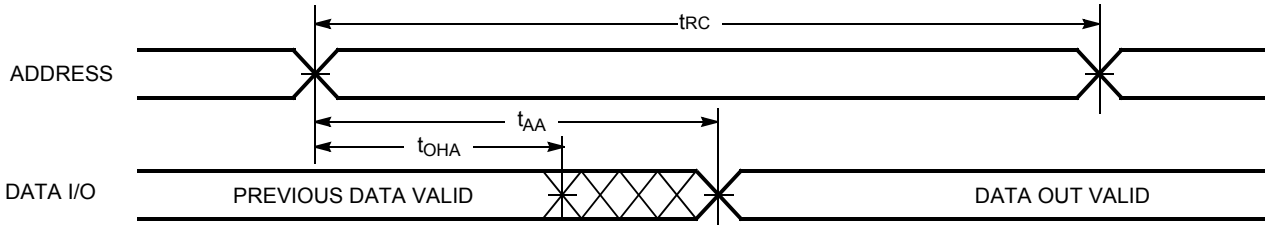
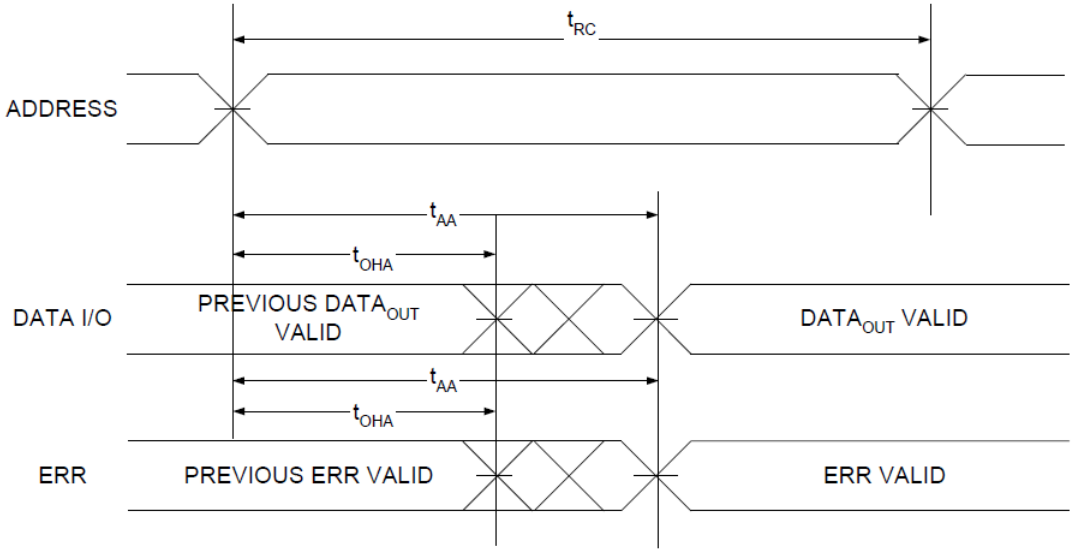


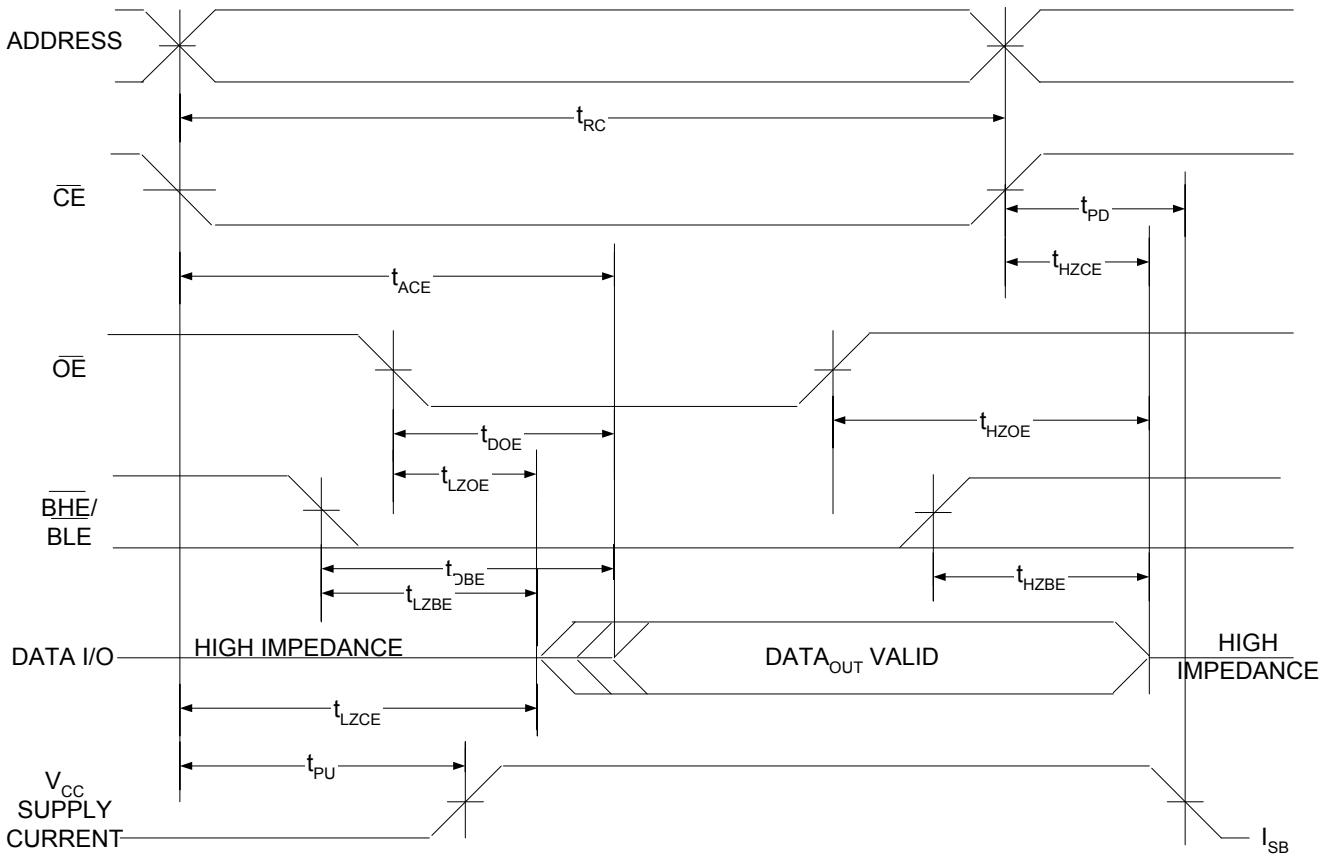
Figure 6. Read Cycle No. 1 (Address Transition Controlled) for CY7C10612GE [20, 21]



Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 (OE Controlled) [22, 23]



Notes
22. WE is HIGH for read cycle.
23. Address valid before or similar to CE transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{CE}$ Controlled) [24, 25, 26]

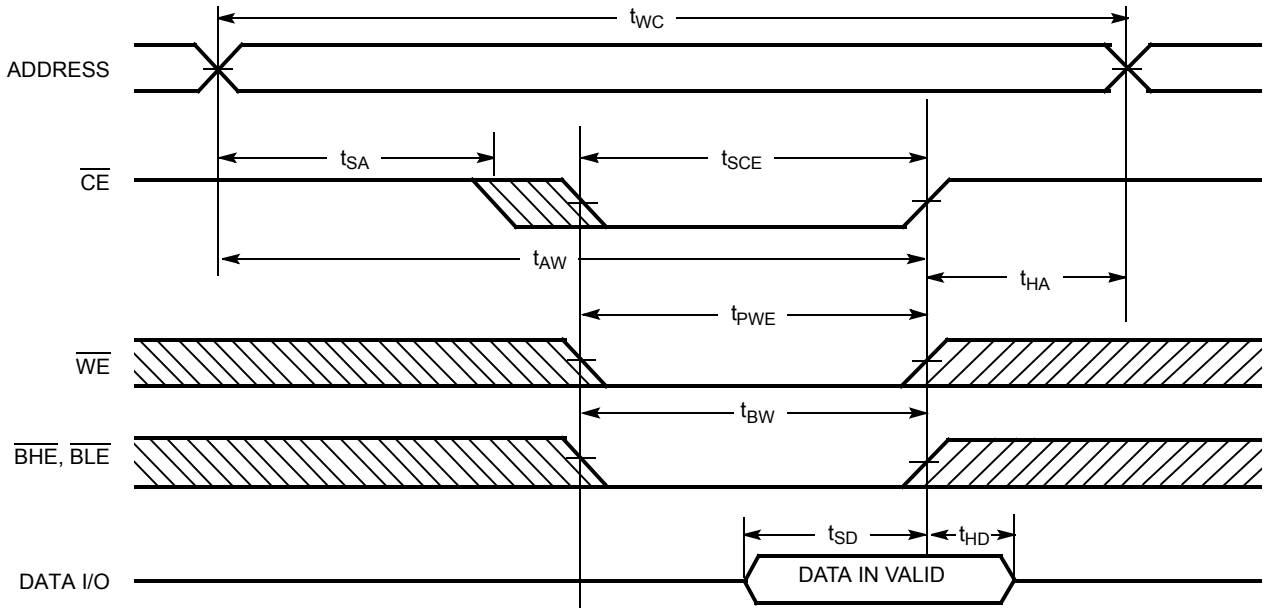
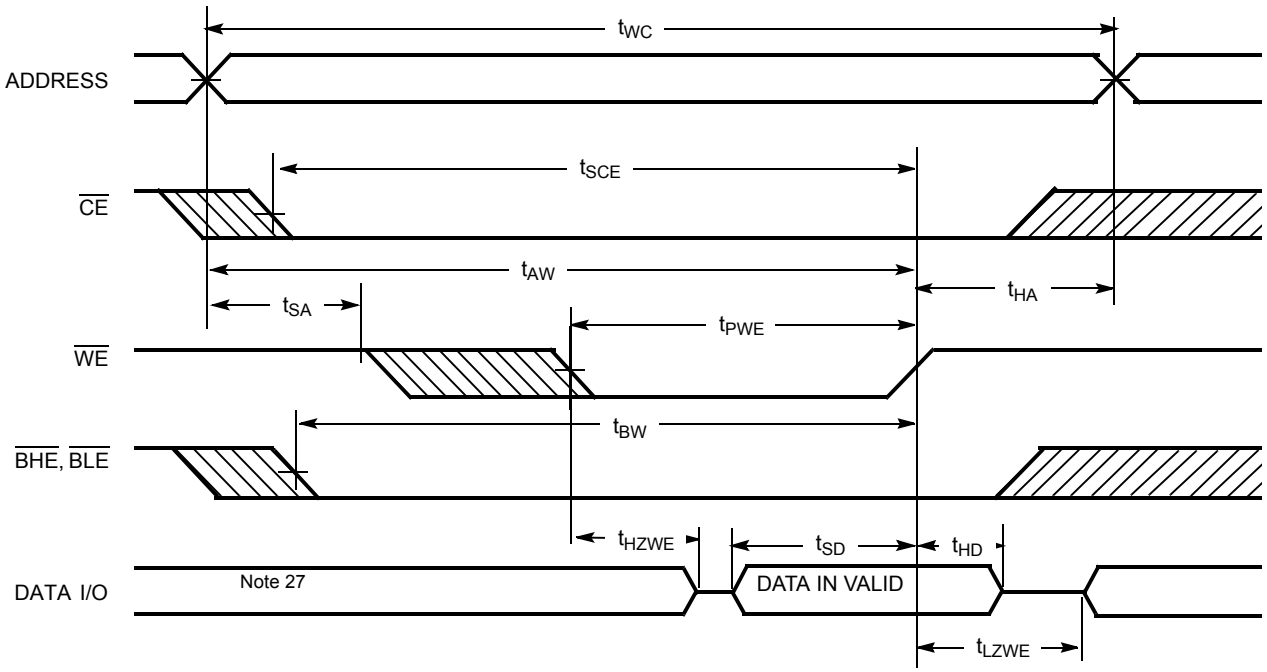


Figure 9. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [24, 25, 26]

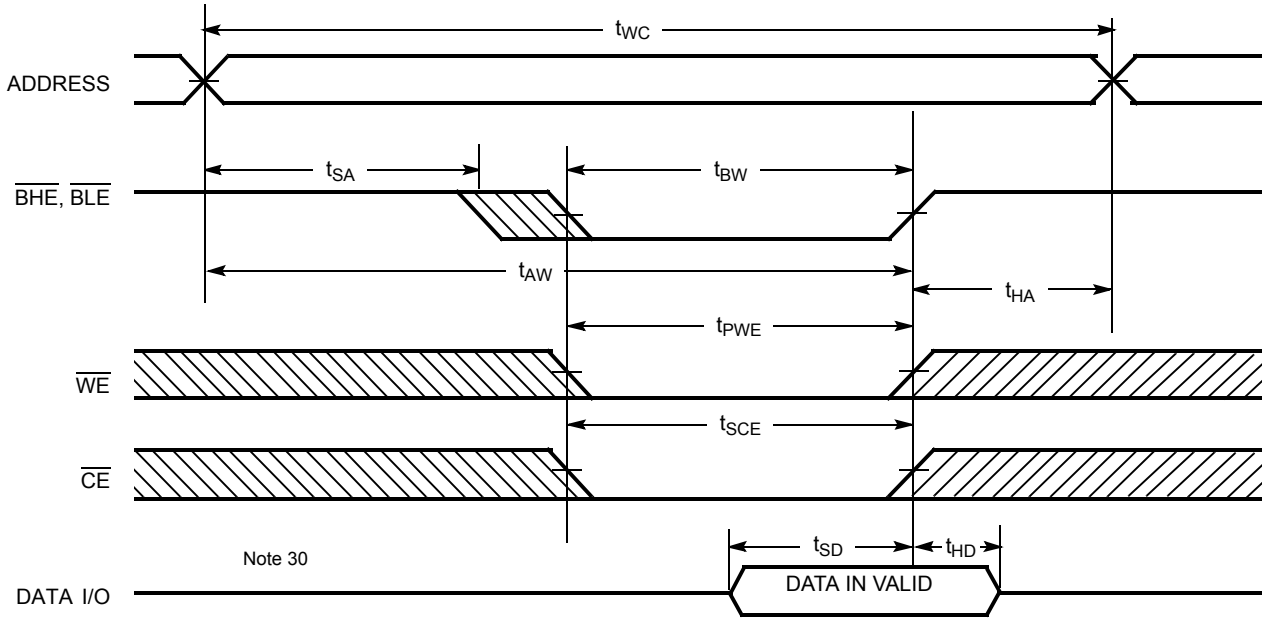


Notes

24. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
27. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [28, 29]



Notes

28. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
29. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}$ = V_{IL} and $\overline{BHE}$ or $\overline{BLE}$ = V_{IL}. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
30. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write all bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

ERR Output – CY7C10612GE

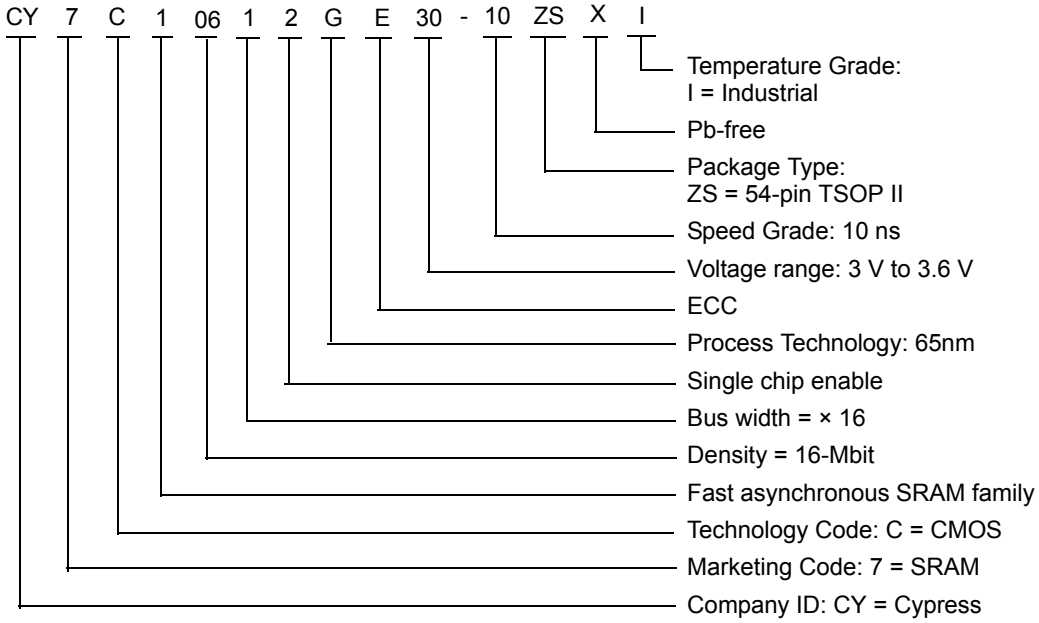
Output [31]	Mode
0	Read Operation, no error in the stored data.
1	Read Operation, single-bit error detected and corrected.
High-Z	Device deselected or Outputs disabled or Write Operation.

Note
31. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

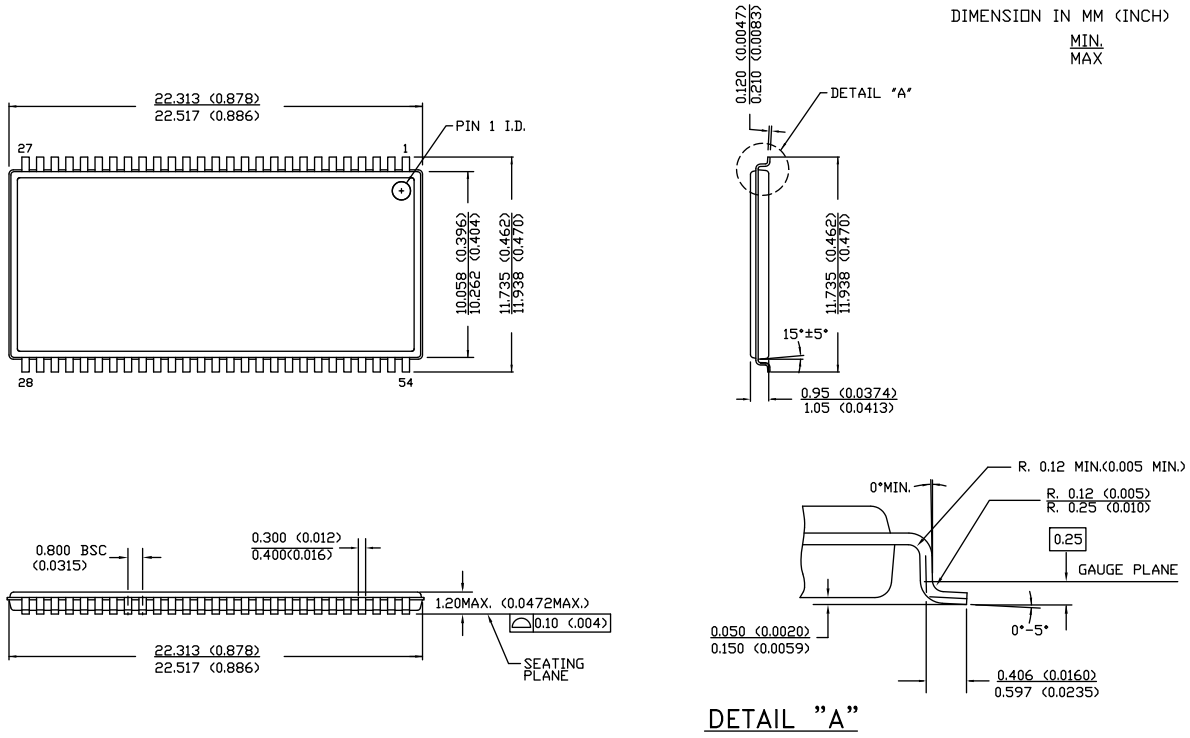
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C10612G30-10ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial
	CY7C10612GE30-10ZSXI			

Ordering Code Definitions



Package Diagrams

Figure 11. 54-pin TSOP Type II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160



Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C10612G/CY7C10612GE, 16-Mbit (1 M × 16) Static RAM Document Number: 001-88702				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4104325	VINI	08/26/2013	New data sheet.
*A	4525600	VINI	10/06/2014	Updated Features: Changed value of I_{SB2} from “10 mA typical” to “20 mA typical”. Replaced “1.5 V data retention” with “1 V data retention”. Updated Logic Block Diagram – CY7C10612GE. Updated Selection Guide: Changed value of Maximum CMOS Standby Current from 10 mA to 20 mA. Updated DC Electrical Characteristics: Added a column “Typ” and added details in that column. Added Note 5 and referred the same note in “Typ” column. Added Note 5 and referred the same note in Test Conditions of I_{SB1} and I_{SB2} parameters. Updated AC Switching Characteristics: Added t_{POWER} parameter and its details. Changed minimum value of t_{LZOE} parameter from 1 ns to 0 ns. Updated Switching Waveforms: Removed Note “For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.” and its reference in Figure 7. Updated Package Diagrams: spec 51-85160 – Changed revision from *D to *E. Completing Sunset Review.
*B	4571739	VINI	11/16/2015	Added related documentation hyperlink in page 1.
*C	4571766	NILE	02/12/2015	Updated Selection Guide: Changed value of Maximum Active current from 90 mA to 110 mA. Changed value of Maximum Standby current from 20 mA to 30 mA. Updated Pin Configurations: Added Note 3 and referred the same note in Figure 2. Updated Maximum Ratings: Updated ratings corresponding to “Supply Voltage on V_{CC} Relative to GND”. Updated AC Test Loads and Waveforms: Updated Note 7. Updated Data Retention Characteristics: Updated Note 9. Referred Note 9 in t_R parameter. Updated AC Switching Characteristics: Referred Note 12 in description of t_{POWER} parameter. Added Notes 14, 15 and referred the same notes in description of t_{LZOE}, t_{HZOE}, t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE} parameters. Updated Switching Waveforms: Updated Note 25. Added Notes 26, 27 and referred the same notes in Figure 9. Added Notes 29, 30 and referred the same notes in Figure 10.

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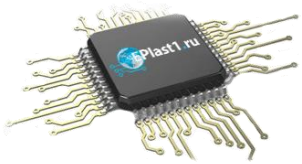
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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