

MAX16072/MAX16073/ MAX16074

nanoPower μ P Supervisory Circuits in a 4-Bump (1mm x 1mm) Chip-Scale Package

General Description

The MAX16072/MAX16073/MAX16074 ultra-small, ultra-low-power, microprocessor (μ P) supervisory circuits feature a precision band-gap reference, comparator, and internally trimmed resistors that set the threshold voltage. Designed to monitor the system supply voltage and assert an output during power-up, power-down, and brownout conditions, these devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltage from 1.8V to 3.6V.

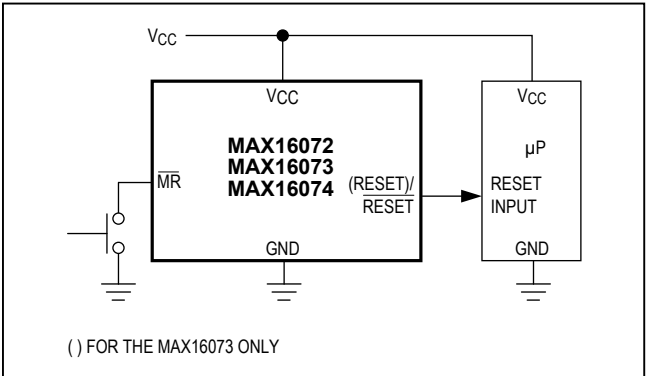
The MAX16072 has a push-pull, active-low reset output, the MAX16073 has a push-pull, active-high reset output, and the MAX16074 has an open-drain active-low reset output. The devices are designed to ignore fast transients on V_{CC} . The devices also include a manual reset input (MR).

The MAX16072/MAX16073/MAX16074 are available in a 1mm x 1mm, space-saving, 4-bump, chip-scale package (UCSP™).

Applications

- Portable/Battery-Powered Equipment
- Cell Phones
- PDAs
- MP3 Players
- Digital Cameras

Typical Application Circuit



Features

- Ultra-Low, 0.7 μ A Supply Current
- Ultra-Small (1mm x 1mm), 4-Bump UCSP
- 20 μ s, 8ms, 34ms, and 140ms Reset Timeout Options Available
- Factory-Trimmed Reset Thresholds Available from 1.58V to 3.08V in Approximately 100mV Increments
- $\pm 2.5\%$ Threshold Accuracy Over Temperature
- Manual Reset Input
- Guaranteed Reset Valid to $V_{CC} = 1.0V$
- Immune to Short V_{CC} Transient

Ordering Information

| PART | RESET OUTPUT TYPE | PIN-PACKAGE |
|-----------------|------------------------|-------------|
| MAX16072RS__D_+ | Push-Pull, Active-Low | 4 UCSP |
| MAX16073RS__D_+ | Push-Pull, Active-High | 4 UCSP |
| MAX16074RS__D_+ | Open-Drain, Active-Low | 4 UCSP |

+Denotes a lead(Pb)-free/RoHS-compliant package.

Note: All devices are specified over the $-40^{\circ}C$ to $+85^{\circ}C$ operating temperature range.

Insert the desired suffix numbers (from Table 1) into the blanks "RS__D" to indicate the reset trip threshold. Insert the desired suffix number (from Table 2) into the blank "D_+" to indicate the reset timeout. Minimum order quantity may apply.

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Absolute Maximum Ratings

(Voltages referenced to GND.)

V_{CC} , \overline{MR}-0.3V to +6V
 \overline{RESET} , \overline{RESET} Push-Pull-0.3V to (V_{CC} + 0.3V)
 \overline{RESET} Open-Drain.....-0.3V to +6V
 Output Current (all pins)..... ± 20 mA
 Continuous Power Dissipation (T_A = +70°C)
 4-Bump UCSP (derate 3mW/°C above +70°C).....239mW

Operating Temperature Range.....-40°C to +85°C
 Storage Temperature Range.....-65°C to +150°C
 Junction Temperature.....+150°C
 Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.6V.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------------------|---|--|------------------|------------------|------------|
| Operating Voltage Range | V_{CC} | T_A = 0°C to +85°C | 1.0 | | 5.5 | V |
| | | T_A = -40°C to +85°C | 1.2 | | 5.5 | |
| Supply Current | I_{CC} | V_{CC} = 1.8V for $V_{TH} \leq 1.66$ V | | 0.7 | 1.2 | μ A |
| | | V_{CC} = 3.6V, no load | | 1.0 | 1.5 | |
| Detector Threshold | V_{TH} | See Table 1 | V_{CC} falling, T_A = +25°C | $V_{TH} - 1.5\%$ | $V_{TH} + 1.5\%$ | V |
| | | | V_{CC} falling, T_A = -40°C to +85°C | $V_{TH} - 2.5\%$ | $V_{TH} + 2.5\%$ | |
| Detector Threshold Hysteresis | V_{HYST} | V_{CC} rising, $V_{TH} \leq 1.66$ V (Note 2) | | 6.3 | | mV |
| Detector Threshold Tempco | $\Delta V_{TH}/^\circ\text{C}$ | (Note 2) | | 40 | | ppm/°C |
| \overline{MR} INPUT | | | | | | |
| \overline{MR} Input High Voltage | V_{IH} | | 0.7 x V_{CC} | | | V |
| | V_{IL} | | | 0.7 x V_{CC} | | |
| \overline{MR} Pullup Resistance | | | 25 | 50 | 75 | k Ω |
| $\overline{RESET}/RESET$ OUTPUT (Note 3) | | | | | | |
| Output-Voltage Low | V_{OL} | $V_{CC} \geq 1.2$ V, $I_{SINK} = 100\mu$ A | | | 0.4 | V |
| | | $V_{CC} \geq 1.65$ V, $I_{SINK} = 1$ mA | | | 0.3 | |
| Output-Voltage High | V_{OH} | $V_{CC} \geq 1.65$ V, $I_{SOURCE} = 500\mu$ A | 0.8 x V_{CC} | | | V |
| | | $V_{CC} \geq 1.2$ V, $I_{SOURCE} = 50\mu$ A | 0.8 x V_{CC} | | | |
| Open-Drain \overline{RESET} Output Leakage Current | | \overline{RESET} not asserted (Note 2) | | | 0.1 | μ A |
| TIMING | | | | | | |
| \overline{MR} Minimum Pulse Width | t_{MPW} | (Note 2) | 0.8 | | | μ s |
| \overline{MR} Glitch Rejection | t_{EGR} | (Note 2) | | 100 | | ns |
| \overline{MR} to $\overline{RESET}/RESET$ Propagation Delay | t_{OFF} | \overline{MR} falling | | 1 | 2 | μ s |
| | t_{ON} | \overline{MR} rising | | 200 | 400 | ns |
| V_{CC} to Reset Delay | t_{DL} | $V_{CC} = (V_{TH} + 100\text{mV})$ to $(V_{TH} - 100\text{mV})$ | | 20 | 90 | μ s |

MAX16072/MAX16073/
MAX16074

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4-Bump (1mm x 1mm) Chip-Scale Package

Electrical Characteristics (continued)

(V_{CC} = 1.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.6V.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|-----------------------------|-----------------|--|---------------|-----|-----|-----|-------|
| Reset Active Timeout Period | t _{RP} | V _{CC} rising, V _{CC} = (V _{TH} - 100mV) to (V _{TH} + 100mV) | MAX1607_RSD0+ | 20 | 80 | 120 | μs |
| | | | MAX1607_RSD1+ | 8 | 13 | 17 | ms |
| | | | MAX1607_RSD2+ | 34 | 52 | 69 | ms |
| | | | MAX1607_RSD3+ | 140 | 210 | 280 | ms |

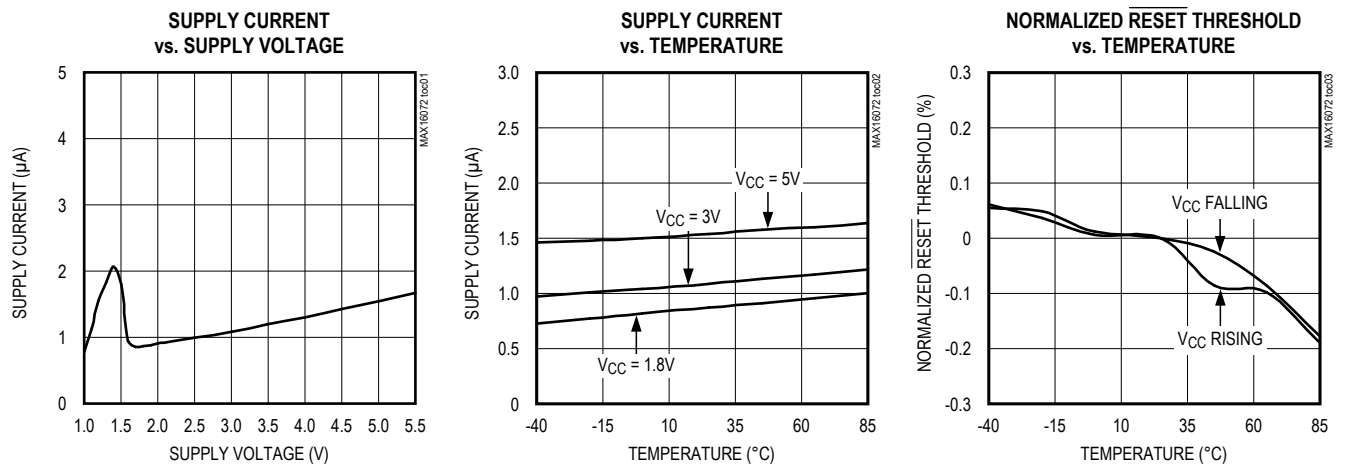
Note 1: Production testing done at T_A = +25°C only. Overtemperature limits are guaranteed by design and are not production tested.

Note 2: Guaranteed by design.

Note 3: Reset is guaranteed down to V_{CC} = 1.0V.

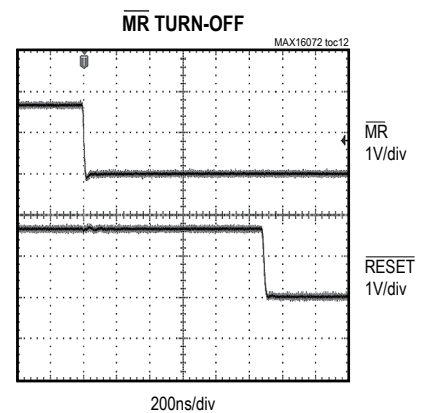
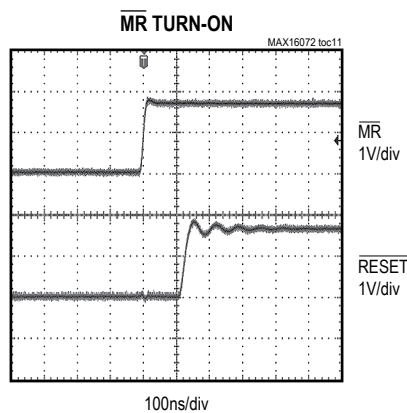
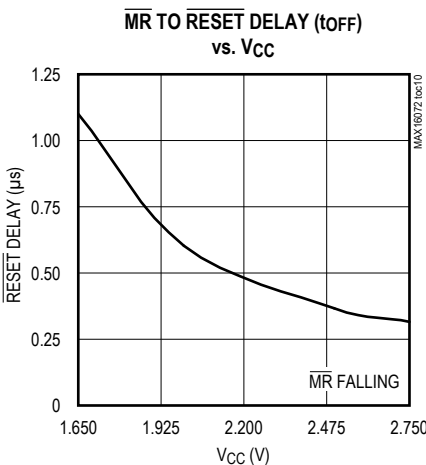
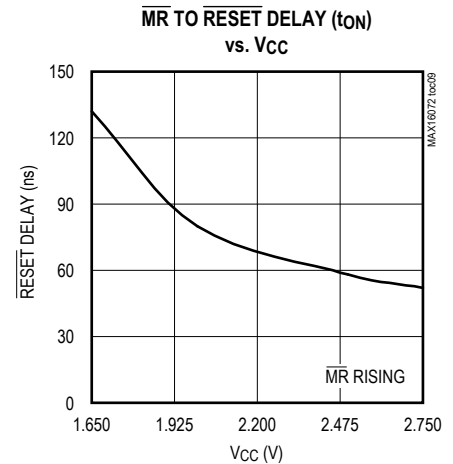
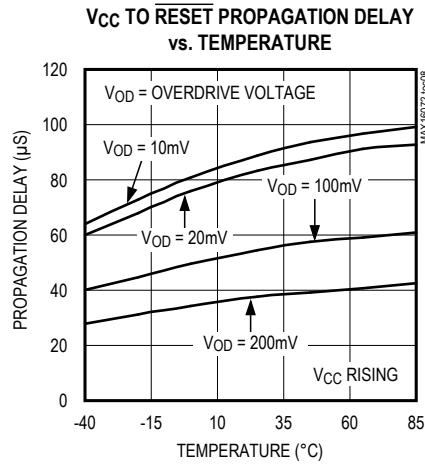
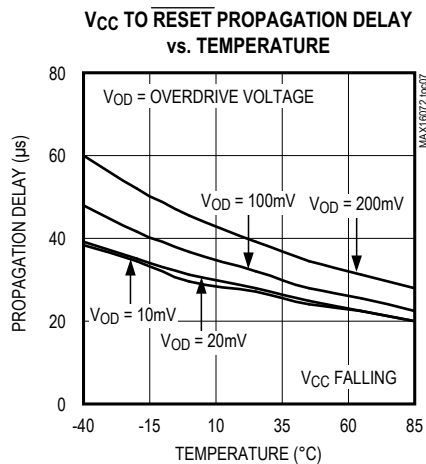
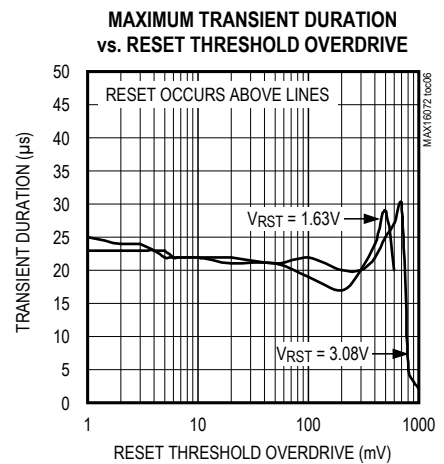
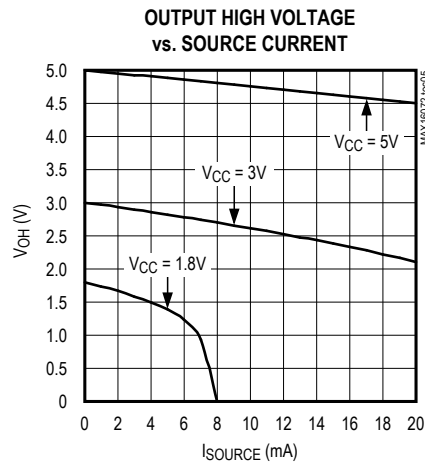
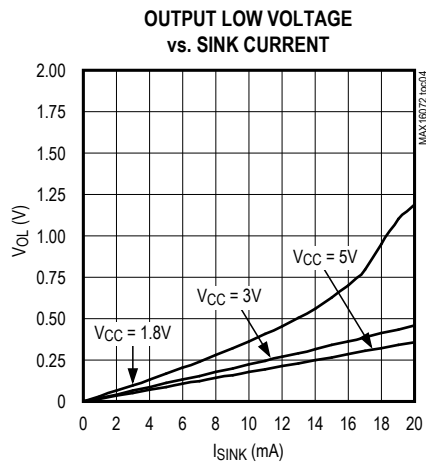
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



Typical Operating Characteristics (continued)

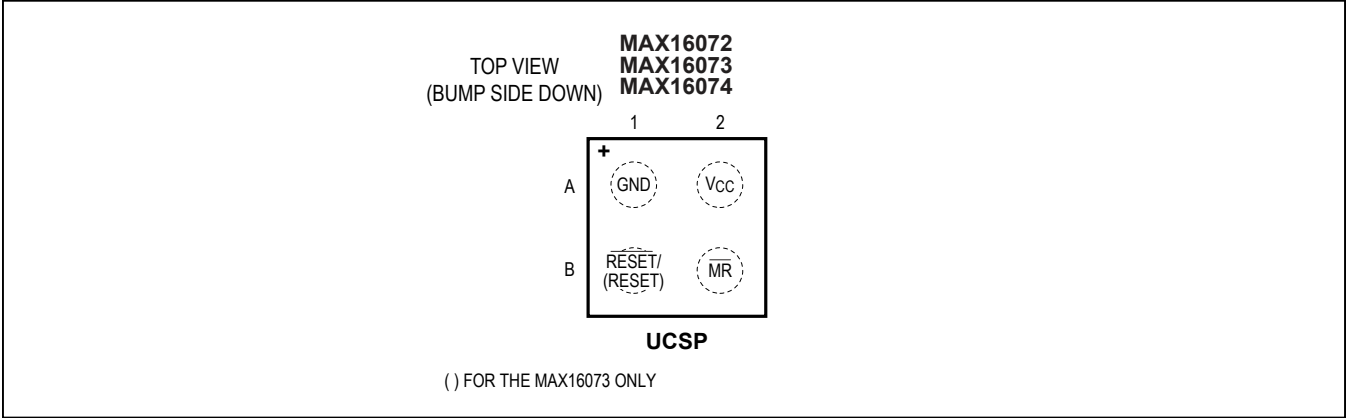
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



MAX16072/MAX16073/
MAX16074

nanoPower μ P Supervisory Circuits in a
4-Bump (1mm x 1mm) Chip-Scale Package

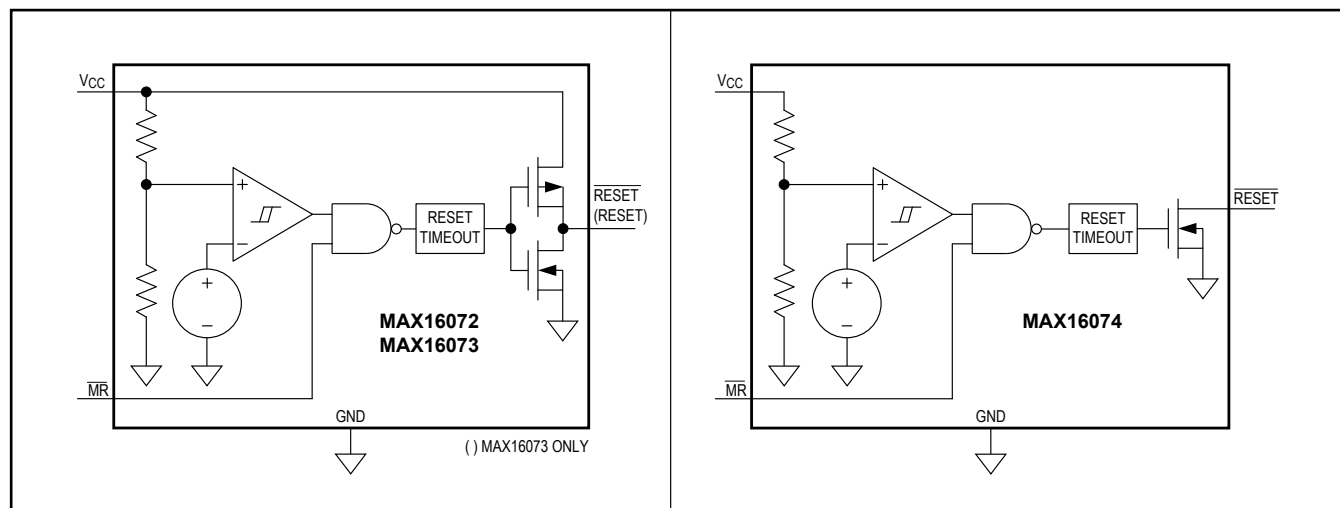
Bump Configuration



Bump Description

| BUMP | | | NAME | FUNCTION |
|----------|----------|----------|-------|---|
| MAX16072 | MAX16073 | MAX16074 | | |
| A1 | A1 | A1 | GND | Ground |
| B1 | — | — | RESET | Active-Low Push-Pull Reset Output. RESET changes from high to low when VCC drops below the detector threshold (VTH) or MR is pulled low. RESET remains low for the reset timeout period after VCC exceeds VTH and MR is high. When MR is low, RESET is low. |
| — | B1 | — | RESET | Active-High Push-Pull Reset Output. RESET changes from low to high when VCC drops below the detector threshold (VTH) or MR is pulled low. RESET remains high for the reset timeout period after VCC exceeds VTH and MR is high. When MR is low, RESET is high. |
| — | — | B1 | RESET | Active-Low Open-Drain Reset Output. RESET changes from high-impedance to active-low when VCC drops below the detector threshold (VTH) or MR is pulled low. RESET remains low for the reset timeout period after VCC exceeds the reset threshold and MR is high. When MR is low, RESET is low. |
| A2 | A2 | A2 | VCC | Supply Voltage and Input for the Reset Threshold Monitor |
| B2 | B2 | B2 | MR | Active-Low Manual-Reset Input. Drive low to force a reset. Reset remains active as long as MR is low and for the reset timeout period (if applicable) after MR is driven high. MR has an internal pullup resistor connected to VCC, and may be left unconnected if not used. |

Functional Diagrams



Detailed Description

The MAX16072/MAX16073/MAX16074 ultra-small, ultra-low-power, μ P supervisory circuits feature a precision band-gap reference, comparator, and internally trimmed resistors that set specified trip threshold voltages. Designed to monitor the system supply voltage and an output during power-up, power-down, and brownout conditions, these devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when monitoring nominal system voltage from 1.8V to 3.6V.

The MAX16072 has a push-pull active-low reset output, the MAX16073 has a push-pull active-high reset output, and the MAX16074 has an open-drain active-low reset

output. The devices are designed to ignore fast transients on V_{CC} . The devices also include a manual reset input (MR). When \overline{MR} is low, reset is asserted. When \overline{MR} is high and V_{CC} is above the detector threshold (V_{TH}), reset is not asserted.

Supply and Monitored Input (V_{CC})

The MAX16072/MAX16073/MAX16074 operate with a V_{CC} supply voltage from 1.2V to 5.5V. V_{CC} has a rising threshold of $V_{TH} + V_{HYST}$ and a falling threshold of V_{TH} . When V_{CC} rises above $V_{TH} + V_{HYST}$ and \overline{MR} is high, \overline{RESET} goes high (RESET goes low) after the reset timeout period (t_{RP}). See Figure 1.

When V_{CC} falls below V_{TH} , \overline{RESET} goes low (RESET goes high) after a fixed delay (t_{RD}).

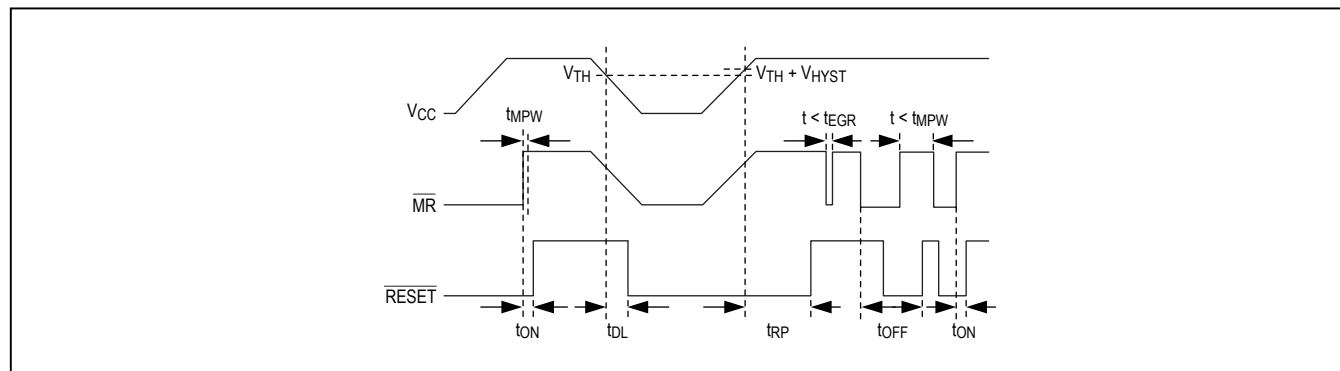


Figure 1. MAX16072/MAX16073/MAX16074 Timing Diagram

Manual Reset Input ($\overline{\text{MR}}$)

Many μ P-based products require manual-reset capability, allowing the operator, a test technician, or external logic circuit to initiate a reset. A logic-low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for the reset active timeout period (t_{RP}) or delay (t_{ON}) after $\overline{\text{MR}}$ returns high. This input has an internal 50k Ω pullup resistor, so it can be left unconnected if it is not used. $\overline{\text{MR}}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. For manual operation, connect a normally open momentary switch from $\overline{\text{MR}}$ to GND; external debouncing circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in a noisy environment, connect a 0.1 μ F capacitor from $\overline{\text{MR}}$ to ground to provide additional noise immunity.

Applications Information

Interfacing to μ P with Bidirectional Reset Pins

Since $\overline{\text{RESET}}$ on the MAX16074 is open-drain, this device interfaces easily with μ Ps that have bidirectional reset pins. Connecting the μ P supervisor's $\overline{\text{RESET}}$ output directly to the μ P's $\overline{\text{RESET}}$ pin with a single pullup resistor allows either device to assert reset (Figure 2).

Negative-Going V_{CC} Transients

The MAX16072/MAX16073/MAX16074 family of devices is relatively immune to short-duration, negative-going V_{CC} transients (glitches). The *Typical Operating Characteristics* show the Maximum Transient Duration vs. Reset Threshold Overdrive graph, for which reset pulses are not generated. The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have when issuing a reset signal. As the amplitude of the transient increases, the maximum allowable pulse width decreases.

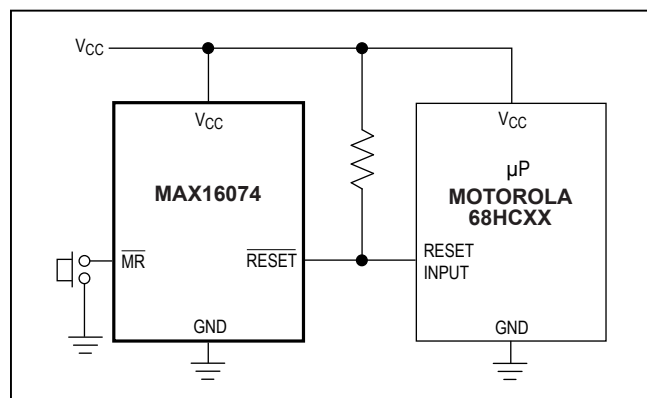


Figure 2. Interfacing to μ P with Bidirectional Reset Pins

Table 1. Factory Trimmed Reset Thresholds

| THRESHOLD SUFFIX | RESET TRIP THRESHOLD (V) | | |
|------------------|---------------------------|-------|---|
| | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ |
| | TYP | MIN | MAX |
| 15 | 1.58 | 1.54 | 1.61 |
| 16 | 1.63 | 1.60 | 1.66 |
| 17 | 1.67 | 1.62 | 1.71 |
| 18 | 1.80 | 1.76 | 1.85 |
| 19 | 1.90 | 1.85 | 1.95 |
| 20 | 2.00 | 1.95 | 2.05 |
| 21 | 2.10 | 2.05 | 2.15 |
| 22 | 2.20 | 2.145 | 2.25 |
| 23 | 2.32 | 2.262 | 2.375 |
| 24 | 2.40 | 2.34 | 2.46 |
| 25 | 2.50 | 2.437 | 2.562 |
| 26 | 2.63 | 2.564 | 2.69 |
| 27 | 2.70 | 2.633 | 2.768 |
| 28 | 2.80 | 2.63 | 2.87 |
| 29 | 2.93 | 2.857 | 3.0 |
| 30 | 3.00 | 2.925 | 3.075 |
| 31 | 3.08 | 3.003 | 3.15 |

Table 2. Reset Timeout Periods

| RESET TIMEOUT PERIODS | | | | |
|-----------------------|-----|-----|-----|---------|
| SUFFIX | MIN | TYP | MAX | UNITS |
| 0 | 20 | 80 | 120 | μ s |
| 1 | 8 | 13 | 17 | ms |
| 2 | 34 | 52 | 69 | ms |
| 3 | 140 | 210 | 280 | ms |

MAX16072/MAX16073/
MAX16074

nanoPower μ P Supervisory Circuits in a
4-Bump (1mm x 1mm) Chip-Scale Package

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. |
|--------------|--------------|-------------------------|
| 4 UCSP | R41C1-1 | 21-0242 |

MAX16072/MAX16073/
MAX16074

nanoPower μ P Supervisory Circuits in a
4-Bump (1mm x 1mm) Chip-Scale Package

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|------------------|--|------------------|
| 0 | 1/10 | Initial release | — |
| 1 | 3/15 | Changed upper V_{CC} supply range from 2.75V to 5.5V | 2, 3, 6 |
| 2 | 3/17 | Updated title to include “nanoPower” | 1–9 |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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