

A full Data Sheet is available to qualified customers. To register, please send an email to TimingandSync@zarlink.com.

## Features

- Single chip low cost solution for synchronizing an Ethernet PHY to a standard telecom clock
- Generates an IEEE 802.3 jitter compliant 25 MHz Gigabit Ethernet output clock
- Supports three modes of operation: Asynchronous Freerun, Synchronous, and Asynchronous Holdover
- Defaults in Asynchronous Freerun mode
- In Asynchronous Freerun mode, the DPLL generates an output clock with a frequency accuracy equal to frequency accuracy of the external crystal oscillator (XO) or a low cost crystal (XTAL)
- In Synchronous mode, the DPLL automatically synchronizes to one of a pre-defined set of frequencies including 2 kHz, 8 kHz, 64 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 38.88 MHz, 77.76 MHz.

## Ordering Information

ZL30107GGG	64 Pin CABGA	Trays
ZL30107GGG2	64 Pin CABGA*	Trays

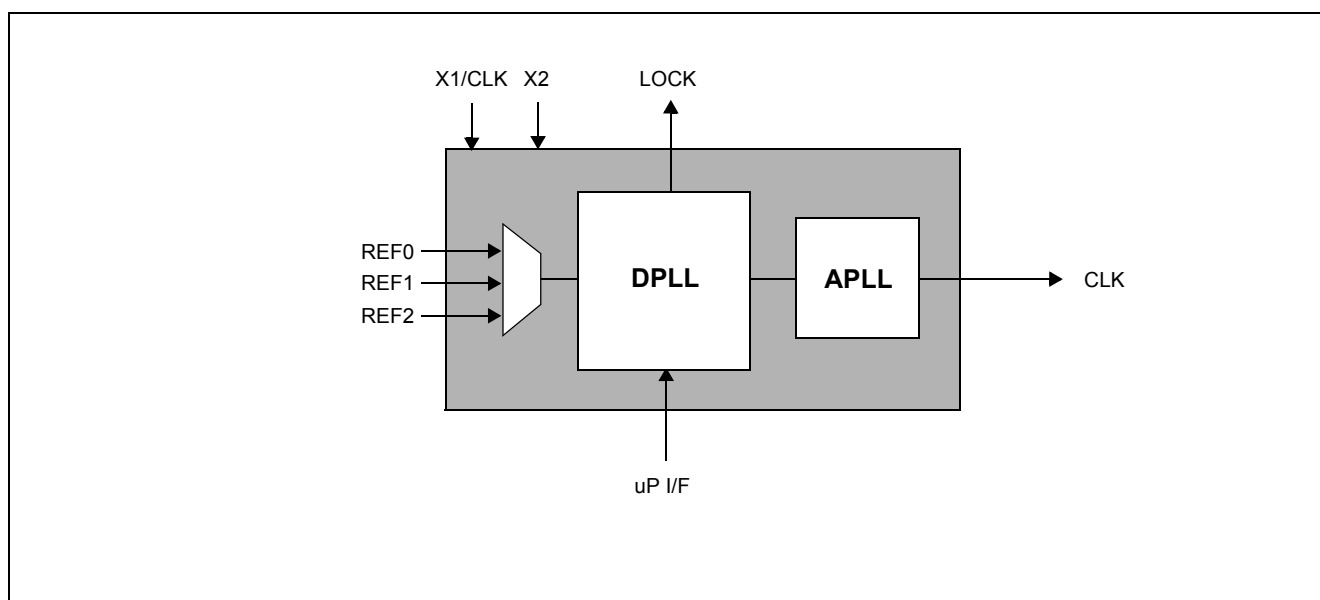
\*Pb Free Tin/Silver/Copper

**-40°C to +85°C**

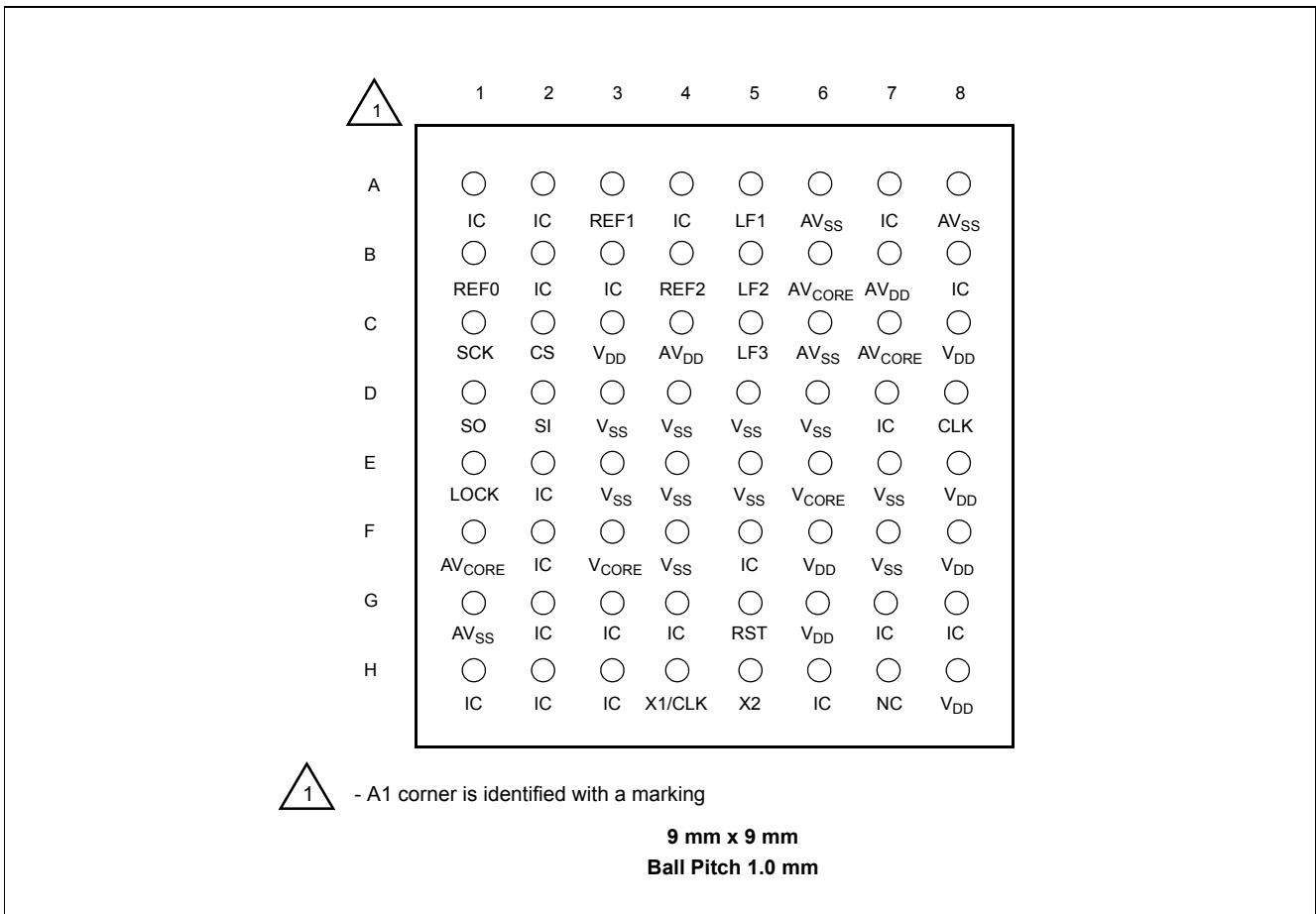
- Configurable to accept a 25 MHz input reference
- Automatic entry into Asynchronous Holdover mode when all input references fail
- Input reference is manually selectable through the serial (SPI) interface
- Hitless input reference switching
- Lock indicator pin
- Input reference status monitors
- Programmable loop bandwidth of 14 Hz, 28 Hz, or 890 Hz

## Applications

- Ethernet Line Cards Supporting Synchronous Transmission



**Figure 1 - Block Diagram**



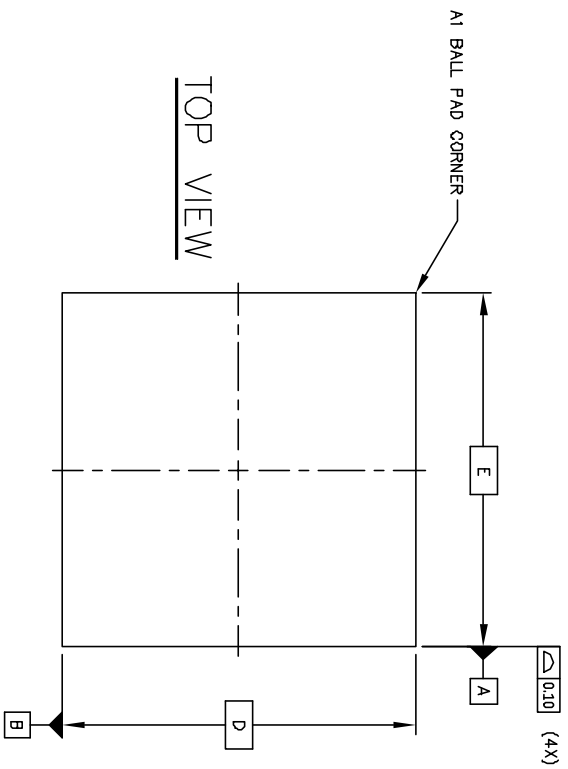
**Figure 2 - Pin Connections**

## Pin Description

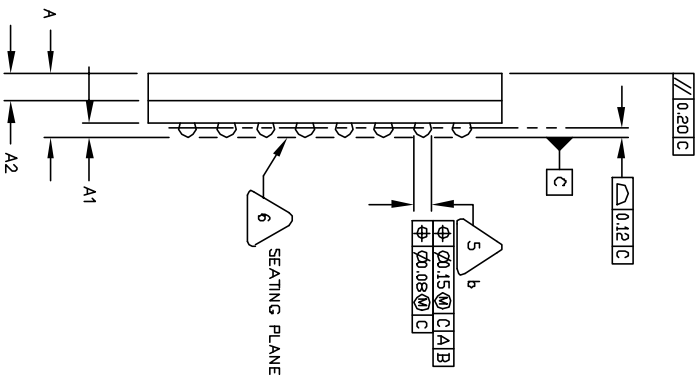
Pin #	Name	I/O Type	Description
B1 A3 B4	REF0 REF1 REF2	I <sub>d</sub>	<b>Reference Inputs (LVCMOS, Schmitt Trigger).</b> These reference inputs are used for synchronizing the PLL. These pins are internally pulled down to Vss.
D8	CLK	O	<b>SONET/SDH/Ethernet Clock Output (LVCMOS).</b> This output clock is configurable as 77.76 MHz, 25 MHz, and 50 MHz. Default is 77.76 MHz.
G5	RST	I	<b>Reset (LVCMOS, Schmitt Trigger).</b> A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
E1	LOCK	O	<b>Lock Indicator (LVCMOS).</b> This is the lock indicator pin for the PLL. This output goes high when the DPLL's output is frequency is phase locked to the input reference.
A5	LF1	A	<b>External Analog PLL Loop Filter terminal.</b>
B5	LF2	A	<b>Analog PLL External Loop Filter Reference.</b>
C5	LF3	A	<b>Analog PLL External Loop Filter Reference.</b>
H4	X1/CLK	I	<b>Oscillator Master Clock Input (LVCMOS).</b> This input accepts a 20 MHz reference from a clock oscillator (XO, XTAL). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
H5	X2	O	<b>Oscillator Master Clock Output (LVCMOS).</b> This pin is used for connection with an crystal. This pin must be left unconnected when the X1 pin is connected to a clock oscillator.
C1	SCK	I	<b>Clock for Serial Interface (LVCMOS).</b> Serial interface clock.
D2	SI	I	<b>Serial Interface Input (LVCMOS).</b> Serial interface data input pin.
D1	SO	O	<b>Serial Interface Output (LVCMOS).</b> Serial interface data output pin.
C2	CS	I <sub>u</sub>	<b>Chip Select for Serial Interface (LVCMOS).</b> Serial interface chip select. This pin is internally pulled up to Vdd.
F5 A1 A2 A4 A7 B8 D7 E2 G7 H1 B2 G4 G2 G3 G8 H3 F2	IC		<b>Internal Connection.</b> Leave unconnected.

Pin #	Name	I/O Type	Description
H6 B3 H2	IC		<b>Internal Connection.</b> Connect to ground.
H7	NC		<b>No Connection.</b> Leave unconnected.
C3 C8 E8 F6 F8 G6 H8	V <sub>DD</sub>	P P P P P P P	<b>Positive Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal.
E6 F3	V <sub>CORE</sub>	P P	<b>Positive Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal.
B7 C4	AV <sub>DD</sub>	P P	<b>Positive Analog Supply Voltage.</b> +3.3 V <sub>DC</sub> nominal.
B6 C7 F1	AV <sub>CORE</sub>	P P P	<b>Positive Analog Supply Voltage.</b> +1.8 V <sub>DC</sub> nominal.
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V <sub>SS</sub>	G G G G G G G G G G	<b>Ground.</b> 0 Volts.
A6 A8 C6 G1	AV <sub>SS</sub>	G G G G	<b>Analog Ground.</b> 0 Volts.

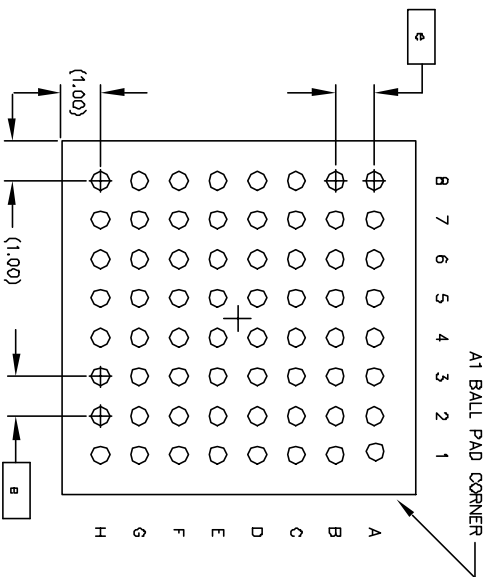
I - Input  
 I<sub>d</sub> - Input, Internally pulled down  
 I<sub>u</sub> - Input, Internally pulled up  
 O - Output  
 A - Analog  
 P - Power  
 G - Ground



**TOP VIEW**



**SIDE VIEW**



**BOTTOM VIEW**

64 SOLDER BALLS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	9.00 REF.		
E	9.00 Ref.		
e	1.0 Ref		
n	64		

- 6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
- 4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.
- 3. Not to Scale.
- 2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.
- 1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

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ISSUE	1		
ACN	CDCA		
DATE	15Apr105		
APPRD.			



Previous package codes

N/A

Package Code GG

Package Outline for 64ball  
9x9mm, 1.0 mm Pitch,  
4 layer, CABGA

111039



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- Техническая поддержка проекта;
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**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.