High Performance, Polyphase Energy Metering AFE

Data Sheet

ADE9078

FEATURES

- 7 high performance analog-to-digital converters (ADCs)
  - 101 dB signal-to-noise ratio (SNR)
  - 10,000:1 dynamic range
  - Wide input range: ±1 V, 0.707 V rms full scale
  - Differential inputs
- ±25 ppm/°C maximum channel temperature drift (including ADC, internal V_{REF}, and PGA drift) enabling Class 0.2 meters with standard external components
- Power quality measurements
  - Line frequency: 1 measurement per phase
  - Zero crossing detection, zero-crossing timeout
  - Phase angle measurements
- Supports current transformers (CTs) and Rogowski coil (di/dt) sensors
  - Multiple range phase/gain compensation for CTs
  - Digital integrator for Rogowski coils
- Flexible waveform buffer
  - Able to resample waveform to ensure 64 points per line cycle for ease of external harmonic analysis
  - Events can trigger waveform storage
  - Simplifies data collection for IEC 61000-4-7 harmonic analysis
- Advanced metrology feature set
  - Total active power, volt-amperes reactive (VAR), volt-amperes (VA), watthour, VAR-hour, and VA-hour
  - Fundamental VAR and VAR-hour
  - Current and voltage rms per phase (xIRMS, xVRMS)
  - Supports active energy standards: IEC 62053-21, IEC 62053-22; EN50470-3; OIML R46, ANSI C12.20
  - Supports reactive energy standards: IEC 62053-23, IEC 62053-4
- High speed communication port
- 10 MHz serial peripheral interface (SPI)

APPLICATIONS

- Polyphase meters
- Power quality monitoring
- Protective device

GENERAL DESCRIPTION

The ADE9078[1] is a highly accurate, fully integrated energy metering device. Interfacing with both current transformer (CT) and Rogowski coil sensors, the ADE9078 enables users to develop a 3-phase metrology platform, which achieves high performance for Class 1 up to Class 0.2 meters.

FUNCTIONAL BLOCK DIAGRAM

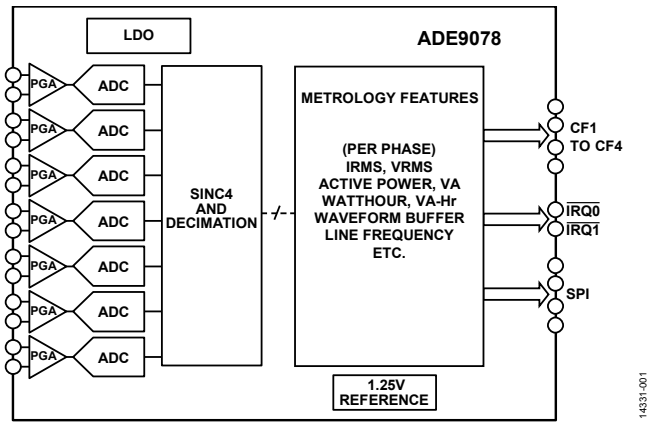

Figure 1.

The ADE9078 integrates seven high performances ADCs and a flexible DSP core. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum per channel, each of which includes a programmable gain amplifier (PGA) and ADC.

The ADE9078 offers an integrated flexible waveform buffer that stores samples at a fixed data rate or a sampling rate that varies based on line frequency to ensure 64 points per line cycle. These two options make it easy to implement harmonic analysis in an external processor according to IEC 61000-4-7.

Two power modes are provided to enable detection of meter tampering: PSM2 uses a low power comparator to compare current channels to a threshold and indicates whether it is exceeded on the $\overline{IRQ0}$ and $\overline{IRQ1}$ outputs; PSM1 enables fast measurement of current and voltage rms (xVRMS and xIRMS), active power, and VAR during a tamper.

The ADE9078 allows advanced and highly accurate energy measurements, enabling one platform to cover a wide range of meters, through a combination of various high end metrology features and superior analog performance.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; 7,558,080. Other patents are pending.

Rev. 0 Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

8/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.63 V, GND = AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz crystal (XTAL), T_{MIN} to T_{MAX} = −40°C to +85°C for minimum and maximum specifications, T_A = 25°C (typical) for typical specifications.

Table 1.[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Measurement error per phase
Total Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation; gain compensation only
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation; gain compensation only
Total Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation; gain compensation only
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation; gain compensation only
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
Fundamental Reactive		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
Active Power, VAR		0.2		%	Over a dynamic range of 5000 to 1, 1 sec accumulation
Power Factor (PF)		±0.001			Over a dynamic range of 5000 to 1
64-Point per Line Cycle Resampled Data		0.1		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the fundamental magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental on voltage channel and fundamental with ninth harmonic at half of full scale on current channel
		0.3		%	An FFT is performed to receive the magnitude response; this error is the magnitude error of ninth harmonic caused by the resampling algorithm distortion input signal is 50 Hz fundamental with ninth harmonic at half of full scale on current channel
		−72		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and ninth harmonic at half of full scale on the current channel
		3		%	An FFT is performed to receive the magnitude response; this error is the magnitude error of 31st harmonic caused by resampling algorithm distortion; input signal is 50 Hz fundamental with 31st harmonic at half of full scale on the current channel
		−38		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and 31st harmonic at half of full scale on the current channel
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Current to Current, Voltage to Voltage, and Voltage to Current Angle Measurement		0.036		Degrees	Resolution at 50 Hz; voltage and current at 1/10th of full scale
PSM1 IRMS		0.2		%	Accuracy achieved 40 ms after entering PSM1 mode at 600:1

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PSM1 Active Power		0.2		%	Accuracy achieved 40 ms after entering PSM1 mode at 600:1
PSM2 Peak Current Detection		5		%	Accuracy of current detection threshold, achieved 120 ms after entering PSM2 mode at 660:1
ADC					See the ADC section
PGA Gain Settings (GAIN)		1, 2, or 4		V/V	PGA gain setting is referred to as GAIN
Differential Input Voltage Range (VxP − VxN, IxP − IxN)	−1/GAIN		+1/GAIN	V	0.707 V rms; when V_{REF} = 1.25 V, this voltage corresponds to 53 million codes
Maximum Operating Voltage on Analog Input Pins (VxP, VxN, IxP, and IxN)	−0.6		0.6	V	Voltage on the pin with respect to ground (GND = AGND = DGND = REFGND), V_{REF} = 1.25 V
Signal-to-Noise Ratio (SNR)[2]					V_{IN} = full scale/gain; see the Terminology section
PGA = 1		101		dB	4 kSPS sinc4 + infinite impulse response (IIR) low-pass filter (LPF) output
		97		dB	16 kSPS sinc4 output
PGA = 4		97		dB	4 kSPS sinc4 + IIR LPF output
		94		dB	16 kSPS sinc4 output
Total Harmonic Distortion (THD)[2]					See the Terminology section
PGA = 1		−106		dB	4 kSPS sinc4 + IIR LPF output
		−106		dB	16 kSPS sinc4 output
PGA = 4		−115		dB	4 kSPS sinc4 + IIR LPF output
		−112		dB	16 kSPS sinc4 output
Signal-to-Noise and Distortion Ratio (SINAD)[2]					See the Terminology section
PGA = 1		100		dB	4 kSPS sinc4 + IIR LPF output
		96		dB	16 kSPS sinc4 output
PGA = 4		96		dB	4 kSPS sinc4 + IIR LPF output
		93		dB	16 kSPS sinc4 output
Spurious-Free Dynamic Range (SFDR)[2]					See the Terminology section
PGA = 1		110		dB	4 kSPS sinc4 + IIR LPF output
Output Pass Band (−0.1 dB)					See the Terminology section
Sinc4 Outputs		0.672		kHz	16 kSPS sinc4 output
Sinc4 + IIR LPF Outputs		0.672		kHz	4 kSPS output
Output Bandwidth (−3 dB)[2]					See the Terminology section
Sinc4 Outputs		3.6325		kHz	16 kSPS sinc4 output
Sinc4 + IIR LPF Outputs		1.6		kHz	4 kSPS output
Crosstalk[2]		−120		dB	See the Terminology section, at 50 Hz and 60 Hz
AC Power Supply Rejection Ratio (AC PSRR)[2]		−120		dB	See the Terminology section, at 50 Hz and 60 Hz
AC Common-Mode Rejection Ratio (AC CMRR)[2]		−115		dB	At 100 Hz and 120 Hz
Gain Error		±0.3	±1	%	See the Terminology section
Gain Drift[2]		±3		ppm/°C	See the Terminology section
Offset		±0.36	±3.8	mV	See the Terminology section
Offset Drift[2]		0	±6	µV/°C	See the Terminology section

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel Drift (PGA, ADC, Internal Voltage Reference)		±7	±25	ppm/°C	PGA = 1, internal V_{REF}
		±7	±25	ppm/°C	PGA = 2, internal V_{REF}
		±7	±25	ppm/°C	PGA = 4, internal V_{REF}
Differential Input Impedance (DC)	330	366		kΩ	See the Terminology section, PGA = 1
	160	180		kΩ	PGA = 2
	80	90		kΩ	PGA = 4
INTERNAL VOLTAGE REFERENCE					Nominal 1.25 V ±1 mV
Voltage Reference		1.250		V	T_A = 25°C, REF pin
Temperature Coefficient[2]		±5	±20	ppm/°C	T_A = −40°C to +85°C
EXTERNAL VOLTAGE REFERENCE					
External Voltage Reference Input Voltage (REF)		1.2, 1.25		V	REFGND must be tied to GND, AGND, and DGND; 1.25 V external reference is preferred; the full-scale values mentioned in this data sheet are for a voltage reference of 1.25 V
Average Reference Current		120		µA/V	
CRYSTAL OSCILLATOR					CLKIN = 12.288 MHz ± 30 ppm (see the Crystal Oscillator/External Clock section)
Input Clock Frequency	12.165	12.288	12.411	MHz	
Internal Capacitance on CLKIN and CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.5		MΩ	
Transconductance (g_m)		9		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	12.165	12.288	12.411	MHz	
Duty Cycle[2]	45:55	50:50	55:45	%	
CLKIN Logic Inputs					3.3 V tolerant
Input Voltage					
High, V_{INH}	1.2			V	V_{DD} = 2.7 V to 3.63 V
Low, V_{INL}			0.5	V	V_{DD} = 2.7 V to 3.63 V
LOGIC INPUTS					
PM0, PM1, $\overline{\text{RESET}}$, MOSI, SCLK, and $\overline{\text{SS}}$					
Input Voltage					
High, V_{INH}	2.4			V	V_{DD} = 2.7 V to 3.63 V
Low, V_{INL}			0.8	V	V_{DD} = 2.7 V to 3.63 V
Input Current, I_{IN}			15	µA	V_{IN} = 0 V
Internal Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
MISO, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$					V_{DD} = 2.97 V to 3.63 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
Internal Capacitance, C_{IN}			10	pF	
CF1, CF2, CF3, and CF4					V_{DD} = 2.97 V to 3.63 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 8 mA
Low, V_{OL}			0.8	V	I_{SINK} = 8 mA
Internal Capacitance, C_{IN}			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
MISO, $\overline{IRQ0}$, and $\overline{IRQ1}$					V_{DD} = 2.7 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 1 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
CF1, CF2, CF3, and CF4					V_{DD} = 2.7 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 3 mA
Low, V_{OL}			0.8	V	I_{SINK} = 8 mA
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	See the Power-On Sequence section
DVDD		1.7		V	
POWER SUPPLY					For specified performance
VDD	2.7	3.3	3.63	V	
Supply Current (VDD)					V_{DD} = 3.63 V
Power Save Mode 0 (PSM0)		10	12	mA	Normal mode, seven ADCs enabled
		9.5	11	mA	Normal mode, seven ADCs enabled, total reactive power computation disabled
		10.5	12	mA	Normal mode, seven ADCs enabled, waveform buffer enabled
		10	11.6	mA	Normal mode, six ADCs enabled
Power Save Mode 1 (PSM1)		9	10.6	mA	Fast rms, active power, and total reactive power measurement within 30 ms for tamper detection
Power Save Mode 2 (PSM2)		115	200	µA	Compares current to threshold, AVDD = 0 V, DVDD = 0 V
Power Save Mode 3 (PSM3)		50	200	nA	Idle, AVDD = 0 V, DVDD = 0 V

[1] Throughout this data sheet, multifunction pins, such as CF3/ZX, are referred to either by the entire pin name or by a single function of the pin, for example, CF3, when only that function is relevant.
[2] Tested during device characterization.

TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency				10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

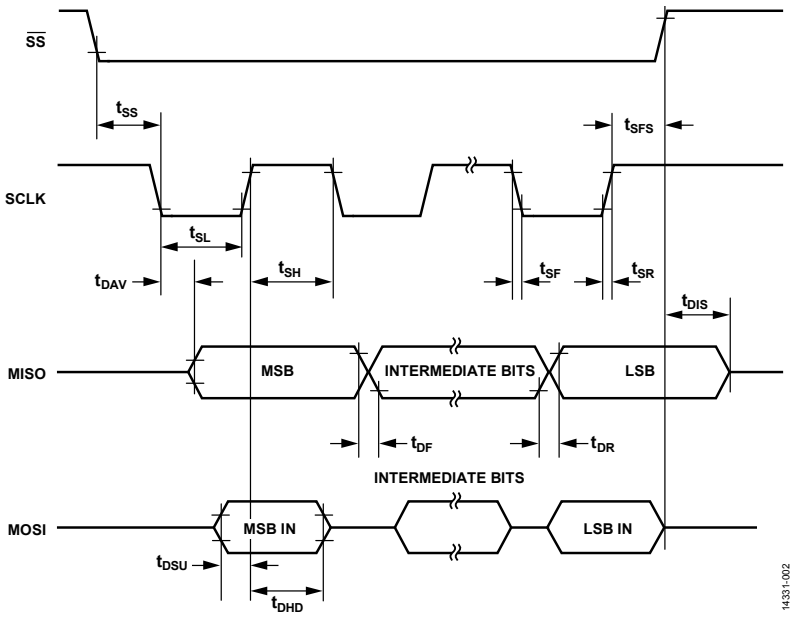


Figure 2. SPI Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +3.96 V
Analog Input Voltage to GND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN VBP, VBN, VCP, VCN	−1.9 V to +2 V
Reference Input Voltage to REFGND	−0.3 V to +2 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[1]	260°C
ESD	
Human Body Model[2]	4 kV
Machine Model[3]	200 V
Field Induced Charged Device Model (FICDM)[4]	1.25 kV

[1] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.
[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable Standard JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-7[1]	27.14	3.13	°C/W

[1] Test Condition 1: The junction to air measurement uses a 2S2P JEDEC test board with 4 × 4 standard JEDEC vias. The junction to case measurement uses a 1S0P JEDEC test board with 4 × 4 standard JEDEC vias. See JEDEC standard JESD51-2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

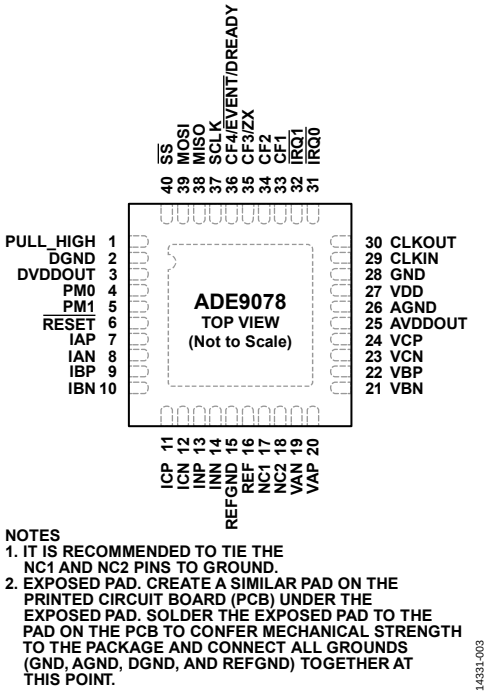


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PULL_HIGH	Pull High. Tie this pin to VDD.
2	DGND	Digital Ground. This pin provides the ground reference for the digital circuitry in the ADE9078. Because the digital return currents in the ADE9078 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
3	DVDDOUT	1.8 V Output of the Digital Low Dropout Regulator (LDO). Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor.
4	PM0	Power Mode Pin 0. PM0, combined with PM1, defines the power mode. For normal operation, PM0 and PM1 must be grounded (see the Power Modes section).
5	PM1	Power Mode Pin 1. PM1 combined with PM0, defines the power mode. For normal operation, PM0 and PM1 must be grounded (see the Power Modes section).
6	$\overline{\text{RESET}}$	Reset Input, Active Low. This pin must stay low for at least 1 µs to trigger a hardware reset.
7, 8	IAP, IAN	Analog Inputs, Channel IA. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
9, 10	IBP, IBN	Analog Inputs, Channel IB. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
11, 12	ICP, ICN	Analog Inputs, Channel IC. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
13, 14	INP, INN	Analog Inputs, Channel IN. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
15	REFGND	Ground Reference, Internal Voltage Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
16	REF	Voltage Reference. The REF pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. An external reference of 1.2 V to 1.25 V can also be connected at this pin. In either case, decouple REF to REFGND with 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor. After reset, the on-chip reference is enabled. To use the internal voltage reference with external circuits, a buffer is required. The full-scale values mentioned in this data sheet are for a voltage reference of 1.25 V.
17	NC1	No Connection. It is recommended to tie this pin to ground.
18	NC2	No Connection. It is recommended to tie this pin to ground.

Pin No.	Mnemonic	Description
19, 20	VAN, VAP	Analog Inputs, Channel VA. The VAP (positive) and VAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
21, 22	VBN, VBP	Analog Inputs, Channel VB. The VBP (positive) and VBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
23, 24	VCN, VCP	Analog Inputs, Channel VC. The VCP (positive) and VCN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
25	AVDDOUT	1.9 V Output of the Analog Low Dropout Regulator (LDO). Decouple AVDDOUT with a 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor. Do not connect external active circuitry to this pin.
26	AGND	Analog Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
27	VDD	Supply Voltage. The VDD pin provides the supply voltage. Decouple VDD to GND with a ceramic 0.1 µF capacitor in parallel with a ceramic 10 µF capacitor.
28	GND	Supply Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
29	CLKIN	Crystal/Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. See the Crystal Selection section for details on choosing a suitable crystal. Alternatively, an external clock can be provided at this logic input.
30	CLKOUT	Crystal Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. When using CLKOUT to drive external circuits, connect an external buffer. When using an external clock on CLKIN, leave CLKOUT unconnected.
31	$\overline{\text{IRQ0}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
32	$\overline{\text{IRQ1}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
33	CF1	Calibration Frequency (CF) Logic Output 1. The CF1, CF2, CF3, and CF4 outputs provide power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers (see the Digital to Frequency Conversion—CFx Output section).
34	CF2	CF Logic Output 2. This pin indicates CF2.
35	CF3/ZX	CF Logic Output 3/Zero Crossing. This pin indicates CF3 or zero crossing.
36	CF4/$\overline{\text{EVENT}}$/DREADY	CF Logic Output 4/Event Pin/Data Ready. This pin indicates CF4, events, or when new data is ready.
37	SCLK	Serial Clock Input for the SPI Port. All serial data transfers synchronize to this clock (see the Accessing On-Chip Data section). The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
38	MISO	Data Output for the SPI Port.
39	MOSI	Data Input for the SPI Port.
40	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EP	Exposed Pad. Create a similar pad on the printed circuit board (PCB) under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package and connect all grounds (GND, AGND, DGND, and REFGND) together at this point.

TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.005% or 0.02% of full scale and with a frequency of 50 Hz; integrator off.

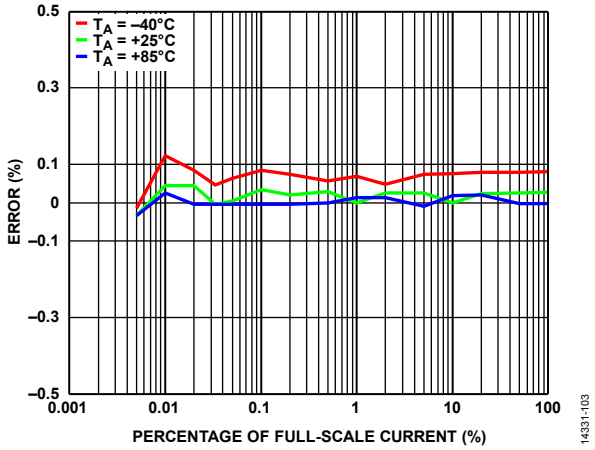


Figure 4. Total Active Energy Error as a Percentage of Reading over Temperature, PF = 1

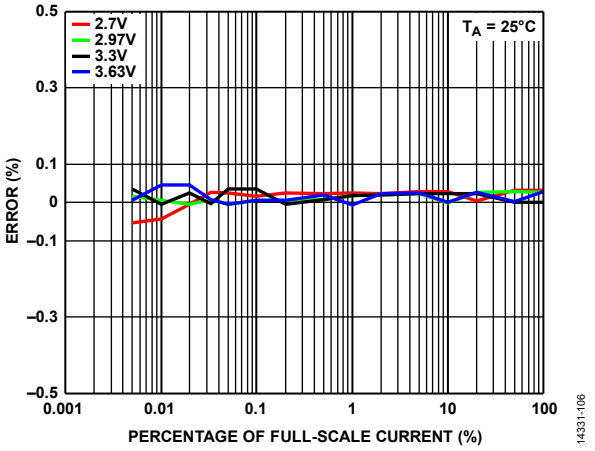


Figure 7. Total Active Energy Error as a Percentage of Reading over Supply Voltage, PF = 1, T_A = 25°C

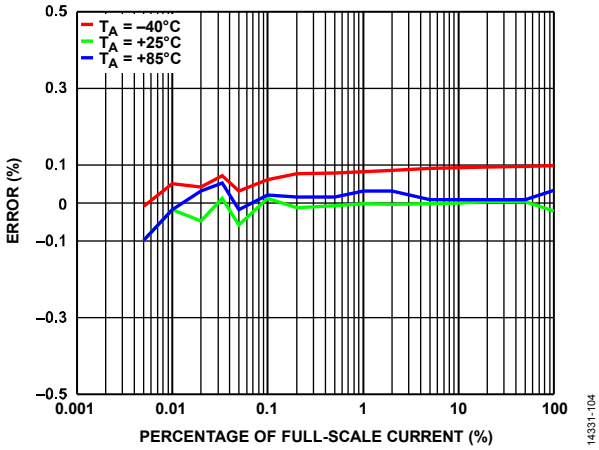


Figure 5. Total Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

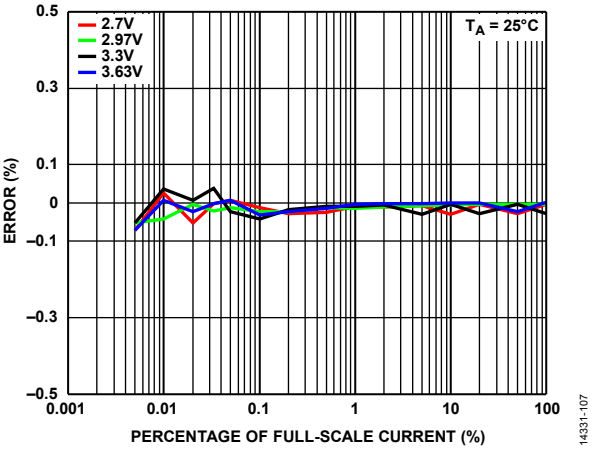


Figure 8. Total Reactive Energy Error as a Percentage of Reading over Supply Voltage, PF = 0, T_A = 25°

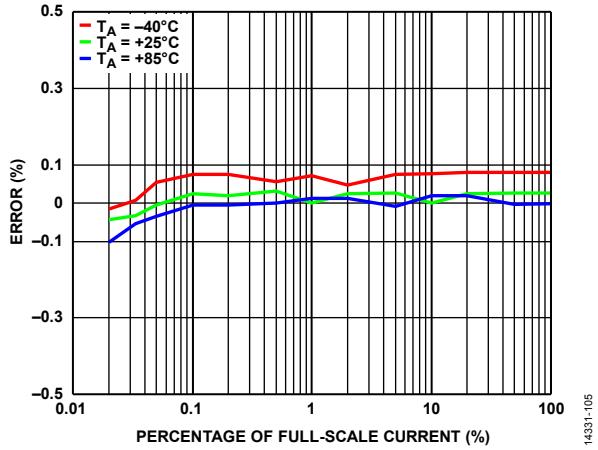


Figure 6. Total Apparent Energy Error as a Percentage of Reading over Temperature, PF = 1

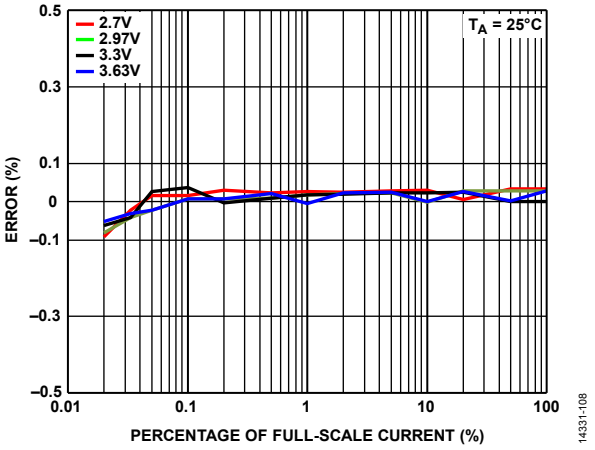


Figure 9. Total Apparent Energy Error as a Percentage of Reading over Supply Voltage, PF = 1, T_A = 25°

FUNDAMENTAL ENERGY LINEARITY WITH FIFTH HARMONIC OVER SUPPLY AND TEMPERATURE

Fundamental voltage component in phase with fifth harmonic; current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.005% of full scale and a fifth harmonic with a constant amplitude of 40% of fundamental; integrator off.

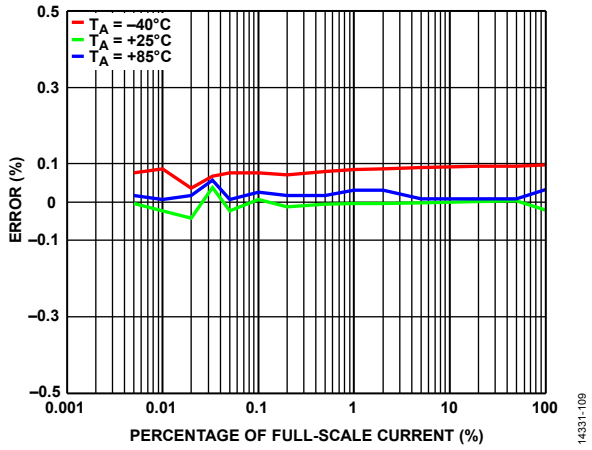


Figure 10. Fundamental Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

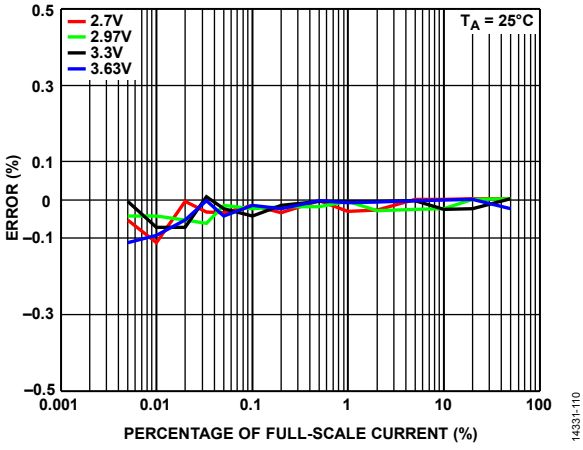


Figure 11. Fundamental Reactive Energy Error as a Percentage of Reading over Supply Voltage, PF = 0, T_A = 25°

TOTAL ENERGY ERROR OVER FREQUENCY

Sinusoidal voltage with a constant amplitude of 50% of full scale; sinusoidal current with a constant amplitude of 10% of full scale; variable frequency between 45 Hz and 65 Hz; integrator off.

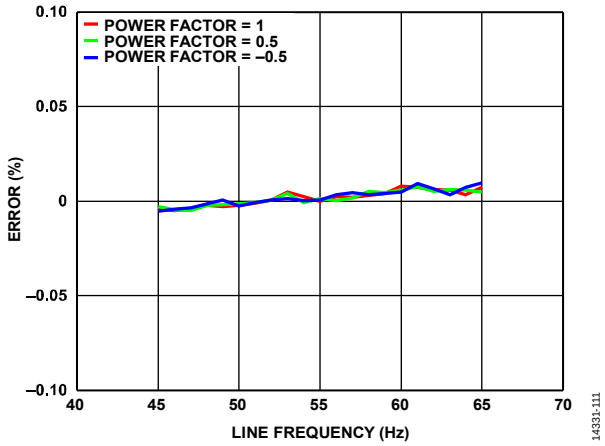


Figure 12. Total Active Energy Error as a Percentage of Reading vs. Line Frequency, PF = –0.5, +0.5, and +1

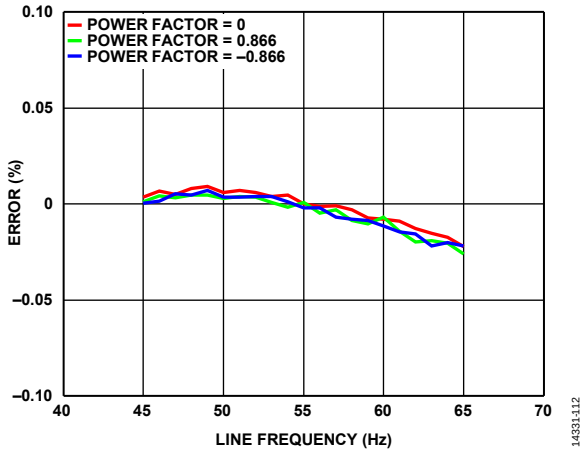


Figure 13. Total Reactive Energy Error as a Percentage of Reading vs. Line Frequency, PF = –0.866, 0, and +0.866

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

Sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.02% of full scale using a frequency of 50 Hz; variable frequency between 45 Hz and 65 Hz; sinusoidal current amplitude of 10% of full scale and voltage amplitude of 50% of full scale; integrator off.

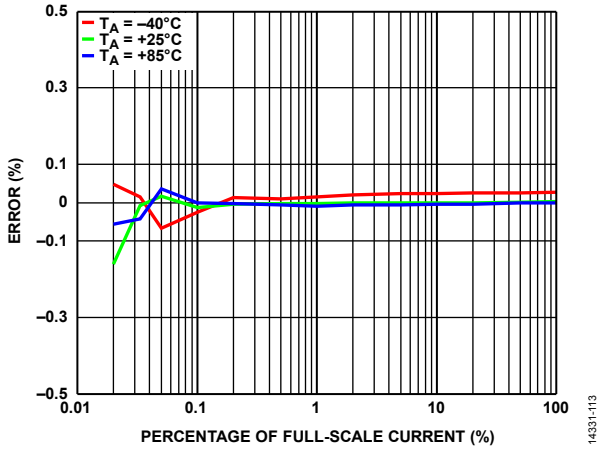


Figure 14. Current RMS Error as a Percentage of Reading over Temperature

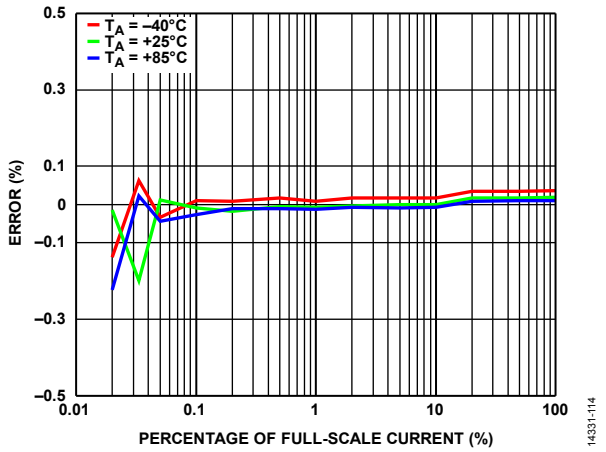


Figure 15. Voltage RMS Error as a Percentage of Reading over Temperature

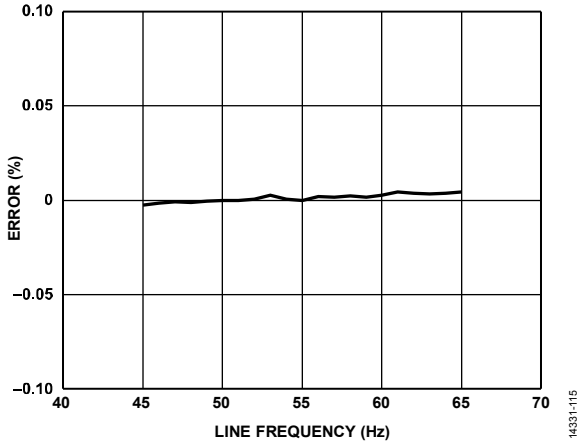


Figure 16. Current RMS Error as a Percentage of Reading vs. Line Frequency

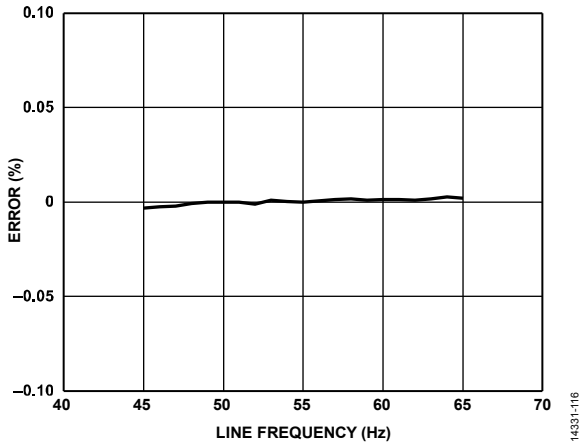


Figure 17. Voltage RMS Error as a Percentage of Reading vs. Line Frequency

ENERGY LINEARITY REPEATABILITY

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.005% of full scale and with a frequency of 50 Hz. For Figure 20, besides the fundamental component, the voltage contained a fifth harmonic with a constant amplitude of 40% of fundamental, and the current contained a fifth harmonic with a constant amplitude of 40% of fundamental. Integrator off. Measurements at 25°C repeated 30 times.

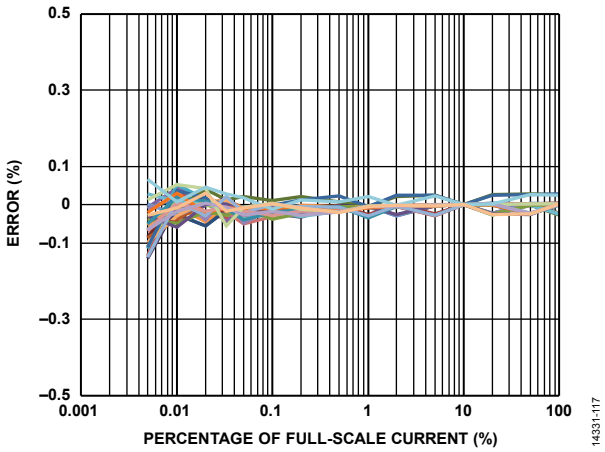


Figure 18. Total Active Energy Error as a Percentage of Reading, PF = 1 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

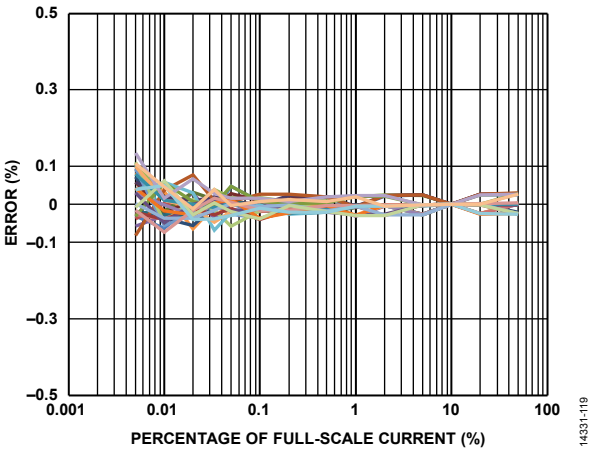


Figure 20. Fundamental Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

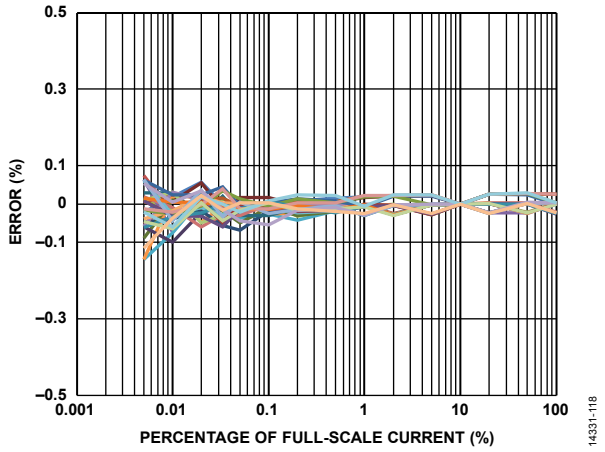


Figure 19. Total Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

TOTAL ENERGY AND RMS LINEARITY WITH INTEGRATOR ON

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; gain of current channel set to 4; sinusoidal current with variable amplitudes from 100% of full scale down to 0.05% or 0.1% of full scale and with a frequency of 50 Hz; full scale at gain of 4 = (full scale at gain of 1)/4, high-pass corner frequency of 4.97 Hz.

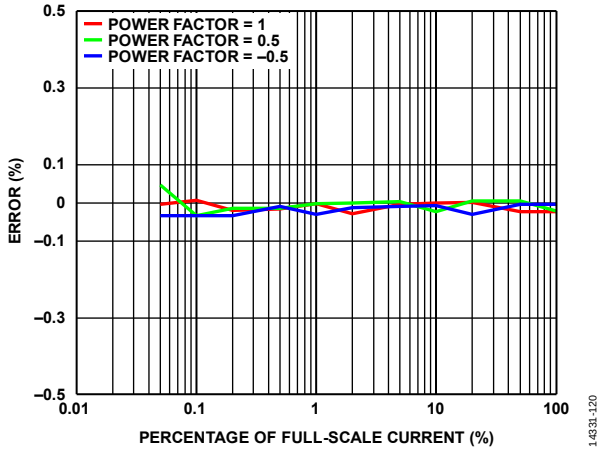


Figure 21. Total Active Energy Error, Gain = 4, Integrator On

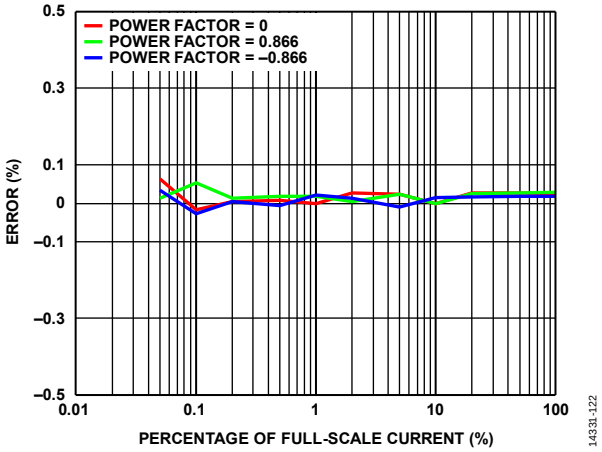


Figure 23. Total Apparent Energy Error, Gain = 4, Integrator On

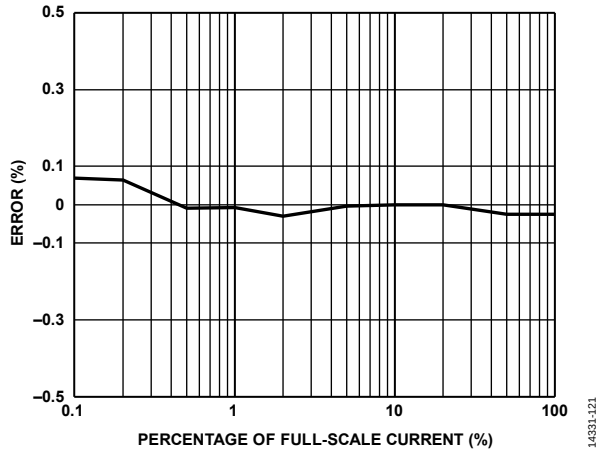


Figure 22. Total Reactive Energy Error, Gain = 4, Integrator On

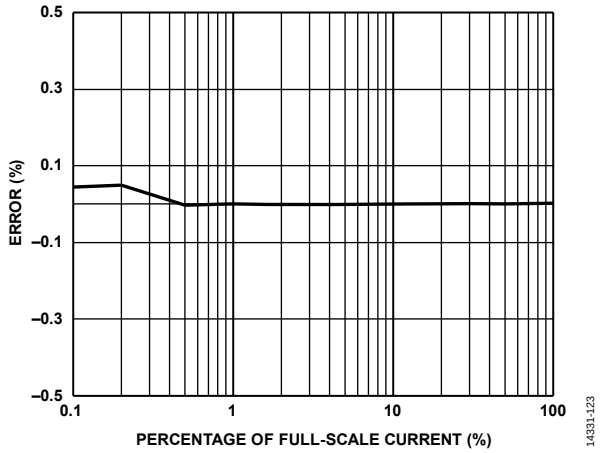


Figure 24. Total RMS Current Error, Gain = 4, Integrator On

TOTAL ENERGY ERROR OVER FREQUENCY WITH INTEGRATOR ON

Sinusoidal voltage with a constant amplitude of 50% of full scale; gain of current channel set to 4; sinusoidal current with a constant amplitude of 10% of full scale; variable frequency between 45 Hz and 65 Hz, gigh-pass corner frequency of 4.97 Hz.

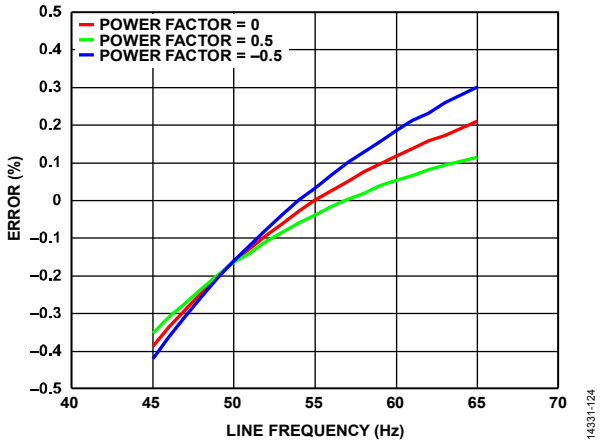


Figure 25. Total Active Energy Error as a Percentage of Reading vs. Line Frequency, Gain = 4, Integrator On

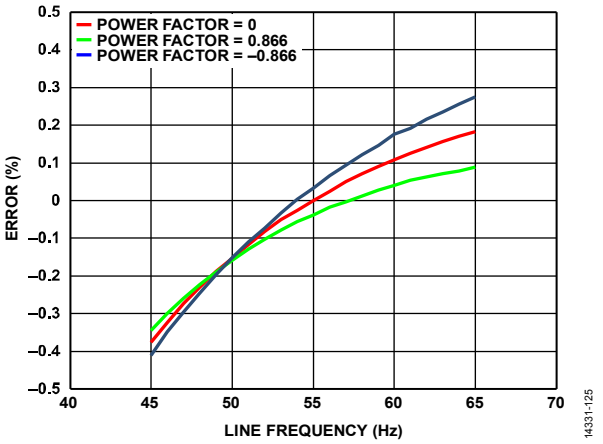


Figure 26. Total Reactive Energy Error as a Percentage of Reading vs. Line Frequency, Gain = 4, Integrator On

TEST CIRCUIT

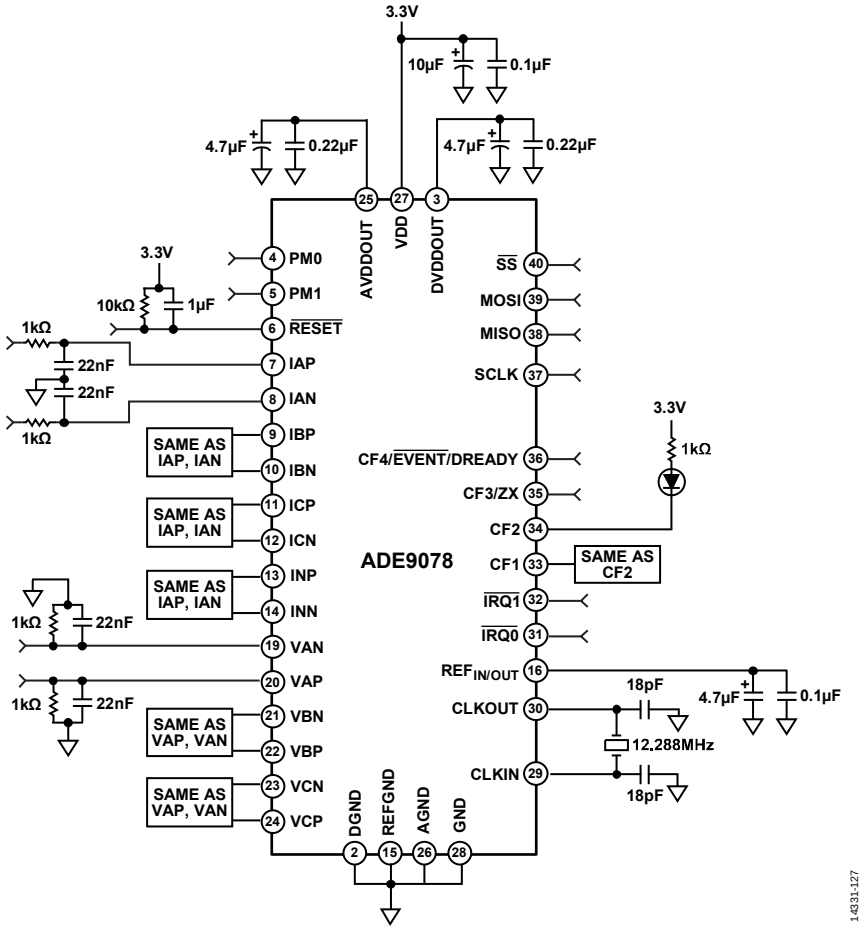


Figure 27. Test Circuit

TERMINOLOGY

Differential Input Voltage Range and Maximum Operating Voltage on VxP, VxN, IxP, and IxN Analog Input Pins

The differential input range describes the maximum difference between the IxP and IxN or VxP and VxN pins. The maximum operating voltage given in Table 1 describes the maximum voltage that can be present on each pin, including any common-mode voltage. Figure 28 illustrates the maximum input between xP and xM, which is seen in the application when a current transformer with center tapped burden resistor is used. Figure 29 illustrates the maximum input voltage range between xP and xN when a pseudo differential input is applied, as is commonly seen when sensing the line voltage.

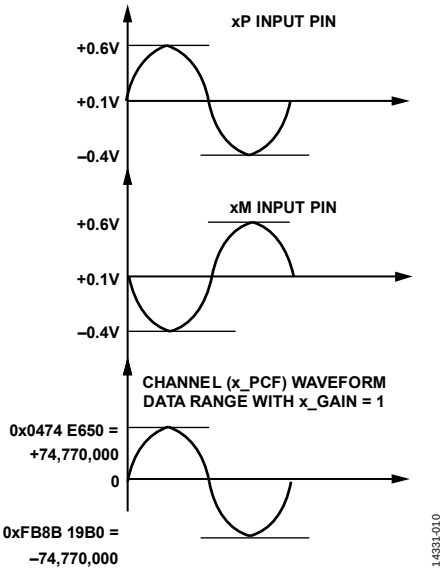


Figure 28. Maximum Input Signal with Differential Antiphase Input with Common-Mode Voltage = 0.1 V Gain = 1

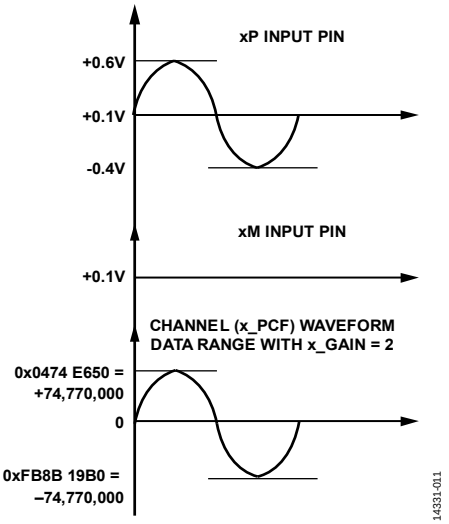


Figure 29. Maximum Input Signal with Pseudo Differential Input with Common-Mode Voltage = 0.1 V, Gain = 2 (x_GAIN = 2)

Crosstalk

Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 60 Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 100 sec. Crosstalk is expressed in decibels.

Differential Input Impedance (DC)

The differential input impedance represents the impedance between the pair IxP and IxN or VxP and VxN. It varies with the PGA gain selection as indicated in Table 1.

ADC Offset

ADC offset is the difference between the average measured ADC output code with both inputs connected to GND and the ideal ADC output code of zero. ADC offset is expressed in microvolts.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. The offset drift over temperature is computed as follows:

$$Drift = \max\left(\left|\frac{Offset(-40°C) - Offset(25°C)}{(-40°C - 25°C)}\right|, \left|\frac{Offset(85°C) - Offset(25°C)}{(85°C - 25°C)}\right|\right)$$

Offset drift is expressed in μV/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.2 V is used (see the Voltage Reference section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one channel.

Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain while using an external voltage reference of 1.2 V. It represents the overall temperature coefficient of one current or voltage channel. With an external voltage reference of 1.2 V in use, the ADC gain is measured at −40°C, +25°C, and +85°C. Then the temperature coefficient is computed as follows:

$$Drift = \max\left(\left|\frac{Gain(-40°C) - Gain(25°C)}{Gain(25°C) \times (-40°C - 25°C)}\right|, \left|\frac{Gain(85°C) - Gain(25°C)}{Gain(25°C) \times (85°C - 25°C)}\right|\right)$$

Gain drift is measured in ppm/°C.

AC Power Supply Rejection (PSRR)
AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is V_{NOM} and modulated with ac and the inputs are grounded. For the ac PSRR measurement, 20 sec of samples is captured with nominal supplies (3.3 V) and a second set are captured with an additional ac signal (330 mV peak at 50 Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = 20 $\log_{10}$(V2/V1).

Signal-to-Noise Ratio (SNR)
SNR is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SINAD, the signal at 50 Hz is compared to the sum of the power from all the other frequencies. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the THD, the amplitudes of the 50 Hz harmonics up to the bandwidth are root sum squared. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SFDR, the amplitude of the largest signal that is not a harmonic of 50 Hz is recorded. The value for SFDR is expressed in decibels.

ADC Output Pass Band
The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

ADC Output Bandwidth
The ADC output bandwidth is the bandwidth within −3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

THEORY OF OPERATION

The ADE9078 integrates seven high performance ADCs and a flexible DSP core. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum for the whole channel including PGA and ADC.

The ADE9078 is a highly accurate, fully integrated energy metering device. Interfacing with both CT and Rogowski coil sensors, the ADE9078 enables users to develop a 3-phase metrology platform, which achieves high performance for Class 1 through Class 0.2 meters. See the Measurements (Normal Mode) section for more information.

Two power modes are provided to enable detection of meter tampering: PSM2 uses a low power comparator to compare current channels to a threshold and indicates whether it has been exceeded on the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ outputs; PSM1 enables fast measurement of current and voltage rms (xVRMS, xIRMS), active power, and VAR during a tamper. See the Measurements (PSM1) section and Measurements (PSM2) section for more information about how to use these modes.

ADC

Overview

The ADE9078 incorporates seven independent, second-order, Σ-Δ ADCs that sample simultaneously. Each ADC is 24 bits and supports fully differential and pseudo differential inputs that can go above and below ground. The ADE9078 includes a low noise, low drift, internal band gap reference. Set the EXT_REF bit in the CONFIG1 register if using an external voltage reference. Each ADC contains a programmable gain amplifier, which allows a gain of 1, 2, or 4. The ADCs incorporate proprietary dither techniques to prevent idle tones at low input levels, extending the accuracy range.

Analog Input Configuration

There is no internal buffering on the device. The impedance of the ADE9078 depends on the programmable gain selected (see the Specifications table).

Fully Differential Inputs

The input signals on the IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, and VCN pins must not exceed 0.6 V relative to AGND, the analog ground reference. The differential full-scale input range of the ADCs is ±1 V peak (0.707 V rms), and the maximum allowed common-mode voltage at the ADC pins must not exceed ±0.1 V.

Figure 30 and Figure 31 show two common types of input signals for an energy metering application. Figure 30 shows the maximum input allowed with differential antiphase signals. A current transformer with center tapped burden resistor generates differential antiphase signals. Figure 31 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the mains voltage signal through a resistive divider or using a Rogowski coil current sensor.

The following conditions must be met for the input signals with gain = 1:

- |IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, and VCN| ≤ 0.6 V peak relative to AGND
- |IxP − IxN| ≤ 1 V peak, |VxP − VxN| ≤ 1 V peak

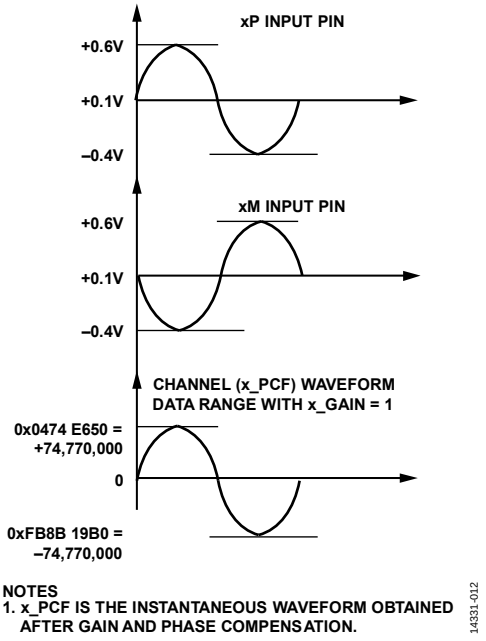


Figure 30. Maximum Input Signal with Differential Antiphase Input with Common-Mode Voltage = 0.1 V, Gain = 1

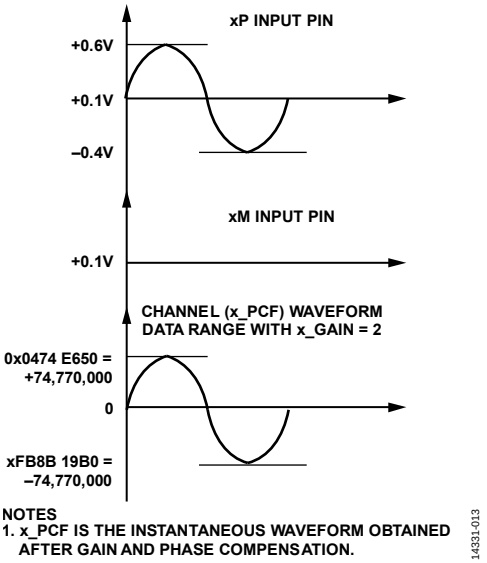


Figure 31. Maximum Input Signal with Pseudo Differential Input with Common-Mode Voltage = 0.1 V, Gain = 2

Each ADC contains a programmable gain amplifier that allows a gain of 1, 2, or 4. The ADC produces full-scale output codes with an input of ±1 V. With a gain of 1, this full-scale input corresponds to a differential antiphase input of 0.707 V rms, as shown in Figure 30. At a gain of 2, full-scale output codes are produced with an input of 0.353 V rms, as shown in Figure 31. At a gain

of 4, full-scale output codes are generated with a 0.1765 V rms input signal. Note that the voltages on the xP and xN pins must be within ±0.6 V as described in this section and Table 1.

Write the x_GAIN bits in the PGA_GAIN register to configure the gain for each channel.

Interfacing to Current and Voltage Sensors

Figure 32 and Figure 34 show the typical circuits to connect to current transformer and Rogowski coil current sensors. Figure 33 shows the typical interface circuit to measure the mains voltage.

The antialiasing filter corner is chosen to be around 7 kHz to provide sufficient attenuation of out of band signals near the modulator clock frequency. The same RC filter corner is used on voltage channels, as well, to avoid phase errors between current and voltage signals. Note that the Rogowski coil (that is, a di/dt sensor) input network has a second-order antialiasing filter. The integrator used in conjunction to the Rogowski coil has a −20 dB/dec attenuation and an approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response is a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it, and it generates significant high frequency noise. An antialiasing filter of at least the second order is required to avoid noise aliasing back in the band of interest when the ADC is sampling. See Figure 34 for the recommended antialiasing filter.

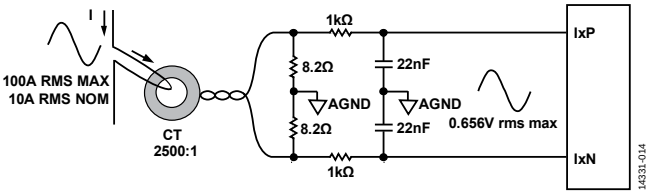


Figure 32. Application Circuit with a Current Transformer Current Sensor

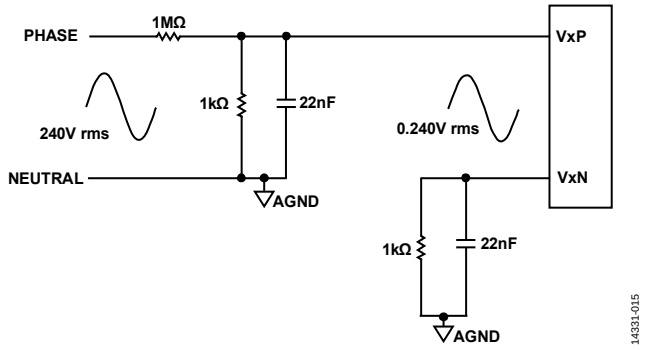


Figure 33. Application Circuit with Voltage Sensed Through Resistor Divider

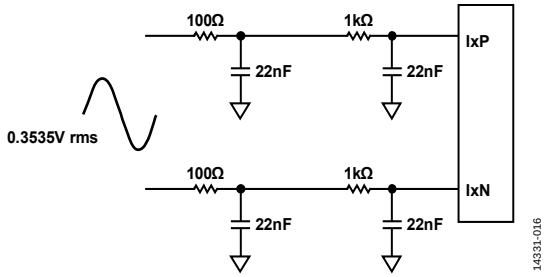


Figure 34. Application Circuit with Rogowski Coil Current Sensor

Internal RF Immunity Filter

Energy metering applications require the meter to be immune to external radio frequency fields of 30 V/m, from 80 MHz to 10 GHz, according to IEC 61000-4-3. The ADE9078 has internal antialiasing filters to improve performance in testing because it is difficult to filter these signals externally. The second-order, internal low-pass filter has a corner frequency of 10 MHz. Note that external antialias filters are required to attenuate frequencies above 7 kHz, as shown in the Interfacing to Current and Voltage Sensors section.

Modes of Operation

Each ADC has two modes of operation: normal mode and disabled mode.

In the normal mode, the ADCs turn on and sample continuously. Use the CHNL_DIS register to disable the ADCs individually.

Four different power modes are available in the ADE9078 (see the Power Modes section). All ADCs turn on during the PSM0 power mode. In the PSM1 power mode, all of the ADCs except for the neutral current ADC are turned on. In PSM2 mode and PSM3 mode, all ADCs are disabled and cannot be turned on.

Table 6. ADC Operation in PSMx Power Modes

PSMx Power Mode	ADC Mode of Operation
PSM0	Normal (on)
PSM1	IA, IB, IC, VA, VB, VC: normal (on) IN: disabled (always off)
PSM2	Disabled (always off)
PSM3	Disabled (always off)

Output Data Rates and Format

When a conversion is complete, the DREADY bit of the STATUS0 register is set to 1. If the CF4_CFG bits in the CONFIG1 register are equal to 11, the CF4/$\overline{\text{EVENT}}$/DREADY pin corresponds to DREADY and pulses high to indicate when seven new ADC results are ready. Note that the DREADY update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.

For the ADE9078, the modulator sampling rate (MODCLK) is fixed at 1.024 MHz (CLKIN/12 = 12.288 MHz/12). The output data rate of the sinc4 filter is 16 kHz (SINC_ODR = MODCLK/64), whereas the low-pass filter/decimator stage yields an output rate four times slower than the sinc4 filter output rate (SINC_ODR). Figure 35 shows the digital filtering, which takes the 1.024 MHz ADC samples and creates waveform information at a decimated rate of 16 kHz or 4 kHz.

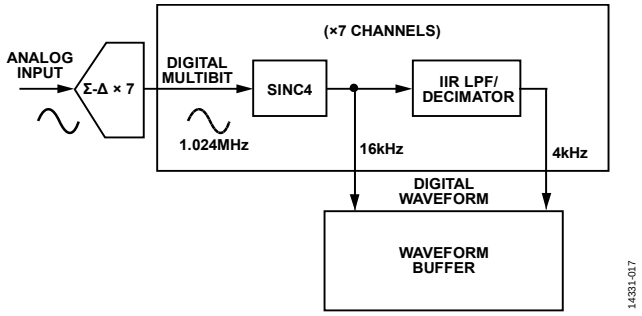


Figure 35. Datapath Following ADC Stage

The output data rates are summarized in Table 7.

Table 7. Output Data Rates

Parameter	Data Rate
CLKIN Frequency	12.288 MHz
ADC Modulator Clock, MODCLK	1.024 MHz
Sinc4, SINC_ODR	16 kHz
Low-Pass Filter	4 kHz
Bandwidth (Pass Band)	0.672 kHz

The ADC data in the waveform buffer is stored as 32-bit data by shifting left by 4 bits and sign extending, as shown in Figure 36.

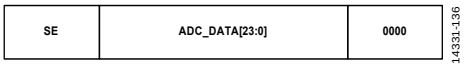


Figure 36. Format for the ADC Data Stored in the Waveform Buffer, x_SINC_DAT and x_LPF_DAT Registers

The expected output code from the sinc4 filter when input is at 1 V peak is 4,190,000 decimal (d), which corresponds to a value of 67,110,000d in the waveform buffer. The expected output code from the decimator filter when input is at 1 V peak is 4,660,000d, which corresponds to a value of 74,520,000d in the waveform buffer (see the Waveform Buffer section for more information).

Voltage Reference

The ADE9078 supports a 1.25 V internal reference. The temperature drift of the reference voltage is ±5 ppm/°C typical, ±20 ppm/°C maximum. An external reference can be connected between the REF and REFGND pins. Set the EXT_REF bit of the CONFIG1 register when using an external voltage reference, which disables the internal reference buffer.

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

The ADE9078 contains a crystal oscillator. Alternatively, a digital clock signal can be applied at the CLKIN pin of the ADE9078.

When a crystal is used as the clock source for the ADE9078, attach the crystal and the ceramic capacitors, with capacitances of C_{L1} and C_{L2}, as shown in Figure 37. It is not recommended to attach an external feedback resistor in parallel to the crystal.

When a digital clock signal is applied at the CLKIN pin, the inverted output is available at the CLKOUT pin. This output is not buffered internally and cannot drive any other external devices directly. Note that CLKOUT is available in the PSM0 and PSM1 operating modes only.

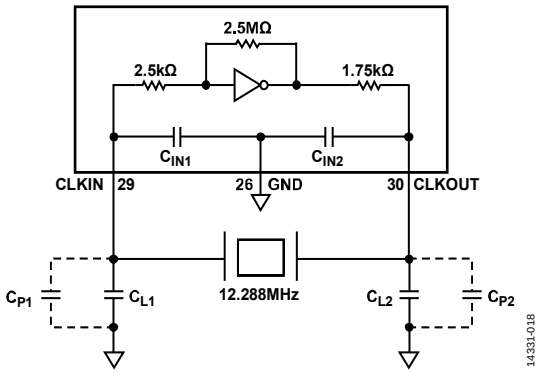


Figure 37. Crystal Application Circuit

Crystal Selection

The transconductance of the crystal oscillator circuit in the ADE9078, g_m, is provided in Table 1. It is recommended to have three to five times more g_m than the calculated $g_{mCRITICAL}$ for the crystal.

The following equation shows how to calculate the $g_{mCRITICAL}$ for the crystal from information given in the crystal data sheet:

$$g_{mCRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK\,(Hz)})^2 \times (C0 + C_L)^2$$

where:

$g_{mCRITICAL}$ is the minimum gain required to start the crystal in mA/V.
ESR_{MAX} is the maximum electrical series resistance (ESR), expressed in Ω.
$f_{CLK\,(Hz)}$ is 12.288 MHz, expressed in Hz as 12.288×10^6.
$C0$ is the maximum shunt capacitance, expressed in farads.
C_L is the total load capacitance, expressed in farads.

Crystals with low ESR and smaller load capacitance have a lower $g_{mCRITICAL}$ and are easier to drive.

The evaluation board of the ADE9078 uses a crystal manufactured by Abracon (ABLS-12.288MHZ-L4Q-T), which has a maximum ESR of 50 Ω, a load capacitance of 18 pF, and a maximum shunt capacitance of 7 pF, which results in a $g_{mCRITICAL}$ of 0.75 mA/V, as follows:

$$g_{mCRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK\,(Hz)})^2 \times (C0 + C_L)^2$$

$$g_{mCRITICAL} = 4 \times 50 \times 1000 \times (2\pi \times 12.288 \times 10^6)^2 \times (7 \times 10^{-120} + 18 \times 10^{-12})^2 = 0.75 \text{ mA/V}$$

The gain of the crystal oscillator circuit in the ADE9078, the g_m, provided in Table 1 is more than $5 \times g_{mCRITICAL}$; thus, there is sufficient margin to start up this crystal.

Load Capacitor Calculation

Crystal manufacturers specify the combined load capacitance across the crystal, C_L. The capacitances in Figure 37 can be described as follows:

- C_{P1} and C_{P2} are the parasitic capacitances on the clock pins formed due to PCB traces.
- C_{IN1} and C_{IN2} are the internal capacitances of the CLKIN and CLKOUT pins, respectively.
- C_{L1} and C_{L2} are the selected load capacitors to reach the correct combined C_L for the crystal.

The internal pin capacitances, C_{IN1} and C_{IN2}, are 4 pF each, as given in Table 1. To find the values of C_{P1} and C_{P2}, measure the capacitance on each of the clock pins of the PCB, CLKIN, and CLKOUT, respectively, with respect to the AGND pin. If the measurement is performed after soldering the IC to the PCB, subtract the 4 pF internal capacitance of the clock pins to determine the actual value of parasitic capacitance on each of the crystal pins.

To select the appropriate capacitance value for the ceramic capacitors, calculate C_{L1} and C_{L2}, from the following expression:

$$C_L = ((C_{L1} + C_{P1} + C_{IN1}) \times (C_{L2} + C_{P2} + C_{IN2}))/(C_{L1} + C_{P1} + C_{IN1} + C_{L2} + C_{P2} + C_{IN2}) \quad (1)$$

Select C_{L1} and C_{L2} such that the total capacitance on each clock pins is equal:

$$C_{L1} + C_{P1} + C_{IN1} = C_{L2} + C_{P2} + C_{IN2} \quad (2)$$

Using Equation 1 and Equation 2, the values of C_{L1} and C_{L2} can be calculated.

Load Capacitor Calculation Example

If a crystal with load capacitance specification of 12 pF is selected, and the measured parasitic capacitances from the PCB traces are $C_{P1} = C_{P2} = 2$ pF, Equation 1 implies,

$$C_L = ((C_{L1} + C_{P1} + C_{IN1}) \times (C_{L2} + C_{P2} + C_{IN2}))/(C_{L1} + C_{P1} + C_{IN1} + C_{L2} + C_{P2} + C_{IN2})$$

$$12 \text{ pF} = ((C_{L1} + 2 \text{ pF} + 4 \text{ pF}) \times (C_{L2} + 2 \text{ pF} + 4 \text{ pF}))/(C_{L1} + 2 \text{ pF} + 4 \text{ pF} + C_{L2} + 2 \text{ pF} + 4 \text{ pF})$$

Assuming $C_{L1} = C_{L2}$, to satisfy Equation 2,

$$12 \text{ pF} = ((C_{L1} + 6 \text{ pF}) \times (C_{L1} + 6 \text{ pF}))/(C_{L1} + 6 \text{ pF} + C_{L1} + 6 \text{ pF})$$

$$12 \text{ pF} = ((C_{L1} + 6 \text{ pF}) \times (C_{L1} + 6 \text{ pF}))/(2 \times (C_{L1} + 6 \text{ pF}))$$

$$12 \text{ pF} = (C_{L1} + 6 \text{ pF})/2$$

Thus, $C_{L1} = C_{L2} = 18$ pF.

Based on this example, 18 pF ceramic capacitors are selected for C_{L1} and C_{L2}. The user must verify the customized values based on careful investigations on multiple devices over the temperature range.

POWER MANAGEMENT

Power Modes

The ADE9078 offers four operating modes: PSM0, PSM1, PSM2, and PSM3. The entry into the power modes is controlled by the PM1 and PM0 pins. These pins are checked continuously to determine which operating mode to enter. Table 8 shows the PMx pin configurations for each power mode.

Most applications use PSM0 (normal mode). If the user wants to put the ADE9078 into a low power reset state, use PSM3.

PSM1 and PSM2, in combination with PSM3, enable low power tamper detection and measurement, which is required in some regions. These operating modes enable the user to check for a tamper condition while minimizing power consumption—because in tamper scenarios, a battery typically powers the ADE9078.

The current peak detection mode, PSM2, checks if the input currents are above a user set amplitude. The tamper measurement mode, PSM1, allows the user to make key measurements quickly for IRMS, VRMS, active power, and VAR with a reduced power consumption compared to PSM0.

In the application, the host microcontroller creates a duty cycle that puts the ADE9078 into PSM2, waits the required time to receive a result indicated in Table 8, and then returns to PSM3. This cycle continues once per minute until the tamper checking cycle ends, which may be up to seven days in some applications. If a tamper is detected in PSM2, PSM1 is entered and the key measurements are made. After the time required for measurements has elapsed, the host microcontroller reads the results via the SPI interface and changes the PM1 and PM0 pins to put the device back into PSM3. This cycle continues once per minute until the tamper checking cycle ends, which may be up to seven days in some applications. Figure 38 shows the functions available in PSM2 and PSM1.

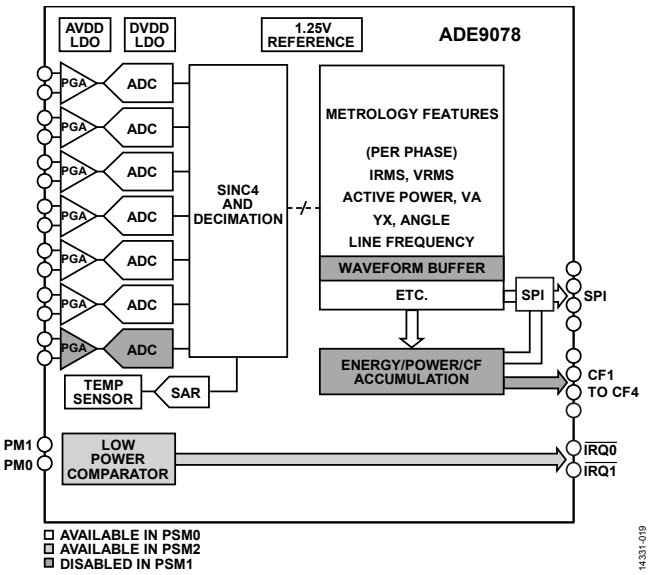


Figure 38. Functions Available in PSM1 and PSM2

As indicated in Table 8, the SPI is not available in PSM2. To check whether the current inputs are above the user configured tamper threshold, check the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins (see the Measurements (PSM2) section for more information).

One register is retained during PSM2 and PSM3: PSM2_CFG, as shown in Table 8. Note that if PSM0 or PSM1 is entered, PSM2_CFG returns to it default value and must be rewritten before reentering PSM2 (see the Measurements (Normal Mode) section, Measurements (PSM1) section, and Measurements (PSM2) section for details on functionality in PSM0, PSM1, and PSM2).

Table 8. Power Modes (PSM0, PSM1, PSM2, and PSM3)

PSMx Power Mode	Description	PM1 Pin	PM0 Pin	Power Consumption	Functions Available	SPI Available	Retained Registers When Switching into Power Mode
PSM0	Normal mode	0	0	10 mA	All functions.	Yes	Not applicable
PSM1	Tamper measurement mode	0	1	9 mA	Active and reactive power, IRMS, VRMS, all calculated using the PSM1 computation method. ZX, period, and angle measurements are available. The neutral current channel, waveform buffer, and energy/power/CF accumulations are disabled.	Yes	Not applicable
PSM2	Current peak detect mode	1	0	115 µA	Current peak detect.	No	PSM2_CFG
PSM3	Idle	1	1	50 nA	None.	No	PSM2_CFG

Power-On Sequence

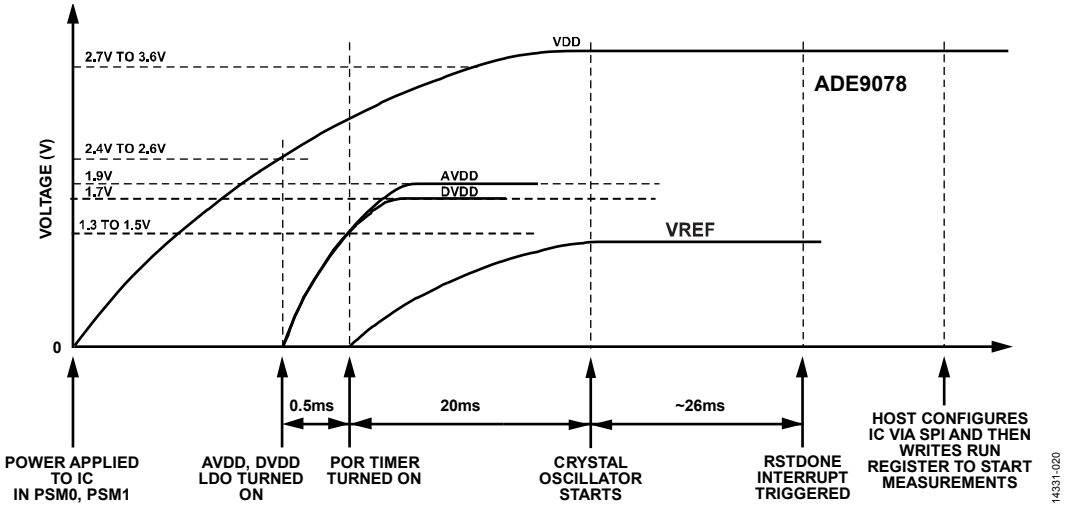


Figure 39. Power-On Sequence for PSM0 and PSM1

After power is applied to the VDD pin of the ADE9078, the device checks the state of the PM0 and PM1 pins to check the power supply mode (see the Power Modes section for more information). If in PSM1 or PSM0 (PM1, PM0 = 00 or 01) and if the $\overline{\text{RESET}}$ pin is high, the AVDD and DVDD LDOs turn on after VDD reaches 2.4 V to 2.6 V. If the $\overline{\text{RESET}}$ pin is low, the AVDD and DVDD LDOs are not turned on. Note that a clamp limits the current used to charge the AVDD and DVDD LDOs to approximately 17 mA per LDO. The power supply source must be able to handle approximate charge current of 40 mA.

When AVDD and DVDD are both above 1.3 V to 1.5 V and VDD is above 2.4 V to 2.6 V, a 20 ms timer is started to allow additional time for the supplies to reach their normal potentials (VDD between 2.7 V and 3.6 V, AVDD at 1.9 V, and DVDD at 1.7 V). After this timer has elapsed, the crystal oscillator starts.

The RSTDONE interrupt is triggered approximately 26 ms later, bringing the $\overline{\text{IRQ1}}$ pin low and setting the RSTDONE bit in the STATUS1 register. This RSTDONE interrupt indicates to the user that the ADE9078 has finished its power-up sequence. Then, the user can configure the IC via the SPI (see the Quick Start section for a list of important registers to configure). After configuring the device, write the run register to start the DSP so that it starts making measurements. Note that registers from Address 0x000 through Address 0x0FF and Address 0x400 through Address 0x5FF are restored to their default values during power-on. Registers from Address 0x200 through Address 0x3FF are cleared within 500 µs from when the run register value changes from 0x0000 to 0x0001. Also note that the waveform buffer, Address 0x800 through Address 0xFFF, is not cleared after reset.

In PSM2 and PSM3, the AVDD and DVDD LDOs are not turned on. The RSTDONE interrupt does not occur and the SPI port is not available (see the Power Modes section for more information on these modes).

Brownout Detection

Power-on reset (POR) circuits monitor the VDD, AVDD, and DVDD supplies. If AVDD or DVDD drop below a threshold between 1.3 V and 1.5 V, or VDD drops below a threshold between 2.4 V and 2.6 V, the IC is held in reset. If the power-on sequence begins again, the ADE9078 waits until AVDD and DVDD are above 1.3 V to 1.5 V and VDD is above 2.4 V to 2.6 V to start the 20 ms POR timer. A RSTDONE interrupt on the $\overline{\text{IRQ1}}$ pin indicates when the ADE9078 can be reinitialized via SPI.

Reset

If the $\overline{\text{RESET}}$ pin goes low for 1 µs, the AVDD and DVDD LDOs turn off. The power on sequence resumes from the point where the AVDD and DVDD LDOs are turned on (see the Power-On Sequence section for details). A software reset is initiated by writing the SWRST bit in the CONFIG1 register, which resets the digital logic and takes ~60 µs to complete.

For applications that require putting the ADE9078 into a low power mode, it is recommended to use PSM3. In this mode, the ADE9078 consumes approximately 2 µA, much lower than the 100 µA current consumption obtained when the ADE9078 $\overline{\text{RESET}}$ pin is held low (see Table 1 for the exact PSM3 current consumption).

Changing to PSM2 or PSM3

The state of the PM1 and PM0 pins is continuously monitored. If the power mode changes from PSM0 or PSM1 to PSM2 or PSM3 (PM1, PM0 = 10 or 11) for 1 µs, the AVDD and DVDD LDOs are turned off. When the power mode switches back to PSM0 or PSM1, the power on sequence resumes from the point where AVDD and DVDD LDOs are turned on (see the Power-On Sequence section for details).

MEASUREMENTS (NORMAL MODE)

The ADE9078 offers per phase total IRMS and VRMS as well as total active power, VAR, VA, and fundamental VAR powers. The instantaneous low-pass filtered powers can be accumulated into power or energy registers and are available in pulsed outputs, CF1 through CF4.

Power quality information, such as zero-crossing detection, line period, and angle measurements, is also available.

A waveform buffer stores samples directly from the ADC, calculated resampled data, or processed current and voltage samples.

The measurements described are available in PSM0, the normal operating mode. A reduced set of features is available in PSM1 and PSM2 (see the Power Modes section for more details on these operating modes).

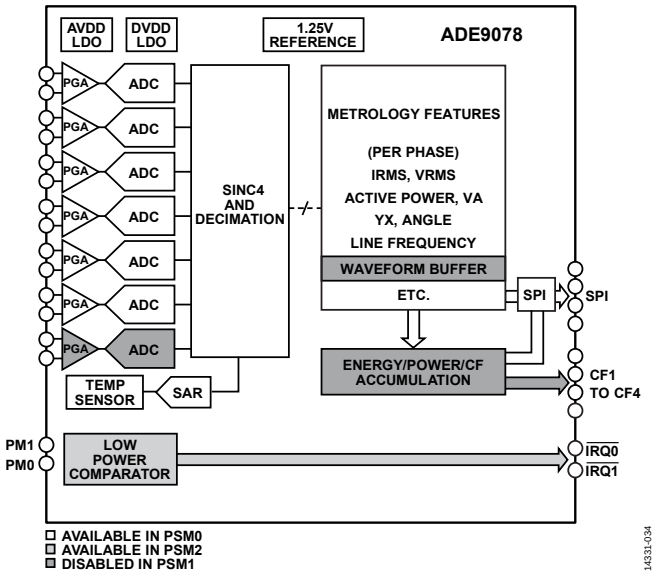


Figure 40. Features Available in Each Operating Mode

Current Channel

The current channel datapath for IA, IB, and IC is shown in Figure 41. The current channel ADC waveforms can be sampled at the sinc4 output in the xI_SINC_DAT registers at 16 kSPS, or further decimated by an IIR low-pass filter in the xI_LPF_DAT registers at 4 kSPS. Gain and phase compensation are applied, creating the xI_PCF instantaneous current waveforms that update at 4 kSPS. The xI_PCF waveforms are used for total active power, VAR, IRMS, VA, and fundamental VAR calculations. The xI_PCF value is also monitored in the current peak detection circuit. The rms of the sum of instantaneous currents measurement uses the AI_PCF, BI_PCF, and CI_PCF current channel waveforms to calculate the neutral current or ro calculate the net vector current sum including the neutral current measurement, NI_PCF (see the Neutral Current RMS, RMS of Sum of Instantaneous Currents section for more information). Finally, the angle measurements indicate the time between the current channel zero crossing and the voltage channel zero crossing on the same phase or current channels on the other phases, updating at 512 kSPS in the ANGLx_x registers.

The neutral current channel, Channel IN, offers a neutral current sum rms and is used in an rms of instantaneous current measurement, as shown in Figure 42. For more information about these calculations, see the Neutral Current RMS, RMS of Sum of Instantaneous Currents section. Channel IN offers a gain calibration (NIGAIN) and a phase calibration (NPHCAL). The digital integrator on Channel IN is enabled by setting the ININTEN bit in the CONFIG0 register. Note that the Channel IN neutral current modulator is turned off in PSM1.

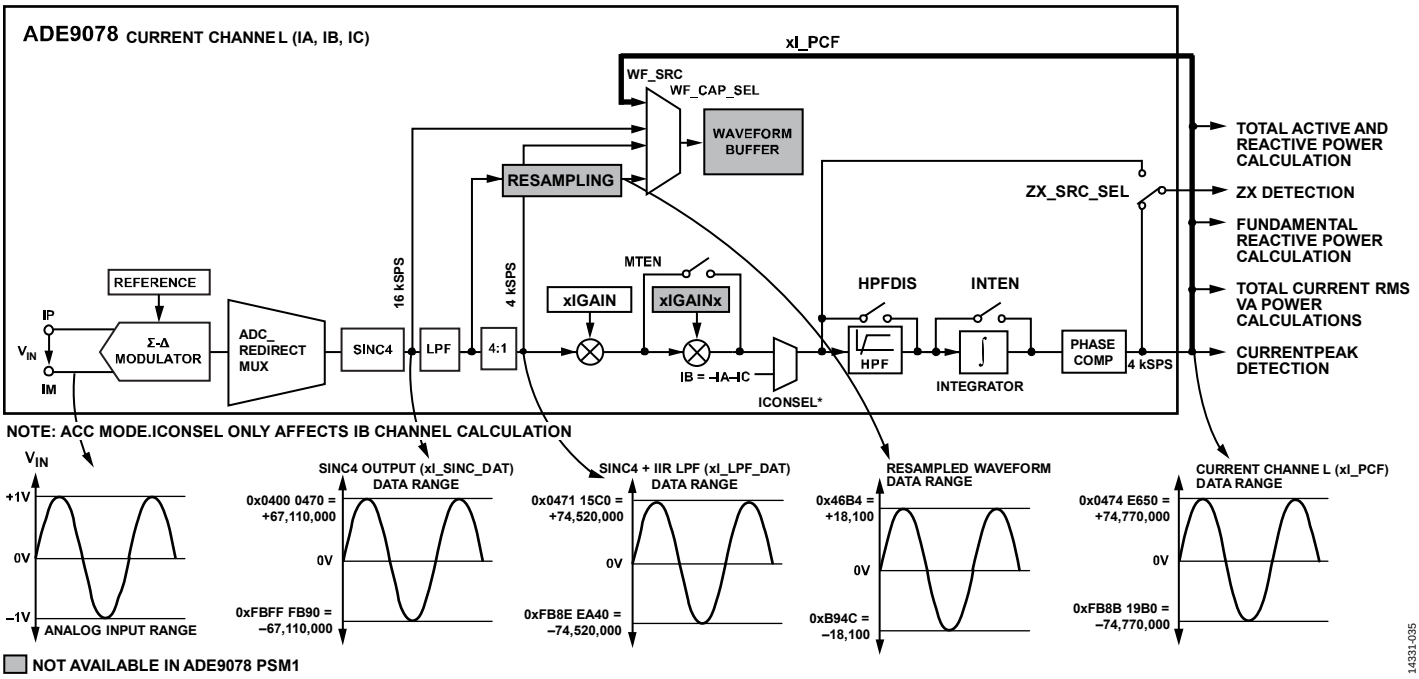


Figure 41. Current Channel Datapath

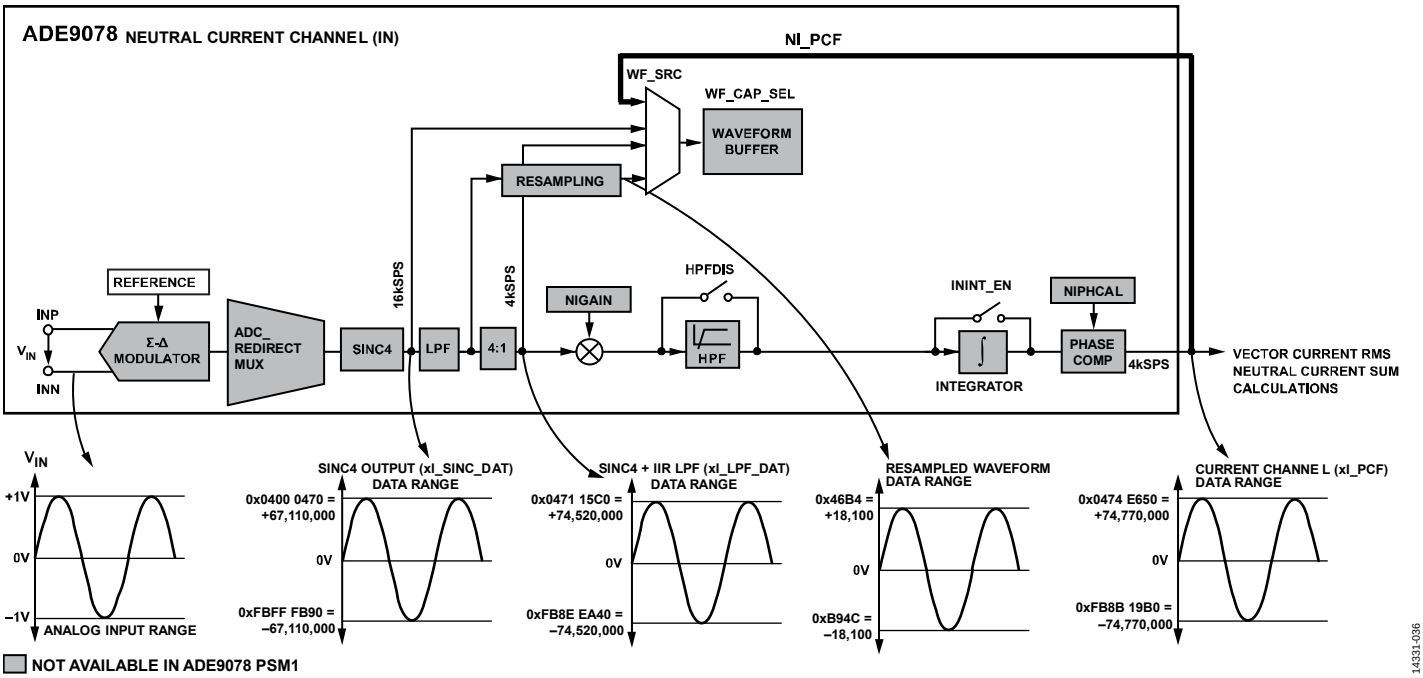


Figure 42. Neutral Current Channel Datapath

Current Channel Measurement Update Rates

Table 9 indicates the registers that hold current channel measurements and the rate at which they update.

Table 9. Current Channel Measurement Update Rates

Register Name	Description	Update Rate (kSPS)
AI_SINC_DAT	IA sinc4 filter output	16
BI_SINC_DAT	IB sinc4 filter output	16
CI_SINC_DAT	IC sinc4 filter output	16
NI_SINC_DAT	IN sinc4 filter output	16
AI_LPF__DAT	IA sinc4 + IIR low-pass filter output and decimation	4
BI_LPF__DAT	IB sinc4 + IIR low-pass filter output and decimation	4
CI_LPF__DAT	IC sinc4 + IIR low-pass filter output and decimation	4
NI_LPF__DAT	IN sinc4 + IIR low-pass filter output and decimation	4
AI_PCF	Instantaneous current on IA	4
BI_PCF	Instantaneous current on IB	4
CI_PCF	Instantaneous current on IC	4
NI_PCF	Instantaneous current on IN	4
AIRMS	Filtered based total rms of IA	4
BIRMS	Filtered based total rms of IB	4
CIRMS	Filtered based total rms of IC	4
NIRMS	Filtered based total rms of IN	4
ISUMRMS	Filtered rms of sum of instantaneous currents (AI_PCF + BI_PCF + CI_PCF ± NI_PCF) (see the Neutral Current RMS, RMS of Sum of Instantaneous Currents section)	4
IPEAK	Peak current channel sample (see the Peak Detection section)	4
ANGLx_x	Voltage to current or current to current phase angle (see the Angle Measurement section)	CLKIN/24 = 512

ADC_REDIRECT Multiplexer

The ADE9078 provides a multiplexer that allows any ADC output to be redirected to any digital processing datapath.

By default, each modulator is mapped to its corresponding datapath. For example, the IAP and IAN pins go into the IA modulator, which is mapped to the IxA digital processing datapath. Write to the ADC_REDIRECT register to change the ADC to digital channel mapping.

The redirection can be useful to simplify PCB layout, depending on if the ADE9078 is on the top or bottom of the PCB by redirecting the IA ADC output to the IC digital datapath and the IC ADC output to the IA digital datapath. To achieve this configuration, write IA_DIN = 010 and IC_DIN = 000 in the ADC_REDIRECT register.

Alternatively, the VA voltage channel output can be used for all three datapaths by writing VB_DIN = 100 and VC_DIN = 100 in the ADC_REDIRECT register.

The neutral current channel does not offer a zero-crossing output or angle measurements. To calibrate the phase of the neutral current NI_PCF signal, direct the neutral current ADC output to Phase B digital current channel and check how its angle corresponds to Phase A by writing IA_DIN = 111.

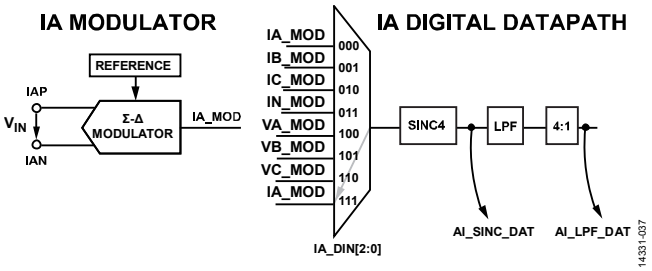


Figure 43. ADC_REDIRECT Modulator to Digital Datapath Multiplexing

Current Channel Gain, xIGAIN

There are many sources of gain error in an energy metering system. The current sensor, including current transformer burden resistors, may have some error. There is device to device gain error in the ADE9078 device itself and the voltage reference may have some variation (see Table 1 for the device specifications).

The ADE9078 provides a current gain calibration register so that each metering device has the same current channel scaling. The current channel gain varies with xIGAIN as shown in the following equation:

$$Current\ Channel\ Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right) \times HPF\_GAIN$$

Use the following equation to calculate the xIGAIN value for a given current channel gain:

$$xIGAIN = \text{round}((Current\ Channel\ Gain - 1) \times 2^{27})$$

where round() is a function to round to the nearest integer.

The current channel gain can be positive or negative.

For example, to increase the gain of the current channel up by 10% to 1.1,

$xIGAIN = \text{round}((1.1 - 1) \times 2^{27}) = 13{,}421{,}773 =$ 0x00CC CCCD

To decrease the gain by 10% to 0.9:

$xIGAIN = \text{round}((0.9 - 1) \times 2^{27}) = -13{,}421{,}773 =$ 0xFF33 3333

It is also possible to use the current channel gain register to change the sign of the current channel, which may be useful if the current sensor was installed backwards. To compensate for this situation, use current channel gain = −1.

$xIGAIN = \text{round}((-1 - 1) \times 2^{27}) = -268{,}435{,}456 =$ 0xF000 0000

If the multipoint gain and phase feature is used, it is recommended to use the xIGAIN for the main correction, performed at the nominal current for the meter (see the Multipoint Gain and Phase Calibration section for more information).

Note that for a given phase,

$|Current\ Channel\ Gain \times Voltage\ Channel\ Gain \times Power\ Gain| \leq 3.75$

IB Calculation Using ICONSEL

Write the ICONSEL bit in the ACCMODE register to calculate $I_B = -I_A - I_C$. This setting can help save the cost of a current transformer in some 3-wire delta configurations. See the Applying the ADE9078 to a 3-Wire Delta Service section for more information.

High-Pass Filter

A high-pass filter is provided to remove dc offsets for accurate rms and energy measurements.

The ADE9078 high-pass filter on the current and voltage channels is enabled by default. It can be disabled by writing the DISPHPF bit in the CONFIG0 register = 1.

It is recommended to leave the high-pass filter enabled to achieve the metering performance listed in the specifications in Table 1.

For some applications, it is desirable to increase the high-pass filter corner, such as to improve performance when a Rogowski coil current sensor is used.

The high-pass filter corner is selectable using the HPF_CRN bits in the CONFIG2 register.

Table 10. HPF Corner Gain with 50 Hz Input Signal

HPF_CRN	$f_{-3\ dB}$ (Hz)	HPF_GAIN	Settling Time to 1% for DC Step (sec)	Settling Time to 0.1% for DC Step (sec)
0	38.7	0.80	0.0178	0.0268
1	19.6	0.94	0.0363	0.0544
2	9.90	0.99	0.0731	0.1097
3	4.97	1.00	0.1468	0.2202
4	2.49	1.00	0.2942	0.4412
5	1.25	1.00	0.5889	0.8833
6 (default)	0.625	1.00	1.1784	1.7675
7	0.313	1.00	2.3573	3.5359

Digital Integrator

A digital integrator is included to allow easy interfacing to di/dt current sensors, also known as Rogowski coils. The di/dt sensor output increases 20 dB/decade over the frequency range. To compensate for this increased output, the digital integrator applies −20 dB/decade gain with a phase shift of approximately −90°.

A second-order antialiasing filter is required to avoid noise aliasing back in the band of interest when the ADC is sampling.

To enable the digital integrator on the IA, IB, and IC channels, set the INTEN bit in the CONFIG0 register. To enable the digital integrator on the neutral current, IN channel, set the ININTEN bit in the CONFIG0 register.

Figure 44 through Figure 47 show the magnitude and phase response of the ADE9078 digital integrator with the recommended DICOEFF value of 0xFFFFE000.

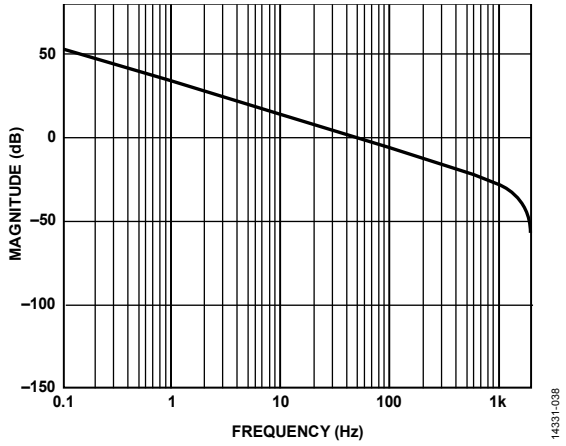


Figure 44. Digital Integrator Magnitude Response, DICOEFF = 0xFFFFE000

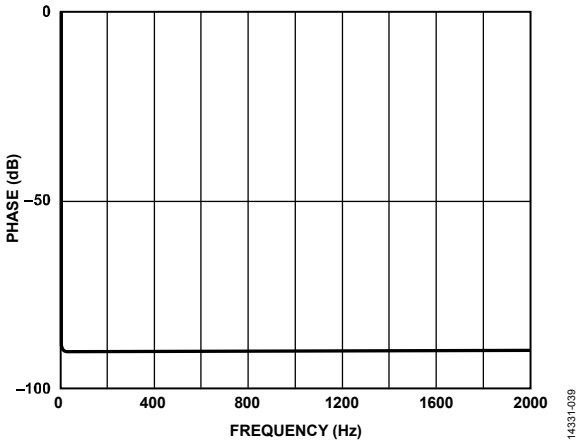


Figure 45. Digital Integrator Phase Response, DICOEFF = 0xFFFFE000

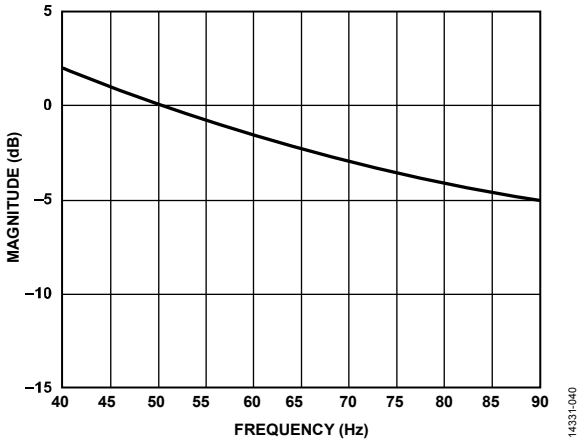


Figure 46. Digital Integrator Magnitude Response from 40 Hz to 90 Hz, DICOEFF = 0xFFFFE000

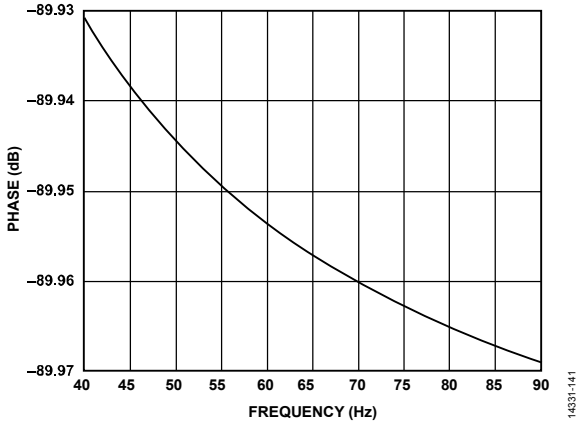


Figure 47. Digital Integrator Phase Response from 40 Hz to 90 Hz, DICOEFF = 0xFFFFE000

The recommended DICOEFF value is 0xFFFFE000.

Phase Compensation

The ADE9078 phase compensation uses a digital filter to achieve a phase adjustment of ±0.001°. This high resolution improves the total active energy and reactive energy performance at low power factors.

The phase calibration range is −15° to +4.5° at 50 Hz.

To achieve this phase compensation, the voltage channel is delayed by one 4 kSPS sample, 4.5° at 50 Hz.

$$Voltage\ Channel\ Delay = \left(\frac{f_{LINE}}{f_{DSP}} \times 360°\right)$$

$$Voltage\ Channel\ Delay = \left(\frac{50}{4000} \times 360°\right) = 4.5°$$

The current channel is then delayed by a digital filter, according to the value programmed into the xPHCALx register. The resulting phase correction depends on the value in the xPHCALx register. The following equation gives the phase correction between the input current and voltage after the combined voltage and current delays. In the following formula, phase correction is positive to correct a current that lags the voltage, and phase correction is negative to correct a situation where the current leads the voltage, such as occurs with a current transformer:

$$Phase\ Correction\ (\text{Degrees}) = \arctan\left(\frac{-\sin\omega}{xPHCALx \times 2^{-27} + \cos\omega}\right) - \arctan\left(\frac{-xPHCALx \times 2^{-27} \times \sin\omega}{1 + xPHCALx \times 2^{-27} \times \cos\omega}\right)$$

where $\omega = 2\pi \times f_{LINE}/f_{DSP}$.

Calculate the xPHCALx register value can from the desired phase correction according to the following equation:

$$xPHALx = \left(\frac{\sin(\varphi - \omega) + \sin\omega}{\sin(2\omega - \varphi)}\right) \times 2^{27}$$

For example, if f_{LINE} = 50 Hz, f_{DSP} = 4 kHz, and the current leads the voltage by 0.1°, the phase correction = −0.1°. Write xPHCALx = 0xFFE9 7889 to correct for this phase difference.

$$\omega = 2\pi \times 50/4000 = 0.07854$$

$$xPHALx = \left(\frac{\sin(RADIANS(-0.1) - 0.07854) + \sin(0.07854)}{\sin(2 \times 0.07854 - RADIANS(-0.1))}\right) \times$$

$$2^{27} = -1{,}476{,}471 = 0\text{xFFE9 7889}$$

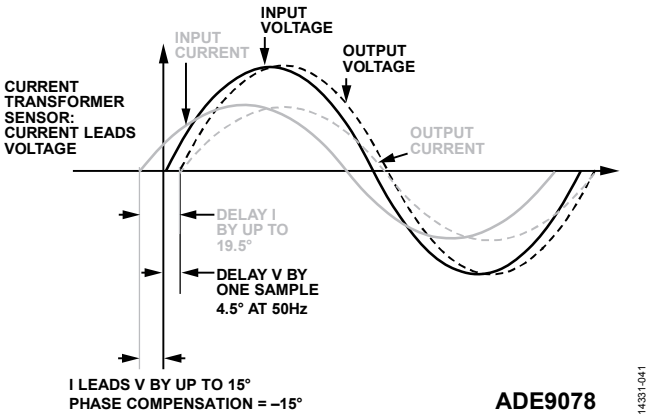


Figure 48. Phase Compensation Example for Current Transformer, Where the Current Leads the Voltage

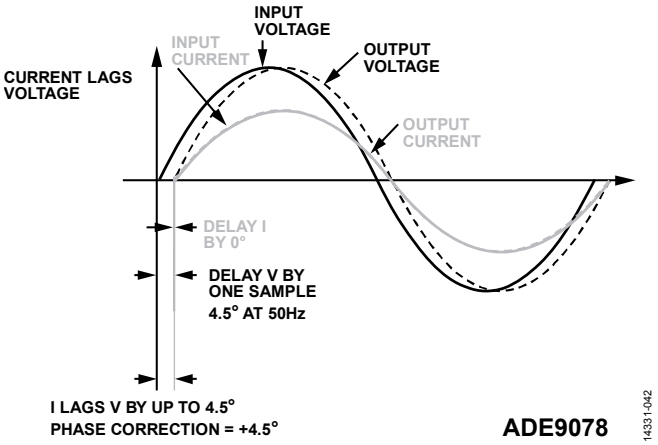


Figure 49. Phase Compensation Example Where Current Lags Voltage

Using the equations in the Phase Compensation section, it can be seen that at 60 Hz, the voltage channel delay is 5.4°, as follows:

$$Voltage\ Channel\ Delay\ (\text{Degrees}) = \left(\frac{60}{4000} \times 360°\right) = 5.4°$$

This calculation leads to a phase calibration range of −15° to +5.4° at 60 Hz.

Note that this phase compensation is equivalent to a delay or advance in time. As the line frequency varies, the applied phase compensation varies as well according to the phase correction equation.

Multipoint Gain and Phase Calibration

The ADE9078 allows the current channel gain and phase compensation to vary as a function of the calculated input current rms amplitude in xIRMS, which is useful to correct for the nonlinearities of current transformer sensors to achieve very high meter accuracy, for example in Class 0.2 meters.

Multipoint Gain and Phase

The current channel gain, xIGAIN, is applied regardless of the xIRMS input signal level. This gain compensates for the nominal gain error of the current channel, including the current transformer and burden resistors. If multipoint gain and phase compensation is enabled, an additional current gain value is applied based on the xIRMS value to compensate for the current transformer gain shift over input signal amplitude. The current channel datapath is shown in Figure 51.

If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, xIGAIN0 through xIGAIN4, is applied based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values, as shown in Figure 50.

The applied current channel phase compensation varies based on the xIRMS input signal level as well if multipoint gain and phase compensation is enabled.

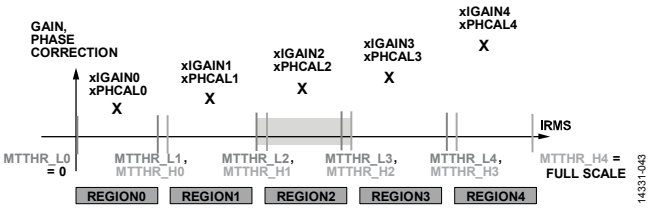


Figure 50. Multipoint Gain and Phase Calibration

The MTTHR_Lx and MTTHR_Hx registers set up the regions in which to apply each set of corrections, allowing hysteresis.

The decision of which coefficients to apply is done according to the following rules:

```
If xIRMS >MTTHR_H[current_region]
If current_region ≤ 3
    Current_region++;
Else If xIRMS < MTTHR_L[current_region]
  If current_region ≥ 1
    current_region--;
xIGAIN = xIGAIN[current_region];
xPHCAL = xPHCAL[current_region];
xMTREGION = current_region;
```

For example, if AIRMS goes above MTTHR_H2, the gain and phase correction is set to AIGAIN3 and APHCAL3, respectively. Then, if AIRMS goes below MTTHR_L3, the gain and phase correction is set to AIGAIN2 and APHCAL2.

For proper operation, the value of the registers must be increasing such that MTTHR_L0 < MTTHR_L1 < MTTHR_H0 < MTTHR_L2 < MTTHR_H1 < MTTHR_L3 < MTTHR_H2 < MTTHR_L4 < MTTHR_H3 < MTTHR_H4.

The following example configuration uses two regions, such that Region 0 is used from 0 A to 20A and Region 1 is used from 22 A to full scale:

- MTTHR_L0 = 0
- MTTHR_L1 = 0x95 9AC1 (20 A for this meter)
- MTTHR_H0 = 0xA4 90A2 (22 A for this meter)
- MTTHR_L2 = 0x7FFFFFFE (maximum positive threshold − 1)
- MTTHR_H1 = 0x7FFFFFFF (maximum positive threshold)

The xMTREGION registers indicate the current region for each phase and correspondingly, which xIGAINx and xPHCALx coefficients are being applied.

Multipoint phase and gain calibration is disabled by default. To enable it, set the MTEN bit in the CONFIG0 register.

Single-Point Gain and Phase

When multipoint gain and phase calibration is disabled, single-point gain and phase calibration is allowed.

In this case, the xIGAIN register is applied. No additional current channel gain is applied based on the xIRMS amplitude.

When multipoint gain and phase calibration is disabled, the xPHCAL0 phase compensation is always applied regardless of the xIRMS value.

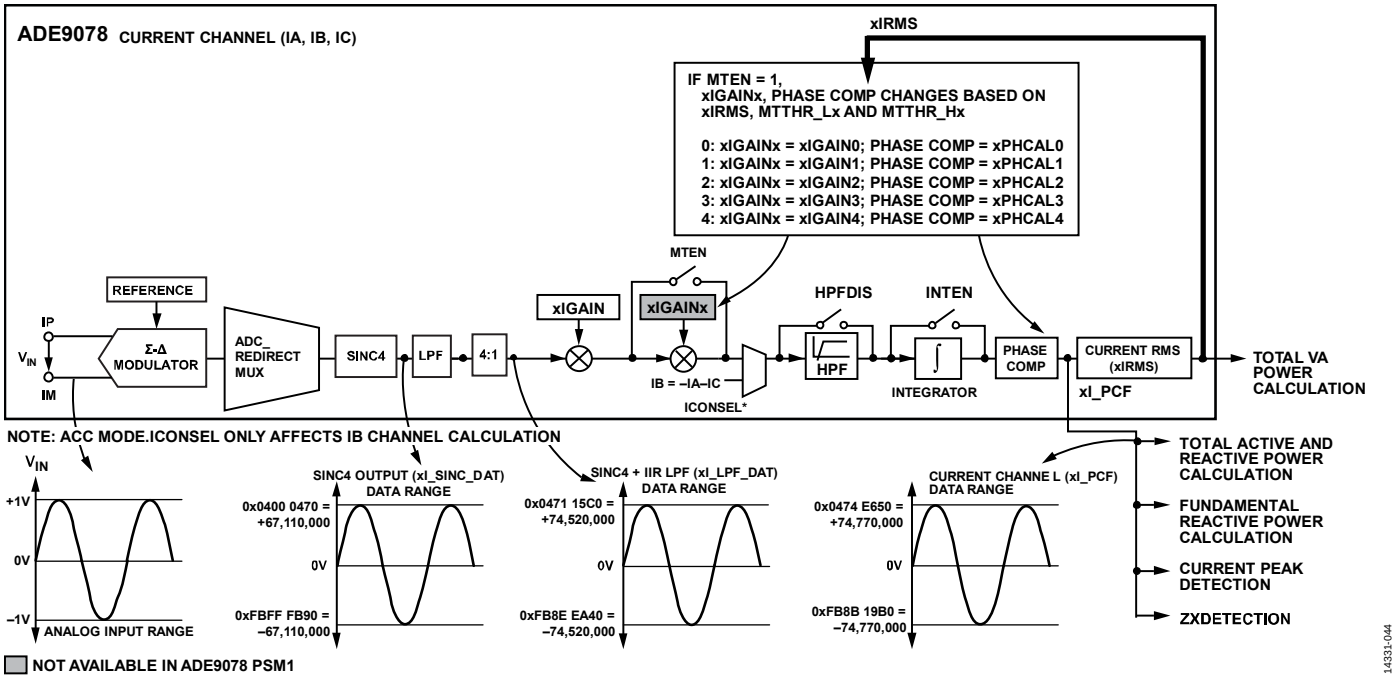


Figure 51. Current Channel with Multi-Point Gain and Phase Correction

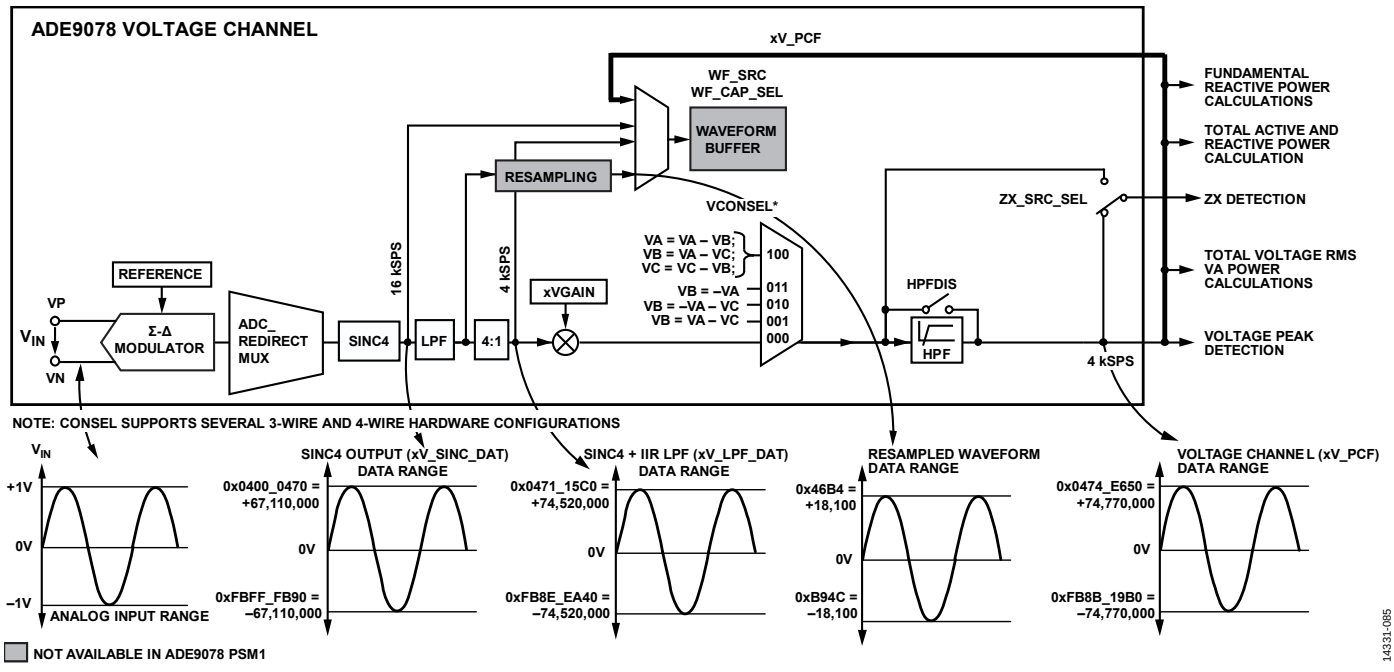


Figure 52. Voltage Channel Datapath

Table 11. Voltage Channel Measurement Update Rates

Register Name	Description	Update Rate
AV_SINC_DAT	VA sinc4 filter output	16 kSPS
BV_SINC_DAT	VB sinc4 filter output	16 kSPS
CV_SINC_DAT	VC sinc4 filter output	16 kSPS
AV_LPF_DAT	VA sinc4 + IIR low-pass filter and decimator output	f_{DSP} = 4 kSPS
BV_LPF_DAT	VB sinc4 + IIR low-pass filter and decimator output	f_{DSP} = 4 kSPS
CV_LPF_DAT	VC sinc4 + IIR low-pass filter and decimator output	f_{DSP} = 4 kSPS
AV_PCF	Instantaneous voltage on VA	f_{DSP} = 4 kSPS
BV_PCF	Instantaneous voltage on VB	f_{DSP} = 4 kSPS
CV_PCF	Instantaneous voltage on VC	f_{DSP} = 4 kSPS
AVRMS	Filtered based total rms of VA	f_{DSP} = 4 kSPS
BVRMS	Filtered based total rms of VB	f_{DSP} = 4 kSPS
CVRMS	Filtered based total rms of VC	f_{DSP} = 4 kSPS
VPEAK	Peak current channel sample (see the Peak Detection section)	f_{DSP} = 4 kSPS
APERIOD	Line period measurement on VA	f_{DSP} = 4 kSPS
BPERIOD	Line period measurement on VB	f_{DSP} = 4 kSPS
CPERIOD	Line period measurement on VB	f_{DSP} = 4 kSPS
COM_PERIOD	Line period measurement on combined signal from VA, VB, VC (see the Combined Voltage Zero Crossing section)	f_{DSP} = 4 kSPS
ANGLx_x	Voltage to current or current to current phase angle (see the Angle Measurement section)	CLKIN/24 = 512 kSPS

Voltage Channel

The voltage channel datapath is shown in Figure 52. The voltage channel ADC waveforms can be sampled at the sinc4 output, in the xV_SINC_DAT registers, at 16 kSPS or further decimated by an IIR low-pass filter, in xV_LPF_DAT registers at f_{DSP} = 4 kSPS. Gain and phase compensation are applied, creating the xV_PCF instantaneous voltage waveforms that update at f_{DSP} = 4 kSPS. The xV_PCF waveforms are used for total active power, VAR, IRMS, VA, and fundamental VAR calculations. The xV_PCF value is also monitored in the voltage peak detection circuit. Finally, angle measurements indicate the time between the voltage channel zero crossing and the current channel zero crossing on the same phase or voltage channels on the other phases, updating at CLKIN/24 = 512 kSPS in the ANGLx_x registers. The line period measurement xPERIOD indicates the line period, as described in the Line Period Calculation section.

Voltage Channel Measurements

Table 11 indicates the registers that hold voltage channel measurements and the rate at which they update.

Voltage Channel Gain

Use the xVGAIN registers to calibrate the voltage channel of each phase. The xVGAIN register has the same scaling as the xIGAIN register.

$$Voltage\ Channel\ Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right) \times HPF\_GAIN$$

See the Current Channel Gain, xIGAIN section for more information about the gain scaling and how it is affected by the high-pass filter corner (HPF_CRN) selection.

Note that for a given phase,

$$|Current\ Channel\ Gain \times Voltage\ Channel\ Gain \times Power\ Gain| \leq 3.75$$

Energy Measurements Overview

Figure 53 shows how AI_PCF and AV_PCF calculate per phase rms and power and how the calculated rms and power are accumulated into the AWATTHR and AWATT_ACC registers and the CFx pulse outputs.

Per Phase Energy Measurements Update Rate

Instantaneous power measurements, including as xWATT, xVAR, xVA, xFVAR, update at a rate of f_{DSP} = 4 kSPS.

These measurements are accumulated into power measurements in xWATT_ACC register that update at a user defined interval ranging from 500 µs to 2 sec, depending on the selection in the PWR_TIME register.

Energy measurements update every 4 kSPS by default and can store up to 211 sec of accumulation at full scale. Alternatively, these registers can be set into a different accumulation mode where they update after a user defined number of line cycles or samples.

The power factor measurements update every 4096/4 kSPS = 1.024 sec.

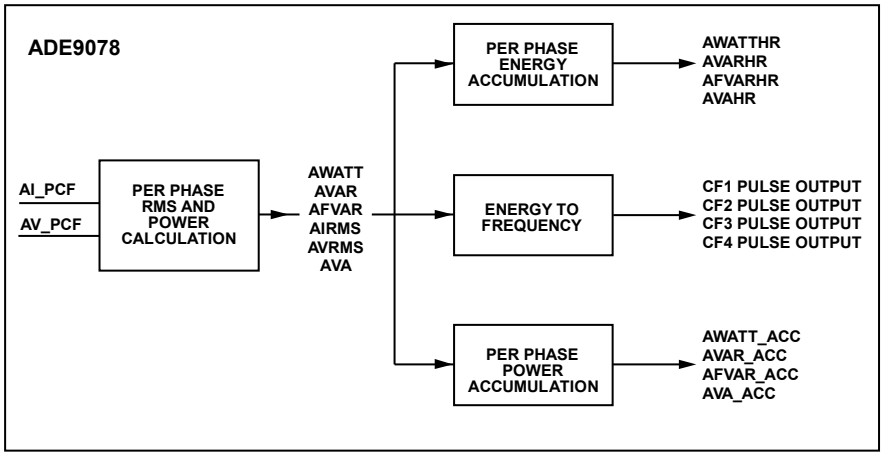


Figure 53. Per Phase Power and Energy Calculations from xI_PCF and xV_PCF Waveforms

Table 12. Active Power Related Register Update Rate

Register Name	Description	Update Rate
AWATT	Low-pass filtered total active power on Phase A	4 kSPS
BWATT	Low-pass filtered total active power on Phase B	4 kSPS
CWATT	Low-pass filtered total active power on Phase C	4 kSPS
AWATT_ACC	Accumulated total active power on Phase A	After the PWR_TIME 4 kSPS samples, from 500 µs to 2.048 sec
BWATT_ACC	Accumulated total active power on Phase B	After the PWR_TIME 4 kSPS samples, from 500 µs to 2.048 sec
CWATT_ACC	Accumulated total active power on Phase C	After the PWR_TIME 4 kSPS samples, from 500 µs to 2.048 sec
AWATTHR	Accumulated total active energy on Phase A	According to the settings in EP_CFG and EP_TIME; holds up to 211 sec of energy at full scale
BWATTHR	Accumulated total active energy on Phase B	According to the settings in EP_CFG and EP_TIME; holds up to 211 sec of energy at full scale
CWATTHR	Accumulated total active energy on Phase C	According to the settings in EP_CFG and EP_TIME; holds up to 211 sec of energy at full scale
APF	Phase A Power Factor (see the Power Factor section)	Every 1.024 sec
BPF	Phase A Power Factor (see the Power Factor section)	Every 1.024 sec
CPF	Phase A Power Factor (see the Power Factor section)	Every 1.024 sec

Power-Based and Filter-Based RMS Measurement Algorithms

Filter-Based Total RMS

The ADE9078 offers current and voltage rms measurements, which are calculated by squaring the input signal, low-pass filtering, and then taking the square root of the result, as shown in Figure 54.

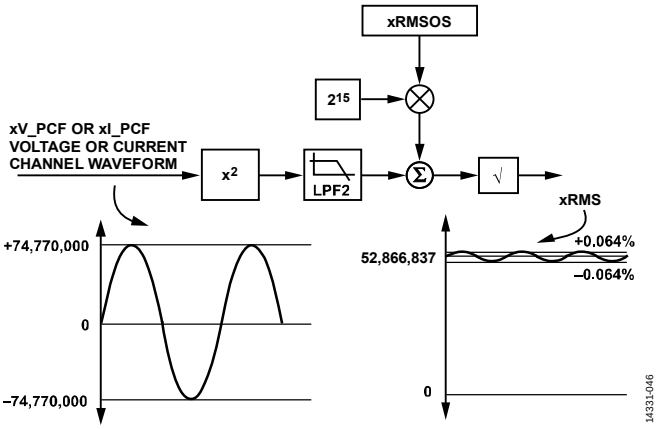


Figure 54. Filter Based RMS

The low-pass filter, LPF2, extracts the rms value, attenuating harmonics of a 50 Hz or 60 Hz fundamental by at least 64 dB so that at full scale, the variation in the calculated rms value is very small, ±0.064% error. Note that the rms reading variation increases as the input signal becomes smaller because the noise in the measurement increases.

The filter based rms measurement is typically within 0.5% error over a 5000:1 dynamic range and within 0.1% error over a 1000:1 dynamic range. Refer to the specifications in Table 1 to understand what performance to expect from this measurement.

Note that the xRMS register does not read 0 with the xP and xN inputs shorted together.

The filter based rms has a bandwidth of 1.6 kHz, as given in Table 1.

The rms calculations, one for each channel, AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, and CVRMS, are updated every 4 kSPS. The ISUMRMS calculation uses the same method to calculate ISUMRMS, where $I_{SUM} = I_A + I_B + I_C \pm I_N$, and also updates at 4 kSPS (see the Neutral Current RMS, RMS of Sum of Instantaneous Currents section for more information).

The xRMS value at full scale is 52,866,837d. Table 13 shows the rms settling time to 99% of full scale for a 50 Hz signal.

Table 13. RMS Settling Time

Configuration	RMS Settling Time, FS = 99% (sec)
Integrator On, HPF On, and LPF2 On	1.09
Integrator Off, HPF On, and LPF2 On	0.96

For high performance at small input signals, below 1000:1, it is recommended to calibrate the offset of this measurement using the xRMSOS registers. The offset must be calibrated at the smallest input signal that requires good performance—do not calibrate this measurement with zero input signal.

The following equation indicates how the xRMSOS register value modifies the result in the xRMS register:

$$xRMS = \sqrt{xRMS0^2 + 2^{15} \times xRMSOS}$$

where *xRMS0* is the initial *xRMS* register value before offset calibration.

At 1000:1, the expected xRMS0 = 52,866,837/1000 = 52,866.837. Then, one bit in the xRMSOS register changes xRMS by (52,867.147 − 52,866.837)/52,866.837 = 0.0006%.

$$xRMS = \sqrt{\left(\frac{52{,}866{,}837}{1000}\right)^2 + 2^{15} \times 1} = 52{,}867.147$$

Neutral Current RMS, RMS of Sum of Instantaneous Currents

The ADE9078 calculates the neutral current rms from a neutral current sensor input into the INP and INN pins, and stores the result in the NIRMS register. A NIRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers (see the Filter-Based Total RMS section for more information).

The ADE9078 also calculates the rms of $I_{SUM} = I_A + I_B + I_C \pm I_N$ and stores the result in ISUMRMS. An ISUMRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers (see the Filter-Based Total RMS section for more information).

If a neutral current sensor is not used, write 0 to the ISUM_CFG bits in the CONFIG0 register, and then ISUMRMS approximates the neutral current from the sum of IA, IB, and IC.

If the measured neutral current, NI_PCF, deviates from the sum of AI_PCF + BI_PCF + CI_PCF current channel waveforms, there may be a fault in the system.

To determine how big the mismatch is between the measured neutral current and the measured Channel A, Channel B, and Channel C currents, select ISUM_CFG[1:0] to 01 or 10 based on the direction of the neutral current with respect to the other current channel waveforms.

Table 14. I_{SUM} Configuration Options

ISUM_CFG[1:0]	I_{SUM} Calculation
00, 11	I_{SUM} = AI_PCF + BI_PCF + CI_PCF
01	I_{SUM} = AI_PCF + BI_PCF + CI_PCF + NI_PCF
10	I_{SUM} = AI_PCF + BI_PCF + CI_PCF − NI_PCF

ISUMRMS has the same scaling as xIRMS. Note that if AI_PCF, BI_PCF, and CI_PCF are all at full scale and in phase with each other, with ISUM_CFG = 00 or 11, ISUMRMS is 3 × 52,866,837d = 158,600,511d. If AI_PCF, BI_PCF, CI_PCF, and NI_PCF are all

at full scale and in phase with each other, with the ISUM_CFG = 01 then ISUMRMS is 4 × 52,866,837d = 211,467,348d.

To receive an indication if ISUMRMS exceeds a threshold, configure ISUMLVL. The MISMTCH bit in STATUS0 and associated interrupt indicate if there is a change in the relationship between ISUMRMS and ISUMLVL.

Calculate the desired value of ISUMLVL according to the following equation:

$$ISUMLVL = \left(\frac{xIRMS\_FULL\_SCALE}{X} \right)$$

where:
xIRMS_FULL_SCALE is the nominal xIRMS value with full-scale inputs, 52,866,837.
X is the desired current level to indicate a MISMTCH error. For example, set the ISUMLVL to warn about a rms of sum of instantaneous currents greater than 10,000:1 from full scale, *X* = 10,000.

Total Active Power

Total active power is commonly used for billing purposes. It includes power on the fundamental and on the harmonics.

Figure 55 shows how the low-pass filtered total active power on Phase A is calculated. First, the AI_PCF and AV_PCF waveforms are multiplied together. Then, the result is low-pass filtered, unless DISAPLPF = 1. Finally, the APGAIN is applied to perform a gain correction and the AWATTOS value is applied to correct the active power offset.

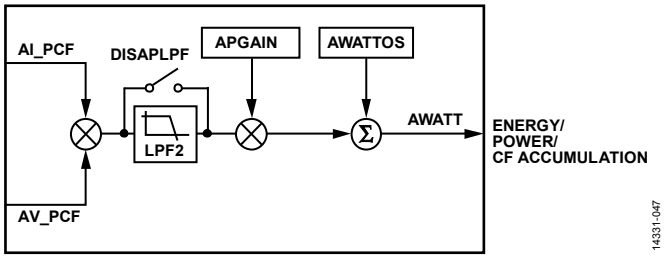


Figure 55. Total Active Power (AWATT) Calculation

Figure 56 shows the relationship between the I and V input signals and the instantaneous active power and low-pass filtered active power, assuming that I and V are at full scale with just the fundamental present and a power factor of 1.

If DISAPLPF = 1, AWATT reflects the instantaneous active power and if it is 0, AWATT reflects the low-pass filtered active power in Figure 56, assuming that APGAIN = 0 and AWATTOS = 0.

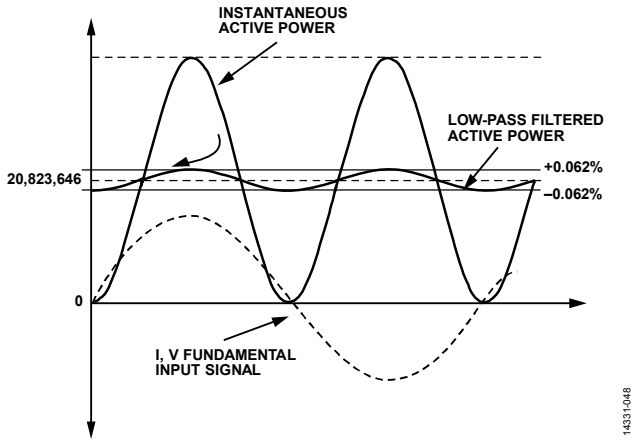


Figure 56. Instantaneous Active Power and Low-Pass Filtered Active Power at a Power Factor of 1

The low-pass filter, LPF2, extracts the total active power, attenuating harmonics of a 50 Hz or 60 Hz fundamental by 64 dB so that at full scale, the variation in the low-pass filtered active power is very small, ±0.062%.

The resulting AWATT signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz, as given in Table 1.

Phase B and Phase C have similar datapaths to those described for AWATT to calculate BWATT and CWATT, with individual gain and phase coefficients, BPGAIN and BWATTOS, and CPGAIN, and CWATTOS.

The xPGAIN register has the same scaling as the xIGAIN register (see the equations in the Current Channel Gain, xIGAIN section).

Note that for a given phase,

$$|Current\ Channel\ Gain \times Voltage\ Channel\ Gain \times Power\ Gain| \leq 3.75$$

xWATTOS has the same scaling as xWATT. To understand how xWATTOS affects the xWATT value, use the following equation:

$$xWATTOS = \left(\frac{1}{\frac{xWATT\_FULL\_SCALE}{X}} \right)$$

where:
xWATT_FULL_SCALE is the nominal xWATT value with full-scale inputs, 20,823,646. Note that xVAR and VA have the same scaling, so the same equation can be used for all three offsets.
X is the smallest power level to calibrate. For example, to calibrate the energy at 10,000 from full scale, *X* = 10,000.

$$xWATTOS = \left(\frac{1}{\frac{20,823,646}{10,000}} \right) = 0.05\%$$

Then, each bit in the xWATTOS register can correct an error of 0.05% at 10,000:1. Note that in most applications, the total active power performance with small inputs is sufficient with xWATTOS at zero.

Table 15 shows the settling times for total active power for a 50 Hz signal.

Table 15. Total Active Power Settling Time

	Total Active Power Settling Time (sec)	
Configuration	**FS = 99%**	**FS = 99.90%**
Integrator On, HPF On, and LPF2 On	0.85	1.2
Integrator Off, HPF On, and LPF2 On	0.85	1.2
Integrator Off, HPF On, and LPF2 Off	0.06	0.66

Total Reactive Power

Total reactive power includes reactive power on the fundamental and on the harmonics. The current channel, AI_PCF, is shifted by 90° at the fundamental and at all harmonics. Then, this signal is multiplied by the voltage waveform, AV_PCF. Then the result is low-pass filtered, unless DISRPLPF = 1. Finally the APGAIN is applied to perform a gain correction and the AVAROS value is applied to correct the VAR offset. Note that, in most applications, the total reactive power performance with small inputs is sufficient with AVAROS at zero.

Figure 57 shows how the total reactive power calculation is performed.

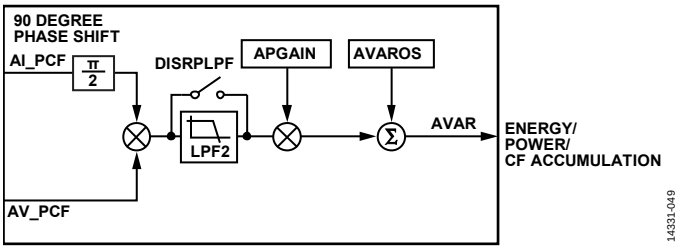


Figure 57. Total Reactive Power (AVAR) Calculation

The total reactive power at a power factor of 0 has a similar ripple to the total active power at a power factor of 1 (see Figure 56).

The resulting AVAR signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz, as given in Table 1.

Phase B and Phase C have similar datapaths to those described for AVAR to calculate BVAR and CVAR, with individual gain and phase coefficients, BPGAIN and BVAROS, and CPGAIN and CVAROS.

XVAROS has the same scaling as xVAR (see the Total Active Power section to understand how to calculate this register value).

It is possible to disable total reactive power by setting the VAR_DIS register. Note that the run register must be set to 0 before changing the VAR_DIS setting and must then be set to 1 again.

Table 16 shows the settling times for total reactive power for a 50 Hz signal.

Table 16. Total Reactive Power Settling Time

	Total Reactive Power Settling Time (sec)	
Configuration	**FS = 99%**	**FS = 99.90%**
Integrator On, HPF On, and LPF2 On	0.85	1.19
Integrator Off, HPF On, and LPF2 On	0.85	1.19
Integrator Off, HPF On, and LPF2 Off	0.02	0.07

Total Apparent Power

Apparent power is generated by multiplying the current rms measurement, xIRMS by the corresponding voltage rms, xVRMS and then applying a gain correction, APGAIN. The result is stored in the AVA register. Note that the offset of the total apparent power calculation is performed by calibrating the AIRMS and AVRMS measurements, using the AIRMSOS and AVRMSOS registers (see the Filter-Based Total RMS section for more information on the rms calculation).

The resulting AVA signal has an update rate of 4 kSPS and a bandwidth of 1.6 kHz, as given in Table 1.

Phase B and Phase C have similar datapaths to those described for AVA to calculate BVA and CVA, with individual gain coefficients, BPGAIN and CPGAIN.

In some applications, if a tamper is detected on the voltage channel inputs, it is desirable to accumulate the apparent energy assuming that the voltage were at a nominal level. The ADE9078 offers a register (VNOM) that can be set to a value to correspond to 240 V rms. If the VNOMx_EN bits in the CONFIG0 register are set, VNOM is multiplied by xIRMS when calculating xVA.

Table 17 shows the settling times for total apparent power for a 50 Hz signal.

Table 17. Total Apparent Power Settling Time

Configuration	**Total Apparent Power Settling Time, FS = 99% (sec)**
Integrator On, HPF On, and LPF2 On	1.09
Integrator Off, HPF On, and LPF2 Off	0.96

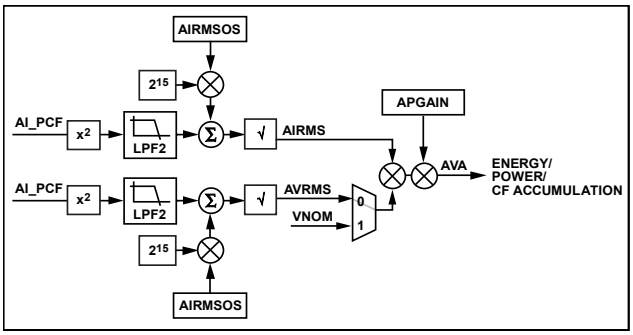


Figure 58. Total Apparent Power (AVA) Calculation

Fundamental Reactive Power

The fundamental reactive power in the ADE9078 is calculated using a proprietary algorithm that requires initialization of the network frequency and of the nominal voltage measured in the voltage channel. The SELFREQ bit in the ACCMODE register selects whether the system is 50 Hz or 60 Hz. For a 50 Hz system, clear the SELFREQ bit, and for a 60 Hz system, set the SELFREQ bit to 1. The SELFREQ selection must be made prior to writing 1 to the run register.

The VLEVEL register indicates the nominal value of the voltage channel. Calculate VLEVEL according to the following equation:

$$VLEVEL = X \times 1{,}144{,}084$$

where X is the dynamic range that the nominal input signal is at with respect to full scale.

It is recommended to set the voltage channel input so that the nominal voltage, for example 240 V rms, corresponds to one half of the analog input signal range of the ADE9078. The ADE9078 can support ±1 V peak, 0.707 V rms inputs, so it is recommended to scale the voltage channel inputs to 0.353 V rms. Then, with a nominal input of 240 V, the input signal is at half of full scale and X is equal to 2. Write 2,288,168d to the VLEVEL register to configure this feature.

$$VLEVEL = 2 \times 1{,}144{,}084 = 2{,}288{,}168$$

After configuring the SELFREQ and VLEVEL parameters, the ADE9078 tracks the fundamental line frequency within ±5 Hz of the 50 Hz or 60 Hz frequency selected in SELFREQ. If a larger frequency range than ±5 Hz is required in the application, monitor the line period (xPERIOD) and change the SELFREQ selection accordingly. Note that the run register must be set to 0 before changing the SELFREQ setting and must then be set to 1 again.

The fundamental current signal is shifted by 90° and multiplied by the fundamental voltage signal. This is then gained by APGAIN and offset correction is applied according to the AFVAROS register.

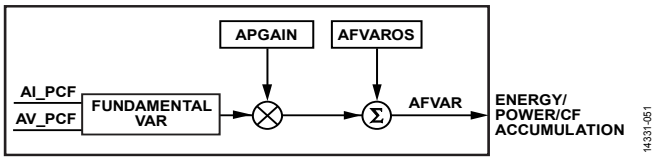


Figure 59. Fundamental Reactive Power, AFVAR

The fundamental reactive power at a power factor of 0 has a similar ripple to the total active power at a power factor of 1 (see Figure 56).

xFVAROS has the same scaling as xFVAR (see the Total Active Power section to understand how to calculate this register value.

Table 18 shows the settling times for fundamental reactive power for a 50 Hz signal.

Table 18. Fundamental Reactive Power Settling Time

	Fundamental Reactive Power Settling Time (sec)	
Configuration	**FS = 99%**	**FS = 99.90%**
Integrator On, HPF On, and LPF2 On	0.86	1.11
Integrator Off, HPF On, and LPF2 On	0.86	1.11

Power Factor

The total active power and total apparent power are accumulated over 1.024 sec. Then the power factor is calculated on each phase according to the following equation:

$$APF = \frac{AWATT\ accumulated\ over\ 1.024\ sec}{AVA\ accumulated\ over\ 1.024\ sec}$$

The sign of the APF calculation follows the sign of AWATT.

To calculate what quadrant the energy is in, look at the sign of the total or fundamental reactive energy in that phase along with the sign of the xPF or xWATT value, as indicated in Figure 60. The quadrants with capacitive power factors are indicated in dark gray whereas the quadrants with inductive power factor are indicated in light gray. Note that for most applications, the watts are received (imported) from the grid and so the active power and VAR stay within Quadrant I and Quadrant IV.

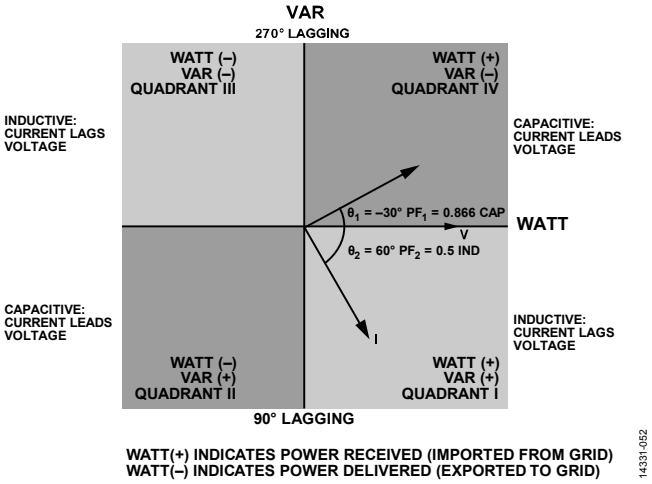


Figure 60. Active Power and VAR Sign for Capacitive and Inductive Loads

The power factor results is stored in 5.27 format. The highest power factor value is 0x07FF FFFF, which corresponds to a power factor of 1. A power factor of −1 is stored as 0xF800 0000. To determine the power factor from the xPF register value, use the following equation:

$$Power\ Factor = APF \times 2^{-27}$$

Energy Accumulation

Figure 61 shows how AWATT is accumulated into the AWATTHR and AWATT_ACC registers. A no load threshold is applied and the energy sign is checked to determine whether to accumulate the AWATT sample into the internal energy accumulator. The internal energy accumulator is either added to the AWATTHR register or latched depending on the EGY_LD_ACCUM setting at a EGYRDY rate (see the Reloading or Accumulating User Energy Register section for more details). The AWATT value is directly accumulated into the internal power accumulator and latched into AWATT_ACC at a PWRRDY rate. Set the EGY_PWR_EN bit in EP_CFG register to run the energy and power accumulator.

Signed Energy Accumulation Modes

Total Active Energy Accumulation Modes

In some installations, it is desirable to bill for only positive total active energy. The ADE9078 offers a way to do so using the WATTACC bits in the ACCMODE register. To set the total active energy accumulation and any corresponding CF pulse output for positive energy only, write 10 to WATTACC.

If WATTACC = 0, the energy accumulation is signed. The MSB of the AWATTHR_HI register indicates whether the energy is negative or positive.

Other accumulation modes include absolute accumulation mode with WATTACC = 01, where the absolute value of AWATT is accumulated, and negative only accumulation mode with WATTACC = 11, where only negative active energy is accumulated.

Reactive Energy Accumulation Modes

In some installations, because reactive energy may change frequently between positive and negative values with inductive and capacitive loads, it is desirable to bill for the absolute value of reactive energy. The ADE9078 offers a way to do so using the VARACC bits in the ACCMODE register. To set the total and fundamental reactive energy register and any corresponding CF pulse output to accumulate the absolute value of reactive energy, write 01 to VARACC.

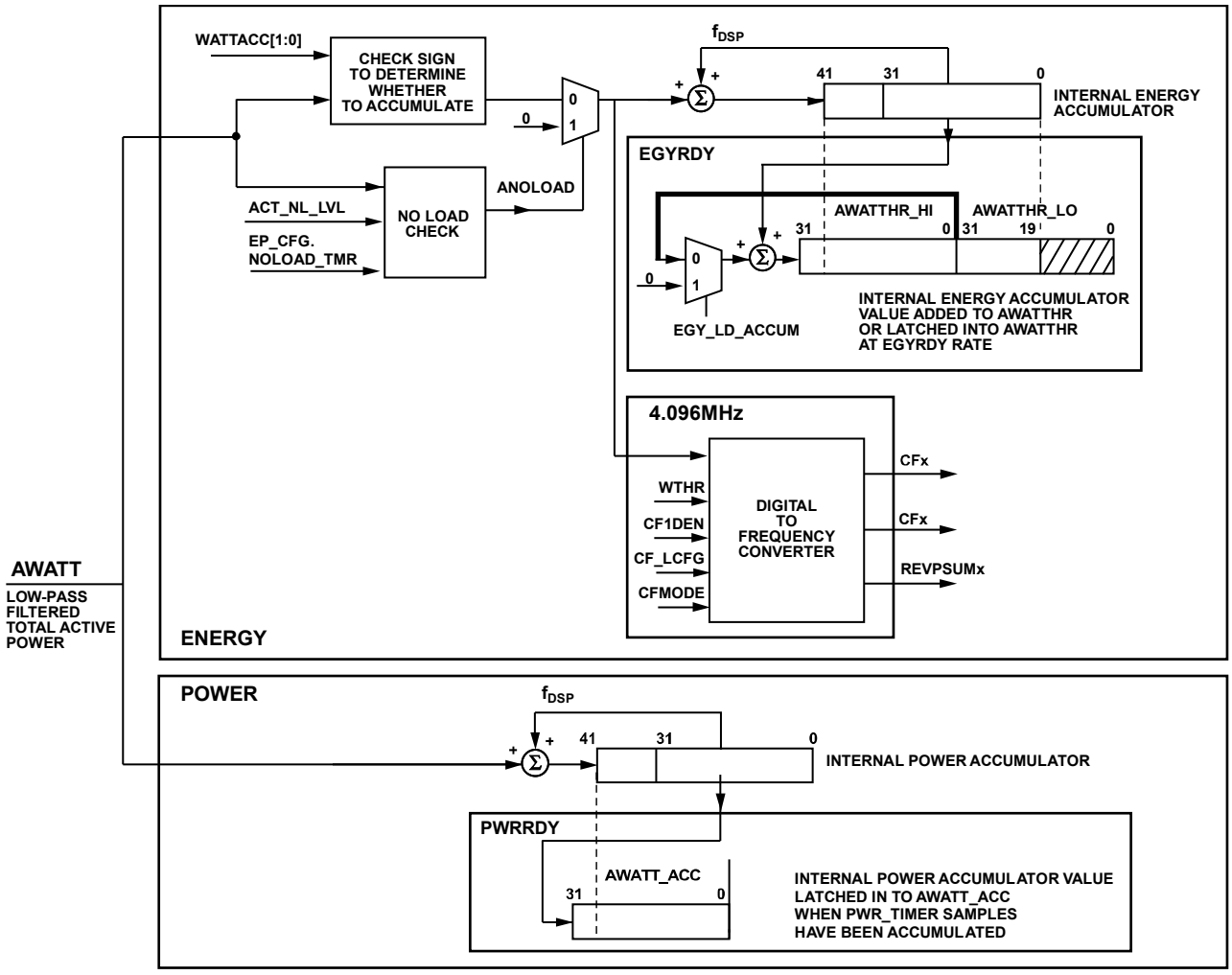


Figure 61. AWATT Accumulation into Energy and Power, Using No Load Threshold and Signed Accumulation Mode

If VARACC = 0, the total and fundamental reactive energy accumulation is signed. The MSB of the AVARHR_HI register indicates whether the energy is negative or positive.

Other accumulation modes offered include positive only accumulation mode with VARACC = 10, and negative only accumulation mode where only negative reactive energy is accumulated with VARACC = 11.

No Load Detection

No load detection prevents energy accumulation due to noise, when the input currents are below a given meter start current.

To determine if a no load condition is present, the ADE9078 evaluates if the accumulated energy is below a user defined threshold over a user defined time period. This no load detection is done on a per phase and per energy basis.

The NOLOAD_TMR bits in the EP_CFG register determine whether to evaluate the no load condition over 64 samples to 4096 samples (64/4 kSPS = 16 ms to 1.024 sec) by writing to the NOLOAD_TMR bits as described in Table 19. No load detection is enabled by default, over the minimum time of 64/4 kSPS = 16 ms. No load detection is disabled when the NOLOAD_TMR[2:0] bits in the EP_CFG register = 111b.

Table 19. No Load Condition Evaluation Time

NOLOAD_TMR	Samples to Evaluate in No Load Condition	Time That No Load Detection Is Evaluated (ms)
0	64	16
1	128	32
2	256	64
3	512	128
4	1024	256
5	2048	512
6	4096	1024
7	No load disabled	No load disabled

The user defined no load thresholds are written into the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers. The ACT_NL_LVL register sets the no load threshold for the total active energy. Correspondingly the REACT_NL_LVL register sets the no load threshold for total and fundamental reactive energy whereas the APP_NL_LVL sets the no load threshold for total apparent energy.

The no load thresholds are calculated according to the following equation:

$$xNL\_LVL = \left(\frac{xWATT\_FULL\_SCALE \times 64}{X} \right)$$

where:
xWATT_FULL_SCALE is the nominal xWATT value with full-scale inputs, 20,823,646. Note that xVAR and VA have the same scaling so the same value can be used for all three thresholds.
X is the desired no load input power level. For example, to set the no load threshold to zero out energy below 50,000 from full scale, X = 50,000.

Thus, for a 50,000:1 no load threshold level, xNL_LVL is 0x6804.

$$xNL\_LVL = \left(\frac{20{,}823{,}646 \times 64}{50{,}000} \right) = 26{,}654 = 0\text{x}681\text{E}$$

When a phase is in no load, every f_{DSP} = 4 kSPS, zero energy is accumulated into the energy registers and CF accumulation.

Note that the x_ACC registers are not affected by no load detection. Even when in no load, any power calculated in the respective xWATT, xVAR, and xVA registers is accumulated into the corresponding x_ACC register every f_{DSP} = 4 kSPS.

No Load Indications

The PHNOLOAD register indicates whether each phase of energy is in no load. For example, Bit 2 through Bit 0 in the PHNOLOAD register indicate whether Phase A total apparent energy, reactive energy, and active energy are in phase on Bit 2 through Bit 0, respectively. If a bit is set, it indicates that the phase energy is in no load—if it is clear, the phase is not in no load.

The user can enable an interrupt to occur when the no load status of one of the per phase energy changes, either going into or out of no load. There is an interrupt enable bit for each type of energy. Set the RFNOLOAD, VANLOAD, RNLOAD, and ANLOAD bits in the STATUS1 register to enable an interrupt on $\overline{\text{IRQ1}}$ when one or more phases of fundamental VAR, total VA, total VAR, and total active power no load changes status.

There is also an option to indicate the no load status on the $\overline{\text{EVENT}}$ pin (see the Interrupts/Events section for more information).

Figure 62 shows what happens when the xWATT, low-pass filtered active power value goes above the user configured, no load threshold and then back down below it again. The same concept applies to all of the energy values (total and fundamental VAR, total VA) with the corresponding REACT_NL_LVL and APP_NL_LVL no load thresholds.

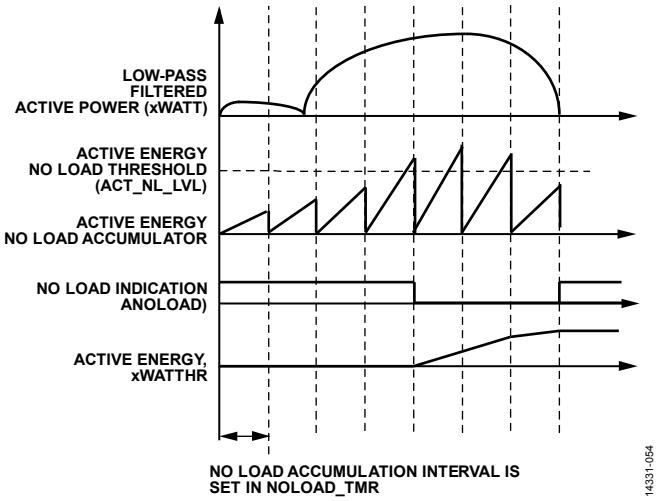


Figure 62. No Load Detection and Indication

Energy Accumulation Details

Internal Energy Register Overflow Rate

There are 42-bit internal signed energy accumulators for each phase of each energy accumulation, as shown in Figure 61. These accumulators update at a rate of f_{DSP} = 4 kSPS. To calculate the time until the internal accumulator overflows with full-scale inputs and all digital gain and offset factors at zero, use the following equation.

Maximum Internal Energy Accumulator Time (sec) =

$$\left(\frac{2^{41}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right)$$

where *AWATT_AT_FULL_SCALE* refers to the nominal AWATT value with full-scale inputs.

For example, with MTEN = 0, for single-point gain compensation and AIGAIN, AVGAIN, APGAIN, and AWATTOS all equal to zero, the Phase A total active energy has a digital gain of 1. Thus, the Phase A total active energy accumulated in the internal accumulator overflows in 26.4 sec with the nominal full-scale AWATT value of 20,823,646.

Maximum Internal Energy Accumulator Time (sec) =

$$\left(\frac{2^{41}}{20{,}823{,}646 \times 4000}\right) = 26.4 \text{ sec}$$

User Energy Register Update Rate, EGYRDY

As shown in Figure 61, the internal energy accumulator is latched into a user accessible energy register or added to a user accessible register at a rate of EGYRDY. Figure 63 further shows how the EGYRDY update rate is generated.

The EGYRDY update rate occurs after EGY_TIME + 1 f_{DSP} samples or EGY_TIME + 1 half line cycles, according to the EGY_TMR_MODE bit in the EP_CFG register.

If EGY_TMR_MODE = 0, select the sample-based accumulation as follows:

Internal Energy Accumulator Time (sec) =

$$\left(\frac{EGY\_TIME + 1}{f_{DSP}}\right)$$

The EGY_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/4000 = 2.048 sec if EGY_TMR_MODE = 0.

Internal Energy Accumulator Time (sec) =

$$\left(\frac{8191+1}{4000}\right) = 2.048 \text{ sec}$$

If EGY_TMR_MODE = 1, select the half line cycle-based accumulation as follows:

Internal Energy Accumulator Time (sec) =

$$\left(\frac{EGY\_TIME + 1}{ZX\_RATE}\right)$$

With a 50 Hz line frequency and a zero-crossing interrupt rate of 100 Hz, the maximum accumulation time is 81.92 sec with EGY_TIME equal to 0x1FFF (8191d).

Internal Energy Accumulator Time (sec) =

$$\left(\frac{8191+1}{100}\right) = 81.92$$

If EGY_TMR_MODE = 1, the zero-crossing source to monitor is selected in the ZX_SEL bits in the ZX_LP_SEL register, as shown in Figure 63.

Note that the internal energy register overflows in 26.4 sec with full-scale inputs so EGY_TIME must be set lower than 2640d to prevent overflow when EGY_TMR_MODE = 1.

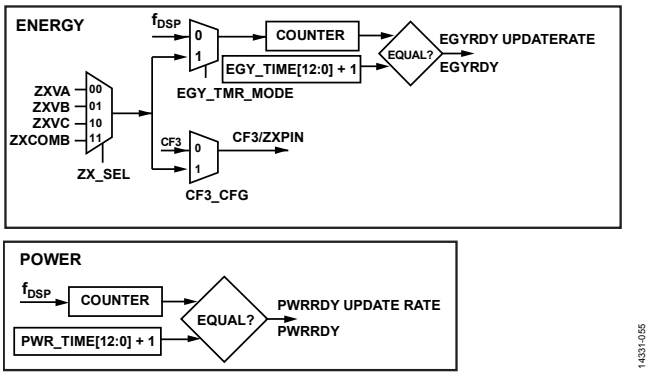


Figure 63. EGYRDY and PWRRDY Update Rates

Reloading or Accumulating User Energy Register

When an EGYRDY event happens, the internal energy accumulation is either directly loaded into the xWATTHR register or added to the existing accumulation based on the state of the EGY_LD_ACCUM bit in the EP_CFG register.

If EGY_LD_ACCUM = 0, the internal energy register is added to the user accessible energy register. If EGY_LD_ACCUM = 1, the internal energy register overwrites the user accessible energy register.

Finally, the internal energy accumulator resets and starts counting again from zero.

User Energy Register Overflow Rate

There are 45-bit user accessible signed energy accumulators for each phase of each energy accumulation. These accumulators update at a rate according to EGYRDY, as described in the User Energy Register Update Rate, EGYRDY section. The following equation shows how to calculate the time until the user accessible accumulator overflows with full-scale inputs and all digital gain and offset factors at zero. For this example, assume that the energy register is updating at every f_{DSP} = 4 kSPS sample.

Maximum User Energy Accumulator Time (sec) =

$$\left(\frac{2^{44}}{AWATT\_AT\_FULL\_SCALE \times f_{DSP}}\right)$$

where *AWATT_AT_FULL_SCALE* refers to the nominal AWATT value with full-scale inputs.

For example, with MTEN = 0, for single-point gain compensation and AIGAIN, AVGAIN, APGAIN, and AWATTOS all = 0, the Phase A total active energy has a digital gain of 1. Then, the Phase A total active energy, accumulated in the user accessible accumulator, overflows in 211 sec with the nominal full-scale AWATT value of 20,823,646.

$$\textit{Maximum User Energy Accumulator Time}\ (\text{sec}) = \left(\frac{2^{44}}{20{,}823{,}646 \times 4000}\right) = 211\ \text{sec}$$

Accessing the User Energy Registers

Each 45-bit user accessible signed energy accumulator is divided into two registers: a register containing the 32 MSBs, xHR_HI, and a register containing the 13 LSBs, xHR_LO, as shown in Figure 64.

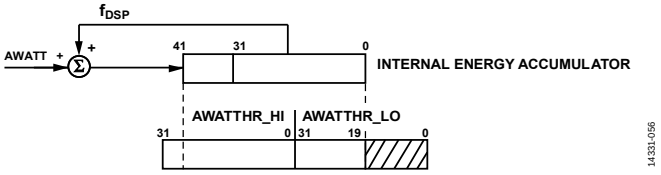


Figure 64. Internal Energy Register to AWATTHR_HI and AWATTHR_LO

The expected user energy accumulation can be calculated according to the following formula based on the average AWATT value:

$$\textit{User Energy Accumulation} = AWATT \times (EGY\_TIME + 1)$$

Then, AWATTHR_HI contains 32 MSBs, which can be calculated by rounding the following equation down to the nearest whole number:

$$AWATTHR\_HI = \text{ROUNDDOWN}(\textit{User Energy Accumulation} \times 2^{-13})$$

where ROUNDDOWN() is a function to round down to the nearest integer.

Finally, AWATTHR_LO is calculated based on the two previous values, as follows:

$$AWATTHR\_LO = (\textit{User Energy Accumulation} - AWATT\_EGY\_USER\_HI \times 2^{13}) \times 2^{19}$$

For example, if 4000 samples of AWATT are accumulated, with full-scale inputs, the expected value of AWATTHR_HI is 0x009B 25F4 and AWATTHR_LO is 0xE600 0000.

$$\textit{User Energy Accumulation} = 20{,}823{,}646 \times (3999 + 1) = 83{,}294{,}584{,}000$$

$$AWATTHR\_HI = ROUNDDOWN(83{,}294{,}584{,}000 \times 2^{-13}) = 10{,}167{,}795 = 0x009B\ 25F3$$

$$AWATTHR\_LO = (83{,}294{,}584{,}000 - 10{,}167{,}795 \times 2^{13}) \times 2^{19} = 3{,}858{,}759{,}680 = 0xE600\ 0000$$

To determine the consumption in watthours, the meter is calibrated using the xIGAIN, xVGAIN, and xPGAIN registers. Then, xWATTHR_HI × watthour/LSB = watthour. The watthour/LSB constant is the same for all meters.

Read User Energy Register with Reset

If the RD_RST_EN bit is set in the EP_CFG register, when a user accessible energy register is read, its contents are reset.

For example, if AWATTHR_HI is read, the AWATTHR_HI register value goes to zero. The AWATTHR_LO register contents are not modified.

It is not recommended to read the xHR_LO registers with reset.

User Energy Register Use Models

There are three main use models for energy accumulation, as follows:

- Read the energy register with reset
- Accumulate energy over a defined number of line cycles
- Accumulate energy over a defined number of samples

To read the energy register with reset, use the following settings:

- Set the configuration register as follows:
  - EGY_LD_ACCUM = 0
  - EGY_TMR_MODE = 0
  - RD_RST_EN = 1
  - EGY_PWR_EN = 1
  - EGY_TIME = 1
- For the output, read only the xHR_HI register, which has enough resolution for most applications. The xHR_LO register is maintained and accumulated and does not need to be read by the user.
- Set the maximum time before reading xHR_HI to prevent overflow with full-scale inputs to 211 sec.

To accumulate energy over a defined number of line cycles, use the following settings:

- Set the configuration register as follows:
  - EGY_LD_ACCUM = 1
  - EGY_TMR_MODE = 1
  - RD_RST_EN = 0
  - EGY_PWR_EN = 1
  - EGY_TIME to the desired number of half line cycles
- For the output, the xHR_HI register has enough resolution for most applications. To maintain perfect synchronization with the CF pulse output, the xHR_LO must be read as well because it is cleared at every EGYRDY cycle.
- Set the maximum time before reading xHR_HI to prevent overflow with full-scale inputs to 26.4 sec.

To accumulate energy over a defined number of samples, use the following settings:

- Set the configuration register as follows:
  - EGY_LD_ACCUM = 1
  - EGY_TMR_MODE = 0
  - RD_RST_EN = 0
  - EGY_PWR_EN = 1
  - EGY_TIME to the desired number of samples
- For the output, the xHR_HI register has enough resolution for most applications. To maintain perfect synchronization with the CF pulse output, the xHR_LO must be read as well because it is cleared at every EGYRDY cycle.
- Set the maximum time before reading xHR_HI to prevent overflow with full-scale inputs to 26.4 sec.

Digital to Frequency Conversion—CFx Output

Many electricity meters are required to provide a pulse output that is proportional to the energy being accumulated, with a given pulse per kWh meter constant.

The ADE9078 includes four pulse outputs that are proportional to the energy accumulation in the CF1 through CF4 output pins. A block diagram of the CFx pulse generation is shown in Figure 65.

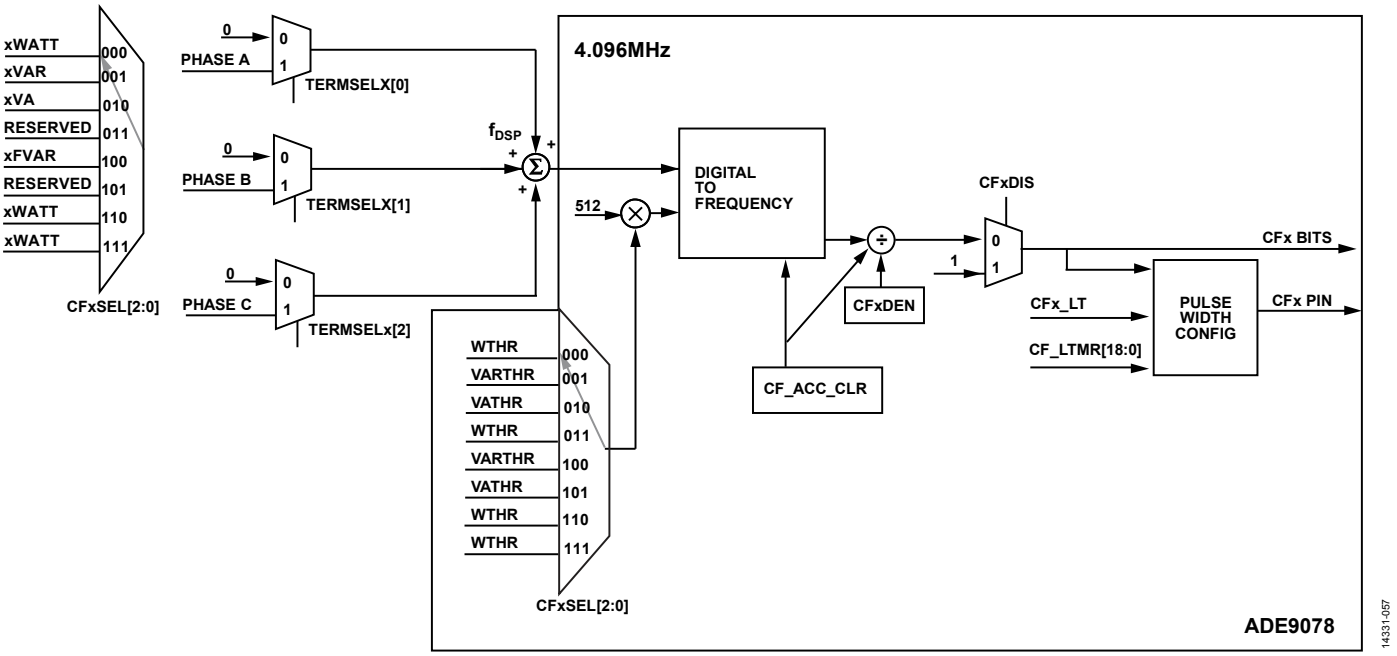


Figure 65. Digital to Frequency Conversion for CFx

Table 20. CFx Active Low Pulse Width and Duty Cycle Based on CFx_LT and CF_LTMR

CFx_LT	Active Low Pulse Width for Low Frequencies (ms)	Active Low Pulse Width for High Frequencies when CFxDEN is Even	Active Low Pulse Width for High Frequencies when CFxDEN is Odd	Behavior when Entering No Load
0	80	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, finish current pulse, return high.
1	CF_LTMR × 6/CLKIN × 1000	50%	(1 + 1/CFxDEN) × 50%	If CFx is low, keep CFx low until the no load state is finished.

Energy and Phase Selection

The CFxSEL[2:0] bits in the CFMODE register select which type of energy to output on the CFx pin, including total active power, VAR, VA, or fundamental VAR. The TERMSELx bits in the COMPMODE register select which phase energies to include in the CFx output.

For example, with CF1SEL = 000 and TERMSEL1 = 111, CF1 indicates the total active power output of Phase A, Phase B, and Phase C.

To calibrate the Phase A, Phase B, and Phase C total active power accumulation at the same time, using CF1 for total AWATT, CF2 for total BWATT, and CF3 for total CWATT, configure TERMSEL1 = 010, and TERMSEL2 = 100.

Configuring the Maximum CF Pulse Output Frequency

The xTHR registers determine the maximum output rate from the digital to frequency converter. It is recommended to write xTHR = 0x0010 0000. After the CFxDEN pulses are generated, a CFx pulse is issued. CFxDEN can range from 2 to 65,535. The relationship between the xTHR, CFxDEN, and AWATT values is given in the following equation:

$$CF(\text{Hz}) = \left(\frac{f_{DTOF} \times AWATT}{xTHR \times 512 \times CFxDEN} \right)$$

where:
f_{DTOF} is 4.096 MHz.
AWATT is the value at full scale, 20,823,646.
xTHR is 0x0010 0000.
CFxDEN is 2.

The maximum recommended CF pulse output frequency is 79.4 kHz.

$$Maximum\ CF\ (\text{Hz}) = \left(\frac{4.096 \times 10^6 \times 20{,}823{,}646}{0\,\text{x}\,0010\ 0000 \times 512 \times 2} \right) = 79.4\ \text{kHz}$$

The default CFx pulse output using power on reset values of xTHR and CFxDEN with full-scale inputs is

$$Maximum\ CF\ (\text{Hz}) = \left(\frac{4.096 \times 10^6 \times 20{,}823{,}646}{0\,\text{x}\,0000\ \text{FFFF} \times 512 \times 0\,\text{x}\,\text{FFFF}} \right) = 38.8\ \text{Hz}$$

Configuring the CF Pulse Width

The pulse width is determined by the CFx_LT bit in the CF_LCFG register and the CF_LTMR register value.

When CFx_LT = 0, the active low pulse width is set at 80 ms for frequencies lower than 1/(2 × 80 ms) = 6.25 Hz. For higher frequencies, the duty cycle is 50% if CFxDEN is even or (1 + 1/CFxDEN) × 50% if CFxDEN is odd.

If CFx_LT is set to 1, the CF active low pulse width is CF_LTMR × 6/CLKIN. The maximum CF_LTMR value is 327,680 = 0x0005 0000, which results in a 327,680/(6/CLKIN) = 80 ms pulse. CF_LTMR must be greater than zero.

CFx Pulse Sign

Some applications must record positive and negative energy usage separately. To enable this operation, the SUMxSIGN bits in the PHSIGN register indicate whether the sum of the energy that went into the last CFx pulse was positive or negative. SUMxSIGN = 0 if the sum of the energy that went into the CFx pulse is positive and equal to one if the sum of the energy was negative.

Additionally, the REVPSUMx bits in the STATUS0 register and EVENT_STATUS register indicate if the CFx polarity changed sign. For example, if the last CF2 pulse was positive reactive energy and the next CF2 pulse is negative reactive energy, the REVPSUM2 bit in the STATUS0 and EVENT_STATUS registers is set, which can be enabled to generate an interrupt on IRQ0.

Clearing the CFx Accumulator

The user may want to clear out a partial CFx accumulation, for example, during the power up and initialization process. To clear the accumulation in the digital to frequency converter and CFDEN counter, write 1 to the CF_ACC_CLR bit in the CONFIG1 register. The CF_ACC_CLR bit automatically clears itself.

Disabling the CFx Pulse Output and CFx Interrupt

To disable the CFx pulse output and keep the CFx output high, write a one to the CFxDIS bit in the CFMODE register. If the CFxDIS bit in the CFMODE register is set, the CFx bit in STATUS0 is not set when a new CFx pulse is ready. Note that the REVPSUMx bits, which indicate if CFx pulses were positive or negative, are not affected by the CFxDIS setting.

MEASUREMENTS (PSM1)

Overview

It is possible to tamper an energy meter by disconnecting the voltage inputs or the neutral. Some regions require monitoring of the current inputs for several days after the voltage inputs to the meter have been cut, to check for this kind of tamper condition. The PSM1 and PSM2 operating modes in conjunction with PSM3 enable low power consumption when checking for and billing for a tamper of this kind.

PSM1 enables fast measurement of IRMS, VRMS, active power, and VAR with a reduced set of functions compared to PSM0.

To measure using PSM1, change the PM1 and PM0 pins to 0 and 1, respectively, to select the PSM1 operating mode. Then, configure the IC by writing to the xIGAIN, xVGAIN, and xPGAIN registers. Write to the run register to start the measurements. To achieve the specified accuracy, stay in PSM1 mode for the time indicated in Table 8 before reading the measurement results via the SPI port (see the PSM1 Startup Flow section for detailed information).

After the PSM1 results are read, change the PM1 and PM0 pins to 1 and 1, respectively, to enter PSM3 for one minute. Then, enter PSM1 by making PM1 and PM0 pins equal to 1 and 0, respectively, to make measurements and begin the process again.

IRMS, VRMS, and Active Power VAR

The PSM1 mode uses a different computation method than is done in PSM0. These measurements are computed over 20 ms. Table 1 gives the expected accuracy achieved 40.5 ms after setting the run register. Figure 66 shows the current channel datapath for the ADE9078 PSM1.

To calibrate these measurements, write the xIGAIN, xVGAIN, and xPGAIN registers before writing the run register to start the calculation. Note that this measurement is updated every 10 ms. There is an option to enable the RMSRDY interrupt in MASK0 to indicate when this result is ready. This interrupt occurs every 10 ms; thus, several interrupts are required to reach 40 ms for the specified accuracy.

Note that these PSM1 IRMS, VRMS, active power, and VAR measurements are total bandwidth measurements—they are done over the whole measurement bandwidth given in Table 1.

PSM1 Startup Flow from PSM2 and PSM3

To start up PSM1 from PSM2 and PSM3, follow these steps:

1. Wait for the RSTDONE interrupt indicated by the $\overline{\text{IRQ1}}$ pin going low.
2. Configure the xIGAIN, xVGAIN, and xPGAIN registers via the SPI to calibrate the measurements.
3. Write run = 1.
4. Wait 40.5 ms, then read the results in the xIRMS, xVRMS, xWATT, and xVAR registers.
5. Optionally, enable the RMSRDY interrupt in MASK0 to indicate when this result is ready. This interrupt occurs every 10 ms; thus, several interrupts are required to reach 40 ms for the specified accuracy.

PSM1 Startup Flow from PSM0

To start up PSM1 from PSM0, follow these steps:

1. If the voltage sags, the host microcontroller changes the PM1 and PM0 pins to 0 and 1, respectively, to change to the PSM1 measurement mode.
2. The configured values in the xIGAIN, xVGAIN, and xPGAIN registers remain valid.
3. Wait 40.5 ms, then read the results in the xIRMS, xVRMS, xWATT, and xVAR registers.
4. Optionally, enable the RMSRDY interrupt in MASK0 to indicate when this result is ready. This interrupt occurs every 10 ms; thus, several interrupts are required to reach 40 ms for the specified accuracy.

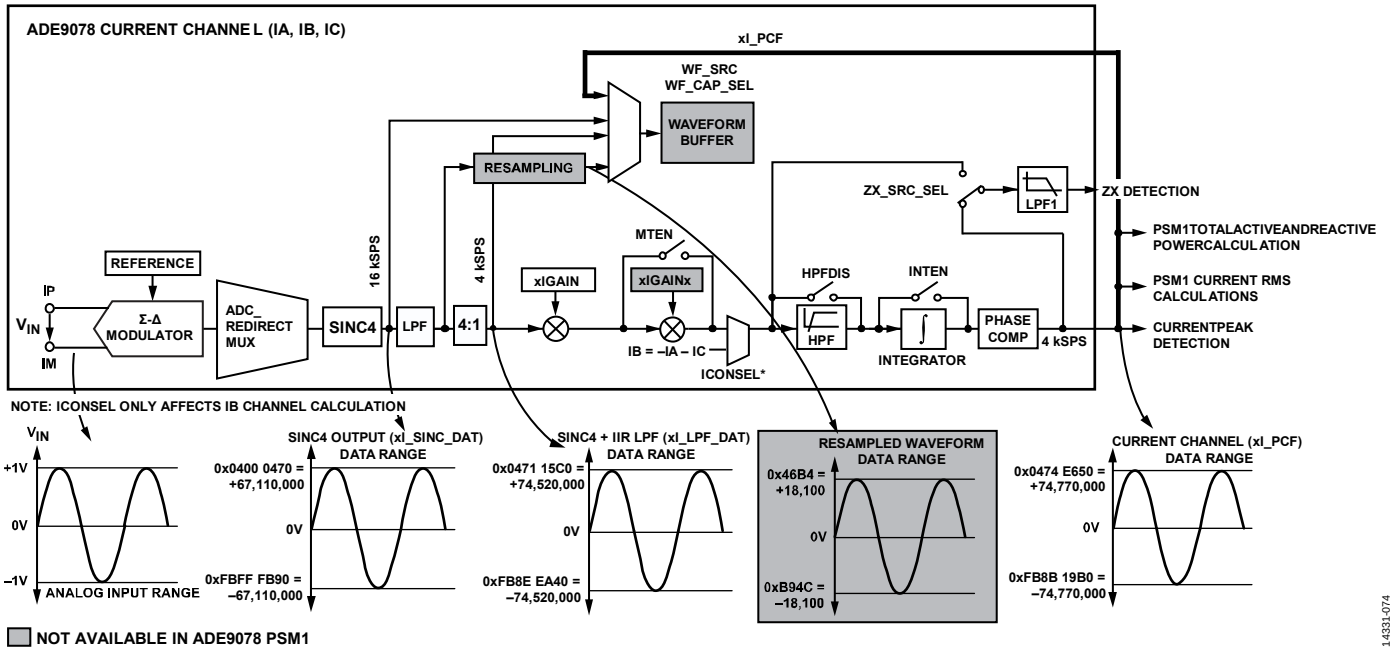


Figure 66. Current Channel PSM1 Datapath

Power Accumulation

Figure 61 shows how AWATT low-pass filtered active power samples are accumulated to provide an accurate active power value in the AWATT_ACC register. The sign of the Phase A total active power accumulation is monitored in the REVAPA bit and interrupts can be enabled if the power changes sign. There are corresponding x_ACC accumulations for each power on each phase and REVx status bits in the STATUS0 register to indicate if the power changes sign.

Power Accumulation Details

Figure 61 shows how AWATT values are accumulated into an internal power accumulator and then are latched into the xWATT_ACC register at a rate of PWRRDY.

PWRRDY is set after (PWR_TIME + 1) 4 kSPS samples accumulate. The power accumulation time can be calculated according to the following equation:

$$\textit{Internal Power Accumulation Time} \text{ (sec)} = \left(\frac{PWR\_TIME + 1}{4000}\right)$$

The PWR_TIME[12:0] register allows up to (8191 + 1) = 8192 samples to be accumulated, which corresponds to 8192/4000 = 2.048 sec.

$$\textit{Internal Power Accumulation Time} \text{ (sec)} = \left(\frac{8191 + 1}{4000}\right) = 2.048 \text{ sec}$$

The internal power accumulator overflows at the same rate as the internal energy accumulator (see the Internal Energy Register Overflow Rate section).

Accessing the User Power Registers

The user accessible signed power accumulator is a 32-bit register that contains 32 MSBs of internal power accumulator, x_ACC, as shown in Figure 67.

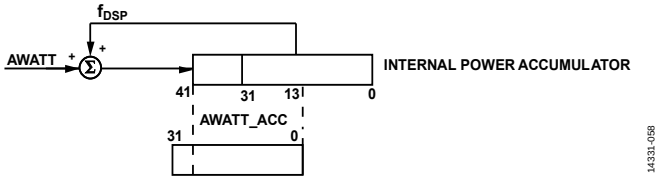


Figure 67. Internal Power Register to AWATT_ACC

Calculate the expected AWATT_ACC according to the following formula based on the average AWATT value:

$$\textit{Internal Power Accumulation} = AWATT \times (PWR\_TIME + 1)$$

Thus, AWATT_ACC is the 32 MSBs, which can be calculated by rounding the following equation down to the nearest whole number:

$$AWATT\_ACC = \text{ROUNDDOWN}(\textit{User Power Accumulation} \times 2^{-13})$$

where ROUNDDOWN()is a function to round down to the nearest integer.

For example, if 4000 samples of AWATT are accumulated at 4 kSPS with full-scale inputs, the expected value of AWATT_ACC is 0x009B 0003.

$$\textit{User Power Accumulation} = 20{,}823{,}646 \times (3999 + 1) = 83{,}294{,}584{,}000$$

$$AWATT\_ACC = \text{ROUNDDOWN}(83{,}294{,}584{,}000 \times 2^{-13}) = 10{,}167{,}795 = 0\text{x}009\text{B } 25\text{F}3$$

Note that W/LSB varies with PWR_TIME accumulation time.

Power Sign Detection

The REVRPC, REVRPB, REVRPA, REVAPC, REVAPB, and REVAPA bits in the STATUS0 register allow the user to monitor if the active or reactive power on any phase has changed sign.

The PWR_SIGN_SEL bit allows the user to select whether the power sign change follows the total or fundamental energies. To track total active power, set the REVAPx power sign status bits, PWR_SIGN_SEL = 0. To track fundamental VAR on the REVRPx bits, write PWR_SIGN_SEL = 1.

The CVARSIGN, CWSIGN, BVARSIGN, BWSIGN, AVARSIGN, and AWSIGN bits in the PHSIGN register indicate whether the total or fundamental VAR selected in the PWR_SIGN_SEL bit is positive or negative.

The power signs are updated at the same time as the xWATT_ACC, xVAR_ACC, and xFVAR_ACC registers and correspond to the sign of these registers. Note that the power registers and signs are updated after the number of 4 kSPS samples configured in the PWR_TIME register have elapsed, from 500 µs to 2.048 sec. The power sign change indication in the REVxPx bits are updated at the same time (see the Power Accumulation Details section for more information).

The ADE9078 allows the user to accumulate total active power and VAR powers into separate positive and negative registers: PWATT_ACC and NWATT_ACC, PVAR_ACC and NVAR_ACC. This accumulation is done by evaluating the AWATT, low-pass filtered active power every 4 kSPS. If AWATT is positive, it is added to the PWATT_ACC accumulation. If AWATT is negative, the absolute value is added to the NWATT_ACC accumulation. A new accumulation from zero begins after the power update interval set in PWR_TIME has elapsed. The positive and negative total active power and total VAR from all three phases are added into the positive/negative active power and VAR accumulations.

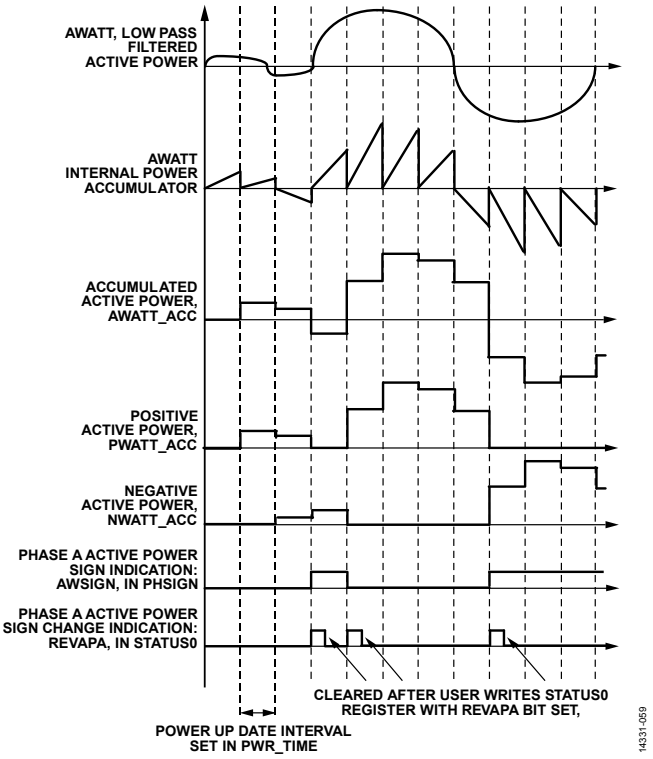


Figure 68. Power Accumulation and Power Sign

Zero-Crossing Detection

The ADE9078 offers zero-crossing detection on the VA, VB, VC, IA, IB, and IC input signals. The neutral current channel, IN, does not contain a zero-crossing detection circuit. Figure 69 shows the current and voltage channel datapaths preceding zero-crossing detection. The zero-crossing circuit is the time base for resampling, line period, angle measurements, and energy accumulation using line cycle accumulation mode. The xV_PCF and xI_PCF are the voltage and current channel waveforms processed by the DSP, which can be stored into the waveform buffer at a 4 kSPS data rate (see the Waveform Buffer section for more information).

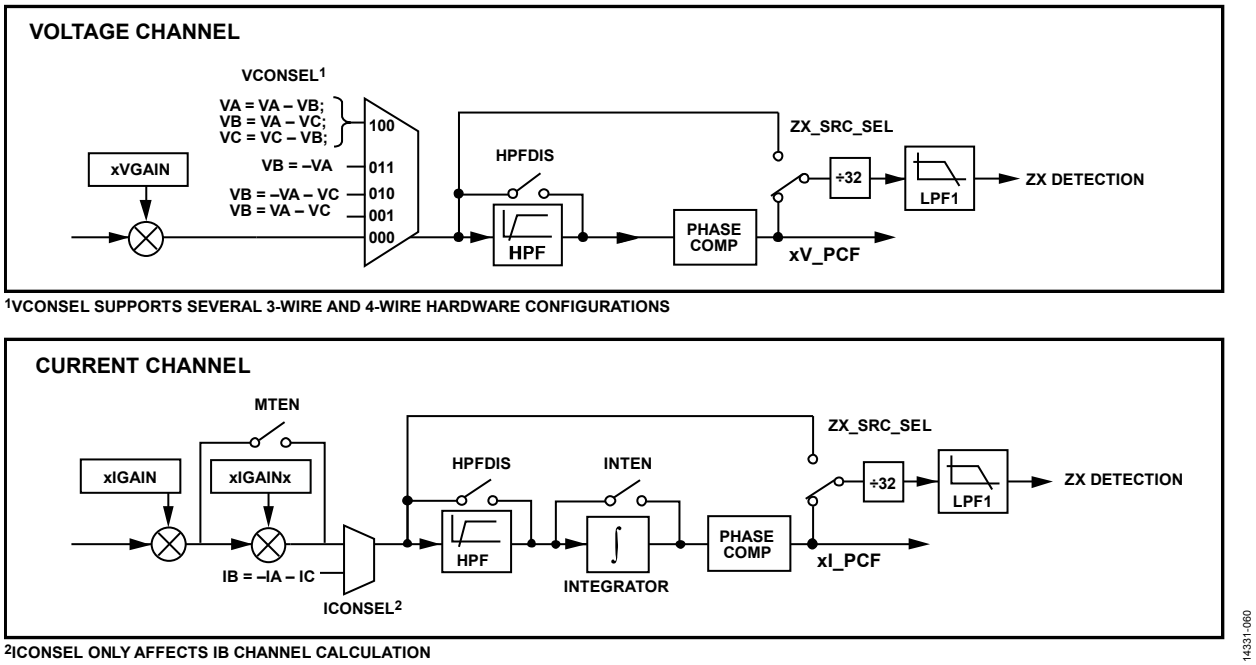


Figure 69. Voltage and Current Channel Signal Chain Preceding Zero-Crossing Detection

The ZX_SRC_SEL in the CONFIG0 register sets whether data going into the zero-crossing detection circuit comes before or after the high-pass filter, integrator, and phase compensation. By default, the data after phase compensation is used. Note that the high-pass filter has settling times given in Table 10. Thus, for a fast response, it is recommended to set ZX_SRC_SEL to look for a zero crossing before the high-pass filter. If the high-pass filter is disabled with HPFDIS = 1 or if ZX_SRC_SEL = 1, note that a dc offset on the input may cause the time between negative to positive and positive to negative zero crossings and positive to negative to negative to positive zero crossings to change, indicating that the ZX detection does not have a 50% duty cycle.

The current and voltage signals are low-pass filtered to remove harmonics. The low-pass filter, LPF1, has a corner of 85 Hz and the equation is as follows:

$$H(z) = \frac{2^{-3}}{1-(1-3)z^{-1}}$$

The low-pass filter settling time is 51 samples, 51/4 kSPS, which results in 12.75 ms.

Figure 70 shows the delay between the detected zero-crossing signal and the input. Note that there is a 4.3 ms delay between the input signal zero crossing and the ZX zero crossing indication, with a 50 Hz input signal. Zero crossings are generated on both negative to positive and positive to negative transitions.

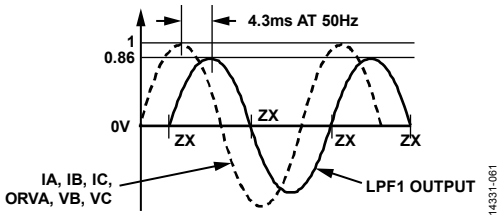


Figure 70. Zero Crossing Detection on Voltage and Current Channels

To provide protection from noise, voltage channel zero-crossing events (ZXVA, ZXVB, and ZXVC) are not generated if the absolute value of the LPF1 output voltage is smaller than the threshold, ZXTHRSH. The current channel zero-crossing detection outputs (ZXIA, ZXIB, and ZXIC) are active for all input signals levels.

Calculate the voltage channel zero-crossing threshold, ZXTHRSH, from the following equation:

$$ZXTHRSH = \frac{(V\_PCF\ at\ Full\ Scale) \times (LPF1\ Attenuation)}{X \times 32 \times 2^8}$$

where:
V_PCF at Full Scale is ±74,680,000d.
LPF1 Attenuation is 0.86 at 50 Hz, and 0.81 at 60 Hz, the gain attenuation of the LPF1 filter.
X is the dynamic range below which the voltage channel zero-crossing must be blocked.

For example, assume that the full-scale input corresponds to 440 V rms. To prevent signals 100× lower than full scale (signals smaller than 4.4 V rms) from generating a voltage channel zero-crossing output, set ZXTHRSH to 78d.

$$ZXTHRSH = \frac{(74{,}680{,}000) \times (0.86)}{100 \times 32 \times 2^8} = 78\,\text{d}$$

Additionally, to prevent false zero crossings after a zero crossing is generated, 1 ms must elapse before the next zero crossing can be output.

Combined Voltage Zero Crossing

Phase A, Phase B, and Phase C voltage channel signals are combined to generate one zero-crossing signal, ZX_COMB, which is stable even if one or more phases drops out.

The input to the zero-crossing detection is (VA + VB − VC)/2 with the signal chain corresponding to Figure 71. As described in the Applications Information section, the ADE9078 can meter different polyphase configurations. The VCONSEL bits indicate this selection. If VCONSEL is not equal to 0, the VB component in the combined zero-crossing circuit is set to zero.

Use the same precautions to prevent noise from generating zero-crossing interrupts on this output. As described in the Zero-Crossing Detection section, signals below the ZXTHRSH threshold do not generate ZXCOMB outputs, and a minimum of 1 ms is required between ZXCOMB generations.

Zero-Crossing Output Rates

Seven zero-crossing detection circuits monitor the IA, IB, IC, VA, VB, VC, and the combined (VA + VB − VC)/2 signals. The zero-crossing detection circuits have two output rates: 4 kSPS and 512 kSPS. The 4 kSPS zero-crossing signal is used to calculate the line period, sent to the ZXx bits in the STATUS1 register, and is monitored by the zero-crossing timeout, phase sequence error detection, resampling, and energy accumulation functions. The 512 kSPS signal is used for angle measurements and is output on the CF3/ZX pin if the CF3_CFG bit in the CONFIG1 register = 1.

Table 21 indicates which zero-crossing edges (negative to positive and positive to negative) are used for each function and indicates what happens if a zero crossing is blocked because the input signal is below the user configured ZXTHRSH.

The CF3/ZX output pin goes from low to high when a negative to positive transition is detected and from high to low when a positive to negative transition occurs. The ZX_SEL bits in the ZX_LP_SEL register select the zero-crossing output used for line cycle energy accumulation and the ZX output pin.

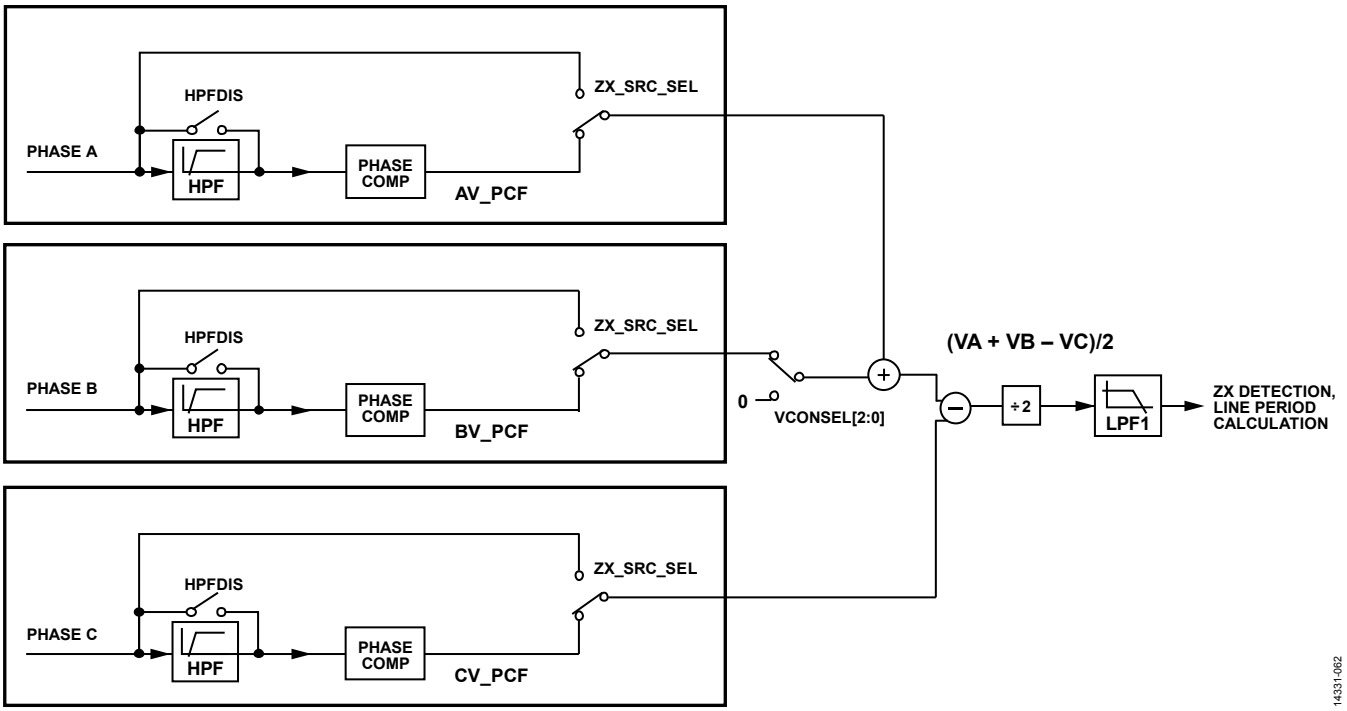


Figure 71. Combined Zero-Crossing Detection

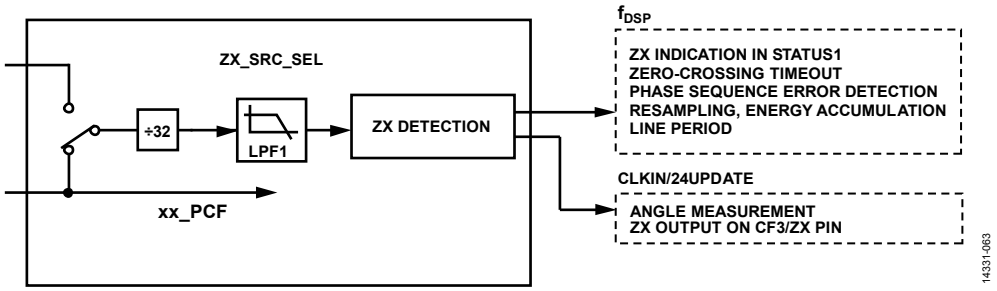


Figure 72. Zero-Crossing Output Rates

Table 21. Zero Crossing Use in Other Functions

Functions Using Zero Crossing	ZX Transitions Used	Corresponding STATUS1 Bits	Selecting Which Phase to Use for Measurement	Effect if ZX Does Not Occur
ZX Indication in STATUS1 Register	Negative to positive and positive to negative	ZXIA, ZXIB, ZXIC, ZXVA, ZXVB, ZXVC, and ZXCOMB	Not applicable	The ZXx bit is latched in STATUS1. If it is cleared, it is not set again. A ZXx interrupt does not occur.
Zero-Crossing Timeout	Negative to positive and positive to negative	ZXTOVA, ZXTOVB, and ZXTOVC	Not applicable	Zero-crossing timeout is indicated by the ZXTOVx bits in the STATUS1 register and an interrupt can be enabled to occur.
Phase Sequence Error Detection	Depends on VCONSEL setting	SEQERR	Not applicable	If one to two ZX events are missing, SEQERR is generated. If all ZX events are missing, the SEQERR bit is not set.
Energy Accumulation	Negative to positive and positive to negative	Not applicable	ZX_SEL selects the zero-crossing output used for line cycle energy accumulation and ZX output pin	Line cycle accumulation does not update.
Line Period Measurement	Negative to positive	Not applicable	One line period measurement per phase (APERIOD, BPERIOD, CPERIOD, COMPERIOD)	Coerced to default value of 0x00500000 if SELFREQ = 0 for a 50 Hz network or 0x0042AAAB if SELFREQ = 1 for a 60 Hz network.

Functions Using Zero Crossing	ZX Transitions Used	Corresponding STATUS1 Bits	Selecting Which Phase to Use for Measurement	Effect if ZX Does Not Occur
Resampling	None	Not applicable	LP_SEL selects the phase voltage line period used as the basis for resampling calculation	If the line period used for resampling is invalid because zero crossings are not detected or the calculation results in something outside a 40 Hz to 70 Hz range, the line period used for resampling is coerced to the default line period of 0x00500000 if SELFREQ = 0 for a 50 Hz network, or 0x0042AAAB if SELFREQ = 1 for a 60 Hz network.
Angle Measurements	Negative to positive	Not applicable	Not applicable	The register does not update, keeps last value.
ZX Output on the CF3/ZX Pin	Negative to positive and positive to negative	Not applicable	ZX_SEL selects the zero-crossing output used for line cycle energy accumulation and the ZX output pin	The ZX output remains at the current state, high or low.

Zero-Crossing Timeout

The zero-crossing timeout feature alerts the user if a zero-crossing event is not generated after a user configured amount of time. If a zero crossing event is not received after ZXTOUT/4 kSPS clocks, the corresponding ZXTOx bit in the STATUS1 register is set. For example, if ZXTOUT is equal to 4000, if a zero crossing is not received on Phase A for 4000/4 kSPS = 1 sec, the ZXTOA bit is set in the STATUS1 register. The maximum value that can be written to the ZXTOUT register is 0xFFFF/4000 = 16.38 sec.

Line Period Calculation

The ADE9078 line period measurement is performed by taking the values low-pass filtered by LPF1 as described in the Zero-Crossing Detection section and then using the two values near the negative to positive zero crossing (POS1 and POS2) to calculate the exact zero-crossing point using linear interpolation. Use this information to calculate the line period precisely, which is stored in the xPERIOD register.

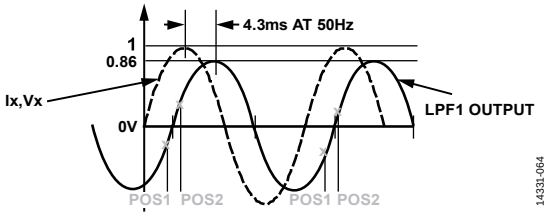


Figure 73. Line Period Calculation Using Zero-Crossing Detection and Linear Interpolation

The line period, t_L, can be calculated from the xPERIOD register, according to the following equation:

$$t_L = \frac{xPERIOD + 1}{4000 \times 2^{16}} (\text{sec})$$

Similarly, the line frequency can be calculated from the xPERIOD register using the following equation:

$$f_L = \frac{4000 \times 2^{16}}{xPERIOD + 1} (\text{Hz})$$

With a 50 Hz input, the xPERIOD register is 0x0050 0000, 5242880d, and with a 60 Hz input, it is 0x0042 AAAA = 4369066d.

If the calculated period value is outside the range of 40 Hz to 70 Hz, or if the negative to positive zero crossings for that phase are not detected, the xPERIOD register is coerced to correspond to 50 Hz or 60 Hz, according to the setting of the SELFREQ bit in the ACCMODE register. With SELFREQ = 0 for a 50 Hz network, xPERIOD register is coerced to 0x0050 0000. If SELFREQ = 1, indicating a 60 Hz network, the xPERIOD register is coerced to 0x0042 AAAA.

The line period is calculated for the Phase A, Phase B, and Phase C voltages and the combined voltage signal, as described in the Combined Voltage Zero Crossing section, and stored in the APERIOD, BPERIOD, CPERIOD, and COM_PERIOD, registers respectively.

Select the phase voltage line period to use as the basis for the resampling calculation using the LP_SEL bits in the ZX_LP_SEL register or select a user configured value written in USER_PERIOD using the UPERIOD_SEL bit in the CONFIG2 register, as shown in Figure 74.

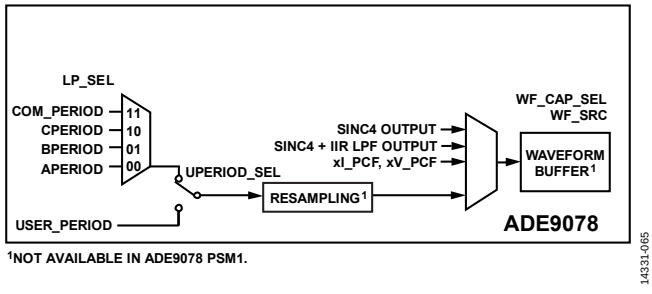


Figure 74. Line Period Selection for Resampling

The user period selection is helpful in applications where the user has another algorithm to determine the line frequency or if it is preferred to always assume a certain line frequency when resampling. USER_PERIOD[31:0] has the same scaling as the xPERIOD registers. Write USER_PERIOD[31:0] to 0x00500000 for 50 Hz and 0x0042AAAB for 60 Hz.

Angle Measurement

The ADE9078 measures the time between zero crossings on each phase. This measurement determines if the system is balanced properly or to determine if there was an installation

error. It can be checked if the phase angles correspond to the ones in the phasor diagrams given in the Applications Information section.

The times between negative to positive zero crossings are measured using a CLKIN/24 = 12.288/12 = 512 kHz clock. The time between the zero-crossing on Phase A and Phase B is stored in the ANGL_VA_VB register. The resolution of the ANGLx_x2x register is (1/512000)/20 ms × 360° = 0.03515625° at 50 Hz.

The time between the zero crossing on Phase B and Phase C is stored in the ANGL_VB_VC register and the time in between the zero crossings on Phase A and Phase C is stored in the ANGL_VA_VC register, as shown in Figure 75.

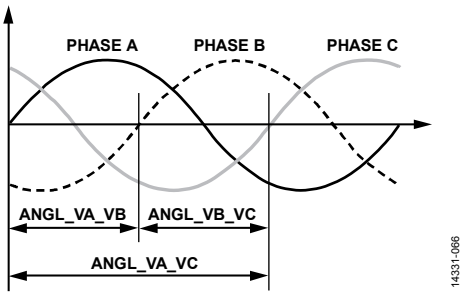


Figure 75. Voltage to Voltage Phase Angle

The angle in degrees can be calculated from the following equation with a 50 Hz line period:

$$Angle \text{ (degrees)} = ANGL\_VA\_VB \times 0.03515625/\text{LSB}$$

For a 4-wire wye configuration, the expected ANGL_VA_VB and ANGL_VB_VC is 120°/0.03515625 = 3413d. Note that the expected ANGL_VA_VC from Phase A voltage to Phase C voltage is 240°/0.03515625 = 6826d, which corresponds to a 120° angle between Phase C and Phase A.

The current to current zero crossings are also measured. This measurement is done similarly to the voltage to voltage phase angle described previously, except the current channel zero crossings are used as the reference. The time between the zero crossing on Phase A and Phase B is stored in the ANGL_IA_IB register. The time between the zero crossing on Phase B and Phase C is stored in the ANGL_IB_IC register and the time in between the zero crossings on Phase A and Phase C is stored in the ANGL_IA_IC register.

The voltage to current phase angles are measured as well. Use these measurements to determine the power factor at the fundamental. ANGL_VA_IA reflects the phase angle between the Phase A voltage and current, as shown in Figure 76. ANGL_VB_IB holds the Phase B voltage to current phase angle, whereas ANGL_VC_IC holds the Phase C voltage to current phase angle.

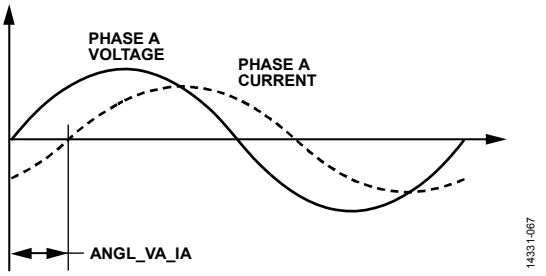


Figure 76. Voltage to Current Phase Angles

Note that if the magnitude of the voltage channel is below the user configured zero-crossing threshold, the zero-crossing output for that phase is not generated. In this event, the corresponding ANGLx_x2x measurements are not updated—the last value remains in the register. The current channel does not have these thresholds. When low input signal levels occur, spurious zero-crossing events may be generated on the current channel, which results in ANGLx_I2I and ANGLx_V2I readings that are not meaningful.

Phase Sequence Error Detection

4-Wire Wye and 4-Wire Delta

For 4-wire wye and 4-wire delta meters, the normal phase sequence is shown in Figure 77.

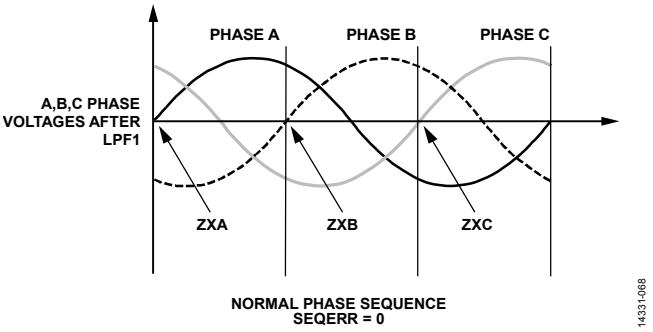


Figure 77. 4-Wire Wye and 4-Wire Delta Normal Phase Sequence

For a 4-wire wye or 4-wire delta system, VCONSEL = 000, 010, or 011 as described in the Applications Information section. In these 4-wire systems, the negative to positive transitions on ZXVA, ZXVB, and ZXVC are monitored to determine if there is a phase sequence error as shown in Figure 79. To detect a phase sequence error, set how many sequences to observe in the SEQ_CYC register. It is recommended to set SEQ_CYC to 1.

Figure 78 shows a phase sequence error for a 4-wire wye or 4-wire delta due to a wiring or installation error.

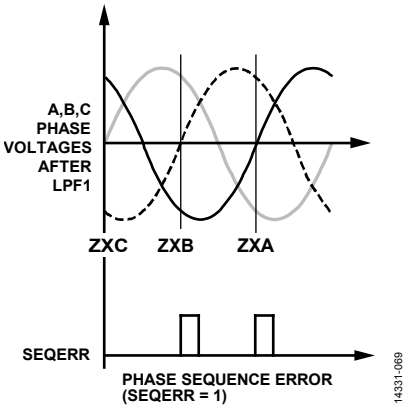


Figure 78. 4-Wire Wye and 4-Wire Delta Phase Sequence Error (Wiring Error)

Figure 79 shows that in an installation with the normal phase sequence, a phase sequence error is generated if a phase voltage drops below the ZXTHRSH value.

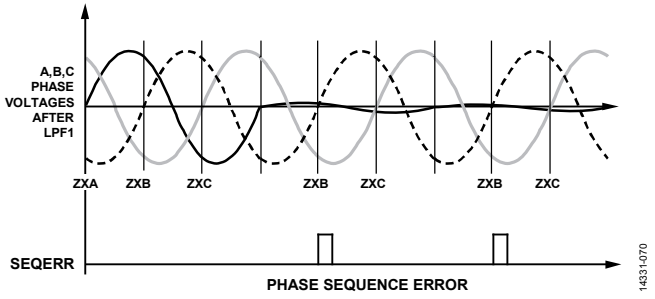


Figure 79. 4-Wire Wye, 4-Wire Delta Phase Sequence Error from a Phase Voltage Dropping Below ZXTHRSH with SEQ_CYC = 1

3-Wire Delta

For a 3-wire delta system, VCONSEL = 001 or 100 as described in the Applications Information section. In a 3-wire delta system, the ZXVC and ZXVA positive to negative (ZXx_POS) and negative to positive (ZXx_NEG) transitions are monitored to detect a phase sequence error. Figure 80 shows the normal phase sequence for a 3-wire delta with VCONSEL = 001.

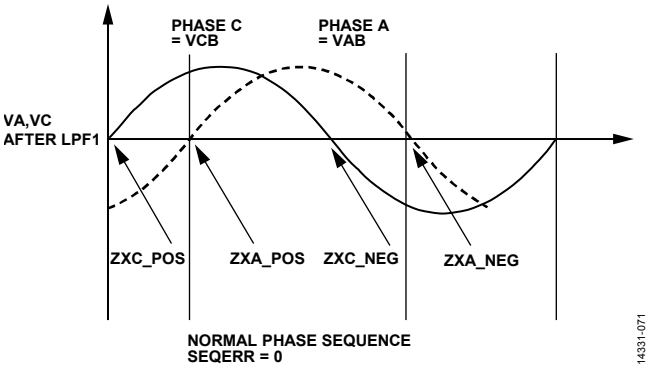


Figure 80. 3-Wire Delta Normal Phase Sequence

Write SEQ_CYC to indicate how many consecutive incorrect transitions must be observed before raising the SEQ_ERR interrupt. It is recommended to set SEQ_CYC to 1. Figure 81 shows an installation error for 3-wire delta that results in a detected phase sequence error.

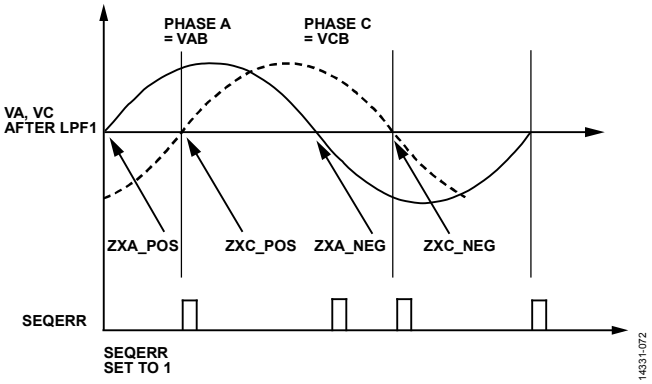


Figure 81. 3-Wire Delta Phase Sequence Error (Wiring Error)

Figure 82 shows that in an installation with the normal phase sequence, a phase sequence error is generated if one of the phase voltages drops below the ZXTHRSH value.

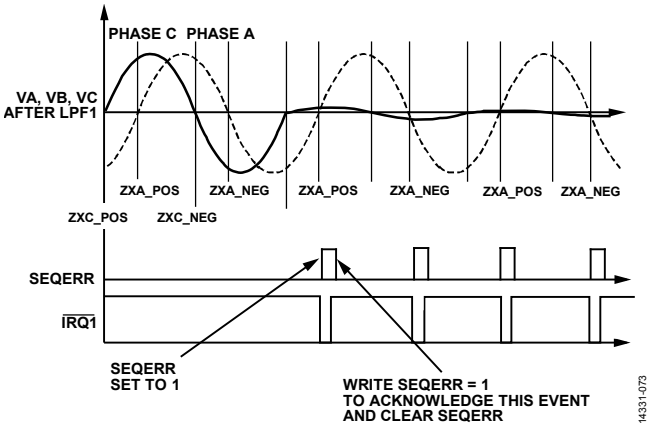


Figure 82. 3-Wire Delta Phase Sequence Error from a Phase Voltage Dropping Below ZXTHRSH with SEQ_CYC = 1

Peak Detection

The ADE9078 records the peak value measured on the current and voltage channels, from the xI_PCF and xV_PCF waveforms. The PEAKSEL bits in the CONFIG3 register allow the user to select which phases to monitor. Set PEAKSEL, Bit 2 to monitor Phase C; PEAKSEL, Bit 1 for Phase B; and PEAKSEL, Bit 0 for Phase A. Set PEAKSEL = 111b to monitor all three phases.

The IPEAK register stores the peak current value in IPEAKVAL, Bits[23:0] and indicates which phase currents reached the value in the IPPHASE bits. IPEAKVAL is equal to xI_PCF/2^5.

IPPHASE, Bit 2 indicates that Phase C had the peak value; IPPHASE, Bit 1 indicates Phase B; and IPPHASE, Bit 0 indicates Phase A.

Similarly, VPEAK stores the peak voltage value in VPEAKVAL, Bits[23:0]. VPEAKVAL is equal to xV_PCF/2^5.

VPPHASE, Bit 2 indicates that Phase C had the peak voltage value; VPPHASE, Bit 1 indicates Phase B; and VPPHASE, Bit 0 indicates Phase A.

When the user reads the IPEAK register, its value is reset. The same is true for reading VPEAK.

MEASUREMENTS (PSM2)

Overview

It is possible to tamper with an energy meter by disconnecting the voltage inputs or the neutral. Some regions require monitoring of the current inputs for several days after the voltage inputs to the meter have been cut, to check for this kind of tamper condition. The PSM1 and PSM2 operating modes in conjunction with PSM3 enable low power consumption when checking for and billing for a tamper of this kind.

To use this feature, first write the PSM2_CFG register to configure the current threshold to compare the input current level to and for how long to perform the detection while in either PSM0 or PSM1 operating modes. Then, change the PM1 and PM0 pins to 1 and 0, respectively, to select the PSM2 operating mode. To achieve the specified accuracy, stay in PSM2 mode for the time indicated in Table 8 before checking the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins to see if a tamper has occurred.

If no tampering is detected, change the PM1 and PM0 pins to 1 and 1, respectively, to enter PSM3 for one minute. Then, enter PSM2 by making PM1 and PM0 pins to 1 and 0, respectively, to check for tamper and begin the process again.

Low Power Comparator

In the PSM2 operating mode, the ADE9078 enters a low power state where only a low power comparator is active. The 1.8 V LDOs, ADCs, DSP, and crystal oscillator are turned off.

In this mode, the input currents (IA, IB, IC) are compared against a user selected level set in PSM2_CFG register. The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins indicate whether any of the three currents exceeds the threshold. The amount of time allowed for the detection is decided by the user and set in the LPLINE bits of the PSM2_CFG register. The measurement time is the period of (LPLINE + 4)/50 sec. The ADE9078 indicates that a tamper is detected if at least LPLINE + 1 peaks are obtained on a current channel. The maximum allowed value in LPLINE is 0x0A.

For example, if LPLINE = 2, six cycles of measurement time and three peaks are required on a given channel to indicate a tamper event.

The level to compare the current against is set in the PSM2_CFG register, PKDET_LVL bits, as shown in Table 22.

Table 22. PSM2 Current Peak Detect Thresholds

PKDET_LVL	Threshold Level
0	144:1
1	271:1
2	377:1
3	498:1
4	578:1
5	660:1
6	764:1
7	845:1
8	970:1
9	1100:1
10	1196:1
11	1312:1
12	1371:1
13	1464:1
14	1559:1
15	1629:1

After the configured measurement time set and (LPLINE + 4)/50 sec has elapsed, the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins indicate if a tamper has occurred. If $\overline{\text{IRQ0}}$ is low, all the currents have had less than LPLINE + 1 peaks; no tamper is detected. If $\overline{\text{IRQ1}}$ is low, at least one current was above LPLINE + 1 peaks and a tamper is detected.

After the tamper is detected, switch to PSM1 power mode by changing the PM1 and PM0 pins to 0 and 1, respectively, to measure key measurements quickly: IRMS, VRMS, active power, VAR, VA, and others (see the Measurements (PSM1) section for more information).

KEY FEATURES

FLEXIBLE WAVEFORM BUFFER WITH RESAMPLING

An integrated flexible waveform buffer stores samples at a fixed data rate or a sampling rate that varies based on the line frequency to ensure 64 points per line cycle. These two options make it easy to implement harmonic analysis in an external processor according to IEC 61000-4-7. There is a choice of data rate for the fixed data rate samples: 4 kSPS or 16 kSPS (see the Waveform Buffer section for more details).

MULTIPOINT PHASE/GAIN CALIBRATION

To provide more accurate measurements when using current transformers, the ADE9078 provides a multipoint gain and phase calibration option. If selected, the user can enter unique gain and phase calibrations for up to five regions of CT operation. Use the current rms (IRMS) value to select the current region of operation and to determine which gain and phase calibration to apply (see the Multipoint Gain and Phase Calibration section for more details).

RMS OF SUM OF INSTANTANEOUS CURRENTS MEASUREMENT

The ADE9078 offers an rms measurement of the sum of instantaneous currents. Use this measurement to estimate the neutral current rms if a neutral current sensor is not available. If a neutral current sensor is used, the rms of the sum of instantaneous currents can include IA + IB + IC ± IN. Ideally, IA + IB + IC ± IN = 0. The rms of the sum of instantaneous currents is compared to a user configured threshold. If it is greater than the threshold, a mismatch interrupt is generated. This mismatch indication can help detect earth currents or tamper, which is a safety hazard (see the Neutral Current RMS, RMS of Sum of Instantaneous Currents section for more details).

TAMPER MODES

Two power modes are provided to enable detection of meter tampering: PSM2 uses a low power comparator to compare current channels to a threshold and indicates whether it is exceeded on the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ outputs; and PSM1 enables fast measurement of current and voltage rms, active power, and VAR during a tamper. The PM0 and PM1 pins control which power supply mode is selected: PSM0 (normal mode), PSM1 (tamper measurement mode), PSM2 (tamper detection mode), or PSM3 (idle). The user application manages the PM0 and PM1 pins to put the ADE9078 in PSM1 or PSM2 modes for the required time to perform the measurement or detection. Then, the user application changes PM0 and PM1 to put the ADE9078 in PSM3, idle mode, until the cycle must begin again—usually once per minute (see the Power Modes section for more details).

POWER FACTOR

The power factor (PF) is calculated for each phase and is updated at the user configured power update rate, which can be up to 1 sec. PF is the total active power divided by the total apparent power. To determine the quadrant, use the sign in the reactive power register (see the Power Factor section for more details).

ZERO-CROSSING TIMEOUT DETECTION

Zero-crossing timeout detection is provided on each phase voltage to indicate if the phase voltage has been low for a user configured time period. An interrupt is generated if this event occurs (see the Zero-Crossing Timeout section for more details).

LINE PERIOD MEASUREMENT

The ADE9078 offers a highly accurate line period measurement that provides 0.001 Hz resolution. It is possible to measure the line period on all three phases as well as a combined signal that reflects the line period, regardless of if there is one or many phases present (see the Line Period Calculation section for more details).

ANGLE MEASUREMENT

Voltage to voltage, voltage to current, and current to current angles are measured simultaneously with 0.036° resolution at 50 Hz. These measurements allow fundamental power factor calculations and checks of the balance of the system (see the Angle Measurement section for more details).

PHASE SEQUENCE ERROR DETECTION

Voltage channel zero crossings are monitored to indicate if a phase sequence error occurs in both 3-phase, 4-wire (wye), and 3-wire (delta) connections (see the Phase Sequence Error Detection section for more details).

QUICK START

There are a few important steps to note when using the ADE9078 IC.

For most applications, ensure that the PM1 and PM0 pins are low to enter normal measurement mode (PSM0).

The following initialization sequence is recommended:

1. Wait for the RSTDONE interrupt, indicated by the $\overline{\text{IRQ1}}$ pin going low.
2. Configure the xIGAIN, xVGAIN, and xPGAIN registers via the SPI to calibrate the measurements.
3. If other calibration values are required, for example, to improve rms performance at low input signal levels, write these registers.
4. If the CFx pulse output is used, configure the CFxDEN and xTHR registers.
5. Configure the expected fundamental frequency (50 Hz or 60 Hz network) in the SELFREQ bit and write VLEVEL = 0x117514.
6. If a Rogowski coil sensor is used, write the INTEN bit in the CONFIG0 register to enable the digital integrator on the IA, IB, and IC channels. To enable the digital integrator on the neutral current, IN, channel, set the ININTEN bit. Additionally, write DICOEF = 0xFFFFE000 to configure the digital integrator. If current transformers are used, INTEN and ININTEN in the CONFIG0 register must = 0.
7. If the service bring measured is something other than 4-wire wye, see Table 24 to determine how to configure ICONSEL and VCONSEL in the ACCMODE register.
8. Write a 1 to the run register.
9. Write a 1 to the EP_CFG register.

The ADE9078 IC sampling capacitors vary device to device (see Table 1). For this reason, gain calibration is required to be able to accurately measure connected loads. If a current transformer sensor is used, phase calibration is required to remove any device to device variation in the phase error to accurately measure loads over power factor.

Use the following example to determine if the ADE9078 IC is correctly measuring the input voltage signal.

In this example, a 1 MΩ and 1 kΩ resistor divider network measures the voltage between the Phase A voltage and the neutral. If the input signal is 240 V rms, the expected voltage at the input to the ADE9078 IC is 240 V rms ×1000/(1000 + 1,000,000) = 0.2397 V rms. The ADE9078 ADC full-scale input is ±1 V, 0.707 V rms. Thus, 0.2397 V rms/0.707 V rms = 33.9% of full scale. It is recommended to scale the nominal voltage input to about ½ of full scale to allow room for overvoltage events. As described in the Filter-Based Total RMS section, the full-scale voltage rms register output reading is given as 52,866,837d. Thus, with this 33.9% of full-scale input, the expected VRMS register reading is 17,921,858. Note that the actual xVRMS register reading varies based on the external component gain error, combined with the ADE9078 IC device to device gain error. Assume that 18,000,000d is read when the 240 V rms load was applied. Thus, there are 18,000,000 output codes per 240 V rms, which means there are 75,000 output codes per volt. Take the xVRMS register reading and divide by 75,000 to determine the voltage in volts.

$$Volts = xVRMS/75{,}000$$

A similar exercise can be performed to determine if the ADE9078 IC is correctly measuring the input power.

For example, if the same 240 V rms signal is applied along with a 10 A load, the applied power is 240 V × 10 A = 2.4 kW. Assuming that the 10 A load is connected to a current transformer with 1000:1 turn ratio on the secondary side, the current is 10 mA. Assume a center tapped burden resistor is used so that there is 10 Ω total burden resistance. Thus, 10 mA × 10 Ω yields a 0.1 V rms signal. The ADE9078 IC allows full-scale inputs of ±1 V, 0.707 V rms, which means that the 10 A input is 0.1 V rms/0.707 V rms = 14.1% of full scale.

For the active power measurement, with a 240 V × 10 A load, the ADE9078 IC sees 33.9% of full scale on the voltage side and 14.1% on the current side, so 33.9%×14.1% = 4.8% of the full-scale output power. As described in the Total Active Power section, the xWATT register reads 20,823,646 with full-scale inputs. Thus, with this load applied, 4.8% × 20,823,646 = 999,535 is the expected register reading. Assume that 1,000,000d is read when the 240 V rms, 10 A load is applied. Thus, there are 1,000,000 output codes per 2.4 kW, which means there are 416,667 output codes per kW. Read the xWATT register and divide by 416,667 to determine the power in watts.

$$Watts = xWATT/416{,}667$$

APPLICATIONS INFORMATION

The voltage and current waveforms of a polyphase system are defined in the following equations:

$$V_A(t) = \sqrt{2}\sin(\omega t)$$

$$V_B(t) = \sqrt{2}\sin(\omega t - 120°)$$

$$V_C(t) = \sqrt{2}\sin(\omega t + 120°)$$

$$I_A(t) = \sqrt{2}\sin(\omega t - \theta)$$

$$I_B(t) = \sqrt{2}\sin(\omega t - \theta - 120°)$$

$$I_C(t) = \sqrt{2}\sin(\omega t - \theta + 120°)$$

To understand how these signals relate to each other, create a phasor diagram following a convention using lagging phase angles. Figure 83 shows a common polyphase metering configuration, the 4-wire wye, with V_A, V_B, and V_C. Phase B lags Phase A by 120°, and Phase C lags Phase A by 240°. Currents are shown at a power factor of 1, PF = 1, where θ = 0 in the expressions for I_A, I_B, and I_C, and the current is in phase with the voltage.

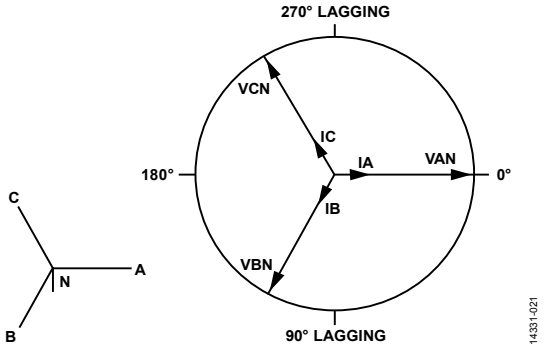


Figure 83. 4-Wire Wye Service Vector Diagram

Figure 84 to Figure 87 show common metering configurations: 3-wire delta, 4-wire delta, and 3-wire residential and network. The ADE9078 can also measure multiple single-phase circuits.

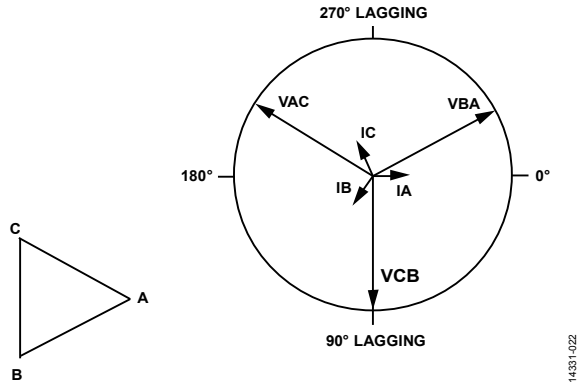


Figure 84. 3-Wire Delta Service Vector Diagram

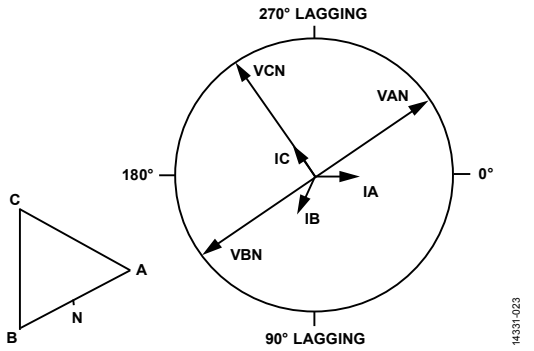


Figure 85. 4-Wire Delta Service Vector Diagram

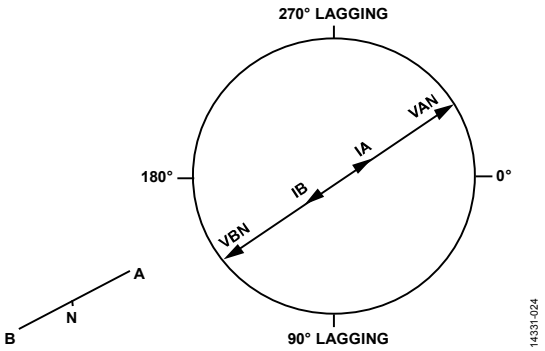


Figure 86. 3-Wire Residential Single-Phase Service Vector Diagram

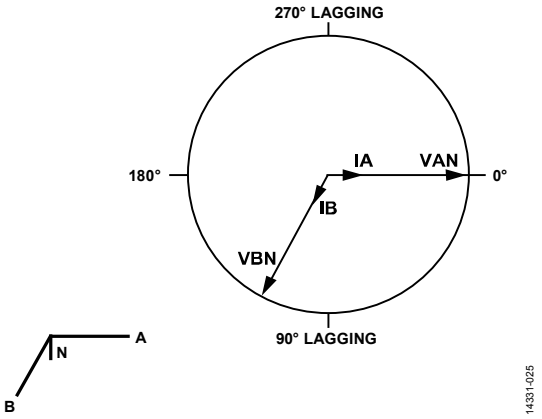


Figure 87. 3-Wire Network Meter Vector Diagram

The phasor diagrams show how the voltages and currents are related in time. Figure 88 shows the 4-wire wye voltage phase sequence in time, corresponding to the Figure 83 phasor diagram and equations for V_A, V_B, and V_C, provided previously in this section.

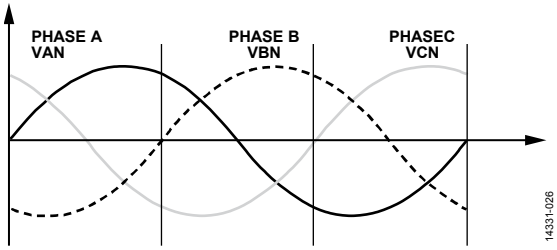


Figure 88. 4-Wire Wye, Voltage Phase Sequence in Time

NON-BLONDEL COMPLIANT METERS

Blondel's theorem states that there must be n − 1 measuring elements in a meter, where n is the number of the wires of the electric system. In this way, a Blondel compliant 4-wire wye or 4-wire delta measures three voltages and three currents. In a 3-wire delta service, at least two voltages and two currents must be measured to be Blondel compliant.

IEC meter forms are all Blondel compliant. ANSI has some meter forms that are not Blondel compliant, meaning that there are fewer than n − 1 elements, so that in a 4-wire wye or 4-wire delta configuration, two voltages and three currents are measured. The ADE9078 has provisions to deal with non-Blondel compliant meter forms. Use the VCONSEL bits in the ACCMODE register to select what calculation to use for V_B based on the V_A and V_C signals.

Table 23. Non-Blondel Compliant Meter Forms

Service Type	Non-Blondel Compliant ANSI Meter Form	VCONSEL	V_B Calculation
4-Wire Wye, Two Voltages, Three Currents	6S, 7S, 14S, 29S, 36S, 46S, 76S	010	$V_B = -V_A - V_C$
4-Wire Delta, Two Voltages, Three Currents	8S, 15S, 24S	011	$V_B = -V_A$

APPLYING THE ADE9078 TO A 4-WIRE WYE SERVICE

For the highest level of performance when measuring a 4-wire wye service, connect the neutral to ground, as shown in Figure 89. For this configuration, VCONSEL = 000.

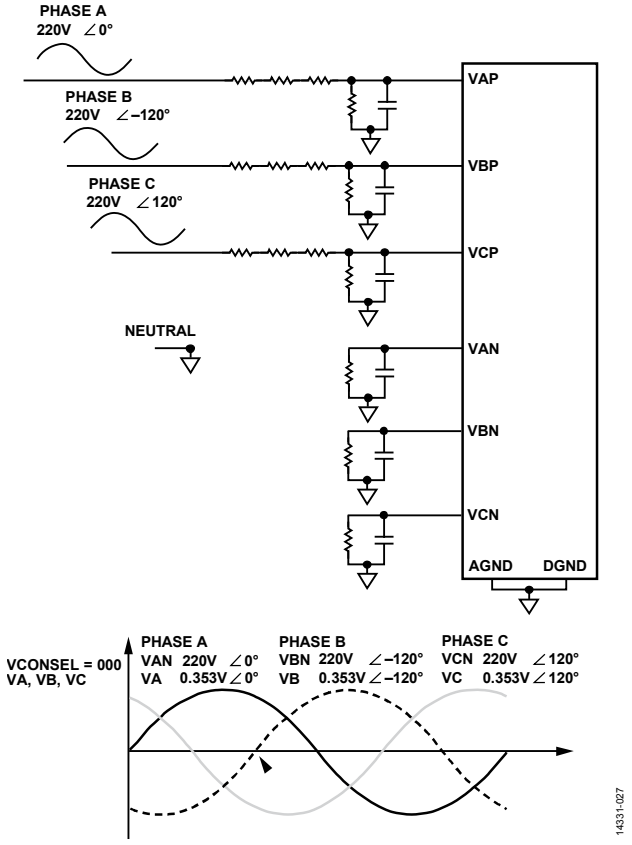


Figure 89. 4-Wire Wye, Neutral Connected to Ground

Alternatively, a series impedance can be used on the neutral, as shown in Figure 90, which can be advantageous if an isolated power supply is used. Note that this configuration has poor performance if the phase voltages are not balanced. For more information, see the AN-1334 Application Note. For this configuration, VCONSEL = 000.

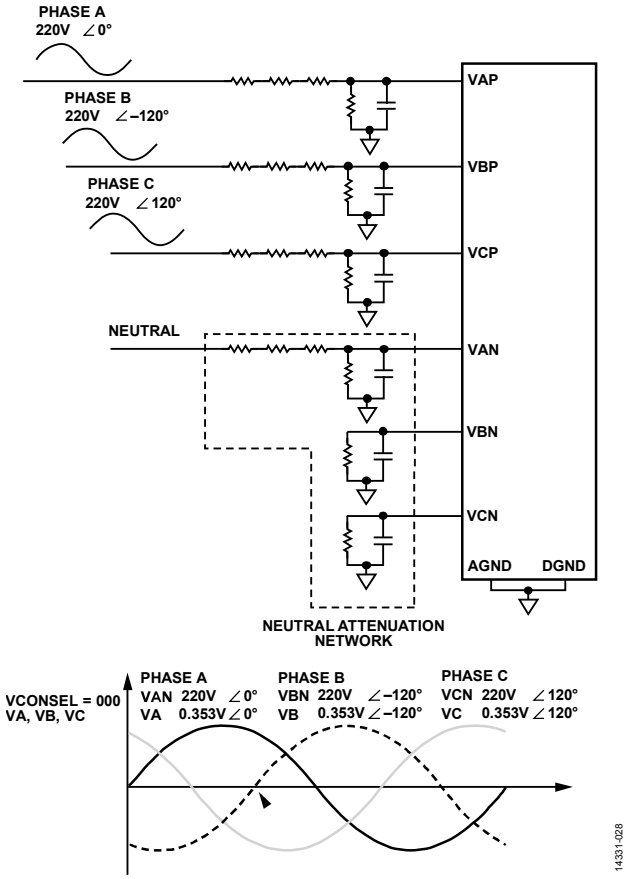


Figure 90. 4-Wire Wye, Series Impedance on the Neutral

Phase sequence error detection is performed based on the expected ABC sequence (see the Phase Sequence Error Detection section for more information).

To calculate the overall power consumed by the system (active, reactive, and apparent), add the contribution from the Phase A, Phase B, and Phase C accumulations.

APPLYING THE ADE9078 TO A 3-WIRE DELTA SERVICE

For the highest level of performance when measuring a 3-wire delta service, connect Phase B to ground, as shown in Figure 91. For this configuration, write VCONSEL = 001 in the ACCMODE register. Then, $V_B = V_A - V_C$ and the ADE9078 calculates the VAC potential in the BVRMS register. To calculate the current flowing through I_B from the I_A and I_C measurements, set ICONSEL = 1 in the ACCMODE register so that $I_B = -I_A - I_C$.

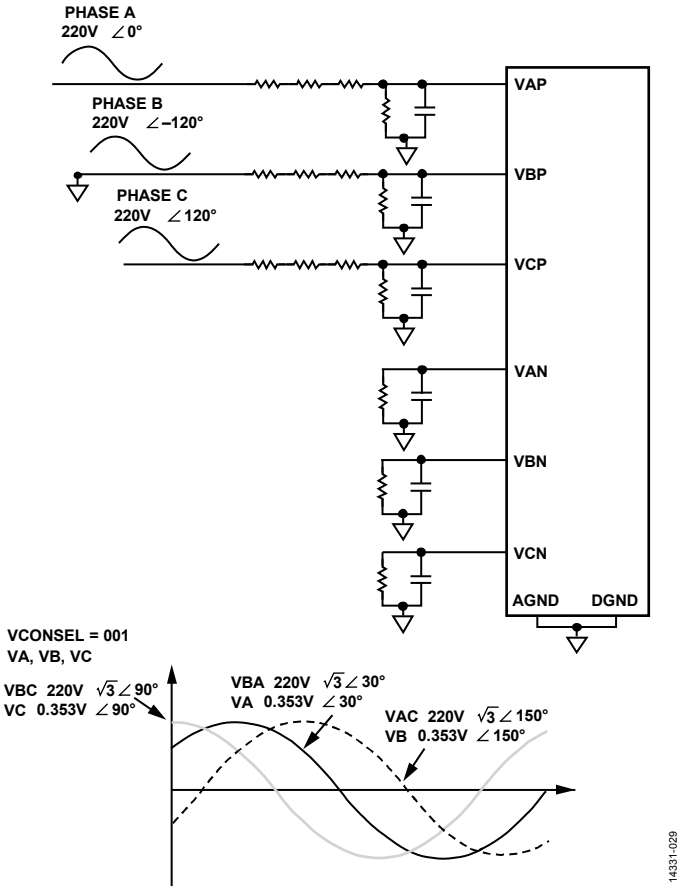


Figure 91. 3-Wire Delta, Phase B Connected to Ground

Note that for this 3-wire delta, Phase B connected to ground configuration, the phasor diagram of the AV_PCF, BV_PCF, and CV_PCF waveforms inside the ADE9078 IC, shown in Figure 92, is shifted compared to the service diagram given in Figure 84.

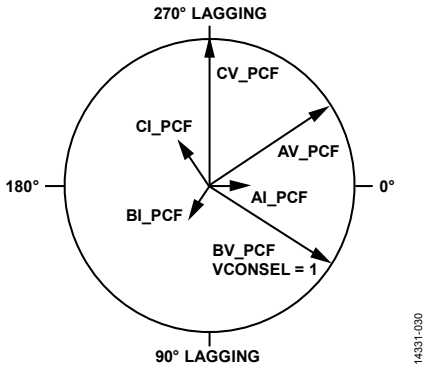


Figure 92. Phasor Diagram of xV_PCF and xI_PCF Waveforms Inside the IC with 3-Wire Delta with Phase B as Ground and VCONSEL = 001

To use the same PCB for both 4-wire wye and 3-wire delta circuits, another option is to wire Phase B to the neutral terminal of the meter, keeping the same circuit as used in Figure 89 or Figure 90. Note that VCONSEL bits in the ACCMODE register must be set to 001 if it is desired to obtain the VAC rms value, which is calculated in the BVRMS register, and to use the correct phase sequence detection method for the 3-wire delta configuration. To calculate the current flowing through IB from the IA and IC measurements, set ICONSEL = 1 in the ACCMODE register so that $I_B = -I_A - I_C$.

Alternatively, a series impedance can be used on Phase B, as shown in Figure 93. This configuration can be advantageous if an isolated power supply is used; however, it has poor performance if the phase voltages are not balanced. Use VCONSEL = 100 with this configuration so that $V_A = V_A - V_B$; $V_B = V_A - V_C$; and $V_C = V_C - V_B$. To calculate the current flowing through I_B from the I_A and I_C measurements, set ICONSEL = 1 so that $I_B = -I_A - I_C$.

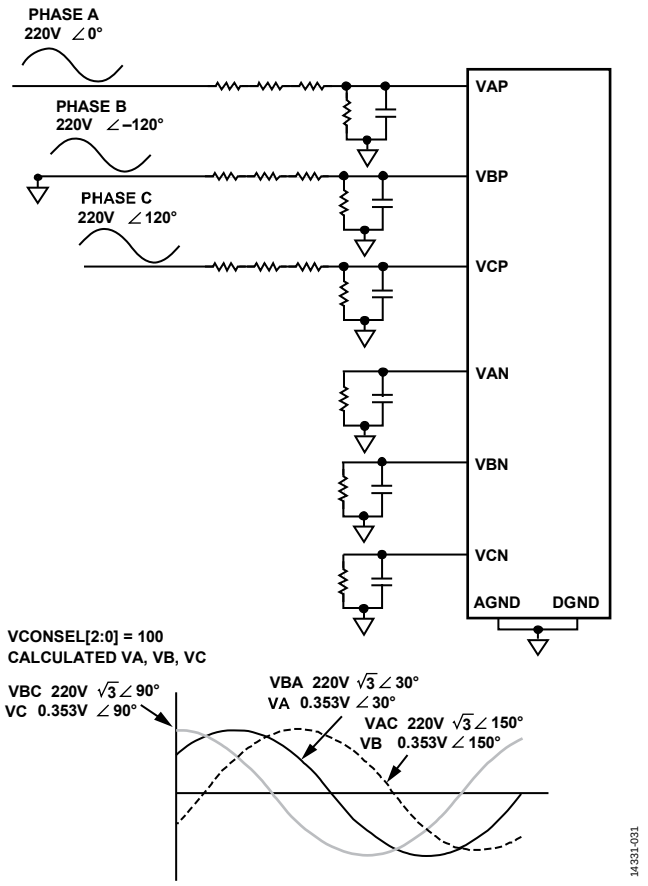


Figure 93. 3-Wire Delta, Series Impedance on Phase B and VCONSEL = 100

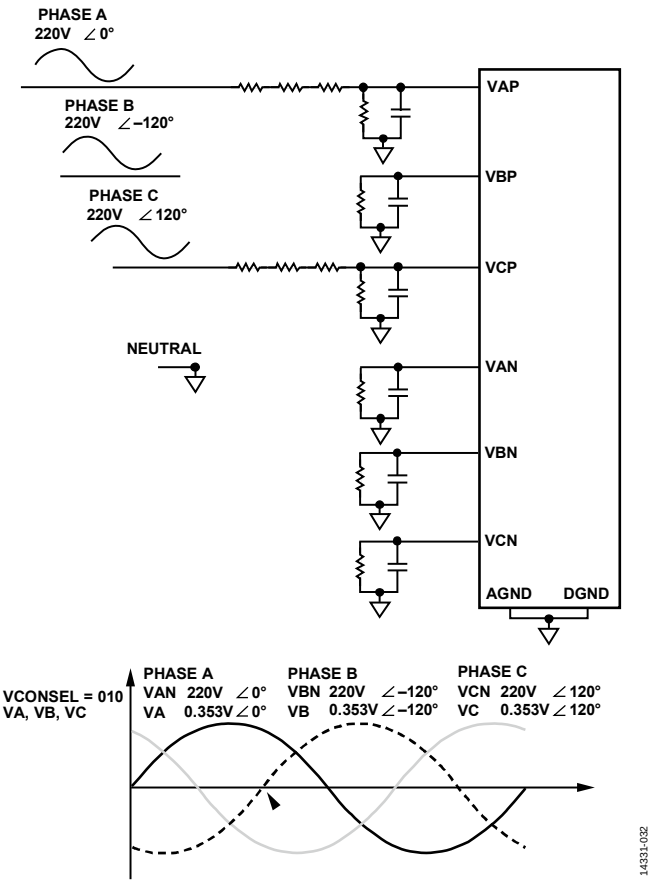


Figure 94. Non-Blondel Compliant 4-Wire Wye

The V_A, V_B, and V_C waveforms computed inside the ADE9078 for the 3-wire delta with series impedance on Phase B and VCONSEL = 100 are shown in the time domain in Figure 93 and correspond to the phasor diagram shown in Figure 92.

Phase sequence error detection is performed with the expectation that the VC waveform leads V_A (see the Phase Sequence Error Detection section for more information).

In a Blondel compliant 3-wire delta meter, only the overall power consumed by the system is meaningful; the individual phase powers are not meaningful because a line current is multiplied by a line to line voltage. To calculate the overall power consumed by the system (active, reactive, and apparent), add the contribution from Phase A and Phase C.

APPLYING THE ADE9078 TO A NON-BLONDEL COMPLIANT, 4-WIRE WYE SERVICE

To use the ADE9078 in a non-Blondel compliant 4-wire wye service, such as for ANSI Meter Forms 6S, 7S, 14S, 29S, 36S, 46S, 76S, the Phase A and Phase C voltages are measured and the Phase B voltage is calculated, $V_B = V_A - V_C$. All three phase currents are measured. For this configuration, write VCONSEL = 010 and connect as shown in Figure 94.

The phasor diagram follows Figure 83. Phase sequence error detection is performed based on the expected ABC sequence (see the Phase Sequence Error Detection section for more information).

To calculate the total power (active, reactive, and apparent), add the contribution from Phase A, Phase B, and Phase C.

APPLYING THE ADE9078 TO A NON-BLONDEL COMPLIANT, 4-WIRE DELTA SERVICE

To use the ADE9078 in a non-Blondel compliant 4-wire delta service, such as for ANSI Meter Forms 8S, 15S, and 24S, measure the Phase A and Phase C voltages and calculate the Phase B voltage, $V_B = -V_A$. All three phase currents are measured. For this configuration, write VCONSEL = 011 in the ACCMODE register and connect as shown in Figure 95.

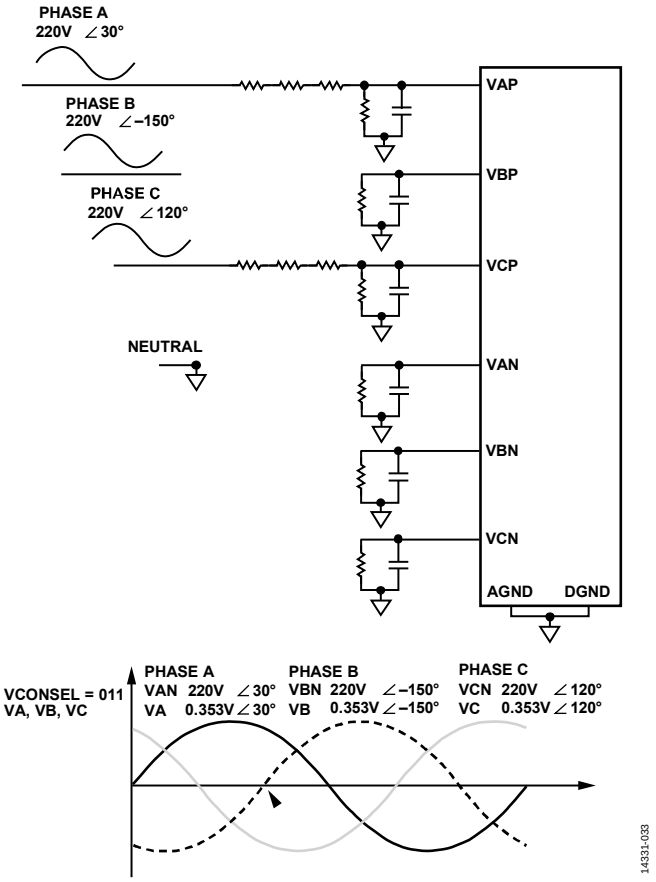


Figure 95. Non-Blondel Compliant 4-Wire Delta

The phasor diagram is shown in Figure 85. Phase sequence error detection is performed based on the expected ABC sequence (see the Phase Sequence Error Detection section for more information).

To calculate the total power (active, reactive and apparent), add the contribution from Phase A, Phase B, and Phase C.

SERVICE TYPE SUMMARY

To summarize, the ADE9078 can be used in many different configurations to measure 4-wire wye, 4-wire delta, and 3-wire delta installations. Table 24 summarizes which VCONSEL and ICONSEL settings to use for each configuration.

Table 24. Service Type and VCONSEL and ICONSEL Setting Summary

Service Type	Ground Reference	Figure Reference	No. of Voltage Sensors Required	VCONSEL Setting	No. of Current Sensors Required	ICONSEL Setting
4-Wire Wye	Neutral	Figure 89	3	000	3	0
	Isolated	Figure 90	3	000	3	0
3-Wire Delta	Phase B	Figure 91; Figure 89 with Phase B tied to neutral	2	001 ($V_B = V_A - V_C$)	2	0: I_B has current sensor 1: $I_B = -I_A - I_C$
	Isolated	Figure 90 with Phase B tied to neutral	2	001 ($V_B = V_A - V_C$)	2	0: I_B has current sensor 1: $I_B = -I_A - I_C$
	Isolated	Figure 93	2	100 ($V_A = V_A - V_B$; $V_B = V_A - V_C$; $V_C = V_C - V_B$)	2	0: I_B has current sensor 1: $I_B = -I_A - I_C$
4-Wire Delta	Neutral	Figure 89 (note that the VA and VB phasor diagram follows Figure 85)	3	000	3	0
4-Wire Wye, Non-Blondel Compliant	Neutral	Figure 94	2	010 ($V_B = V_A - V_C$)	3	0
4-Wire Delta, Non-Blondel Compliant	Neutral	Figure 95	2	011 ($V_B = -V_A$)	2	0: I_B has current sensor 1: $I_B = -I_A - I_C$
3-Wire Single-Phase	Neutral	Not applicable	1 or 2	000	1 to 2	0
3-Wire Network	Neutral	Not applicable	2	000	2	0
Multiple Single-Phase Circuits	Neutral	Not applicable	3	000	3	0

ACCESSING ON-CHIP DATA

SPI PROTOCOL OVERVIEW

The ADE9078 has a SPI-compatible interface, consisting of four pins: SCLK, MOSI, MISO, and $\overline{SS}$. The ADE9078 is always a SPI slave—it never initiates SPI communication. The SPI interface is compatible with 16-bit and 32-bit read/write operations. See the Register Information section for information about the length of each register.

Figure 96 shows the connection between the ADE9078 SPI and a master device that contains a SPI interface.

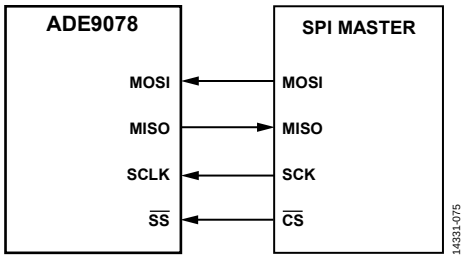


Figure 96. Connecting the ADE9078 Slave SPI Port to a Master SPI Device

The $\overline{SS}$ pin is the chip select input. It starts the SPI communication with the ADE9078.

There are three parts to the ADE9078 SPI protocol: first a 16-bit command is sent, which indicates whether to perform a read or write operation and which register to access. This is followed by the 16- or 32-bit data to write, in the case of a SPI write, or the data read from the register, in the case of a SPI read operation. Finally, in the case of a SPI read operation, a cyclic redundancy check (CRC) of the register data follows, unless the address is in a region that supports burst reading, in which case the data from the next register follows (see the SPI Burst Read section for more information).

The $\overline{SS}$ input must stay low for the whole SPI transaction. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer. A new transfer can be initiated by returning the $\overline{SS}$ logic input low. It is not recommended to tie $\overline{SS}$ to ground because the high to low transition on $\overline{SS}$ starts the ADE9078 SPI transaction.

Data shifts into the device at the MOSI logic input on the falling edge of SCLK, and the device samples the input data on the rising edge of SCLK. Data shifts out of the ADE9078 at the MISO logic output on the falling edge of SCLK and must be sampled by the master device on the rising edge of SCLK. The MSB of the word is shifted in and out first.

MISO has an internal weak pull-up of 100 kΩ, making the default state of the MISO pin high. It is possible to share the SPI bus with multiple devices, including multiple ADE9078 devices, if desired.

The ADE9078 is compatible with the following microcontroller SPI port clock polarity and phase settings: CPOL = 0 and CPHA = 0 (typically Mode 0) or CPOL = 1 and CPHA = 1 (typically Mode 3).

Note that the default state of the MOSI pin depends on the master SPI device. In Figure 97, Figure 98, and Figure 100, it is assumed to be high (Logic 1).

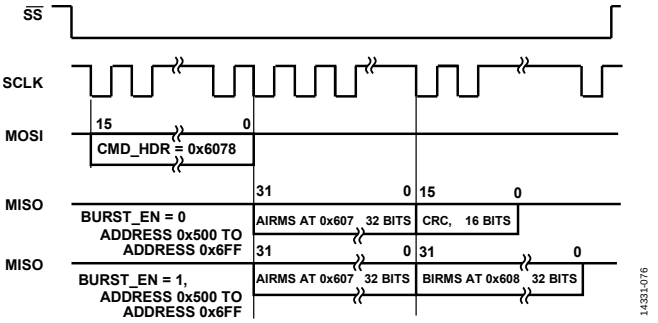


Figure 97. SPI Read Protocol Example—CRC or Next Data Can Follow

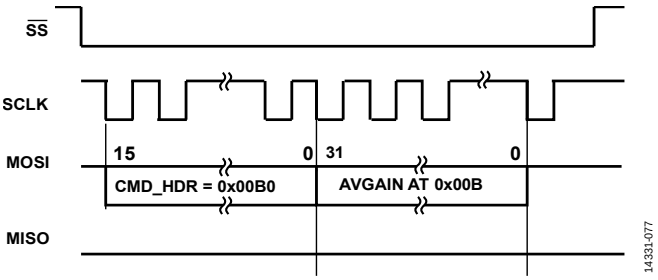


Figure 98. SPI Write Protocol Example

The maximum serial clock frequency supported by this interface is 10 MHz.

The SPI read/write operation starts with a 16-bit command (CMD_HDR), which contains the following information:

- CMD_HDR, Bits[15:4] are the 12 MSBs of the command header, and contains the address of the register (ADDR, Bits[11:0]) to be read or written.
- CMD_HDR, Bit 3 is the bit that specifies if the current operation is read/write. Set this bit to 1 for read and 0 for write.
- CMD_HDR, Bits[2:0] are required for internal chip timing and can be 1s or 0s. Note that these bits are read back as 000 in the LAST_CMD register.

Figure 99 shows the information contained in the command header.

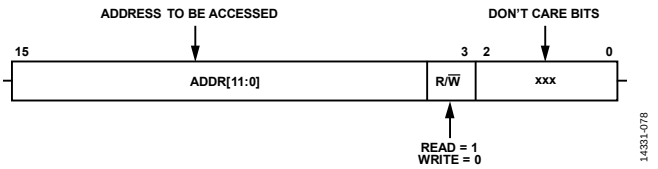


Figure 99. Command Header, CMD_HDR, Bits[15:0]

SPI WRITE

A write operation using the SPI interface of the ADE9078 is initiated when the $\overline{SS}$ pin goes low and the ADE9078 receives a 16-bit command header (CMD_HDR), with CMD_HDR, Bit 3 = 0.

The 16-bit or 32-bit data to write follows the command header, with the MSB first.

After the last bit of data has been clocked out, the master brings the $\overline{SS}$ line high to release the SPI bus. It is recommended to have the SCLK line idle high.

SPI READ

A read operation using the SPI interface of the ADE9078 is initiated when the $\overline{SS}$ pin goes low and the ADE9078 receives a 16-bit command header (CMD_HDR), with CMD_HDR, Bit 3 = 1.

The 16-bit or 32-bit data from the register follows the command header, with the MSB first.

The CRC of the register data is appended if

- BURST_EN = 0 and the address is within the range of Address 0x000 to Address 0x6FF.
- BURST_EN = 0 and the address is in the waveform buffer, Address 0x800 to Address 0xFFF and BURST_CHAN = 1111b.

The ADE9078 provides a SPI burst read functionality—instead of sending the CRC, the following data is sent from the next address if these conditions apply (see the SPI Burst Read section for more information):

- BURST_EN = 1 and the address is within the range of Address 0x500 to Address 0x516, Address 0x600 to Address 0x63C, or Address 0x680 to Address 0x6BC.
- The address is within the range of Address 0x800 to Address 0xFFF and BURST_CHAN is not equal to 1111b.

If none of these cases apply, and extra clocks are sent, the original read data is resent.

Table 25 summarizes what data is sent after the data from the register addressed in the CMD_HDR—it varies based on the address being accessed and the BURST_EN selection.

Table 25. Data Clocked Out After Addressed Data in SPI Read Operation

Address	BURST_EN = 0	BURST_EN = 1
0x000 to 0x4FF	CRC	Same data is resent
0x500 to 0x6FF	CRC	Next address
0x800 to 0xFFF (Waveform Buffer)	If BURST_CHAN = 1111, CRC; otherwise, next address	If BURST_CHAN = 1111, the same data is resent; otherwise, next address

If this information is not needed in the application, the $\overline{SS}$ line can be brought high before clocking out the CRC.

After the last bit of data, or CRC, is clocked out, the master must bring the $\overline{SS}$ line high to release the SPI bus. Then the ADE9078 stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high.

An example of what happens when reading the AVGAIN register, Address 0x00B, when BURST_EN = 0 and 1, is given in Figure 100.

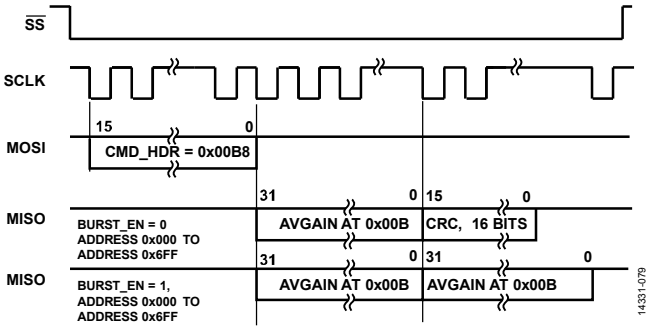


Figure 100. SPI Read Protocol Example Where the Following Data Is the CRC or the Initial Data Is Repeated

SPI BURST READ

SPI burst read allows multiple registers to be read after sending one CMD_HDR. After the register data has been clocked out, the ADE9078 auto-increments the address and starts clocking out the data from the next register address.

SPI burst read access is available on registers with addresses ranging from Address 0x500 to Address 0x6FF and in the waveform buffer, with Address 0x800 to Address 0xFFF. SPI burst read is not available on other register addresses. A SPI burst read operation occurs for the options in Table 25 where the next address is written.

To enable burst read functionality on the registers from Address 0x500 to Address 0x6FF, set the BURST_EN bit in the CONFIG1 register to 1.

The waveform buffer burst read functionality is enabled by default and is managed by BURST_CHAN in the WFB_CFG register. If these bits are set to 1111b, the burst read functionality of the waveform buffer is disabled. For further details on the burst read operation of waveform buffer contents, see the Burst Read Waveform Buffer Samples from SPI section.

A burst read operation using the SPI interface of the ADE9078 is initiated when the $\overline{SS}$ pin goes low and the ADE9078 receives a 16-bit command header (CMD_HDR), with CMD_HDR, Bit 3 = 1 that meets the criteria in Table 25 where the next address is written.

Following the command header, the ADE9078 sends the register data for the register addressed in the command. After the last bit of the first register value is received, the ADE9078 auto-increments the address and starts clocking out the data from the next register address. This process continues until the master sets the $\overline{SS}$ line high. If the starting address is in the range of Address 0x500 to Address 0x516 and the SPI is clocked beyond Address 0x516, the address is auto-incremented until it reaches Address 0x5FF and then wraps back to the initial address. If the initial address is in the Address 0x600 to Address 0x63C or Address 0x680 to Address 0x6BC range and the SPI is clocked beyond Address 0x63C or Address 0x6BC, it wraps back to the initial address. Note that certain reserved registers in the valid SPI burst address range reads zero during burst read operation.

After the $\overline{SS}$ line is set high by master, the ADE9078 stops driving MISO and enables a 100 kΩ weak pull-up. It is recommended to have the SCLK line idle high. An example of a SPI burst read operation is given in Figure 97, when BURST_EN = 1. For other examples, see the Burst Read Waveform Buffer Samples from SPI section.

SPI PROTOCOL CRC

The ADE9078 SPI port calculates a 16-bit cyclic redundancy check (CRC-16) of the data sent out on its MOSI pin so that the integrity of the data received by the master can be checked. The CRC of the data sent out on the MOSI pin during the last register read is offered in a 16-bit register, CRC_SPI, and can be appended to the SPI read data as part of the SPI transaction.

The CRC_SPI register value is appended to the 16-/32-bit data read from the register addressed in the CMD_HDR for the cases in Table 25 where CRC is written (see the SPI Read section for more information).

The CRC result can always be read from the CRC_SPI register directly.

There is no CRC checking as part of the SPI write register protocol. To ensure the data integrity of the SPI write operation, read the register back to verify that the value is written to the ADE9078 correctly.

CRC Algorithm

The CRC algorithm implemented within the ADE9078 is based on the CRC-16 CCITT algorithm. The data output on MISO is introduced into a linear feedback shift register (LFSR) based generator one byte at a time, MSB first without bit reversal, as shown in Figure 101 and Figure 102. The 16-bit result is written in the CRC_SPI register.

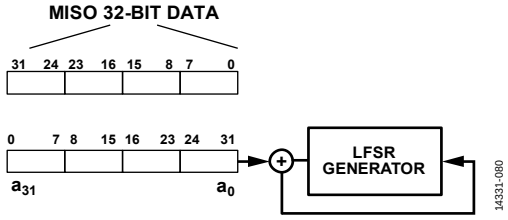


Figure 101. CRC Calculation of 32-Bit SPI Data

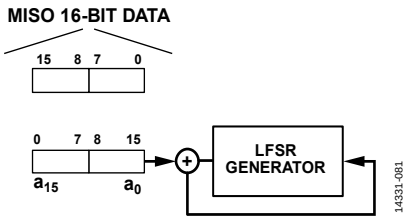


Figure 102. CRC Calculation of 16-Bit SPI Data

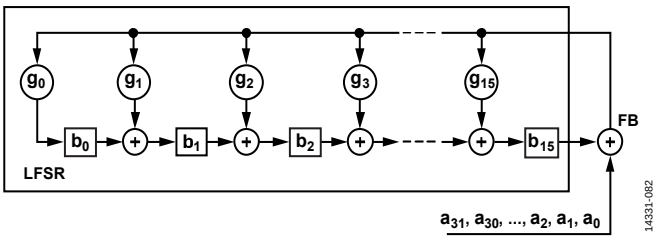


Figure 103. LFSR Generator Used for CRC_SPI Calculation

Figure 103 shows how the LFSR works. The MISO 32-bit data forms the [a_{31}, a_{30}, …, a_0] bits used by the LFSR. Bit a_0 is Bit 31 of the first MISO 32-bit data to enter the LFSR, whereas the last data to enter the LFSR, Bit a_{31}, corresponds to Bit 0 transmitted on MISO. The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the LSB, and Bit b_{15} is the MSB.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16 CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \quad (1)$$

$$g_0 = g_5 = g_{12} = 1 \quad (2)$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \quad (3)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (4)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, \ldots, 15 \quad (5)$$

Equation 3, Equation 4, and Equation 5 must be repeated for j = 1, 2, …, 32. The value written into the CRC_SPI register contains Bit $b_i(32)$, i = 0, 1, …, 15.

A similar process is followed for 16-bit data (see Figure 102 for information about how the bits are ordered into the LFSR).

ADDITIONAL COMMUNICATION VERIFICATION REGISTERS

The ADE9078 includes three registers that allow SPI operations to be verified. The LAST_CMD (Address 0x04AE, LAST_DATA_16 (Address 0x4AC), and LAST_DATA_32 (Address 0x423) registers record the received CMD_HDR and last read/transmitted data. The LAST_DATA_16 register contains the last data read or written during the last 16-bit transaction, whereas the LAST_DATA_32 holds the data read or written during the last 32-bit transaction.

The LAST_CMD register is updated after the CMD_HDR is received. Note that the three LSBs of LAST_CMD always reads back as 000. Also note that if a command to read the LAST_CMD, LAST_DATA_16, or LAST_DATA_32 registers is received, these three registers are not updated.

During a SPI read operation, LAST_DATA_16 and LAST_DATA_32 are updated within two master clocks after the CMD_HDR is received.

Note that the LAST_DATA_16 and LAST_DATA_32 registers are not updated after a SPI burst read operation—these registers are the cases in Table 25 where the next address is written.

On a write operation, LAST_DATA_16 and LAST_DATA_32 are not updated until all 16 or 32 bits of the write data are received. Note that, on a write register operation, the addressed register is not written until all 16 or 32 bits are received, depending on the length of the register.

Note that when the LAST_CMD, LAST_DATA_16, and LAST_DATA_32 registers are read, their values remain unchanged.

CRC OF CONFIGURATION REGISTERS

The configuration register CRC feature in the ADE9078 monitors certain external and internal register values. It also optionally includes 12 registers that are individually selectable in the CRC_OPTEN register. See the CRC_OPTEN register in Table 32 for more details.

This feature runs as a background task—it takes 10.8 ms to calculate the configuration register CRC. The result is stored in the CRC_RSLT register. If any of the monitored registers change value, the CRC_RSLT register changes as well, and the CRC_CHG bit in the STATUS 1 register is set, which can also be configured to generate an interrupt on $\overline{\text{IRQ1}}$.

After configuring the ADE9078 and writing the required registers to calibrate the measurements, such as xIGAIN or xVGAIN, the configuration register CRC calculation can be started by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register. When the calculation is complete, the CRC_DONE bit is set in the STATUS1 register.

The method used for calculating the configuration register CRC is also based on the CRC-16 CCITT algorithm. The most significant byte of each register is introduced into the LFSR first, without bit reversal (see the CRC Algorithm section for more information).

The order in which the registers are calculated is given in Table 26, with the lowest register introduced first. Note that 32-bit registers have four bytes introduced into the LFSR, whereas 16-bit registers have two bytes introduced into the LFSR.

Note that the default value of certain internal registers can vary for each device and, thus, the default CRC of configuration registers can vary for each device.

Table 26. Order of Registers Included in the Configuration Register CRC

Register Addresses	Register Length (Bits)
0x01 to 0x18	32
0x21 to 0x38	32
0x41 to 0x58	32
0x60 to 0x73	32
0x409	32
0x40F	32
0x420 to 0x422	32
0x424	32
0x470 to 0x475	32
0x480 to 0x481	16
0x490 to 0x497	16
0x499	16
0x4AF to 0x4B2	16
0x425	32
0x4B8 to 0x4B9	16
0x47D	32
0x478 to 0x479	32
0x4EF	16
0x4BA	16
0x47E	32
0x00	32
0x20	32
0x40	32
0x4B6	16
0x4BF	16
0x4B5	16

CONFIGURATION LOCK

The configuration lock feature prevents changes to the ADE9078 configuration. To enable this feature, write 0x3C64 to the WR_LOCK register. To disable the feature, write 0x4AD1.

To determine whether this feature is active, read the WR_LOCK register, which reads as 1 if the protection is enabled and 0 if it is disabled.

When this feature is enabled, it prevents writing to Address 0x000 to Address 0x0FF and Address 0x400 to Address 0x4FF.

WAVEFORM BUFFER

The ADE9078 has a waveform buffer comprised of 2048, 32-bit memory locations with addresses from Address 0x800 to Address 0xFFF. This memory can be filled with samples from the sinc4 or sinc4 + IIR LPF or current and voltage waveform samples processed by the digital signal processor.

Resampled waveforms make it easy to perform harmonic analysis in an external processor that can use the 16-bit, 64 points per line cycle samples directly in a FFT, without having to perform any windowing functions.

The data in the waveform buffer can come from four locations in the signal chain, as follows:

- Sinc4 outputs, xI_SINC_DAT, xV_SINC_DAT: 16 kSPS
- Sinc4 + IIR LPF output, xI_LPF_DAT, xV_LPF_DAT: 4 kSPS
- Current and voltage channel waveforms processed by the DSP (xI_PCF, xV_PCF): 4 kSPS
- Resampled waveforms with 64 points per line cycle processed by the DSP: data rate varies with line period

Figure 104 and Figure 105 show the current and voltage channel datapaths, indicating which waveforms can be stored into the waveform buffer.

Filling and accessing of the waveform buffer depends on which type of data is being filled in the buffer. The waveforms with a fixed data rate, 16 kSPS or 4 kSPS, are referred to as fixed data rate waveforms. The following sections explain what modes/access are available for resampled waveforms versus fixed data rate waveforms.

The waveform buffer samples can be accessed using the SPI burst read functionality so that multiple samples can be read using only one SPI command header (see the Burst Read Waveform Buffer Samples from SPI section).

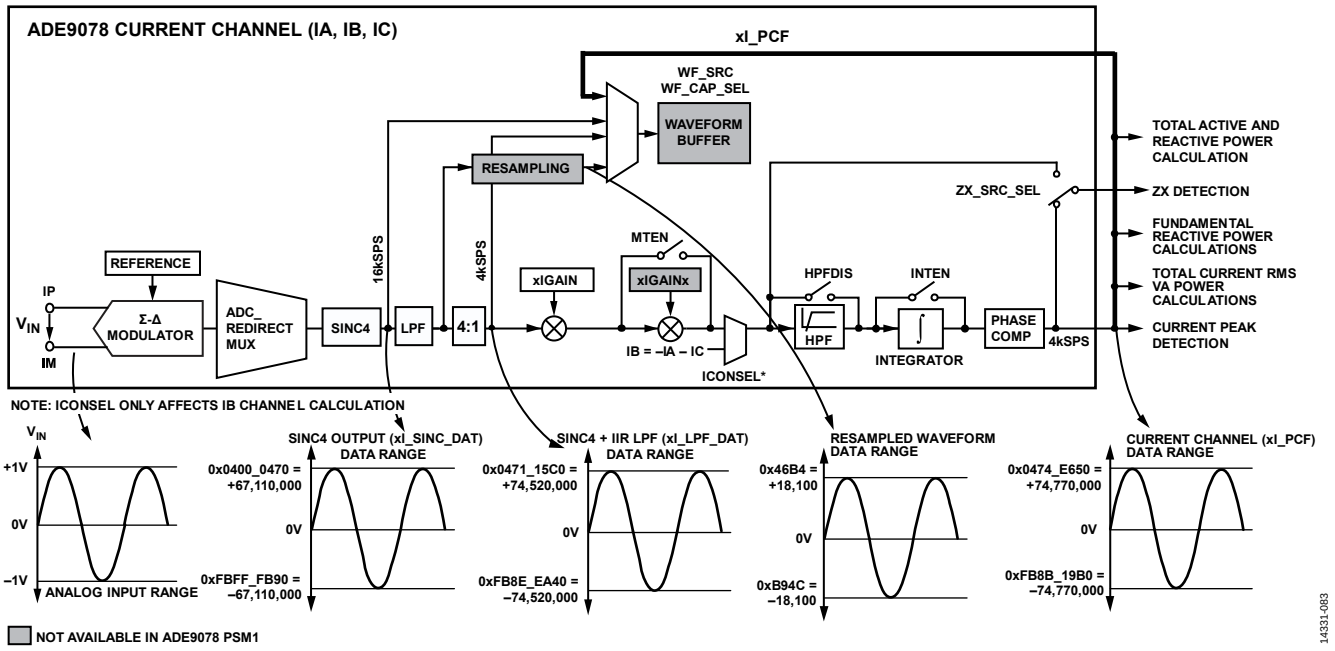


Figure 104. Current Channel Datapath

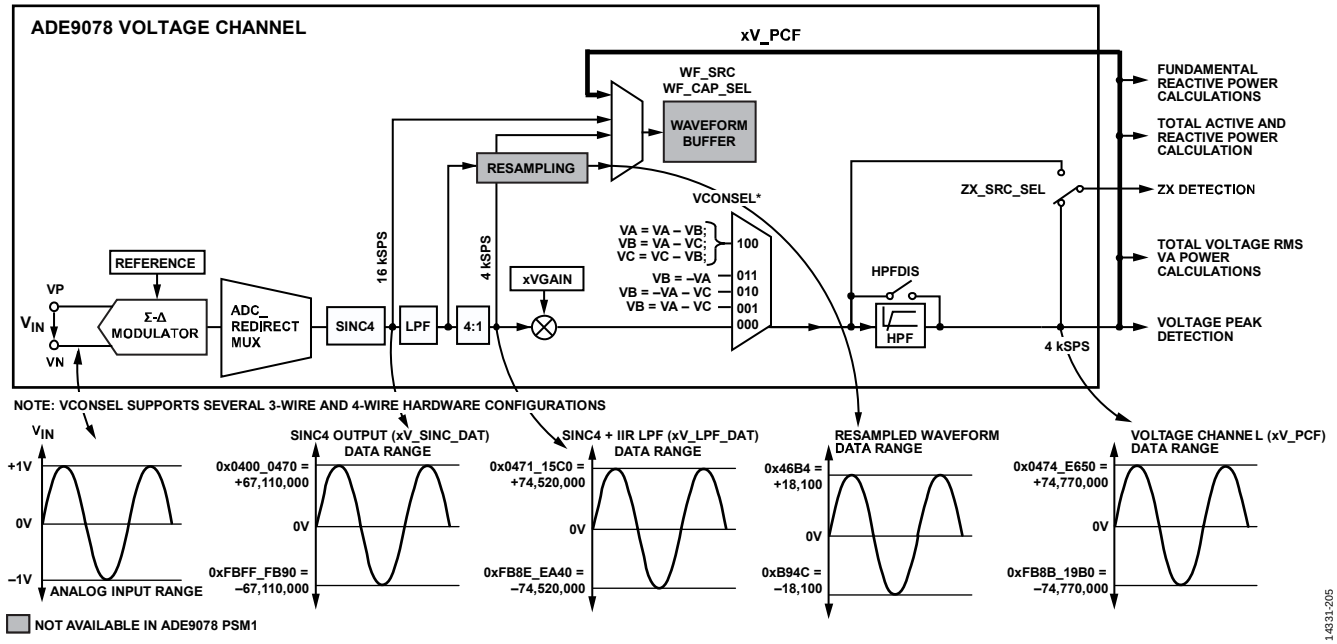


Figure 105. Voltage Channel Datapath

FIXED DATA RATE WAVEFORMS

Fixed data rate waveforms from the signal chain can be stored into the waveform buffer from the sources shown in Table 27.

Table 27. Fixed Data Rate Waveform Sources

Source	WF_SRC	Data Rate (kSPS)	32-Bit Data Format
Sinc4 Outputs	0	16	According to Figure 106
Sinc4 + IIR LPF Output	2	4	According to Figure 106
Waveforms Processed by the DSP (xI_PCF, xV_PCF)	3	4	5.27 format

The 24-bit sinc4 and sinc4 + IIR LPF data is stored as 32 bits in the waveform buffer by shifting left by 4 bits and sign extended.

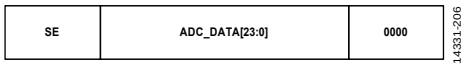


Figure 106. Format for the ADC Data Stored in the Waveform Buffer, x_SINC_DAT, and x_LPF_DAT Registers

Table 27 indicates the WF_SRC selection for each fixed data rate waveform source. Each fixed data rate sample is 32-bit; however, the data format varies between the three sources, as indicated in Table 27. When the waveform buffer is enabled, the data from all seven channels is stored into the buffer. One sample set consists of one sample per channel, seven samples total, which are taken at the same point in time.

Figure 107 shows how the fixed data rate samples are stored into the buffer. Every sample set is separated in memory from the adjacent one by the use of spare cells, which do not contain any sample data, as shown in Figure 107. In this way, every eighth 32-bit memory location in the buffer is reserved as a spare cell. If the seventh channel is disabled, with the WF_IN_EN bit in the WFB_CFG register = 0, the IN sample locations are treated as spare cells as well.

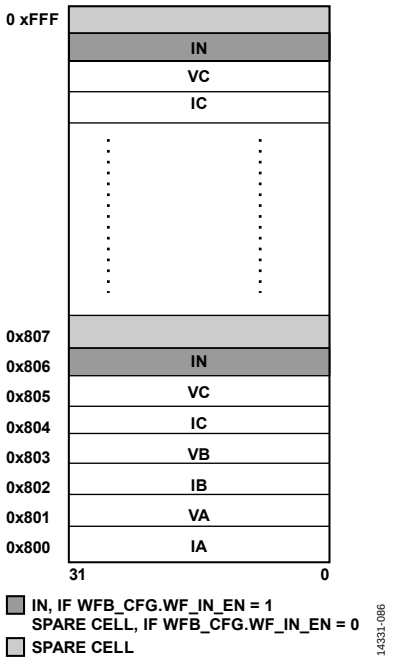


Figure 107. Fixed Data Rate Waveform Sample Storage

There are 256 (2048/8) sample sets that can be stored in the buffer. In the ADE9078, the sinc4 outputs at 16 kSPS so the buffer can contain (256/16,000) = 16 ms of data from the sinc4 filter. The sinc4 + IIR LPF samples and DSP processed xI_PCF and xV_PCF waveform samples are filled at 4 kHz, and the buffer can contain 64 ms (256/4000) of this data.

When used with fixed data rate samples, the waveform buffer is divided into 16 pages, Page 0 to Page 15. Each page contains 128 32-bit memory locations. Figure 108 illustrates this arrangement.

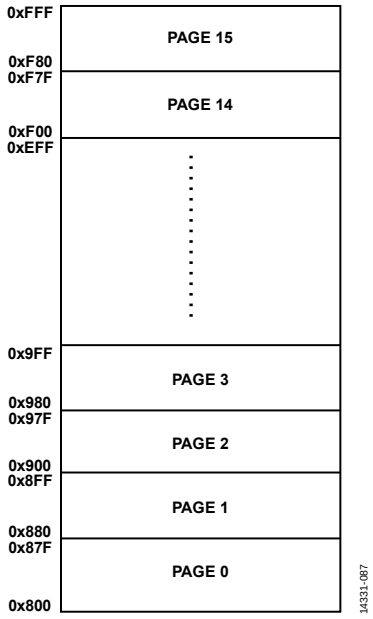


Figure 108. Waveform Buffer Page Arrangement—for Fixed Data Rate Samples Only

Waveform Buffer Filling Indication—Fixed Data Rate Samples

The WFB_PG_IRQEN register allows the user to monitor if specific pages are filled, with one bit available per page. For example, if Bit 0 and Bit 3 of WFB_PG_IRQEN is set, the user receives an indication when Address 0x87F has been written, when Page 0 is full, and when Address 0x9FF has been written, meaning that Page 3 is full. The PAGE_FULL bit of the STATUS0 register is set to 1 when a page enabled in the WFB_PG_IRQEN register is filled. The user can enable an interrupt to occur on $\overline{\text{IRQ0}}$ when the PAGE_FULL bit is set by setting the PAGE_FULL bit in the STATUS0 register.

The WFB_LAST_PAGE bits in the WFB_TRG_STAT register indicate which page was filled last when filling with fixed data rate samples.

FIXED DATA RATE WAVEFORMS FILLING AND TRIGGER-BASED MODES

The waveform buffer offers the following different filling modes to be used with fixed data rate samples:

- Stop when buffer is full
- Continuous filling

The ADE9078 allows a selection of events to trigger waveform buffer captures and there is an option to store the current waveform buffer address during an event to allow the user to synchronize the event with the waveform samples. The following waveform buffer actions can be associated with an event when the buffer is filling continuously:

- Stop filling on trigger
- Center capture around trigger
- Save the event address and keep filling

Stop When Buffer Is Full Mode

The stop when buffer is full mode is enabled when WF_CAP_SEL = 1 and the WF_MODE bits = 0 in the WFB_CFG register. Set the WF_CAP_EN bit in the WFB_CFG register to start filling the buffer from Address 0x800.

After Address 0xFFF in Page 15 is written, the filling operation stops. To receive an indication when the buffer is full, set Bit 15 of the WFB_PG_IRQEN register prior to starting the capture. Then, the PAGE_FULL bit in STATUS0 is set when the buffer is full. This PAGE_FULL status change can be enabled to generate an interrupt on $\overline{\text{IRQ0}}$ as well.

To perform the next filling operation, disable the waveform buffer by clearing bit WF_CAP_EN of the WFB_CFG register to 0, and enable it again by setting the same bit to 1.

Continuous Fill Mode

Continuous fill mode is enabled when WF_CAP_SEL = 1 and WF_MODE in the WFB_CFG register is equal to 1, 2, or 3. Write the WF_CAP_EN bit in the WFB_CFG register to start filling the buffer from Address 0x800.

In this mode, the waveform buffer is filled continuously. After the entire buffer is filled up to Address 0xFFF, the filling continues from Address 0x800 in a circular fashion.

In this mode, it is important to monitor the filling status of the buffer using WFB_PG_IRQEN register in conjunction with the PAGE_FULL bit in the STATUS0 register and WFB_LAST_PAGE bits in the WFB_TRG_STAT register, as described in the Waveform Buffer Filling Indication—Fixed Data Rate Samples section. If the data is not read out of the buffer soon enough, it is overwritten.

To restart the filling operation, disable the waveform buffer by clearing the WF_CAP_EN bit of the WFB_CFG register, and then enable it again by setting this bit.

It is recommended to read the WFB_LAST_PAGE register before stopping the waveform buffer capture by clearing WF_CAP_EN so that the page that contains the most recent valid data is known.

There are two variations on the continuous fill mode that stop filling the waveform buffer based on a trigger event: stop filling on trigger and center capture around trigger modes. These modes are selected when WF_MODE = 1 and 2, respectively (see the Stop Filling on Trigger and Center Capture Around Trigger sections for more information).

Stop Filling on Trigger

When WF_CAP_SEL = 1 and WF_MODE = 1, stop filling on trigger mode is selected. It is recommended to use this mode to analyze the ADC samples leading up to an event of interest.

In this mode, the waveform buffer is filled continuously. After the entire buffer is filled up to Address 0xFFF, the filling continues from Address 0x800 in a circular fashion. The events listed in Table 28 are classified as trigger events. Upon receiving an enabled trigger event, the ADE9078 stops filling the waveform buffer.

The events listed in Table 28 can be enabled as waveform buffer triggers in the WFB_TRG_CFG register.

Table 28. Waveform Buffer Trigger Events in the WFB_TRG_CFG Register

Bit(s)	Bit Name	Comment
10	TRIG_FORCE	Set this bit to trigger an event to stop the waveform buffer filling
9	ZXCOMB	ZX on combined signal from VA, VB, VC
8	ZXVC	ZX event in Phase C voltage
7	ZXVB	ZX event in Phase B voltage
6	ZXVA	ZX event in Phase A voltage
5	ZXIC	ZX event in Phase C current
4	ZXIB	ZX event in Phase B current
3	ZXIA	ZX event in Phase A current
[2:0]	Reserved	Reserved

The trigger events in the WFB_TRG_CFG register, Bits[10:3] correspond to interrupt events within the ADE9078 with the exception of the TRIG_FORCE bit. The user can set the TRIG_FORCE bit, Bit 10 in the WFB_TRG_CFG register, to stop the filling the waveform buffer in this mode.

When one of the events configured in WFB_TRG_CFG occurs, the WFB_TRIG bit is set in the STATUS0 register. This bit can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin.

After the filling of the buffer stops, the WFB_TRG_IRQ bit is set in the STATUS0 register. WFB_TRG_IRQ can also be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. At this time, the address of the IN waveform of the last sample set is stored in the WFB_TRIG_ADDR bits of the WFB_TRG_STAT register. Because the filling stops when the event occurs, any sample sets with addresses greater than the WFB_TRIG_ADDR register contain old data.

To ensure that a buffer's worth of samples are captured before the event, follow this sequence:

1. Select stop capture on trigger mode by setting WF_CAP_SEL = 1 and WF_MODE = 1.
2. Disable all trigger events by writing WFB_TRG_CFG = 0.
3. Ensure that the buffer is filled one time by enabling an interrupt to occur on $\overline{\text{IRQ0}}$ when the last page is filled by setting only Bit 15 in the WFB_PG_IRQEN register and enabling the PAGE_FULL bit in the STATUS0 register. Alternatively, read the LAST_PAGE register instead of using the interrupt.
4. Start the capture by writing WF_CAP_EN = 1.
5. Wait for the buffer to be filled, indicated by when the PAGE_FULL interrupt occurs or LAST_PAGE = 15.
6. Then, enable the desired waveform buffer events in the WFB_TRG_CFG register and set the WFB_TRIG_IRQ bit in STATUS0 to generate an interrupt when the event has occurred and the waveform buffer has stopped filling.
7. When the WFB_TRIG_IRQ occurs, read WFB_TRIG_ADDR to see the address of the trigger event, which is within a sample or two of when the event occurred and is the last filled address.

Waveform buffer values are retained when the waveform buffer is disabled by clearing WF_CAP_EN in the WFB_CFG register; however WFB_LAST_PAGE and WFB_TRIG_ADDR are reset when that bit is cleared. Read the WFB_LAST_PAGE and WFB_TRIG_ ADDR bits before writing WF_CAP_EN = 0.

Trigger events given in Table 28 must be enabled or disabled before enabling the waveform buffer by writing to the WFB_TRG_CFG register.

To perform the next filling operation in the stop filling on trigger mode, disable the waveform buffer by clearing the WF_CAP_EN bit of the WFB_CFG and then enable it again by setting the same bit to 1. Note that if the TRIG_FORCE bit was set to force a trigger that it must be cleared in the WFB_TRG_CFG register before starting the next capture (before writing WF_CAP_EN = 1).

Center Capture Around Trigger

The center capture around trigger mode is enabled when WF_CAP_SEL = 1 and WF_MODE = 2 and is similar to the stop on trigger, except that the waveform buffer does not stop filling after the trigger event. Even after the occurrence of the trigger event, the filling of the buffer continues to occur for the next 1024 32-bit memory locations before stopping. It is recommended to use this mode to analyze samples before and after an event. See the Stop Filling on Trigger section for more information about trigger events.

Note that in the center trigger mode, the WFB_TRIG bit in STATUS0 is set when the enabled trigger event occurs while the WFB_TRG_IRQ bit in STATUS0 is set when the 1024 additional memory locations are filled and the waveform buffer filling stops. Both of these status bits can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. Calculate the last filled address, using WFB_TRIG_ADDR, as follows:

$$Last\ Filled\ Address = WFB\_TRIG\_ADDR - 1024$$

where $WFB\_TRIG\_ADDR + 1024 > 0xFFF$.

$$Last\ Filled\ Address = WFB\_TRIG\_ADDR + 1024$$

where $WFB\_TRIG\_ADDR + 1024 \leq 0xFFF$.

To ensure that a buffer's worth of samples is captured before the event, follow this sequence:

1. Select center capture on trigger mode by setting WF_CAP_SEL = 1 and WF_MODE = 2.
2. Disable all trigger events by writing WFB_TRG_CFG = 0.
3. Ensure that at least half of the buffer is filled by enabling an interrupt to occur on $\overline{\text{IRQ0}}$ when the Page 7 is filled by setting only Bit 7 in the WFB_PG_IRQEN register and enabling the PAGE_FULL bit in the STATUS0 register. Alternatively, read the WFB_LAST_PAGE register instead of using the interrupt.
4. Start the capture by writing WF_CAP_EN = 1.
5. Wait for the buffer to be filled, which is indicated by the PAGE_FULL interrupt occurring or WFB_LAST_PAGE = 15.
6. Enable the desired waveform buffer events in the WFB_TRG_CFG register and set the WFB_TRIG_IRQ bit in the STATUS0 register to generate an interrupt when the event has occurred and the waveform buffer has stopped filling.
7. When the WFB_TRIG_IRQ occurs, read the WFB_TRIG_ADDR register to acquire the address of the trigger event that is within a sample or two of when the event occurred. The last filled address is 1024 samples later.

Save Event Address and Keep Filling

To record the waveform buffer address when a trigger event occurs while still filling the buffer, select WF_MODE = 3 for continuous filling. When a trigger event that is enabled in the WFB_TRG_CFG register occurs, the WFB_TRIG bit in the STATUS0 register is set. WFB_TRIG can be configured to generate an interrupt on the $\overline{\text{IRQ0}}$ pin. Read the WFB_TRIG_ADDR bits in the WFB_TRIG_STAT register to acquire the waveform buffer address for the event. Only the first enabled trigger address is stored; any later trigger events are ignored.

RESAMPLED WAVEFORMS

When resampling is enabled, the data from all seven channels is calculated and stored into the buffer. One sample set consists of one sample per channel, seven samples total, which are from the same point in time. Each resampled waveforms sample is 16 bits.

Figure 109 shows how the resampled waveforms are stored into the buffer. Every sample set is separated in memory from the adjacent one by the use of spare cells, as shown in Figure 109. These spare cells do not contain any sample data. There is one 16-bit spare cell at the end of every fourth consecutive 32-bit memory location. If the neutral current channel is disabled, the 16-bit location that stores IN samples also act as spare cells.

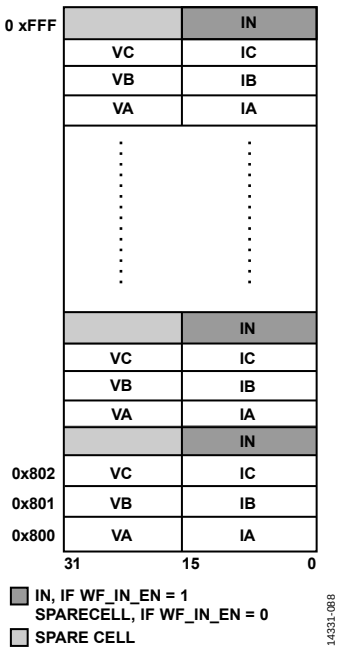


Figure 109. Resampled Waveform Sample Storage

The waveform buffer contains 2048 32-bit memory locations and can hold 512 (2048/4) sets of samples in coherent fill mode. In the ADE9078, the buffer is filled with 64 points per line cycle, which implies that the buffer can hold eight line cycles worth of data at any instant in time. With a 50 Hz line frequency, the buffer contains 160 ms worth of resampled data.

First, to disable the waveform buffer, clear the WF_CAP_EN bit. Then, clear the WF_CAP_SEL bit in the WFB_CFG register to select resampled data to be stored in the waveform buffer. Finally, set the WF_CAP_EN bit to start the resampling process. The waveform buffer starts filling from its first address location, Address 0x800. When the waveform buffer is full, the COH_WFB_FULL bit of STATUS0 goes high, which can be enabled to generate an interrupt on $\overline{\text{IRQ0}}$. Note that this bit is the only status bit available for the resampled waveforms.

The time taken to fill the buffer depends on the line frequency. The waveform buffer values are retained even when the waveform buffer is disabled, by clearing the WF_CAP_EN bit in the WFB_CFG register.

To receive a new set of resampled data, disable the waveform buffer by resetting the WF_CAP_EN bit of the WFB_CFG register to 0, and enable it again by setting the same bit to 1.

CONFIGURING THE WAVEFORM BUFFER

The waveform source, type of capture (fixed data rate or resampled), and fill mode (continuous, one time, or based on trigger) must be configured in the WFB_CFG register. To do so, first disable the waveform buffer by writing WF_CAP_EN = 0. Then, write the WF_SRC, WF_CAP_SEL, and WF_MODE bits of the WFB_CFG register.

When the WF_CAP_EN bit is set, whichever mode selected by the WF_CAP_SEL and WF_MODE bits in the WFB_CFG register is initiated.

For example, if WF_CAP_SEL = 0, the resampled waveforms are stored into the buffer. If WF_CAP_SEL = 1, the fixed data rate samples are stored into the buffer, and the WF_MODE bits indicate whether the buffer is filled continuously or only one time, and if trigger events affects the buffer filling. All of these bits must be configured before writing the WF_CAP_EN bit in the WFB_CFG register.

When the waveform buffer is disabled by clearing the WF_CAP_EN bit, the waveform buffer data remains valid; however, the WFB_LAST_ADDR and WFB_TRIG_ADDR registers are reset.

To start a new waveform capture, disable the waveform buffer by writing WF_CAP_EN = 0. Then, configure the WF_CAP_SEL and WF_MODE bits as desired by writing to the WFB_CFG register. Finally, set the WF_CAP_EN bit in the WFB_CFG register to start the capture. Do not change the WF_CAP_SEL or WF_MODE bits while the WF_CAP_EN bit is set.

BURST READ WAVEFORM BUFFER SAMPLES FROM SPI

The waveform buffer contents can be read using the SPI burst read mode. The SPI burst read mode allows many samples of data to be read while only sending one SPI command header.

To make it easier to read out the desired data using the SPI burst read functionality, the user can indicate which channels of data to read out of the waveform buffer, using the BURST_CHAN bits in the WFB_CFG register, as shown in Table 29.

Table 29. Waveform Buffer Burst Read

BURST_CHAN	Channels to Burst
0000 (default)	All channels
0001	IA and VA
0010	IB and VB
0011	IC and VC
1000	IA
1001	VA
1010	IB
1011	VB
1100	IC
1101	VC
1110	IN if WF_IN_EN = 1 in the WFB_CFG register
1111	Single address read (SPI burst mode is disabled)

The same BURST_CHAN options are available for both fixed data rate samples and resampled data.

The waveform buffer sample that is read out depends on the selection in BURST_CHAN and whether the stored data is fixed data rate data or resampled data.

If BURST_CHAN is not equal to 1111, and the fixed data rate data is stored in the waveform buffer, when WF_CAP_SEL = 1, the three LSBs of the address are masked out when determining which sample set to read out.

If BURST_CHAN is not equal to 1111, and resampled data is stored in the waveform buffer, when WF_CAP_SEL = 0, the two LSBs of the address are masked out when determining which sample set to read out.

If BURST_CHAN = 1111, whichever address was written in the CMD_HDR is read out.

These cases are summarized in Table 30.

Table 30. SPI Address Interpretation when Reading from Waveform Buffer

	Address of Sample (Set)	
Capture Type	BURST_CHAN ≠ 1111	BURST_CHAN = 1111
Fixed Data Rate Samples (WF_CAP_SEL = 1)	ADDR, Bits[11:3]	ADDR, Bits [11:0]
Resampled Data (WF_CAP_SEL = 0)	ADDR, Bits [11:2]	ADDR, Bits [11:0]

Example 1: Fixed Data Rate Data, Seven Channel Samples

In this example, WFB_CAP_SEL = 1, WF_IN_EN = 1, and BURST_CHAN = 0000 in the WFB_CFG register, which indicates that there is fixed data rate data in the waveform buffer, and the user wants to read out samples from all seven channels. A command is sent to read Address 0x801, which is interpreted as a read to the sample set starting at Address 0x800. The first 32 SPI clocks return IA from Address 0x800, followed by VA from Address 0x801, and so on until IN returns from Address 0x806. Then, the sample set auto-increments and the next data is IA from Address 0x808, followed by VA. This example is depicted in Figure 110.

Example 2: Resampled Data, Phase C (I and V Samples)

In this example, WFB_CAP_SEL = 0 and BURST_CHAN = 0011 in the WFB_CFG register, which indicates that there is resampled data in the waveform buffer, and the user wants to read out IC and VC samples. A command is sent to read Address 0x801, which is interpreted as a read to the sample set starting at Address 0x800. The first 16 SPI clocks return the IC waveform from Address 0x802, followed by VC from Address 0x802. Then, the sample set auto-increments and the next data is IC from Address 0x806, followed by VC from the same address. Then, IC from Address 0x80A and VC from Address 0x80A and are read out. This example is depicted in Figure 111.

Example 3: Fixed Data Rate Data, Single Address Read Mode

In this example, WFB_CAP_SEL = 1 and BURST_CHAN = 1111 in the WFB_CFG register, which indicates that there is fixed data rate data in the waveform buffer, and the user wants to read out one single address. A command is sent to read Address 0x801, which is interpreted as a read to Address 0x801. The first 32 SPI clocks return the VA waveform from Address 0x801, followed by CRC if BURST_EN = 0. If BURST_EN = 1, the VA waveform data from Address 0x801 is repeated again. This example is depicted in Figure 112.

Example 4: Resampled Data, Single Address Read Mode

In this example, WFB_CAP_SEL = 0 and BURST_CHAN = 1111 in the WFB_CFG register, which indicates that there is resampled data in the waveform buffer, and the user wants to read out one a single address. A command is sent to read Address 0x801, which is interpreted as a read to Address 0x801. The first 16 SPI clocks return the VA waveform from Address 0x801, followed by the IA waveform from Address 0x801, and, finally, the CRC if BURST_EN = 0. If BURST_EN = 1, the VA and IA waveform data from Address 0x801 is repeated again. This example is depicted in Figure 113.

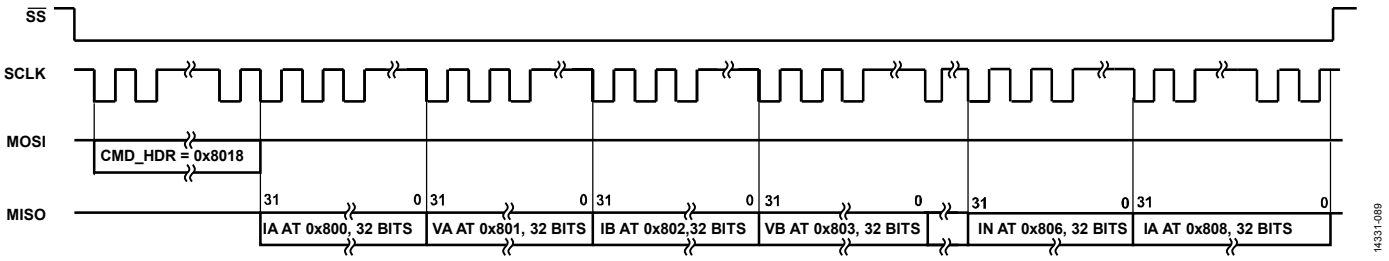


Figure 110. Waveform Buffer SPI Burst Read of Fixed Data Rate Samples, with BURST_CHAN = 0000, to Read out All Channels (the Default State of the MOSI Pin Depends on the Master SPI Device; It Is Assumed to Be High (Logic 1))

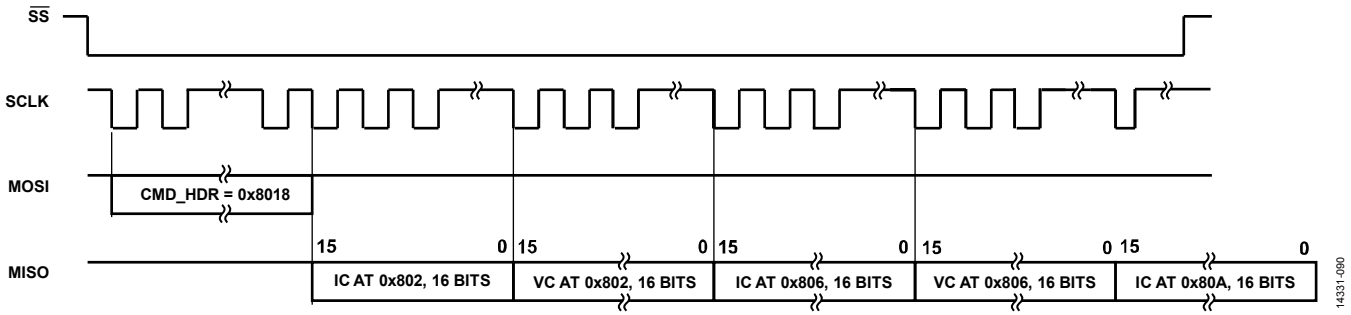


Figure 111. Waveform Buffer SPI Burst Read of Resampled Data, with BURST_CHAN = 0011, to Read out IC and VC Data

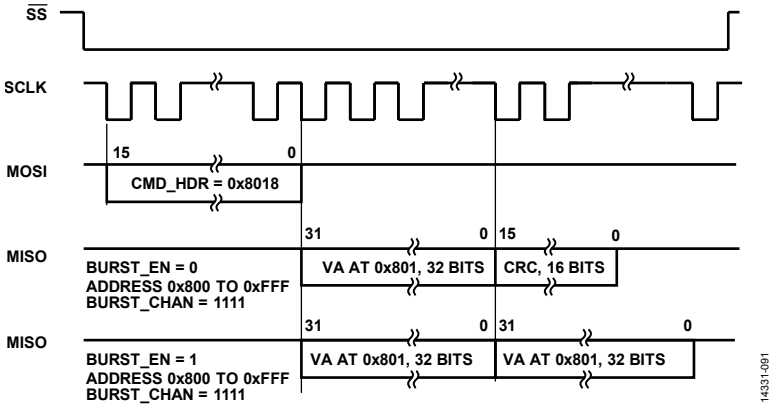


Figure 112. Waveform Buffer SPI Single Address Read of Fixed Rate Data with BURST_CHAN = 1111

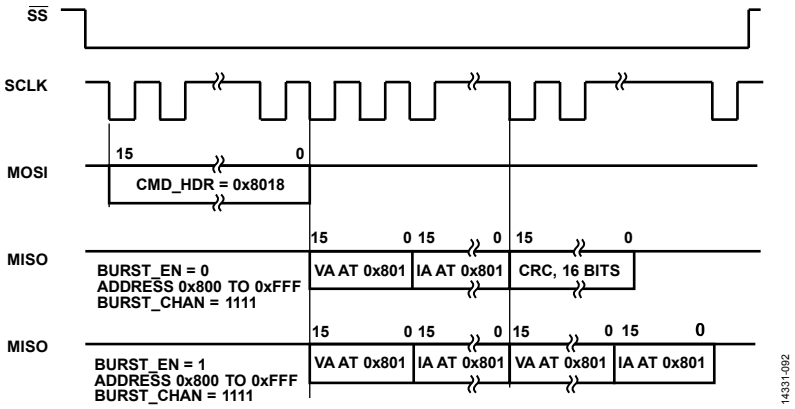


Figure 113. Waveform Buffer SPI Single Address Read of Resampled Data with BURST_CHAN = 1111

SPI CRC when Reading the Waveform Buffer

When reading fixed data rate samples with WF_CAP_SEL = 1, data read out of the waveform buffer has a CRC calculated, which is stored into the CRC_SPI register and can be read back after the waveform buffer burst read.

When reading a single address of waveform buffer data, the CRC_SPI is calculated and appended after the 32-bit data, as shown in Figure 112.

Note that when reading resampled data out of the waveform buffer, when WF_CAP_SEL = 0, the CRC _RSLT register is not updated. It is recommended to read the waveform buffer a second time to check the integrity of the SPI read data.

SPI Last Data Register when Reading the Waveform Buffer

If BURST_CHAN = 1111, the LAST_DATA_32 register is updated after reading a sample in the waveform buffer.

Note that the LAST_DATA_32 register is not updated when reading the waveform buffer samples if BURST_CHAN is not equal to 1111.

INTERRUPTS/EVENTS

The ADE9078 has three pins ($\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and CF4/$\overline{\text{EVENT}}$/$\overline{\text{DREADY}}$) that can be used as interrupts to the host processor. The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins go low when an enabled interrupt occurs and stay low until the event is acknowledged by setting the corresponding status bit in the STATUS0 and STATUS1 registers, respectively. The $\overline{\text{EVENT}}$ function, which is multiplexed with the CF4 and DREADY options on the CF4/$\overline{\text{EVENT}}$/$\overline{\text{DREADY}}$ pin, tracks the state of the enabled signals and goes low and high with these internal signals. The $\overline{\text{EVENT}}$ function is especially useful for measuring the duration of events, such as no load, externally.

INTERRUPTS ($\overline{\text{IRQ0}}$ AND $\overline{\text{IRQ1}}$)

The $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins are managed by 32-bit interrupt mask registers, MASK0 and MASK1, respectively. Every event that can generate an interrupt has a corresponding bit in the MASK0 or MASK1 register and STATUS0 or STATUS1 register.

To enable an interrupt, set the corresponding bit in the MASK0 or MASK1 register. To disable an interrupt, the corresponding bit in MASK0 or MASK1 must be cleared.

The STATUS0 and STATUS1 registers indicate if an event that can generate an interrupt has occurred. If the corresponding bit in the MASK0 or MASK1 register is set, an interrupt is generated on the corresponding $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin, and the pin goes low.

To determine the source of the interrupt, read the corresponding STATUS0 or STATUS1 register and identify which enabled bits are set to 1. To acknowledge the event and clear bits in the STATUSx register, write to the STATUSx register with the desired bit positions set to 1. Then, the corresponding $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin goes high.

For example, if a zero crossing occurs on the Phase A voltage input and the ZXVA bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ pin goes low, indicating that an enabled event has occurred. To acknowledge the event, write a 1 to the ZXVA bit in the STATUS1 register and then the $\overline{\text{IRQ1}}$ goes high. The ZXVA bit in the STATUS1 register is set regardless of whether the ZXVA bit is enabled in the MASK1 register.

There are a few interrupts that are nonmaskable, meaning that they are generated even if the corresponding bit in the MASKx register is 0. These nonmaskable interrupts include RSTDONE and ERROR0.

There is an option to combine all the interrupts onto a single interrupt pin, $\overline{\text{IRQ1}}$, instead of using two pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. To activate this option, set the IRQ0_ON_IRQ1 bit in the CONFIG1 register. When IRQ0_ON_IRQ1 = 1, $\overline{\text{IRQ1}}$ indicates both $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ events, and $\overline{\text{IRQ0}}$ indicates $\overline{\text{IRQ0}}$ events.

$\overline{\text{EVENT}}$

The $\overline{\text{EVENT}}$ function is multiplexed with CF4 and DREADY on the CF4/$\overline{\text{EVENT}}$/DREADY pin. To enable the $\overline{\text{EVENT}}$ function to be output on this pin, write CF4_CFG = 10 in the CONFIG1 register.

The EVENT_MASK register manages which signals are incorporated into the $\overline{\text{EVENT}}$ pin. All of these events sources are maskable and disabled by default.

Events are enabled by setting the corresponding mask bit to 1 in the EVENT_MASK register. The $\overline{\text{EVENT}}$ pin goes low whenever one of the enabled events occurs and stay lows until all the enabled signals go high. Then, the $\overline{\text{EVENT}}$ pin goes high. The logic level of the $\overline{\text{EVENT}}$ output is solely dependent on the enabled events; it cannot be changed by the user. Note that the status sources that generate the $\overline{\text{EVENT}}$ signal are not latched—if one event source is selected, the $\overline{\text{EVENT}}$ pin tracks the status of that source.

STATUS BITS IN ADDITIONAL REGISTERS

Several interrupts are used in conjunction with other status registers.

No Load

The RFNOLOAD, VANLOAD, and ANLOAD bits in the MASK1 register function in conjunction with additional status bits in the PHNOLOAD register.

The following bits in the MASK0 register work with the status bits in the PHSIGN register: REVAPx, REVRPx, and REVPSUMx

See Table 32 for more information when the corresponding bits are set in the STATUSx register.

TROUBLESHOOTING

SPI DOES NOT WORK

Check the PMx pins to ensure that PM0 and PM1 are set for the correct power mode (see the Power Modes section).

PSM2_CFG REGISTER VALUE IS NOT RETAINED WHEN GOING FROM PSM2 OR PSM3 TO PSM0

This response is expected. PSM2_CFG must be rewritten after entering PSM0 or PSM1 (see the Power Modes section).

REGISTER INFORMATION

Table 31. Register Summary

Addr.	Name	Description	Len (Bits)	Reset	Access
0x000	AIGAIN	Phase A current gain adjust.	32	0x00000000	R/W
0x001	AIGAIN0	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x002	AIGAIN1	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x003	AIGAIN2	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x004	AIGAIN3	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x005	AIGAIN4	Phase A multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, AIGAIN0 through AIGAIN4, is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x006	APHCAL0	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x007	APHCAL1	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, thn the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x008	APHCAL2	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x009	APHCAL3	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x00A	APHCAL4	Phase A multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the APHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the APHCAL0 through APHCAL4 value is applied based on the AIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x00B	AVGAIN	Phase A voltage gain adjust.	32	0x00000000	R/W
0x00C	AIRMSOS	Phase A current rms offset for filter based AIRMS calculation.	32	0x00000000	R/W
0x00D	AVRMSOS	Phase A voltage rms offset for filter based AVRMS calculation.	32	0x00000000	R/W
0x00E	APGAIN	Phase A power gain adjust for AWATT, AVA, AVAR, and AFVAR calculations.	32	0x00000000	R/W
0x00F	AWATTOS	Phase A total active power offset correction for AWATT calculation.	32	0x00000000	R/W
0x010	AVAROS	Phase A total reactive power offset correction for AVAR calculation.	32	0x00000000	R/W
0x012	AFVAROS	Phase A fundamental reactive power offset correction for AFVAR calculation.	32	0x00000000	R/W
0x020	BIGAIN	Phase B current gain adjust.	32	0x00000000	R/W
0x021	BIGAIN0	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x022	BIGAIN1	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x023	BIGAIN2	Phase B multipoint gain correction facto. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x024	BIGAIN3	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x025	BIGAIN4	Phase B multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, BIGAIN0 through BIGAIN4, is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x026	BPHCAL0	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x027	BPHCAL1	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x028	BPHCAL2	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x029	BPHCAL3	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x02A	BPHCAL4	Phase B multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the BPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the BPHCAL0 through BPHCAL4 value is applied based on the BIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x02B	BVGAIN	Phase B voltage gain adjust.	32	0x00000000	R/W
0x02C	BIRMSOS	Phase B current rms offset for BIRMS calculation.	32	0x00000000	R/W
0x02D	BVRMSOS	Phase B voltage rms offset for BVRMS calculation.	32	0x00000000	R/W
0x02E	BPGAIN	Phase B power gain adjust for BWATT, BVA, BVAR, and BFVAR calculations.	32	0x00000000	R/W
0x02F	BWATTOS	Phase B total active power offset correction for BWATT calculation.	32	0x00000000	R/W
0x030	BVAROS	Phase B total reactive power offset correction for BVAR calculation.	32	0x00000000	R/W
0x032	BFVAROS	Phase B fundamental reactive power offset correction for BFVAR calculation.	32	0x00000000	R/W
0x040	CIGAIN	Phase C current gain adjust.	32	0x00000000	R/W
0x041	CIGAIN0	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x042	CIGAIN1	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x043	CIGAIN2	Phase C multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x044	CIGAIN3	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x045	CIGAIN4	Phase C Multipoint gain correction factor. If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, an additional gain factor, CIGAIN0 through CIGAIN4, is applied based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x046	CPHCAL0	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x047	CPHCAL1	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x048	CPHCAL2	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x049	CPHCAL3	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x04A	CPHCAL4	Phase C multipoint phase correction factor. If multipoint phase and gain calibration is disabled, with MTEN = 0 in the CONFIG0 register, the CPHCAL0 phase compensation is applied. If multipoint phase and gain correction is enabled, with MTEN = 1, the CPHCAL0 through CPHCAL4 value is applied, based on the CIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	32	0x00000000	R/W
0x04B	CVGAIN	Phase C voltage gain adjust.	32	0x00000000	R/W
0x04C	CIRMSOS	Phase C current rms offset for CIRMS calculation.	32	0x00000000	R/W
0x04D	CVRMSOS	Phase C voltage rms offset for CVRMS calculation.	32	0x00000000	R/W
0x04E	CPGAIN	Phase C power gain adjust for CWATT, CVA, CVAR, and CFVAR calculations.	32	0x00000000	R/W
0x04F	CWATTOS	Phase C total active power offset correction for CWATT calculation.	32	0x00000000	R/W
0x050	CVAROS	Phase C total reactive power offset correction for CVAR calculation.	32	0x00000000	R/W
0x052	CFVAROS	Phase C fundamental reactive power offset correction for CFVAR calculation.	32	0x00000000	R/W
0x060	CONFIG0	Configuration Register 0.	32	0x00000000	R/W
0x061	MTTHR_L0	Multipoint phase/gain threshold. If MTEN = 1 in the CONFIG0 register, the MTTHR_Lx and MTTHR_Hx registers set up the ranges in which to apply each set of corrections, allowing for hysteresis. See the Multipoint Gain and Phase Calibration section for more information.	32	0x00000000	R/W
0x062	MTTHR_L1	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x063	MTTHR_L2	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x064	MTTHR_L3	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x065	MTTHR_L4	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x066	MTTHR_H0	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x067	MTTHR_H1	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x068	MTTHR_H2	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x069	MTTHR_H3	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x06A	MTTHR_H4	Multipoint phase/gain threshold--see MTTHR_L0 for more information.	32	0x00000000	R/W
0x06B	NIRMSOS	Neutral current rms offset for NIRMS calculation.	32	0x00000000	R/W
0x06C	ISUMRMSOS	Offset correction for ISUMRMS calculation based on the sum of IA + IB + IC ± IN.	32	0x00000000	R/W
0x06D	NIGAIN	Neutral current gain adjust.	32	0x00000000	R/W
0x06E	NPHCAL	Neutral current phase compensation.	32	0x00000000	R/W
0x071	VNOM	Nominal phase voltage rms used in the computation of apparent power, xVA, when VNOMx_EN bit is set in the CONFIG0 register.	32	0x00000000	R/W
0x072	DICOEFF	Value used in the digital integrator algorithm. If the integrator is turned on, with INTEN or ININTEN equal to one in the CONFIG0 register, it is recommended to set this value to 0xFFFFE000.	32	0x00000000	R/W
0x073	ISUMLVL	Threshold to compare ISUMRMS against. Configure this register to receive a MISMTCH indication in STATUS0 if ISUMRMS exceeds this threshold.	32	0x00000000	R/W
0x20A	AI_PCF	Instantaneous Phase A current channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x20B	AV_PCF	Instantaneous Phase A voltage channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x20C	AIRMS	Phase A filter based current rms value, updates at 4 kSPS.	32	0x00000000	R
0x20D	AVRMS	Phase A filter based voltage rms value, updates at 4 kSPS.	32	0x00000000	R
0x210	AWATT	Phase A low-pass filtered total active power, updated at 4 kSPS.	32	0x00000000	R
0x211	AVAR	Phase A low-pass filtered total reactive power, updated at 4 kSPS.	32	0x00000000	R
0x212	AVA	Phase A total apparent power, updated at 4 kSPS.	32	0x00000000	R
0x214	AFVAR	Phase A fundamental reactive power, updated at 4 kSPS.	32	0x00000000	R
0x216	APF	Phase A power factor, updated at 1.024 sec.	32	0x00000000	R
0x21D	AMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which AIGAINx and APHCALx is currently being used.	32	0x0000000F	R
0x22A	BI_PCF	Instantaneous Phase B current channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x22B	BV_PCF	Instantaneous Phase B voltage channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x22C	BIRMS	Phase B filter based current rms value, updates at 4 kSPS.	32	0x00000000	R
0x22D	BVRMS	Phase B filter based voltage rms value, updates at 4 kSPS.	32	0x00000000	R
0x230	BWATT	Phase B low-pass filtered total active power, updated at 4 kSPS.	32	0x00000000	R
0x231	BVAR	Phase B low-pass filtered total reactive power, updated at 4 kSPS.	32	0x00000000	R
0x232	BVA	Phase B total apparent power, updated at 4 kSPS.	32	0x00000000	R
0x234	BFVAR	Phase B fundamental reactive power, updated at 4 kSPS.	32	0x00000000	R
0x236	BPF	Phase B power factor, updated at 1.024 sec.	32	0x00000000	R
0x23D	BMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the COFIG0 register, these bits indicate which BIGAINx and BPHCALx is currently being used.	32	0x0000000F	R
0x24A	CI_PCF	Instantaneous Phase C current channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x24B	CV_PCF	Instantaneous Phase C voltage channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x24C	CIRMS	Phase C filter based current rms value, updates at 4 kSPS.	32	0x00000000	R

Addr.	Name	Description	Len (Bits)	Reset	Access
0x24D	CVRMS	Phase C filter based voltage rms value, updates at 4 kSPS.	32	0x00000000	R
0x250	CWATT	Phase C low-pass filtered total active power, updated at 4 kSPS.	32	0x00000000	R
0x251	CVAR	Phase C low-pass filtered total reactive power, updated at 4 kSPS.	32	0x00000000	R
0x252	CVA	Phase C total apparent power, updated at 4 kSPS.	32	0x00000000	R
0x254	CFVAR	Phase C fundamental reactive power, updated at 4 kSPS.	32	0x00000000	R
0x256	CPF	Phase C power factor, updated at 1.024 sec.	32	0x00000000	R
0x25D	CMTREGION	If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	32	0x0000000F	R
0x265	NI_PCF	Instantaneous neutral current channel waveform processed by the DSP, at 4 kSPS.	32	0x00000000	R
0x266	NIRMS	Neutral current filter based rms value.	32	0x00000000	R
0x269	ISUMRMS	Filter based rms based on the sum of IA + IB + IC ± IN.	32	0x00000000	R
0x26A	VERSION2	This register indicates the version of the metrology algorithms after the user writes run = 1 to start the measurements.	32	0x0000000C	R
0x2E5	AWATT_ACC	Phase A accumulated total active power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x2E6	AWATTHR_LO	Phase A accumulated total active energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x2E7	AWATTHR_HI	Phase A accumulated total active energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x2EF	AVAR_ACC	Phase A accumulated total reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x2F0	AVARHR_LO	Phase A accumulated total reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x2F1	AVARHR_HI	Phase A accumulated total reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x2F9	AVA_ACC	Phase A accumulated total apparent power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x2FA	AVAHR_LO	Phase A accumulated total apparent energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x2FB	AVAHR_HI	Phase A accumulated total apparent energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x30D	AFVAR_ACC	Phase A accumulated fundamental reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x30E	AFVARHR_LO	Phase A accumulated fundamental reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x30F	AFVARHR_HI	Phase A accumulated fundamental reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x321	BWATT_ACC	Phase B accumulated total active power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x322	BWATTHR_LO	Phase B accumulated total active energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x323	BWATTHR_HI	Phase B accumulated total active energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x32B	BVAR_ACC	Phase B accumulated total reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R

Addr.	Name	Description	Len (Bits)	Reset	Access
0x32C	BVARHR_LO	Phase B accumulated total reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x32D	BVARHR_HI	Phase B accumulated total reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x335	BVA_ACC	Phase B accumulated total apparent power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x336	BVAHR_LO	Phase B accumulated total apparent energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x337	BVAHR_HI	Phase B accumulated total apparent energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x349	BFVAR_ACC	Phase B accumulated fundamental reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x34A	BFVARHR_LO	Phase B accumulated fundamental reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x34B	BFVARHR_HI	Phase B accumulated fundamental reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x35D	CWATT_ACC	Phase C accumulated total active power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x35E	CWATTHR_LO	Phase C accumulated total active energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x35F	CWATTHR_HI	Phase C accumulated total active energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x367	CVAR_ACC	Phase C accumulated total reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x368	CVARHR_LO	Phase C accumulated total reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x369	CVARHR_HI	Phase C accumulated total reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x371	CVA_ACC	Phase C accumulated total apparent power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x372	CVAHR_LO	Phase C accumulated total apparent energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x373	CVAHR_HI	Phase C accumulated total apparent energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x385	CFVAR_ACC	Phase C accumulated fundamental reactive power, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x386	CFVARHR_LO	Phase C accumulated fundamental reactive energy, LSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x387	CFVARHR_HI	Phase C accumulated fundamental reactive energy, MSBs. Updated according to the settings in EP_CFG and EGY_TIME registers.	32	0x00000000	R
0x397	PWATT_ACC	Accumulated Positive Total Active Power, MSBs, from AWATT, BWATT and CWATT registers, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x39B	NWATT_ACC	Accumulated Negative Total Active Power, MSBs, from AWATT, BWATT and CWATT registers, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x39F	PVAR_ACC	Accumulated Positive Total Reactive Power, MSBs, from AVAR, BVAR and CVAR registers, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x3A3	NVAR_ACC	Accumulated Negative Total Reactive Power, MSBs, from AVAR, BVAR and CVAR registers, updated after PWR_TIME 4 kSPS samples.	32	0x00000000	R
0x400	IPEAK	Current peak register.	32	0x00000000	R

Addr.	Name	Description	Len (Bits)	Reset	Access
0x401	VPEAK	Voltage peak register.	32	0x00000000	R
0x402	STATUS0	Status Register 0.	32	0x00000000	R/W
0x403	STATUS1	Status Register 1.	32	0x00000000	R/W
0x404	EVENT_STATUS	Event Status Register.	32	0x00000000	R
0x405	MASK0	Interrupt Enable Register 0.	32	0x00000000	R/W
0x406	MASK1	Interrupt Enable Register 1.	32	0x00000000	R/W
0x407	EVENT_MASK	Event enable register.	32	0x00000000	R/W
0x40E	USER_PERIOD	User configured line period value used for resampling when the UPERIOD_SEL bit in the CONFIG2 register is set.	32	0x00500000	R/W
0x40F	VLEVEL	Register used in the algorithm that computes the fundamental reactive power.	32	0x00045D45	R/W
0x418	APERIOD	Line period on Phase A voltage.	32	0x00A00000	R
0x419	BPERIOD	Line period on Phase B voltage.	32	0x00A00000	R
0x41A	CPERIOD	Line period on Phase C voltage.	32	0x00A00000	R
0x41B	COM_PERIOD	Line period measurement on combined signal from Phase A, Phase B, and Phase C voltages.	32	0x00A00000	R
0x41C	ACT_NL_LVL	No load threshold in the total active power datapath.	32	0x0000FFFF	R/W
0x41D	REACT_NL_LVL	No load threshold in the total and fundamental reactive power datapath.	32	0x0000FFFF	R/W
0x41E	APP_NL_LVL	No load threshold in the total apparent power datapath.	32	0x0000FFFF	R/W
0x41F	PHNOLOAD	Phase no load register.	32	0x00000000	R
0x420	WTHR	Sets the maximum output rate from the digital to frequency converter for the total active power for the CF calibration pulse output. It is recommended to write WTHR = 0x0010 0000.	32	0x0000FFFF	R/W
0x421	VARTHR	Sets the maximum output rate from the digital to frequency converter for the total and fundamental reactive power for the CF calibration pulse output. It is recommended to write VARTHR = 0x0010 0000.	32	0x0000FFFF	R/W
0x422	VATHR	Sets the maximum output rate from the digital to frequency converter for the total apparent power for the CF calibration pulse output. It is recommended to write VATHR = 0x0010 0000.	32	0x0000FFFF	R/W
0x423	LAST_DATA_32	This register holds the data read or written during the last 32-bit transaction on the SPI port.	32	0x00000000	R
0x424	ADC_REDIRECT	This register allows any ADC output to be redirected to any digital datapath.	32	0x001FFFFF	R/W
0x425	CF_LCFG	CF calibration pulse width configuration register.	32	0x00000000	R/W
0x472	PART_ID	This register identifies the IC. If the ADE9000_ID bit is 0, the IC is an ADE9078.	32	0x00000000	R
0x480	RUN	Write this register to 1 to start the measurements.	16	0x0000	R/W
0x481	CONFIG1	Configuration Register 1.	16	0x0000	R/W
0x482	ANGL_VA_VB	Time between positive to negative zero crossings on Phase A and Phase B voltages.	16	0x0000	R
0x483	ANGL_VB_VC	Time between positive to negative zero crossings on Phase B and Phase C voltages.	16	0x0000	R
0x484	ANGL_VA_VC	Time between positive to negative zero crossings on Phase A and Phase C voltages.	16	0x0000	R
0x485	ANGL_VA_IA	Time between positive to negative zero crossings on Phase A voltage and current.	16	0x0000	R
0x486	ANGL_VB_IB	Time between positive to negative zero crossings on Phase B voltage and current.	16	0x0000	R

Addr.	Name	Description	Len (Bits)	Reset	Access
0x487	ANGL_VC_IC	Time between positive to negative zero crossings on Phase C voltage and current.	16	0x0000	R
0x488	ANGL_IA_IB	Time between positive to negative zero crossings on Phase A and Phase B current.	16	0x0000	R
0x489	ANGL_IB_IC	Time between positive to negative zero crossings on Phase B and Phase C current.	16	0x0000	R
0x48A	ANGL_IA_IC	Time between positive to negative zero crossings on Phase A and Phase C current.	16	0x0000	R
0x490	CFMODE	CFx configuration register.	16	0x0000	R/W
0x491	COMPMODE	Computation mode register.	16	0x0000	R/W
0x492	ACCMODE	Accumulation mode register.	16	0x0000	R/W
0x493	CONFIG3	Configuration Register 3.	16	0x0000	R/W
0x494	CF1DEN	CF1 denominator register.	16	0xFFFF	R/W
0x495	CF2DEN	CF2 denominator register.	16	0xFFFF	R/W
0x496	CF3DEN	CF3 denominator register.	16	0xFFFF	R/W
0x497	CF4DEN	CF4 denominator register.	16	0xFFFF	R/W
0x498	ZXTOUT	Zero-crossing timeout configuration register.	16	0xFFFF	R/W
0x499	ZXTHRSH	Voltage channel zero-crossing threshold register.	16	0x0009	R/W
0x49A	ZX_LP_SEL	This register selects which zero crossing and which line period measurement are used for other calculations.	16	0x001E	R/W
0x49C	SEQ_CYC	Number of line cycles used for phase sequence detection. It is recommended to set this register to 1.	16	0x00FF	R/W
0x49D	PHSIGN	Power sign register.	16	0x0000	R
0x4A0	WFB_CFG	Waveform buffer configuration register.	16	0x0000	R/W
0x4A1	WFB_PG_IRQEN	This register enables interrupts to occur after specific pages of the waveform buffer have been filled.	16	0x0000	R/W
0x4A2	WFB_TRG_CFG	This register enables events to trigger a capture in the waveform buffer.	16	0x0000	R/W
0x4A3	WFB_TRG_STAT	This register indicates the last page that was filled in the waveform buffer and the location of trigger events.	16	0x0000	R/W
0x4A4	CONFIG5	Configuration Register 5.	16	0x0063	R/W
0x4A8	CRC_RSLT	This register holds the CRC of configuration registers.	16	0x0000	R
0x4A9	CRC_SPI	This register holds the 16-bit CRC of the data sent out on the MOSI pin during the last SPI register read.	16	0x0000	R
0x4AC	LAST_DATA_16	This register holds the data read or written during the last 16-bit transaction on the SPI port.	16	0x0000	R
0x4AE	LAST_CMD	This register holds the address and read/write operation request (CMD_HDR) for the last transaction on the SPI port.	16	0x0000	R
0x4AF	CONFIG2	Configuration Register 2.	16	0x0C00	R/W
0x4B0	EP_CFG	Energy and power accumulation configuration.	16	0x0000	R/W
0x4B1	PWR_TIME	Power update time configuration.	16	0x00FF	R/W
0x4B2	EGY_TIME	Energy accumulation update time configuration.	16	0x00FF	R/W
0x4B4	CRC_FORCE	This register forces an update of the CRC of configuration registers.	16	0x0000	R/W
0x4B5	CRC_OPTEN	This register selects which registers are optionally included in the configuration register CRC feature.	16	0x0000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x4B8	PSM2_CFG	This register configures settings for the low power PSM2 operating mode. This register value is retained in PSM2 and PSM3 but is rewritten to its default value when entering PSM0 or PSM1.	16	0x001F	R/W
0x4B9	PGA_GAIN	This register configures the PGA gain for each ADC.	16	0x0000	R/W
0x4BA	CHNL_DIS	This register can be disables the ADCs individually.	16	0x0000	R/W
0x4BF	WR_LOCK	This register enables the configuration lock feature.	16	0x0000	R/W
0x4E0	VAR_DIS	Enable/disable total reactive power calculation.	16	0x0000	R/W
0x4F0	RESERVED1	This register is reserved.	16	0x0000	R
0x4FE	VERSION	Version of the ADE9078 IC.	16	0x0040	R
0x500	AI_SINC_DAT	Current Channel A ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x501	AV_SINC_DAT	Voltage Channel A ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x502	BI_SINC_DAT	Current Channel B ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x503	BV_SINC_DAT	Voltage Channel B ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x504	CI_SINC_DAT	Current Channel C ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x505	CV_SINC_DAT	Voltage Channel C ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x506	NI_SINC_DAT	Neutral current channel ADC waveforms from sinc4 output, at 16 kSPS.	32	0x00000000	R
0x510	AI_LPF_DAT	Current Channel A ADC waveforms from sinc4 + IIR LPF and decimator output, at 4 kSPS.	32	0x00000000	R
0x511	AV_LPF_DAT	Voltage Channel A ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x512	BI_LPF_DAT	Current Channel B ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x513	BV_LPF_DAT	Voltage Channel B ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x514	CI_LPF_DAT	Current Channel C ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x515	CV_LPF_DAT	Voltage Channel C ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x516	NI_LPF_DAT	Neutral current channel ADC waveforms from sinc4 + IIR LPF output, at 4 kSPS.	32	0x00000000	R
0x600	AV_PCF_1	SPI burst read accessible. Registers organized functionally. See AV_PCF in Table 31.	32	0x00000000	R/W
0x601	BV_PCF_1	SPI burst read accessible. Registers organized functionally. See BV_PCF in Table 31.	32	0x00000000	R/W
0x602	CV_PCF_1	SPI burst read accessible. Registers organized functionally. See CV_PCF in Table 31.	32	0x00000000	R/W
0x603	NI_PCF_1	SPI burst read accessible. Registers organized functionally. See NI_PCF in Table 31.	32	0x00000000	R/W
0x604	AI_PCF_1	SPI burst read accessible. Registers organized functionally. See AI_PCF in Table 31.	32	0x00000000	R/W
0x605	BI_PCF_1	SPI burst read accessible. Registers organized functionally. See BI_PCF in Table 31.	32	0x00000000	R/W
0x606	CI_PCF_1	SPI burst read accessible. Registers organized functionally. See CI_PCF in Table 31.	32	0x00000000	R/W
0x607	AIRMS_1	SPI burst read accessible. Registers organized functionally. See AIRMS in Table 31.	32	0x00000000	R/W
0x608	BIRMS_1	SPI burst read accessible. Registers organized functionally. See BIRMS in Table 31.	32	0x00000000	R/W
0x609	CIRMS_1	SPI burst read accessible. Registers organized functionally. See CIRMS in Table 31.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x60A	AVRMS_1	SPI burst read accessible. Registers organized functionally. See AVRMS in Table 31.	32	0x00000000	R/W
0x60B	BVRMS_1	SPI burst read accessible. Registers organized functionally. See BVRMS in Table 31.	32	0x00000000	R/W
0x60C	CVRMS_1	SPI burst read accessible. Registers organized functionally. See CVRMS in Table 31.	32	0x00000000	R/W
0x60D	NIRMS_1	SPI burst read accessible. Registers organized functionally. See NIRMS in Table 31.	32	0x00000000	R/W
0x60E	AWATT_1	SPI burst read accessible. Registers organized functionally. See AWATT in Table 31.	32	0x00000000	R/W
0x60F	BWATT_1	SPI burst read accessible. Registers organized functionally. See BWATT in Table 31.	32	0x00000000	R/W
0x610	CWATT_1	SPI burst read accessible. Registers organized functionally. See CWATT in Table 31.	32	0x00000000	R/W
0x611	AVA_1	SPI burst read accessible. Registers organized functionally. See AVA in Table 31.	32	0x00000000	R/W
0x612	BVA_1	SPI burst read accessible. Registers organized functionally. See BVA in Table 31.	32	0x00000000	R/W
0x613	CVA_1	SPI burst read accessible. Registers organized functionally. See CVA in Table 31.	32	0x00000000	R/W
0x614	AVAR_1	SPI burst read accessible. Registers organized functionally. See AVAR in Table 31.	32	0x00000000	R/W
0x615	BVAR_1	SPI burst read accessible. Registers organized functionally. See BVAR in Table 31.	32	0x00000000	R/W
0x616	CVAR_1	SPI burst read accessible. Registers organized functionally. See CVAR in Table 31.	32	0x00000000	R/W
0x617	AFVAR_1	SPI burst read accessible. Registers organized functionally. See AFVAR in Table 31.	32	0x00000000	R/W
0x618	BFVAR_1	SPI burst read accessible. Registers organized functionally. See BFVAR in Table 31.	32	0x00000000	R/W
0x619	CFVAR_1	SPI burst read accessible. Registers organized functionally. See CFVAR in Table 31.	32	0x00000000	R/W
0x61A	APF_1	SPI burst read accessible. Registers organized functionally. See APF in Table 31.	32	0x00000000	R/W
0x61B	BPF_1	SPI burst read accessible. Registers organized functionally. See BPF in Table 31.	32	0x00000000	R/W
0x61C	CPF_1	SPI burst read accessible. Registers organized functionally. See CPF in Table 31.	32	0x00000000	R/W
0x680	AV_PCF_2	SPI burst read accessible. Registers organized by phase. See AV_PCF in Table 31.	32	0x00000000	R/W
0x681	AI_PCF_2	SPI burst read accessible. Registers organized by phase. See AI_PCF in Table 31.	32	0x00000000	R/W
0x682	AIRMS_2	SPI burst read accessible. Registers organized by phase. See AIRMS in Table 31.	32	0x00000000	R/W
0x683	AVRMS_2	SPI burst read accessible. Registers organized by phase. See AVRMS in Table 31.	32	0x00000000	R/W
0x684	AWATT_2	SPI burst read accessible. Registers organized by phase. See AWATT in Table 31.	32	0x00000000	R/W
0x685	AVA_2	SPI burst read accessible. Registers organized by phase. See AVA in Table 31.	32	0x00000000	R/W

Addr.	Name	Description	Len (Bits)	Reset	Access
0x686	AVAR_2	SPI burst read accessible. Registers organized by phase. See AVAR in Table 31.	32	0x00000000	R/W
0x687	AFVAR_2	SPI burst read accessible. Registers organized by phase. See AFVAR in Table 31.	32	0x00000000	R/W
0x688	APF_2	SPI burst read accessible. Registers organized by phase. See APF in Table 31.	32	0x00000000	R/W
0x693	BV_PCF_2	SPI burst read accessible. Registers organized by phase. See BV_PCF in Table 31.	32	0x00000000	R/W
0x694	BI_PCF_2	SPI burst read accessible. Registers organized by phase. See BI_PCF in Table 31.	32	0x00000000	R/W
0x695	BIRMS_2	SPI burst read accessible. Registers organized by phase. See BIRMS in Table 31.	32	0x00000000	R/W
0x696	BVRMS_2	SPI burst read accessible. Registers organized by phase. See BVRMS in Table 31.	32	0x00000000	R/W
0x697	BWATT_2	SPI burst read accessible. Registers organized by phase. See BWATT in Table 31.	32	0x00000000	R/W
0x698	BVA_2	SPI burst read accessible. Registers organized by phase. See BVA in Table 31.	32	0x00000000	R/W
0x699	BVAR_2	SPI burst read accessible. Registers organized by phase. See BVAR in Table 31.	32	0x00000000	R/W
0x69A	BFVAR_2	SPI burst read accessible. Registers organized by phase. See BFVAR in Table 31.	32	0x00000000	R/W
0x69B	BPF_2	SPI burst read accessible. Registers organized by phase. See BPF in Table 31.	32	0x00000000	R/W
0x6A6	CV_PCF_2	SPI burst read accessible. Registers organized by phase. See CV_PCF in Table 31.	32	0x00000000	R/W
0x6A7	CI_PCF_2	SPI burst read accessible. Registers organized by phase. See CI_PCF in Table 31.	32	0x00000000	R/W
0x6A8	CIRMS_2	SPI burst read accessible. Registers organized by phase. See CIRMS in Table 31.	32	0x00000000	R/W
0x6A9	CVRMS_2	SPI burst read accessible. Registers organized by phase. See CVRMS in Table 31.	32	0x00000000	R/W
0x6AA	CWATT_2	SPI burst read accessible. Registers organized by phase. See CWATT in Table 31.	32	0x00000000	R/W
0x6AB	CVA_2	SPI burst read accessible. Registers organized by phase. See CVA in Table 31.	32	0x00000000	R/W
0x6AC	CVAR_2	SPI burst read accessible. Registers organized by phase. See CVAR in Table 31.	32	0x00000000	R/W
0x6AD	CFVAR_2	SPI burst read accessible. Registers organized by phase. See CFVAR in Table 31.	32	0x00000000	R/W
0x6AE	CPF_2	SPI burst read accessible. Registers organized by phase. See CPF in Table 31.	32	0x00000000	R/W
0x6B9	NI_PCF_2	SPI burst read accessible. Registers organized by phase. See NI_PCF in Table 31.	32	0x00000000	R/W
0x6BA	NIRMS_2	SPI burst read accessible. Registers organized by phase. See NIRMS in Table 31.	32	0x00000000	R/W

REGISTER DETAILS

Table 32. Register Details

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x060	CONFIG0	[31:14]	RESERVED		Reserved.	0x0	R
		13	DISRPLPF		Set this bit to disable the low-pass filter in the total reactive power datapath.	0x0	R/W
		12	DISAPLPF		Set this bit to disable the low-pass filter in the total active power datapath.	0x0	R/W
		11	ININTEN		Set this bit to enable the digital integrator in the Neutral Current channel.	0x0	R/W
		10	VNOMC_EN		Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase C total apparent power, CVA.	0x0	R/W
		9	VNOMB_EN		Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase B total apparent power, BVA.	0x0	R/W
		8	VNOMA_EN		Set this bit to use the nominal phase voltage rms, VNOM, in the computation of Phase A total apparent power, AVA.	0x0	R/W
		7	RESERVED		Reserved.	0x0	R
		6	ZX_SRC_SEL		This bit selects whether data going into the zero-crossing detection circuit comes before the high-pass filter, integrator, and phase compensation or afterwards.	0x0	R/W
				0	After the high-pass filter, integrator, and phase compensation.		
				1	Before the high-pass filter, integrator, and phase compensation.		
		5	INTEN		Set this bit to enable the integrators in the phase current channels. The neutral current channel integrator is managed by the ININTEN bit in the CONFIG0 register.	0x0	R/W
		4	MTEN		Set this bit to enable multipoint phase and gain compensation. If enabled, an additional gain factor, xIGAIN0 through xIGAIN4, is applied to the current channel based on the xIRMS current rms amplitude and the MTTHR_Lx and MTTHR_Hx register values.	0x0	R/W
		3	HPFDIS		Set this bit to disable high-pass filters in all the voltage and current channels.	0x0	R/W
		2	RESERVED		Reserved.	0x0	R
		[1:0]	ISUM_CFG		ISUM Calculation configuration.	0x0	R/W
				00	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		
				01	ISUM = AI_PCF + BI_PCF + CI_PCF + NI_PCF (to determine mismatch between neutral and phase currents).		
				10	ISUM = AI_PCF + BI_PCF + CI_PCF - NI_PCF (to determine mismatch between neutral and phase currents).		
				11	ISUM = AI_PCF + BI_PCF + CI_PCF (for approximated neutral current rms calculation).		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21D	AMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	AREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which AIGAINx and APHCALx is currently being used.	0xF	R
				0000	AIGAIN0, APHCAL0.		
				0001	AIGAIN1, APHCAL1.		
				0010	AIGAIN2, APHCAL2.		
				0011	AIGAIN3, APHCAL3.		
				0100	AIGAIN4, APHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x23D	BMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	BREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which BIGAINx and BPHCALx is currently being used.	0xF	R
				0000	BIGAIN0, BPHCAL0.		
				0001	BIGAIN1, BPHCAL1.		
				0010	BIGAIN2, BPHCAL2.		
				0011	BIGAIN3, BPHCAL3.		
				0100	BIGAIN4, BPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x25D	CMTREGION	[31:4]	RESERVED		Reserved.	0x0	R
		[3:0]	CREGION		If multipoint gain and phase compensation is enabled, with MTEN = 1 in the CONFIG0 register, these bits indicate which CIGAINx and CPHCALx is currently being used.	0xF	R
				0000	CIGAIN0, CPHCAL0.		
				0001	CIGAIN1, CPHCAL1.		
				0010	CIGAIN2, CPHCAL2.		
				0011	CIGAIN3, CPHCAL3.		
				0100	CIGAIN4, CPHCAL4.		
				1111	This feature is disabled because MTEN = 0 in the CONFIG0 register.		
0x400	IPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	IPPHASE		These bits indicate which phases generate IPEAKVAL value. Note that the PEAKSEL[2:0] bits in the CONFIG3 register determine which current channel to monitor the peak value on. When IPPHASE, Bit 0 is set to 1, Phase A current generated IPEAKVAL, Bits[23:0] value. Similarly, IPPHASE, Bit 1 indicates Phase B and IPPHASE, Bit 2 indicates Phase C current generated the peak value.	0x0	R
		[23:0]	IPEAKVAL		The IPEAK register stores the absolute value of the peak current. IPEAK is equal to xI_PCF/2^5.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x401	VPEAK	[31:27]	RESERVED		Reserved.	0x0	R
		[26:24]	VPPHASE		These bits indicate which phases generate VPEAKVAL value. Note that the PEAKSEL[2:0] bits in the CONFIG3 register determine which voltage channels to monitor the peak value on. When VPPHASE[0] is 1, Phase A voltage generated VPEAKVAL[23:0] value. Similarly, VPPHASE[1] indicates Phase B and VPPHASE[2] indicates Phase C voltage generated the peak value.	0x0	R
		[23:0]	VPEAKVAL		The VPEAK register stores the absolute value of the peak voltage. VPEAK is equal to xV_PCF/2^5.	0x0	R
0x402	STATUS0	[31:25]	RESERVED		Reserved.	0x0	R
		24	MISMTCH		This bit is set to indicate a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W1
		23	COH_WFB_FULL		This bit is set when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W1
		22	WFB_TRIG		This bit is set when one of the events configured in WFB_TRIG_CFG occurs.	0x0	R/W1
		21	PF_RDY		This bit goes high to indicate when the power factor measurements have been updated, every 1.024 sec.	0x0	R/W1
		[20:19]	RESERVED		Reserved.	0x0	R
		18	PWRRDY		This bit is set when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFVAR_ACC registers have been updated, after PWR_TIME 4 kSPS samples.	0x0	R/W1
		17	PAGE_FULL		This bit is set when a page enabled in the WFB_PG_IRQEN register has been filled with fixed data rate samples, when WF_CAP_SEL bit in the WFB_CFG register = 0.	0x0	R/W1
		16	WFB_TRIG_IRQ		This bit is set when the waveform buffer has stopped filling after an event configured in WFB_TRIG_CFG occurs. This happens with fixed data rate samples only, when WF_CAP_SEL bit in the WFB_CFG register = 0.	0x0	R/W1
		15	DREADY		This bit is set when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W1
		14	CF4		This bit is set when a CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W1
		13	CF3		This bit is set when a CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W1
		12	CF2		This bit is set when a CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W1
		11	CF1		This bit is set when a CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W1
		10	REVPSUM4		This bit is set to indicate if the CF4 polarity changed sign. For example, if the last CF4 pulse was positive reactive energy and the next CF4 pulse is negative reactive energy, the REVPSUM4 bit is set. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W1

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		9	REVPSUM3		This bit is set to indicate if the CF3 polarity changed sign. See REVPSUM4.	0x0	R/W1
		8	REVPSUM2		This bit is set to indicate if the CF2 polarity changed sign. See REVPSUM4.	0x0	R/W1
		7	REVPSUM1		This bit is set to indicate if the CF1 polarity changed sign. See REVPSUM4.	0x0	R/W1
		6	REVRPC		This bit indicates if the Phase C total or fundamental reactive power has changed sign. The PWR_SIGN_SEL bit in the EP_CFG register selects whether total or fundamental reactive power is monitored. This bit is updated when the power values in the xVAR_ACC and xFVAR_ACC registers have been updated, after PWR_TIME 4 kSPS samples.	0x0	R/W1
		5	REVRPB		This bit indicates if the Phase B total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W1
		4	REVRPA		This bit indicates if the Phase A total or fundamental reactive power has changed sign. See REVRPC.	0x0	R/W1
		3	REVAPC		This bit indicates if the Phase C total active power has changed sign. This bit is updated when the power values in the xWATT_ACC and xWATT_ACC registers have been updated, after PWR_TIME 4 kSPS samples.	0x0	R/W1
		2	REVAPB		This bit indicates if the Phase B total active power has changed sign. See REVAPC.	0x0	R/W1
		1	REVAPA		This bit indicates if the Phase A total active power has changed sign. See REVAPC.	0x0	R/W1
		0	EGYRDY		This bit is set when the power values in the xWATTHR, xVAHR, xVARHR, xFVARHR registers have been updated, after EGY_TIME 4 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W1
0x403	STATUS1	31	ERROR3		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R/W1
		30	ERROR2		This bit indicates that an error was detected and corrected. No action is required.	0x0	R/W1
		29	ERROR1		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		28	ERROR0		This bit indicates an error and generates a non-maskable interrupt. Issue a software or hardware reset to clear this error.	0x0	R
		27	CRC_DONE		This bit is set to indicate when the configuration register CRC calculation is done, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W1
		26	CRC_CHG		This bit is set if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W1
		[25:19]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		18	SEQERR		This bit is set to indicate a phase sequence error on the Phase Voltage zero crossings.	0x0	R/W1
		17	RESERVED		Reserved.	0x0	R
		16	RSTDONE		This bit is set to indicate that the IC has finished its power-up sequence after a reset or after changing between PSM2 or PSM3 operating mode to PSM0 or PSM1. This indicates that the user can configure the IC via the SPI port.	0x0	R/W1
		15	ZXIC		When this bit is set to 1, it indicates a zero crossing has been detected on Phase C current.	0x0	R/W1
		14	ZXIB		When this bit is set to 1, it indicates a zero crossing has been detected on Phase B current.	0x0	R/W1
		13	ZXIA		When this bit is set to 1, it indicates a zero crossing has been detected on Phase A current.	0x0	R/W1
		12	ZXCOMB		When this bit is set, it indicates a zero crossing has been detected on the combined signal from VA, VB, and VC.	0x0	R/W1
		11	ZXVC		When this bit is set, it indicates a zero crossing has been detected on the Phase C voltage channel.	0x0	R/W1
		10	ZXVB		When this bit is set, it indicates a zero crossing has been detected on the Phase B voltage channel.	0x0	R/W1
		9	ZXVA		When this bit is set, it indicates a zero crossing has been detected on the Phase A voltage channel.	0x0	R/W1
		8	ZXTOVC		This bit is set to indicate a zero crossing timeout on Phase C. This means that a zero crossing on the Phase C voltage is missing.	0x0	R/W1
		7	ZXTOVB		This bit is set to indicate a zero crossing timeout on Phase B. This means that a zero crossing on the Phase B voltage is missing.	0x0	R/W1
		6	ZXTOVA		This bit is set to indicate a zero crossing timeout on Phase A. This means that a zero crossing on the Phase A voltage is missing.	0x0	R/W1
		5	RESERVED		Reserved.	0x0	R
		4	RFNOLOAD		This bit is set when one or more phase fundamental reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W1
		3	RESERVED		Reserved.	0x0	R
		2	VANLOAD		This bit is set when one or more phase total apparent energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W1
		1	RNLOAD		This bit is set when one or more phase total reactive energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W1
		0	ANLOAD		This bit is set when one or more phase total active energy enters or exits the no load condition. The phase is indicated in the PHNOLOAD register.	0x0	R/W1

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x404	EVENT_STATUS	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		This bit changes from a one to a zero when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R
		15	RESERVED		Reserved.	0x0	R
		14	RFNOLOAD		This bit is set when the fundamental reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R
		13	RESERVED		Reserved.	0x0	R
		12	VANLOAD		This bit is set when the total apparent energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total apparent energy accumulation goes into no load.	0x0	R
		11	RNLOAD		This bit is set when the total reactive energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total reactive energy accumulation goes into no load.	0x0	R
		10	ANLOAD		This bit is set when the total active energy accumulations in all phases are out of no load. This bit goes to zero when one or more phases of total active energy accumulation goes into no load.	0x0	R
		9	REVPSUM4		This bit indicates the sign of the last CF4 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R
		8	REVPSUM3		This bit indicates the sign of the last CF3 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R
		7	REVPSUM2		This bit indicates the sign of the last CF2 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R
		6	REVPSUM1		This bit indicates the sign of the last CF1 pulse. A zero indicates that the pulse was from negative energy and a one indicates that the energy was positive. This bit is updated when a CF1 pulse is output, when the CF1 pin goes from high to low.	0x0	R
		[5:0]	RESERVED		Reserved.	0x0	R
0x405	MASK0	[31:25]	RESERVED		Reserved.	0x0	R
		24	MISMTCH		Set this bit to enable an interrupt when there is a change in the relationship between ISUMRMS and ISUMLVL.	0x0	R/W
		23	COH_WFB_FULL		Set this bit to enable an interrupt when the waveform buffer is full with resampled data, which is selected when WF_CAP_SEL = 0 in the WFB_CFG register.	0x0	R/W
		22	WFB_TRIG		Set this bit to enable an interrupt when one of the events configured in WFB_TRIG_CFG occurs.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		21	PF_RDY		Set this bit to enable an interrupt when the power factor measurements have been updated, every 1.024 sec.	0x0	R/W
		[20:19]	RESERVED		Reserved.	0x0	R
		18	PWRRDY		Set this bit to enable an interrupt when the power values in the xWATT_ACC, xVA_ACC, xVAR_ACC, xFVAR_ACC registers have been updated, after PWR_TIME 4 kSPS samples.	0x0	R/W
		17	PAGE_FULL		Set this bit to enable an interrupt when a page enabled in the WFB_PG_IRQEN register has been filled.	0x0	R/W
		16	WFB_TRIG_IRQ		Set this bit to enable an interrupt when This bit is set when the waveform buffer has stopped filling after an event configured in WFB_TRIG_CFG occurs.	0x0	R/W
		15	DREADY		Set this bit to enable an interrupt when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		14	CF4		Set this bit to enable an interrupt when the CF4 pulse is issued, when the CF4 pin goes from a high to low state.	0x0	R/W
		13	CF3		Set this bit to enable an interrupt when the CF3 pulse is issued, when the CF3 pin goes from a high to low state.	0x0	R/W
		12	CF2		Set this bit to enable an interrupt when the CF2 pulse is issued, when the CF2 pin goes from a high to low state.	0x0	R/W
		11	CF1		Set this bit to enable an interrupt when the CF1 pulse is issued, when the CF1 pin goes from a high to low state.	0x0	R/W
		10	REVPSUM4		Set this bit to enable an interrupt when the CF4 polarity changed sign.	0x0	R/W
		9	REVPSUM3		Set this bit to enable an interrupt when the CF3 polarity changed sign.	0x0	R/W
		8	REVPSUM2		Set this bit to enable an interrupt when the CF2 polarity changed sign.	0x0	R/W
		7	REVPSUM1		Set this bit to enable an interrupt when the CF1 polarity changed sign.	0x0	R/W
		6	REVRPC		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W
		5	REVRPB		Set this bit to enable an interrupt when the Phase C total or fundamental reactive power has changed sign.	0x0	R/W
		4	REVRPA		Set this bit to enable an interrupt when the Phase A total or fundamental reactive power has changed sign.	0x0	R/W
		3	REVAPC		Set this bit to enable an interrupt when the Phase C total active power has changed sign.	0x0	R/W
		2	REVAPB		Set this bit to enable an interrupt when the Phase B total active power has changed sign.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	REVAPA		Set this bit to enable an interrupt when the Phase A total active power has changed sign.	0x0	R/W
		0	EGYRDY		Set this bit to enable an interrupt when the power values in the xWATTHR, xVAHR, xVARHR, and xFVARHR registers have been updated, after EGY_TIME 4 kSPS samples or line cycles, depending on the EGY_TMR_MODE bit in the EP_CFG register.	0x0	R/W
0x406	MASK1	31	ERROR3		Set this bit to enable an interrupt if ERROR3 occurs. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		30	ERROR2		Set this bit to enable an interrupt if ERROR2 occurs.	0x0	R/W
		29	ERROR1		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		28	ERROR0		This interrupt is not maskable. Issue a software reset or hardware reset to clear this error.	0x0	R/W
		27	CRC_DONE		Set this bit to enable an interrupt when the configuration register CRC calculation is done, after initiated by writing the FORCE_CRC_UPDATE bit in the CRC_FORCE register.	0x0	R/W
		26	CRC_CHG		Set this bit to enable an interrupt if any of the registers monitored by the configuration register CRC change value. The CRC_RSLT register holds the new configuration register CRC value.	0x0	R/W
		[25:19]	RESERVED		Reserved.	0x0	R
		18	SEQERR		Set this bit to set an interrupt when on a phase sequence error on the phase voltage zero crossings.	0x0	R/W
		[17:16]	RESERVED		Reserved.	0x0	R
		15	ZXIC		Set this bit to set an interrupt when a zero crossing has been detected on the Phase C current channel.	0x0	R/W
		14	ZXIB		Set this bit to set an interrupt when a zero crossing has been detected on the Phase B current channel.	0x0	R/W
		13	ZXIA		Set this bit to set an interrupt when a zero crossing has been detected on the Phase A current channel.	0x0	R/W
		12	ZXCOMB		Set this bit to set an interrupt when a zero crossing has been detected on the combined signal from VA, VB, and VC.	0x0	R/W
		11	ZXVC		Set this bit to set an interrupt when a zero crossing has been detected on the Phase C voltage channel.	0x0	R/W
		10	ZXVB		Set this bit to set an interrupt when a zero crossing has been detected on the Phase B voltage channel.	0x0	R/W
		9	ZXVA		Set this bit to set an interrupt when a zero crossing has been detected on the Phase A voltage channel.	0x0	R/W
		8	ZXTOVC		Set this bit to set an interrupt when there is a zero crossing timeout on Phase C. This means that a zero crossing on the Phase C voltage is missing.	0x0	R/W
		7	ZXTOVB		Set this bit to set an interrupt when there is a zero crossing timeout on Phase B. This means that a zero crossing on the Phase B voltage is missing.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		6	ZXTOVA		Set this bit to set an interrupt when there is a zero crossing timeout on Phase A. This means that a zero crossing on the Phase A voltage is missing.	0x0	R/W
		5	RESERVED		Reserved.	0x0	R
		4	RFNOLOAD		Set this bit to set an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		3	RESERVED		Reserved.	0x0	R
		2	VANLOAD		Set this bit to set an interrupt when one or more phase total apparent energy enters or exits the no load condition.	0x0	R/W
		1	RNLOAD		Set this bit to set an interrupt when one or more phase total reactive energy enters or exits the no load condition.	0x0	R/W
		0	ANLOAD		Set this bit to set an interrupt when one or more phase total active energy enters or exits the no load condition.	0x0	R/W
0x407	EVENT_MASK	[31:17]	RESERVED		Reserved.	0x0	R
		16	DREADY		Set this bit to enable the EVENT pin to go low when new waveform samples are ready. The update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.	0x0	R/W
		15	RESERVED		Reserved.	0x0	R
		14	RFNOLOAD		Set this bit to enable the EVENT pin to go low when one or more phases of fundamental reactive energy accumulation goes into no load.	0x0	R/W
		13	RESERVED		Reserved.	0x0	R
		12	VANLOAD		Set this bit to enable the EVENT pin to go low when one or more phases of total apparent energy accumulation goes into no load.	0x0	R/W
		11	RNLOAD		Set this bit to enable the EVENT pin to go low when one or more phases of total reactive energy accumulation goes into no load.	0x0	R/W
		10	ANLOAD		Set this bit to enable the EVENT pin to go low when one or more phases of total active energy accumulation goes into no load.	0x0	R/W
		9	REVPSUM4		Set this bit to enable the EVENT pin to go low to indicate if the last CF4 pulse was from negative energy. This bit is updated when a CF4 pulse is output, when the CF4 pin goes from high to low.	0x0	R/W
		8	REVPSUM3		Set this bit to enable the EVENT pin to go low to indicate if the last CF3 pulse was from negative energy. This bit is updated when a CF3 pulse is output, when the CF3 pin goes from high to low.	0x0	R/W
		7	REVPSUM2		Set this bit to enable the EVENT pin to go low to indicate if the last CF2 pulse was from negative energy. This bit is updated when a CF2 pulse is output, when the CF2 pin goes from high to low.	0x0	R/W
		6	REVPSUM1		Set this bit to enable the EVENT pin to go low to indicate if the last CF1 pulse was from negative energy. This bit is updated when a CF1 pulse is output, when the CF1 pin goes from high to low.	0x0	R/W
		[5:0]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x40F	VLEVEL	[31:24]	RESERVED		Reserved.	0x0	R
		[23:0]	VLEVEL_VAL		Register used in the algorithm that computes the fundamental reactive power.	0x45D45	R/W
0x41F	PHNOLOAD	[31:17]	RESERVED		Reserved.	0x0	R
		16	CFVARNL		This bit is set if the Phase C fundamental reactive energy is in no load.	0x0	R
		15	RESERVED		Reserved.	0x0	R
		14	CVANL		This bit is set if the Phase C total apparent energy is in no load.	0x0	R
		13	CVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		12	CWATTNL		This bit is set if the Phase C total active energy is in no load.	0x0	R
		11	RESERVED		Reserved.	0x0	R
		10	BFVARNL		This bit is set if the Phase B fundamental reactive energy is in no load.	0x0	R
		9	RESERVED		Reserved.	0x0	R
		8	BVANL		This bit is set if the Phase B total apparent energy is in no load.	0x0	R
		7	BVARNL		This bit is set if the Phase B total reactive energy is in no load.	0x0	R
		6	BWATTNL		This bit is set if the Phase B total active energy is in no load.	0x0	R
		5	RESERVED		Reserved.	0x0	R
		4	AFVARNL		This bit is set if the Phase A fundamental reactive energy is in no load.	0x0	R
		3	RESERVED		Reserved.	0x0	R
		2	AVANL		This bit is set if the Phase A total apparent energy is in no load.	0x0	R
		1	AVARNL		This bit is set if the Phase A total reactive energy is in no load.	0x0	R
		0	AWATTNL		This bit is set if the Phase A total active energy is in no load.	0x0	R
0x424	ADC_REDIRECT	[31:21]	RESERVED		Reserved.	0x0	R
		[20:18]	VC_DIN		Voltage C channel data can be selected from:	0x7	R/W
				000	IA ADC data.		
				001	IB ADC data.		
				010	IC ADC data.		
				011	IN ADC data.		
				100	VA ADC data.		
				101	VB ADC data.		
				110	VC ADC data.		
				111	VC ADC data.		
		[17:15]	VB_DIN		VB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	VB ADC Data.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[14:12]	VA_DIN		VA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	VA ADC data.		
		[11:9]	IN_DIN		IN channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	IN ADC data.		
		[8:6]	IC_DIN		IC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	IC ADC data.		
		[5:3]	IB_DIN		IB channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	IB ADC data.		
		[2:0]	IA_DIN		IA channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b then:	0x7	R/W
				111	IA ADC data.		
0x425	CF_LCFG	[31:23]	RESERVED		Reserved.	0x0	R
		22	CF4_LT		If this bit is set, the CF4 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		21	CF3_LT		If this bit is set, the CF3 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		20	CF2_LT		If this bit is set, the CF2 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		19	CF1_LT		If this bit is set, the CF1 pulse width is determined by the CF_LTMR register value. If this bit = 0, the active low pulse width is set at 80 ms for frequencies lower than 6.25 Hz.	0x0	R/W
		[18:0]	CF_LTMR		If the CFx_LT bit in CF_LCFG register is set, this value determines the active low pulse width of the CFx pulse.	0x0	R/W
0x472	PART_ID	[31:22]	RESERVED		Reserved.	0x0	R
		21	AD73370_ID		This bit is set to identify an AD73370 IC.	0x0	R
		20	ADE9000_ID		This bit is set to identify an ADE9000 IC.	0x0	R
		[19:17]	RESERVED		Reserved.	0x0	R
		16	ADE9004_ID		This bit is set to identify an ADE9004 IC.	0x0	R
		[15:0]	RESERVED		Reserved.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x481	CONFIG1	15	EXT_REF		Set this bit if using an external voltage reference.	0x0	R/W
		[14:13]	RESERVED		Reserved.	0x0	R
		12	IRQ0_ON_IRQ1		Set this bit to combine all the interrupts onto a single interrupt pin, IRQ1, instead of using two pins, IRQ0 and IRQ1. Note that the IRQ0 pin still indicates the enabled IRQ0 events while in this mode and the IRQ1 indicates both IRQ1 and IRQ0 events.	0x0	R/W
		11	BURST_EN		Set this bit to enable burst read functionality on the registers from Address 0x500 to Address 0x6FF. Note that this bit disables the CRC being appended to SPI register reads.	0x0	R/W
		10	RESERVED		Reserved.	0x0	R
		[9:8]	PWR_SETTLE		These bits configure the time for the power and filter based rms measurements to settle before starting the power, energy and CF accumulations. 0: 64 ms. 1: 128 ms. 2: 256 ms. 3: 0 ms.	0x0	R/W
		[7:6]	RESERVED		Reserved.	0x0	R
		5	CF_ACC_CLR		Set this bit to clear the accumulation in the digital to frequency converter and CFDEN counter. Note that this bit automatically clears itself.	0x0	W
		4	RESERVED		Reserved.	0x0	R
		[3:2]	CF4_CFG		These bits select which function to output on the CF4 pin.	0x0	R/W
				00	CF4, from digital to frequency converter.		
				01	CF4, from digital to frequency converter.		
				10	EVENT.		
				11	DREADY.		
		1	CF3_CFG		This bit selects which function to output on the CF3 pin.	0x0	R/W
				0	CF3, from digital to frequency converter.		
				1	Zero Crossing output selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	SWRST		Set this bit to initiate a software reset. Note that this bit is self clearing.	0x0	W1
0x490	CFMODE	15	CF4DIS		CF4 output disable. Set this bit to disable the CF4 output and bring the pin high. Note that when this bit is set, the CFx bit in STATUS0 is not set when a CF pulse is accumulated in the digital to frequency converter.	0x0	R/W
		14	CF3DIS		CF3 output disable--see CF4DIS.	0x0	R/W
		13	CF2DIS		CF2 output disable--see CF4DIS.	0x0	R/W
		12	CF1DIS		CF1 output disable--see CF4DIS	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[11:9]	CF4SEL		Type of energy output on the CF4 pin. Configure TERMSEL4 in the COMPMODE register to select which phases are included.	0x0	R/W
				000	Total active power.		
				001	Total reactive power.		
				010	Total apparent power.		
				100	Fundamental reactive power.		
				110	Total active power.		
				111	Total active power.		
		[8:6]	CF3SEL		Selects type of energy output on CF3 pin--see CF4SEL.	0x0	R/W
		[5:3]	CF2SEL		Selects type of energy output on CF2 pin--see CF4SEL.	0x0	R/W
		[2:0]	CF1SEL		Selects type of energy output on CF1 pin--see CF4SEL.	0x0	R/W
0x491	COMPMODE	[15:12]	RESERVED		Reserved.	0x0	R
		[11:9]	TERMSEL4		Phases to include in CF4 pulse output. Set the TERMSEL4[2] bit to one to include Phase C in the CF4 pulse output. Similarly, set TERMSEL4[1] to include Phase B and TERMSEL4[0] for Phase A.	0x0	R/W
		[8:6]	TERMSEL3		Phases to include in CF3 pulse output--see TERMSEL4.	0x0	R/W
		[5:3]	TERMSEL2		Phases to include in CF2 pulse output--see TERMSEL4.	0x0	R/W
		[2:0]	TERMSEL1		Phases to include in CF1 pulse output--see TERMSEL4.	0x0	R/W
0x492	ACCMODE	[15:9]	RESERVED		Reserved.	0x0	R
		8	SELFREQ		This bit is used to configure the IC for a 50 Hz or 60 Hz system. This setting is used in the fundamental reactive power measurement and to set the default line period used for resampling calculations if a zero crossing is not present.	0x0	R/W
				0	50 Hz.		
				1	60 Hz.		
		7	ICONSEL		Set this bit to calculate the current flowing through IB from the IA and IC measurements. If this bit is set, IB = –IA – IC.	0x0	R/W
		[6:4]	VCONSEL		Three-wire and four-wire hardware configuration selection.	0x0	R/W
				000	4-wire wye.		
				001	3-wire delta. VB' = VA – VC.		
				010	4-wire wye, non-Blondel compliant. VB' = –VA – VC.		
				011	4-wire delta, non- Blondel compliant. VB' = –VA.		
				100	3-wire delta. VA' = VA – VB; VB' = VA – VC; VC' = VC – VB.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[3:2]	VARACC		Total and fundamental reactive power accumulation mode for energy registers and CFx pulses.	0x0	R/W
				00	Signed accumulation mode.		
				01	Absolute Value accumulation mode.		
				10	Positive accumulation mode.		
				11	Negative accumulation mode.		
		[1:0]	WATTACC		Total and fundamental active power accumulation mode for energy registers and CFx pulses--see VARACC.	0x0	R/W
0x493	CONFIG3	[15:5]	RESERVED		Reserved.	0x0	R
		[4:2]	PEAKSEL		Set this bit to select which phase(s) to monitor peak voltages and currents on. Write PEAKSEL[0] to one to enable Phase A peak detection. Similarly, PEAKSEL[1] enables Phase B peak detection and PEAKSEL[2] enables Phase C peak detection.	0x0	R/W
		[1:0]	RESERVED		Reserved.	0x0	R
0x49A	ZX_LP_SEL	[15:5]	RESERVED		Reserved.	0x0	R
		[4:3]	LP_SEL		Selects line period measurement used for resampling.	0x3	R/W
				00	APERIOD, line period measurement from Phase A voltage.		
				01	BPERIOD, line period measurement from Phase B voltage.		
				10	CPERIOD, line period measurement from Phase C voltage.		
				11	COM_PERIOD, line period measurement on combined signal from VA, VB, and VC.		
		[2:1]	ZX_SEL		Selects the zero-crossing signal, which can be routed to CF3/ZX output pin and which is used for line cycle energy accumulation.	0x3	R/W
				00	ZXVA, Phase A voltage zero-crossing signal.		
				01	ZXVB, Phase B voltage zero-crossing signal.		
				10	ZXVC, Phase C voltage zero-crossing signal.		
				11	ZXCOMB, zero crossing on combined signal from VA, VB, and VC.		
		0	RESERVED		Reserved.	0x0	R
0x49D	PHSIGN	[15:10]	RESERVED		Reserved.	0x0	R
		9	SUM4SIGN		Sign of the sum of the powers included in the CF4 datapath. The CF4 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		8	SUM3SIGN		Sign of the sum of the powers included in the CF3 datapath. The CF3 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		7	SUM2SIGN		Sign of the sum of the powers included in the CF2 datapath. The CF2 energy is positive if this bit is clear and negative if this bit is set.	0x0	R
		6	SUM1SIGN		Sign of the sum of the powers included in the CF1 datapath. The CF1 energy is positive if this bit is clear and negative if this bit is set.	0x0	R

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		5	CVARSIGN		Phase C reactive power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		4	CWSIGN		Phase C active power sign bit.	0x0	R
		3	BVARSIGN		Phase B reactive power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		2	BWSIGN		Phase B active power sign bit.	0x0	R
		1	AVARSIGN		Phase A reactive power sign bit. The PWR_SIGN_SEL bit in the EP_CFG selects whether this feature monitors total or fundamental reactive power.	0x0	R
		0	AWSIGN		Phase A active power sign bit.	0x0	R
0x4A0	WFB_CFG	[15:13]	RESERVED		Reserved.	0x0	R
		12	WF_IN_EN		This setting determines whether the IN waveform samples are read out of the waveform buffer through SPI.	0x0	R/W
				0	IN waveform samples are not read out of waveform buffer through SPI.		
				1	IN waveform samples are read out of waveform buffer through SPI.		
		[11:10]	RESERVED		Reserved.	0x0	R
		[9:8]	WF_SRC		Waveform buffer source and DREADY, data ready update rate, selection.	0x0	R/W
				00	Sinc4 output, at 16 kSPS.		
				01	Reserved.		
				10	Sinc4 + IIR LPF output, at 4 kSPS.		
				11	Current and voltage channel waveform samples, processed by the DSP (xI_PCF, xV_PCF) at 4 kSPS.		
		[7:6]	WF_MODE		Fixed data rate waveforms filling and trigger based modes.	0x0	R/W
				00	Stop when waveform buffer is full.		
				01	Continuous fill—stop only on enabled trigger events.		
				10	Continuous filling—center capture around enabled trigger events.		
				11	Continuous fill—save event address of enabled trigger events.		
		5	WF_CAP_SEL		This bit selects whether the waveform buffer is filled with resampled data or fixed data rate data, selected in the WF_CAP_SEL bits.	0x0	R/W
				0	Resampled data.		
				1	Fixed data rate data.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		4	WF_CAP_EN		When this bit is set, a waveform capture is started.	0x0	R/W
				0	The waveform capture is disabled. The waveform buffer contents are maintained.		
				1	The waveform capture is started, according to the type of capture in WF_CAP_SEL and the WF_SRC bits when this bit goes from a 0 to a 1.		
		[3:0]	BURST_CHAN		Selects which data to read out of the waveform buffer through SPI.	0x0	R/W
				0000	All channels.		
				0001	IA and VA.		
				0010	IB and VB.		
				0011	IC and VC.		
				1000	IA.		
				1001	VA.		
				1010	IB.		
				1011	VB.		
				1100	IC.		
				1101	VC.		
				1110	IN if WF_IN_EN = 1 in the WFB_CFG register.		
				1111	Single address read (SPI burst read mode is disabled).		
0x4A2	WFB_TRG_CFG	[15:11]	RESERVED		Reserved.	0x0	R
		10	TRIG_FORCE		Set this bit to trigger an event to stop the waveform buffer filling.	0x0	R/W
		9	ZXCOMB		Zero crossing on combined signal from VA, VB, and VC.	0x0	R/W
			ZXVC		Phase C voltage zero crossing.	0x0	R/W
		7	ZXVB		Phase B voltage zero crossing.	0x0	R/W
		6	ZXVA		Phase A voltage zero crossing.	0x0	R/W
		5	ZXIC		Phase C current zero crossing.	0x0	R/W
		4	ZXIB		Phase B current zero crossing.	0x0	R/W
		3	ZXIA		Phase A current zero crossing.	0x0	R/W
		[2:0]	RESERVED		Reserved.	0x0	R
0x4A3	WFB_TRG_STAT	[15:12]	WFB_LAST_PAGE		These bits indicate which page of the Waveform Buffer was filled last, when filling with Fixed Rate Data samples.	0x0	R/W
		11	RESERVED		Reserved.	0x0	R
		[10:0]	WFB_TRIG_ADDR		This holds the address of the last sample put into the waveform buffer after a trigger event occurred, which is within a sample or two of when the actual trigger event occurred.	0x0	R
0x4AF	CONFIG2	[15:13]	RESERVED		Reserved.	0x0	R
		12	UPERIOD_SEL		Set this bit to use a user configured line period, in USER_PERIOD, for the resampling calculation. If this bit is clear, the phase voltage line period selected by the LP_SEL[1:0] bits in the ZX_LP_SEL register is used.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[11:9]	HPF_CRN		High-pass filter corner (f3dB) enabled when the HPFDIS bit in the CONFIG0 register = 0.	0x6	R/W
				000	38.695 Hz.		
				001	19.6375 Hz.		
				010	9.895 Hz.		
				011	4.9675 Hz.		
				100	2.49 Hz.		
				101	1.2475 Hz.		
				110	0.625 Hz.		
				111	0.3125 Hz.		
		[8:0]	RESERVED		Reserved.	0x0	R
0x4B0	EP_CFG	[15:13]	NOLOAD_TMR		This register configures how many 4 kSPS samples to evaluate the no load condition over.	0x0	R/W
				000	64.		
				001	128.		
				010	256.		
				011	512.		
				100	1024.		
				101	2048.		
				110	4096.		
				111	Disable no load threshold.		
		[12:8]	RESERVED		Reserved.	0x0	R
		7	PWR_SIGN_SEL		Selects whether the REVRPx bit follows the sign of the total or fundamental reactive power.	0x0	R/W
				0	Total reactive power.		
				1	Fundamental reactive power.		
		6	RESERVED		Reserved.	0x0	R
		5	RD_RST_EN		Set this bit to enable the energy register read with reset feature. If this bit is set, when one of the xWATTHR, xVAHR, xVARHR and xFVARHR register is read, it is reset and begins accumulating energy from zero.	0x0	R/W
		4	EGY_LD_ACCUM		If this bit = 0, the internal energy register is added to the user accessible energy register. If the bit is set, the internal energy register overwrites the user accessible energy register when the EGYRDY event occurs.	0x0	R/W
		[3:2]	RESERVED		Reserved.	0x0	R
		1	EGY_TMR_MODE		This bit determines whether energy is accumulated based on the number of 4 kSPS samples or zero crossing events configured in the EGY_TIME register.	0x0	R/W
				0	Accumulate energy based on 4 kSPS samples.		
				1	Accumulate energy based on the zero crossing selected by the ZX_SEL bits in the ZX_LP_SEL register.		
		0	EGY_PWR_EN		Set this bit to enable the energy and power accumulator, when the run bit is also set.	0x0	R/W

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x4B4	CRC_FORCE	[15:1]	RESERVED		Reserved.	0x0	R
		0	FORCE_CRC_UPDATE		Write this bit to force the configuration register CRC calculation to start. When the calculation is complete, the CRC_DONE bit is set in the STATUS1 register.	0x0	R/W
0x4B5	CRC_OPTEN	15	CRC_WFB_TRG_CFG_EN		Set this bit to include the WFB_TRG_CFG register in the configuration register CRC calculation.	0x0	R/W
		14	CRC_WFB_PG_IRQEN		Set this bit to include the WFB_PG_IRQEN register in the configuration register CRC calculation.	0x0	R/W
		13	CRC_WFB_CFG_EN		Set this bit to include the WFB_CFG register in the configuration register CRC calculation.	0x0	R/W
		12	CRC_SEQ_CYC_EN		Set this bit to include the SEQ_CYC register in the configuration register CRC calculation.	0x0	R/W
		11	CRC_ZXLPSEL_EN		Set this bit to include the ZX_LP_SEL register in the configuration register CRC calculation.	0x0	R/W
		10	CRC_ZXTOUT_EN		Set this bit to include the CRC_ZXTOUT_EN register in the configuration register CRC calculation.	0x0	R/W
		9	CRC_APP_NL_LVL_EN		Set this bit to include the APP_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		8	CRC_REACT_NL_LVL_EN		Set this bit to include the REACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		7	CRC_ACT_NL_LVL_EN		Set this bit to include the ACT_NL_LVL register in the configuration register CRC calculation.	0x0	R/W
		[6:3]	RESERVED		Reserved.	0x0	R
		2	CRC_EVENT_MASK_EN		Set this bit to include the EVENT_MASK register in the configuration register CRC calculation.	0x0	R/W
		1	CRC_MASK1_EN		Set this bit to include the MASK1 register in the configuration register CRC calculation.	0x0	R/W
		0	CRC_MASK0_EN		Set this bit to include the MASK0 register in the configuration register CRC calculation.	0x0	R/W
0x4B8	PSM2_CFG	[15:9]	RESERVED		Reserved.	0x0	R
		[8:5]	PKDET_LVL		These bits configure the PSM2 low power comparator peak current detection Level, listed as the input signal level with respect to full scale. The register value is retained in PSM2 and PSM3. It returns to its default value if PSM0 is entered.	0x0	R/W
				0000	100:1.		
				0001	200:1.		
				0010	300:1.		
				0011	400:1.		
				0100	500:1.		
				0101	600:1.		
				0110	700:1.		
				0111	800:1.		
				1000	900:1.		
				1001	1000:1.		
				1010	1100:1.		
				1011	1200:1.		

Addr.	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1100	1300:1.		
				1101	1400:1.		
				1110	1500:1.		
				1111	1600:1.		
		[4:0]	LPLINE		This register determines the time used to detect peak currents in the low power comparator in PSM2 operating mode. Note that this register retains its value in PSM2 and PSM3 operating modes but is reset to its default value upon entering PSM0 or PSM1.	0x1F	R/W
0x4B9	PGA_GAIN	[15:14]	RESERVED		Reserved.	0x0	R
		[13:12]	VC_GAIN		PGA gain for Voltage Channel C ADC.	0x0	R/W
				00	Gain = 1.		
				01	Gain = 2.		
				10	Gain = 4.		
				11	Gain = 4.		
		[11:10]	VB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[9:8]	VA_GAIN		PGA gain for Voltage Channel A ADC. See VC_GAIN.	0x0	R/W
		[7:6]	IN_GAIN		PGA gain for neutral current channel ADC. See VC_GAIN.	0x0	R/W
		[5:4]	IC_GAIN		PGA gain for Current Channel C ADC. See VC_GAIN.	0x0	R/W
		[3:2]	IB_GAIN		PGA gain for Voltage Channel B ADC. See VC_GAIN.	0x0	R/W
		[1:0]	IA_GAIN		PGA gain for Current Channel A ADC. See VC_GAIN.	0x0	R/W
0x4BA	CHNL_DIS	[15:7]	RESERVED		Reserved.	0x0	R
		6	VC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		5	VB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		4	VA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		3	IN_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		2	IC_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		1	IB_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
		0	IA_DISADC		Set this bit to one to disable the ADC.	0x0	R/W
0x4E0	VAR_DIS	[15:1]	RESERVED		Reserved.	0x0	R
		0	VARDIS		Set this bit to disable the total VAR calculation. This bit must be set before writing the run bit for proper operation.	0x0	R/W

OUTLINE DIMENSIONS

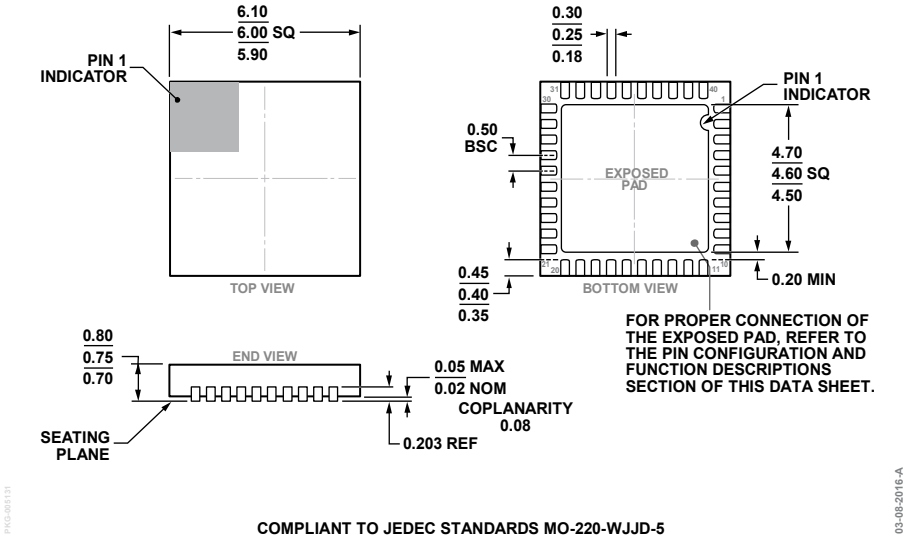


Figure 114. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.75 mm Package Height
(CP-40-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE9078ACPZ	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-7
ADE9078ACPZ-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP], 13″ Tape and Reel	CP-40-7
EVAL-ADE9078EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D14331-0-8/16(0)

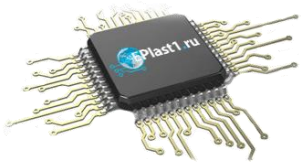
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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