MSP430FE4272 Device Erratasheet

1 Revision History

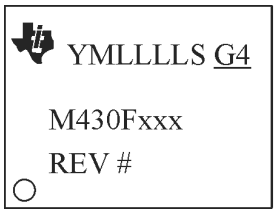
✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev C
CPU4	✓
EEM20	✓
ESP1	✓
ESP4	✓
FLL3	✓
TA12	✓
TA16	✓
TA21	✓
TAB22	✓
US15	✓
WDG2	✓

2 Package Markings

PM64

LQFP (PM), 64 Pin



YM = Year and Month Date Code
LLLL = Assembly Lot Code
S = Assembly Site Code
# = DIE Revision
○ = Pin 1

3 Detailed Bug Description

CPU4 *CPU Module*

Function PUSH #4, PUSH #8

Description The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround Workaround implemented in assembler.

EEM20 *EEM Module*

Function Debugger might clear interrupt flags

Description During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

Workaround None.

ESP1 *ESP Module*

Function Suspending the ESP430CE1

Description Suspending the ESP430 may create an invalid interrupt which can lead to a reset-like behavior of the module.

Workaround Set the bit 0x08 together with the ESPSUSP bit:

bis.w #08h+ESPSUSP, &ESPCTL

This bit also must be cleared when the suspend mode is exited.

bic.w #08h+ESPSUSP, &ESPCTL

NOTE:

- After suspending the ESP430CE1 it can take up to 9 MCLK clock cycles before the CPU can access the SD16 registers.

- An interrupt service routine for the SD16 is required.

```
// Shut down ESP (set Embedded Signal Processing into
// "Suspend" mode)
// ensure that it is not in measurement or calibration mode,
ESPCTL |= 0x08 + ESPSUSP;
// Set ESP into Suspend Mode
// incl. Bug Fix for Suspend Mode
// wait 9 clocks until proper access to the SD16 is possible
__delay_cycles(9);
MBCTL &= ~(IN0IFG + IN0IE);
```

// Clear any Pending MB interrupt and disable

// ESP interrupt

SD16CTL &= ~SD16REFON; // Switch Reference off

ESP4 *ESP Module*

Function Suspending the ESP430 activity

Description Due to timing violations between the ESP CPU and the MSP430 CPU, the SD16 converters are not switched off correctly if the ESP CPU is set into suspend mode immediately after the ESP CPU is checked for idle mode. This leads to an higher current consumption in low-power modes.

Workaround Implement an additional wait loop of 16 clock cycles between checking the ESP for idle mode and set the ESP CPU into suspend mode.

```
while ((RET0 & 0x8000) != 0); // Wait for Idle mode
// wait 16 clocks to exclude timing violations between MSP430 CPU
// and ESP CPU
_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();--
_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();_NOP();
// Shut down ESP (set Embedded Signal Processing into "Suspend" mode)
// ensure that it is not in measurement or calibration mode,
if ((RET0 & 0x8000) == 0)
{
ESPCTL |= 0x08 + ESPSUSP; // Set ESP into Suspend Mode
// incl. Bug Fix for Suspend Mode
}
```

FLL3 *FLL+ Module*

Function FLLDx = 11 for /8 may generate an unstable MCLK frequency

Description When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g. averaged over 2sec) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround None

TA12 *TIMER_A Module*

Function Interrupt is lost (slow ACLK)

Description Timer_A counter is running with slow clock (external TACLK or ACLK)compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt

should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 *TIMER_A Module*

Function First increment of TAR erroneous when IDx > 00

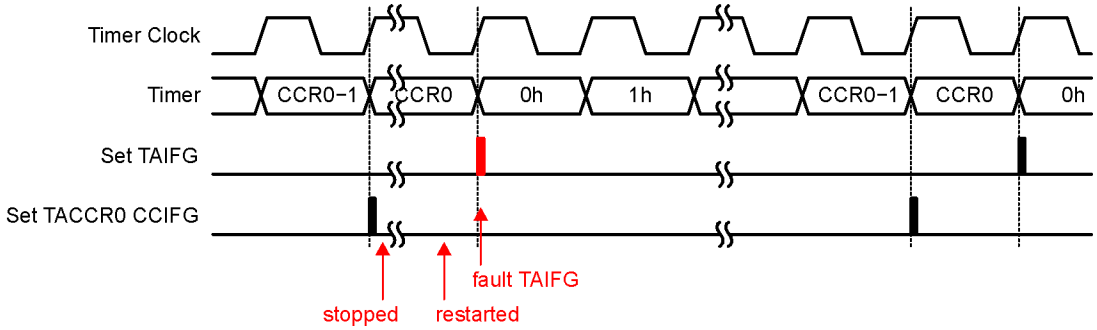
Description The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround None

TA21 *TIMER_A Module*

Function TAIFG Flag is erroneously set after Timer A restarts in Up Mode

Description In Up Mode, the TAIFG flag should only be set when the timer counts from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



Workaround None.

TAB22 *TIMER_A/TIMER_B Module*

Function Timer_A/Timer_B register modification after Watchdog Timer PUC

Description Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running).

Workaround Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

MOV.W #VAL, &TBCTL

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

US15 *USART Module*

Function UART receive with two stop bits

Description USART hardware does not detect a missing second stop bit when SPB = 1.

The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround None (Configure USART for a single stop bit, SPB = 0)

WDG2 *WDT Module*

Function Incorrectly accessing a flash control register

Description If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to the expected PUC.

Workaround None

4 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Errata XOSC5 was removed
2. Errata TA22 was renamed to TAB22
3. Description for TAB22 was updated

Changes from device specific erratasheet to document Revision A.

1. Errata EEM20 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Package Markings section was updated.

Changes from document Revision C to Revision D.

1. TA21 Description was updated.

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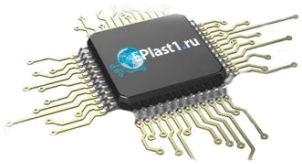

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