

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4022B

MSI

4-stage divide-by-8 Johnson counter

Product specification
File under Integrated Circuits, IC04

January 1995

4-stage divide-by-8 Johnson counter

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DESCRIPTION

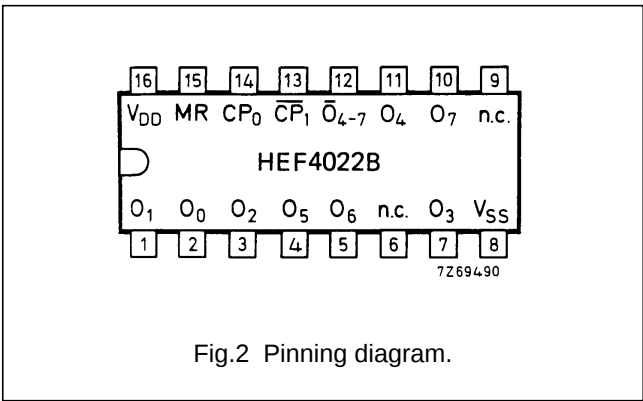
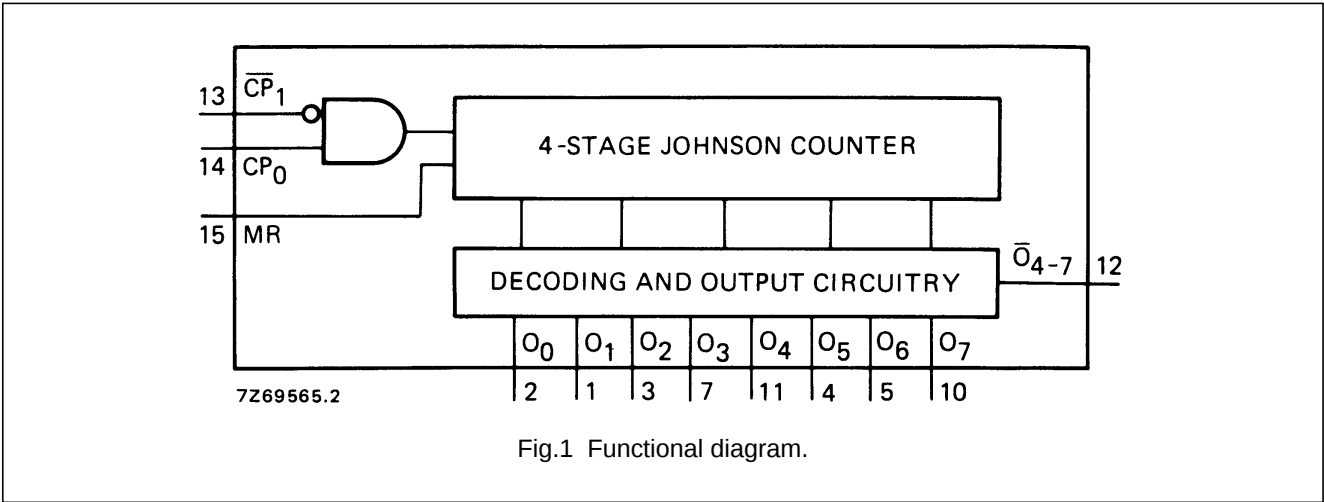
The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop ($\overline{O}_{4-7}$), active HIGH and active LOW clock inputs (CP_0 , $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table). Either CP_0 or CP_1 may be used as clock input to the

counter and the other clock input may be used as a clock enable input. When cascading counters, the $\overline{O}_{4-7}$ output, which is LOW while the counter is in states, 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{4-7} = \text{HIGH}$; O_1 to $O_7 = \text{LOW}$) independent of the clock inputs (CP_0 , $\overline{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit, following any illegal code the counter returns to a proper counting mode within 11 clock pulses.



- HEF4022BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4022BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4022BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI
See Family Specifications

PINNING

- CP_0 clock input (LOW to HIGH; edge-triggered)
- $\overline{CP}_1$ clock input (HIGH to LOW; edge-triggered)
- MR master reset input
- O_0 to O_7 decoded outputs
- O_{4-7} carry output (active LOW)

4-stage divide-by-8 Johnson counter

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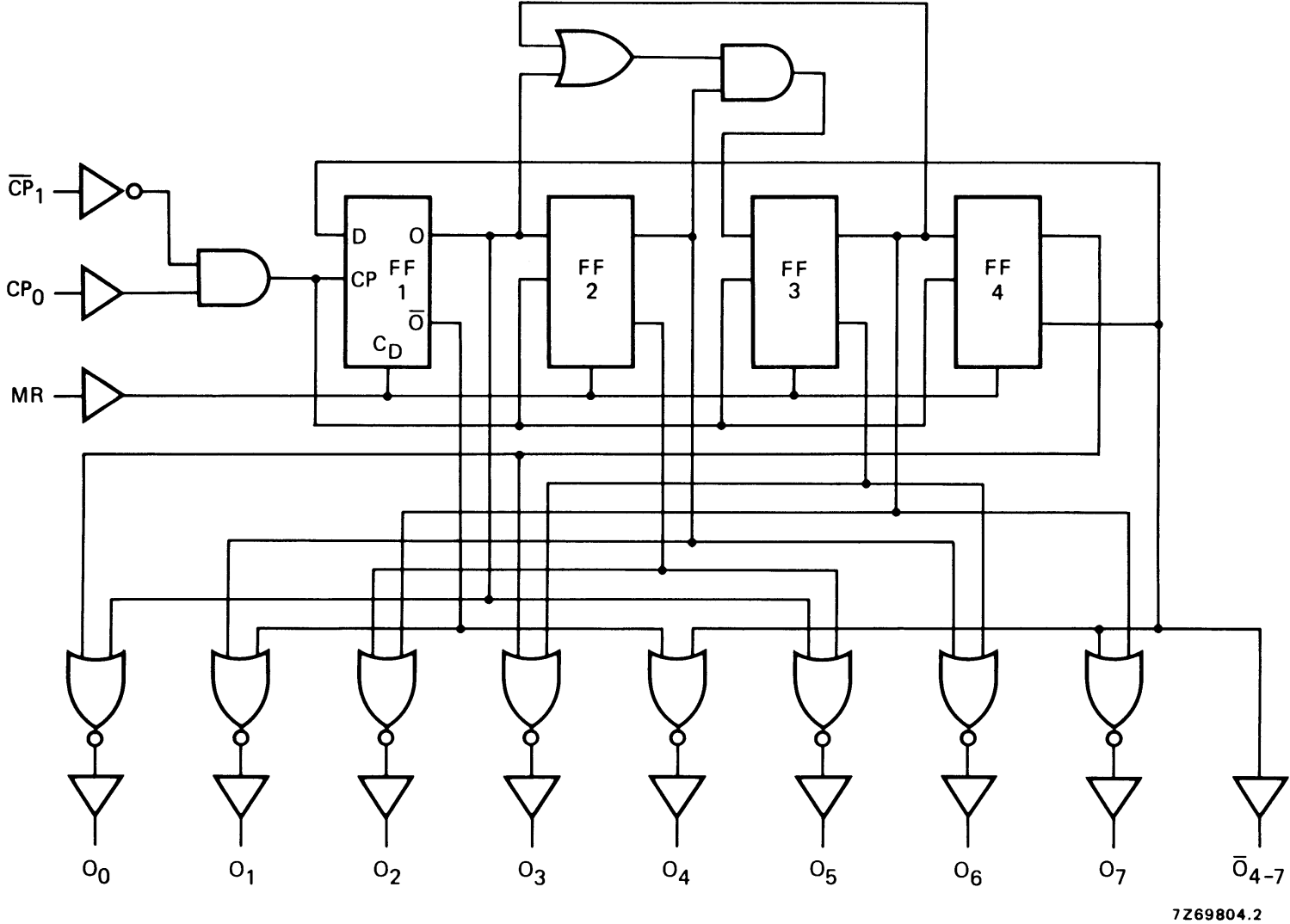


Fig.3 Logic diagram.

4-stage divide-by-8 Johnson counter

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FUNCTION TABLE

MR	CP ₀	CP ₁	OPERATION
H	X	X	O ₀ = $\overline{O_{4-7}}$ = H; O ₁ to O ₇ = L
L	H	$\searrow$	Counter advances
L	$\nearrow$	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	$\nearrow$	No change
L	$\searrow$	L	No change

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 $\nearrow$ = positive-going transition
 $\searrow$ = negative-going transition

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP ₀ , $\overline{CP_1} \rightarrow O_n$	5	t _{PHL}		195	390 ns	168 ns + (0,55 ns/pF) C _L
HIGH to LOW	10			75	145 ns	64 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		245	485 ns	218 ns + (0,55 ns/pF) C _L
	10			95	195 ns	84 ns + (0,23 ns/pF) C _L
	15			60	125 ns	52 ns + (0,16 ns/pF) C _L
CP ₀ , $\overline{CP_1} \rightarrow \overline{O_{4-7}}$	5	t _{PHL}		245	485 ns	218 ns + (0,55 ns/pF) C _L
HIGH to LOW	10			90	185 ns	79 ns + (0,23 ns/pF) C _L
	15			60	120 ns	52 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		190	380 ns	163 ns + (0,55 ns/pF) C _L
	10			75	145 ns	64 ns + (0,23 ns/pF) C _L
	15			50	105 ns	42 ns + (0,16 ns/pF) C _L
MR → O ₁ to O ₇	5	t _{PHL}		130	260 ns	103 ns + (0,55 ns/pF) C _L
HIGH to LOW	10			55	105 ns	44 ns + (0,23 ns/pF) C _L
	15			40	75 ns	32 ns + (0,16 ns/pF) C _L
MR → O ₀	5	t _{PLH}		130	260 ns	103 ns + (0,55 ns/pF) C _L
LOW to HIGH	10			55	105 ns	44 ns + (0,23 ns/pF) C _L
	15			40	75 ns	32 ns + (0,16 ns/pF) C _L
MR → $\overline{O_{4-7}}$	5	t _{PLH}		110	220 ns	83 ns + (0,55 ns/pF) C _L
LOW to HIGH	10			45	90 ns	34 ns + (0,23 ns/pF) C _L
	15			35	70 ns	27 ns + (0,16 ns/pF) C _L
Output transition times	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L
HIGH to LOW	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L

4-stage divide-by-8 Johnson counter

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Hold times $CP_0 \rightarrow \overline{CP_1}$	5	t_{hold}	140	70	ns	see also waveforms Figs 4 and 5
	10		50	25	ns	
	15		30	15	ns	
$\overline{CP_1} \rightarrow CP_0$	5	t_{hold}	170	85	ns	
	10		60	30	ns	
	15		40	20	ns	
Minimum clock pulse width	5	t_{WCP}	75	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	70	35	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	30	10	ns	
	10		15	5	ns	
	15		10	5	ns	
Maximum clock pulse frequency	5	f_{max}	3	6	MHz	
	10		8	16	MHz	
	15		12	24	MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$475 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = total load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2400 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$6700 f_i + \sum (f_o C_L) \times V_{DD}^2$	

4-stage divide-by-8 Johnson counter

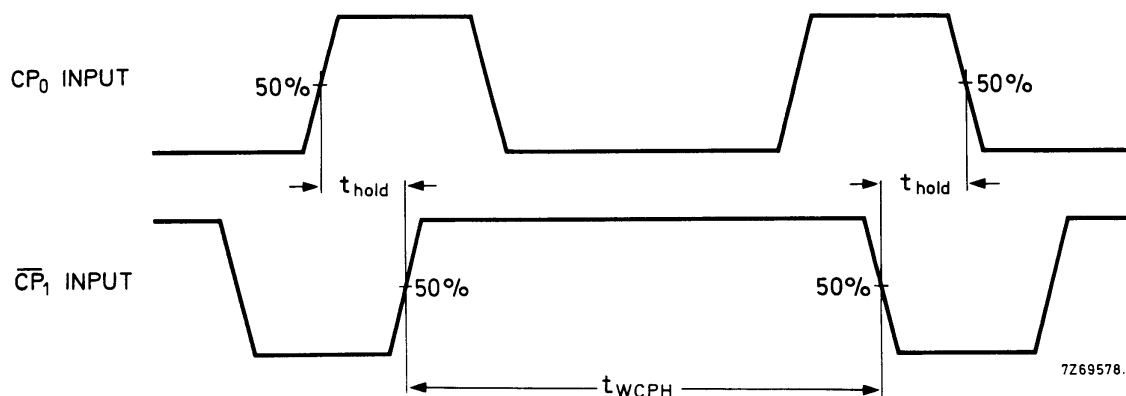
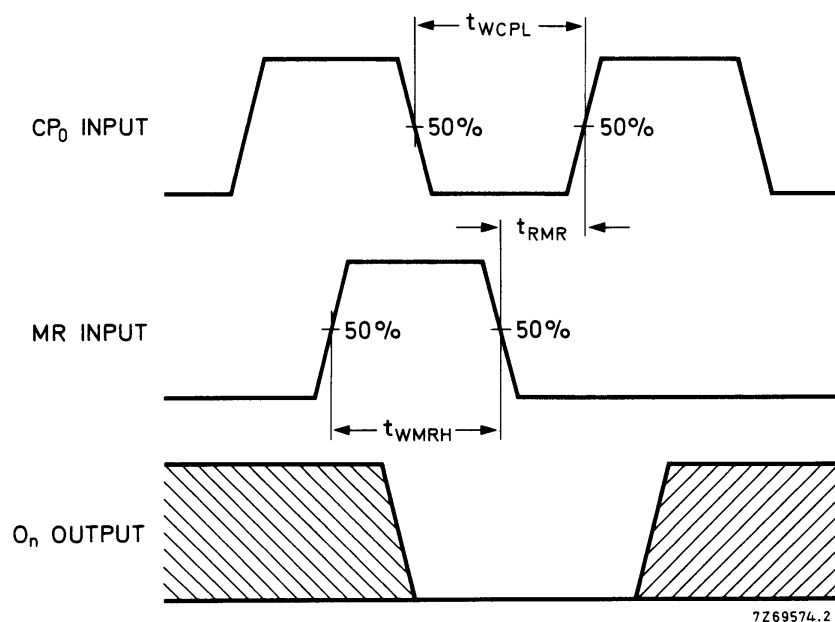
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Fig.4 Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0 . Hold times are shown as positive values, but may be specified as negative values.



Conditions: $\overline{CP}_1 = \text{LOW}$ while CP_0 is triggered on a LOW to HIGH transition.
 t_{WCP} and t_{RMR} also apply when $CP_0 = \text{HIGH}$ and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

Fig.5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

4-stage divide-by-8 Johnson counter

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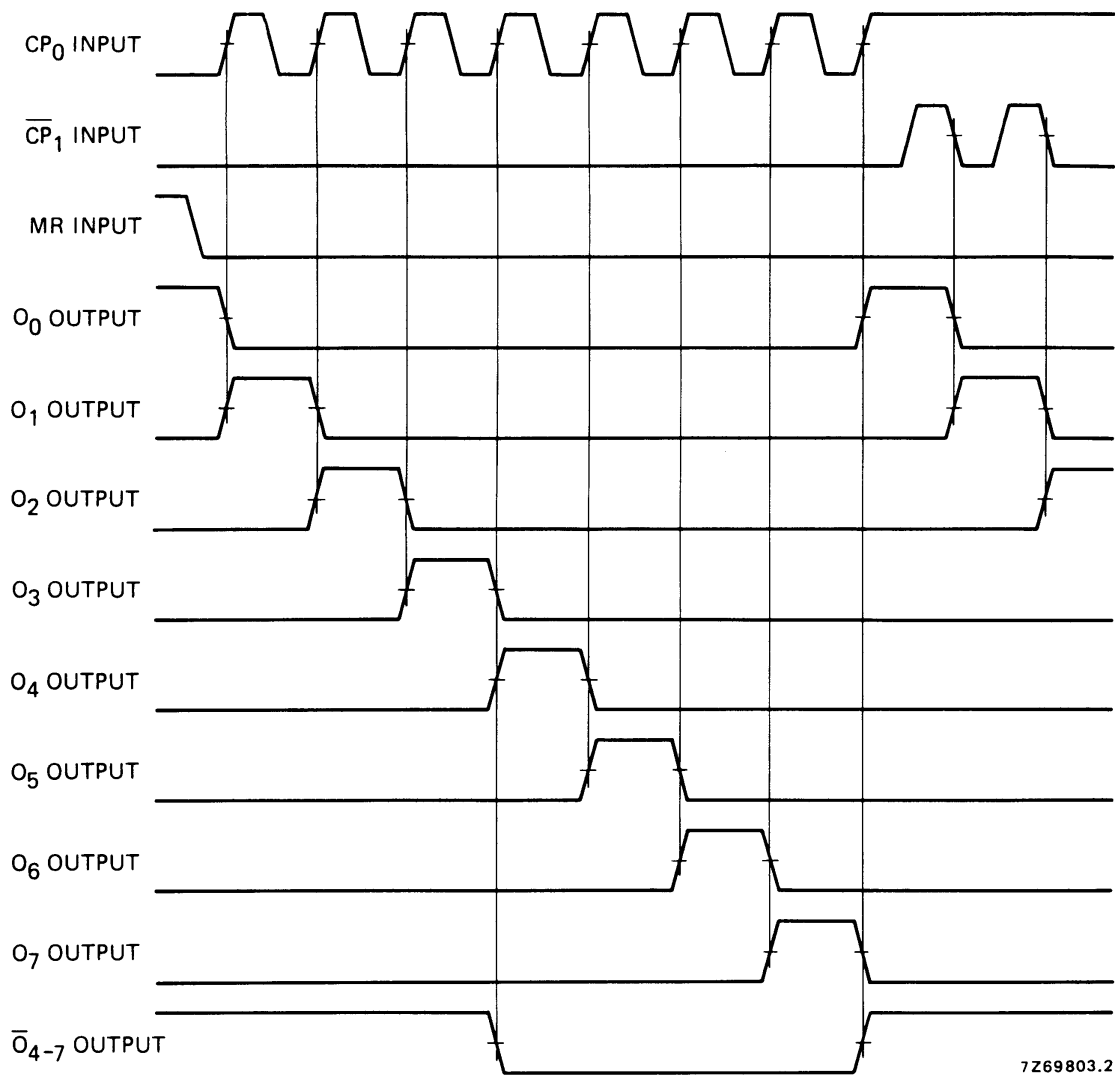


Fig.6 Timing diagram.

4-stage divide-by-8 Johnson counter

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APPLICATION INFORMATION

Some of the features of the HEF4022B are:

- High speed
- Spike-free decoded outputs
- Carry output for cascading

Figure 7 shows a technique for extending the number of decoded output states for the HEF4022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

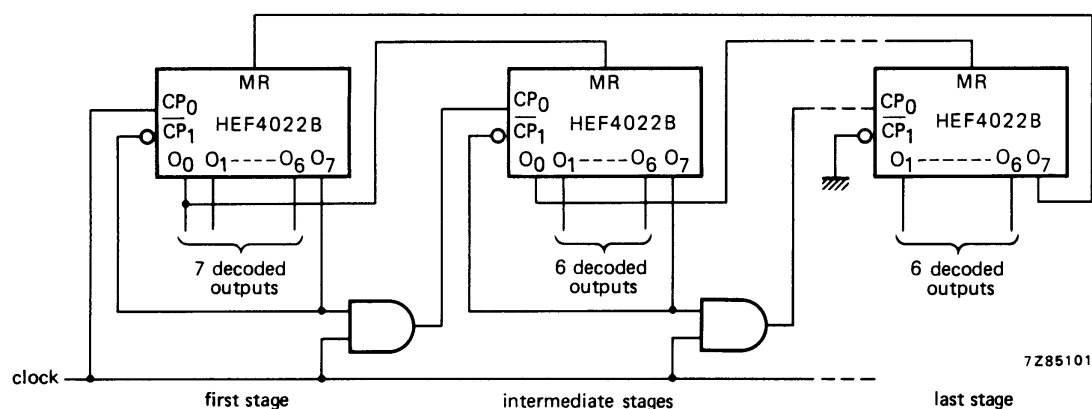


Fig.7 Counter expansion.



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Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.