LYT2001-2005
LYTSwitch™-2 Family

Energy-Efficient, Accurate Primary-Side Regulation CC/CV Switcher for LED Lighting Applications

Product Highlights

Accurate CC Regulation, Meets ±3% in a Typical Design[1]

Controller Automatically Compensates For:
- Transformer inductance variation
- External component changes with temperature
- Input line voltage variations

This enhances production yield

Cost-Effective, Small Size Designs
- Eliminates the optocoupler and secondary CC control circuitry
- Eliminates control loop compensation circuitry
- Frequency-jitter greatly reduces EMI filter cost
- Programmable switching frequency reduces transformer size
- 725 V switching power MOSFET enables clampless flyback designs

Advanced Protection/Safety Features
- Auto-restart protection reduces power delivered by >90% for output short-circuit and control loop faults (open and short-circuit components)
- Hysteretic thermal shutdown – with automatic recovery
- Meets high-voltage creepage requirements between DRAIN and all other pins both on the PCB and at the package

EcoSmart™– Energy Efficient
- No-load consumption <30 mW[1]
- No current sense resistors – maximizes efficiency

Green Package
- All parts are halogen free and RoHS compliant

Applications
- LED bulbs, down lights, luminaires, ballasts and T8 tubes

Description

The LYTSwitch-2 family of ICs dramatically simplifies low power CC LED drivers by eliminating the optocoupler and secondary control circuitry. The family introduces a revolutionary control technique which provides accurate output current regulation, compensating for transformer and external component variations, and device parameter tolerances as well as input voltage variations.

The device incorporates a high-voltage switching MOSFET, an ON/OFF control state-machine, a high-voltage switched current source for self-biasing, frequency jitter to reduce EMI, cycle-by-cycle current limit and hysteretic thermal shutdown circuitry into a monolithic IC. This high level of integration enables cost-effective designs with very few external components, reducing solution cost and driver size.

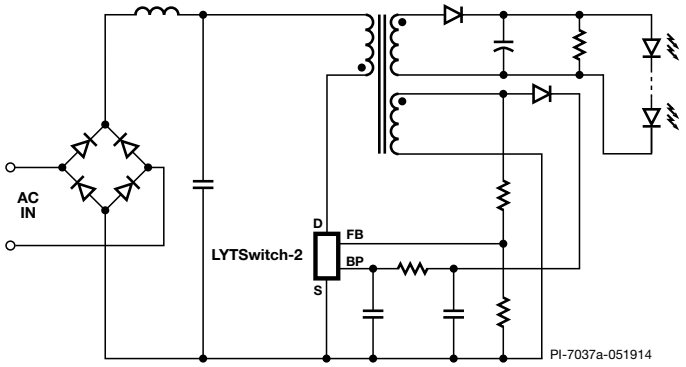


Figure 1. Typical Flyback Implementation – Not a Simplified Circuit.

Output Power Table[2]

Product[5]	90-308 VAC	
	Enclosed Bulb[3]	Ballast Driver[4]
LYT2001D	4 W	5 W
LYT2002D	5 W	6 W
LYT2003D	6 W	7 W
LYT2004D	7 W	8 W
LYT2004E/K	9 W	10 W
LYT2005E/K	10 W	12 W

Table 1. Output Power Table.

Notes:
1. Nominal input and bias supply applied to BYPASS pin.
2. Performance for typical design.
3. Maximum continuous power in a typical non-ventilated bulb measured at +50 °C ambient, device $T_J \leq 100$ °C.
4. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at +50 °C.
5. Packages: D: SO-8C, E: eSIP-7C, K: eSOP-12B.

LYTSwitch-2 parts minimize energy consumption when the output is unloaded. Practical designs can easily achieve less than 30 mW no-load consumption.

The 725 V power MOSFET used in LYTSwitch-2 devices increases the circuits' ability to withstand input surge. In addition, each package is designed to maximize the creepage distance between high-voltage pins and logic level inputs. This increased pin spacing increases driver lifetime and reliability in polluted environments. These in-built protection features also protect the entire circuit from excess temperature operation, increasing lifetime in thermally challenging environments.

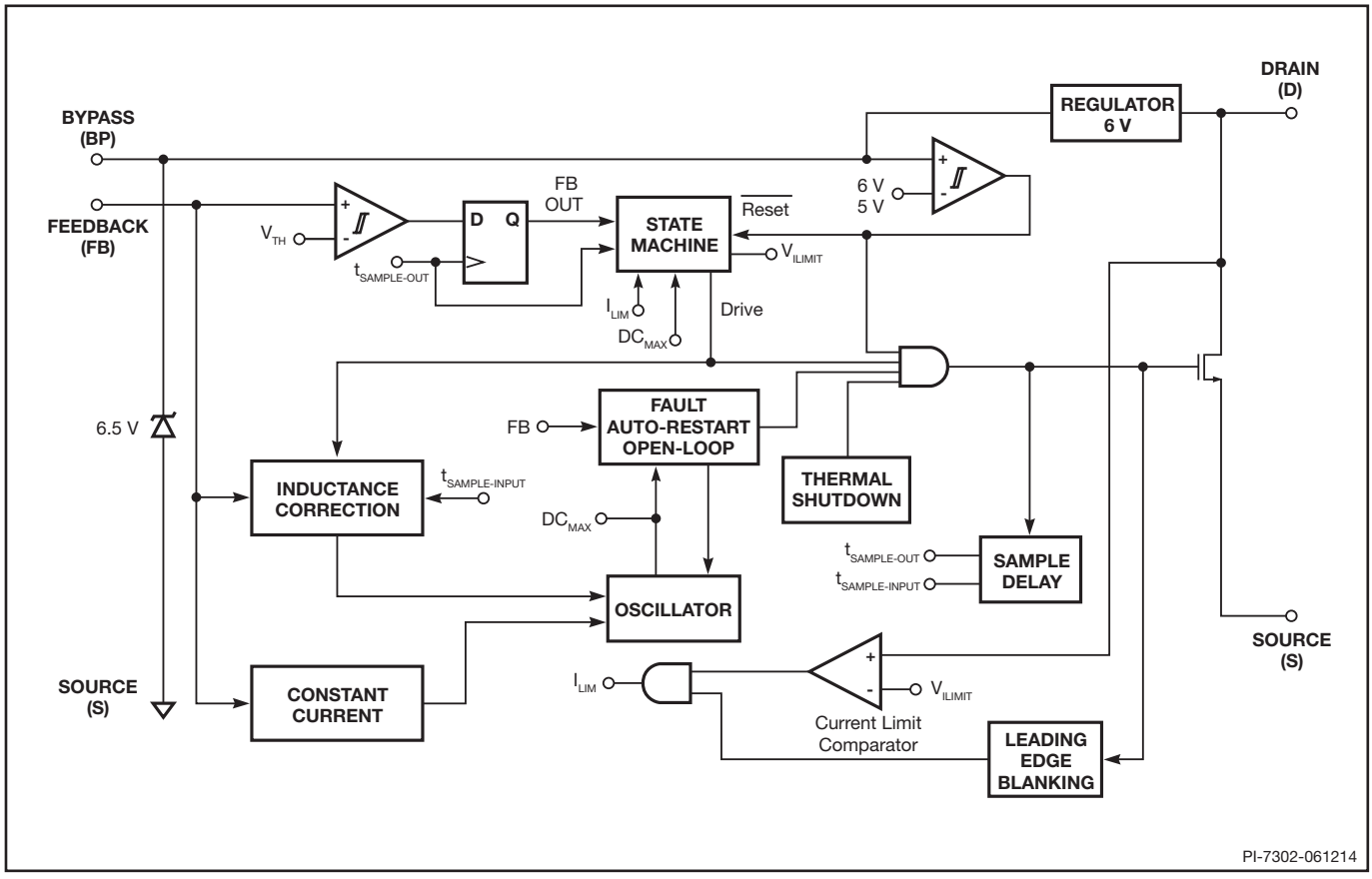


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
Power MOSFET drain connection. It also provides internal operating current during start-up and in steady-state operation.

BYPASS (BP) Pin:
Connection point for the external 1 μF bypass capacitor connected to the internally generated 6 V supply.

FEEDBACK (FB) Pin:
Controls switching of the power MOSFET during normal operation. This pin senses the AC voltage on the bias winding. Input is used to regulate both the output voltage in CV mode and output current in CC mode based on voltage across the bias winding in the flyback portion of the switching cycle. The internal inductance correction circuit uses voltage on the bias winding during forward part of the switching cycle to sense the bulk capacitor voltage.

SOURCE (S) Pin:
Connected to the MOSFET source and is used for high-voltage power and control circuit common returns.

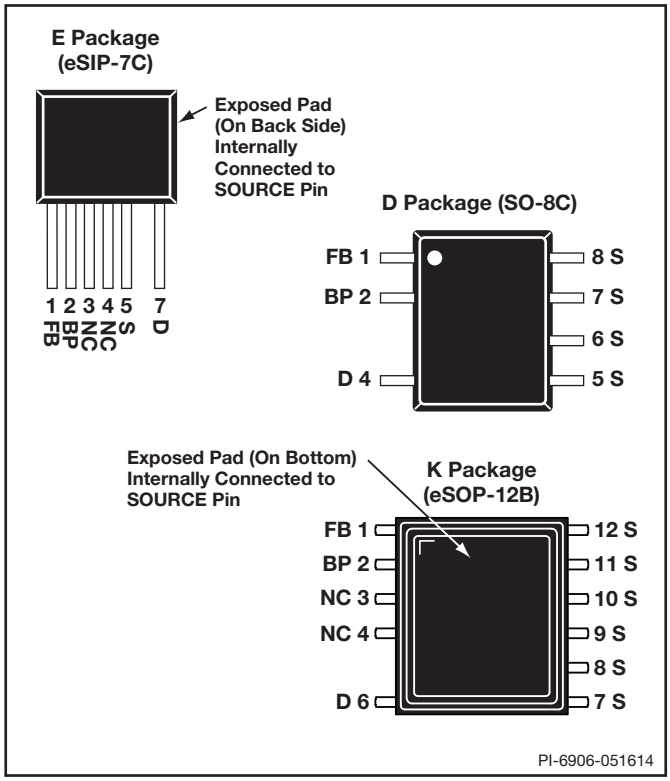


Figure 3. Pin Configuration.

LYTSwitch-2 Functional Description

The LYTSwitch-2 IC combines a high-voltage power MOSFET switch with a power supply controller in one device. Similar to the LinkSwitch-LP and TinySwitch-III ICs it uses an ON/OFF control to regulate the output voltage. In addition, the switching frequency is modulated to regulate the output current to provide a constant current characteristic. The LYTSwitch-2 controller consists of an oscillator, feedback (sense and logic) circuit, 6 V regulator, over-temperature protection, frequency jittering, current limit circuit, leading-edge blanking, inductance correction circuitry, frequency control for constant current regulation and ON/OFF state-machine for CV control.

Inductance Correction Circuitry

If the primary magnetizing inductance is either too high or low the converter will automatically compensate for this by adjusting the oscillator frequency. Since this controller is designed to operate in discontinuous-conduction mode the output power is directly proportional to the set primary inductance and its tolerance can be completely compensated with adjustments to the switching frequency.

Constant Current (CC) Operation

As the output voltage and therefore the flyback voltage across the bias winding ramps up, the FEEDBACK pin voltage increases. The switching frequency is adjusted as the FEEDBACK pin voltage increases to provide a constant output current regulation. The constant current circuit and the inductance correction circuit are designed to operate concurrently in the CC region.

Constant Voltage (CV) Operation

As the FEEDBACK pin approaches 2 V from the constant current regulation mode, the power supply transitions into CV operation. The switching frequency at this point is at its maximum value, corresponding to the peak power point of the CV/CC characteristic. The controller regulates the FEEDBACK pin voltage to remain at FEEDBACK pin threshold (V_{FBTH}) using an ON/OFF state-machine. The FEEDBACK pin voltage is sampled 2.5 μs after the turn-off of the high-voltage switch. At light loads the current limit is also reduced to decrease the transformer flux density and the FEEDBACK pin sampling is done earlier.

Auto-Restart and Open-Loop Protection

In the event of a fault condition such as an output short or an open-loop condition the LYTSwitch-2 IC enters into an appropriate protection mode.

In the event the FEEDBACK pin voltage during the flyback period falls below 0.7 V before the FEEDBACK pin sampling delay (~2.5 μs) for a duration in excess of ~450 ms (auto-restart on-time (t_{AR-ON}) the converter enters into auto-restart, wherein the power MOSFET is disabled for 1.2 seconds. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

In addition to the conditions for auto-restart described above, if the sensed FEEDBACK pin current during the forward period of the conduction cycle (switch “on” time) falls below 120 μA, the converter annunciates this as an open-loop condition (top resistor in potential divider is open or missing) and reduces the auto-restart time from 450 ms to approximately 6 clock cycles (90 μs), whilst keeping the disable period of 2 seconds.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 60 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 60 °C, at which point the MOSFET is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction. The LYTSwitch-2 IC also contains a “di/dt” correction feature to minimize CC variation across the input line range.

6 V Regulator

The 6 V regulator charges the bypass capacitor connected to the BYPASS pin to 6 V by drawing a current from the voltage on the DRAIN pin, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the device runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LYTSwitch-2 IC to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 1 μF is sufficient for both high frequency decoupling and energy storage.

Applications Example

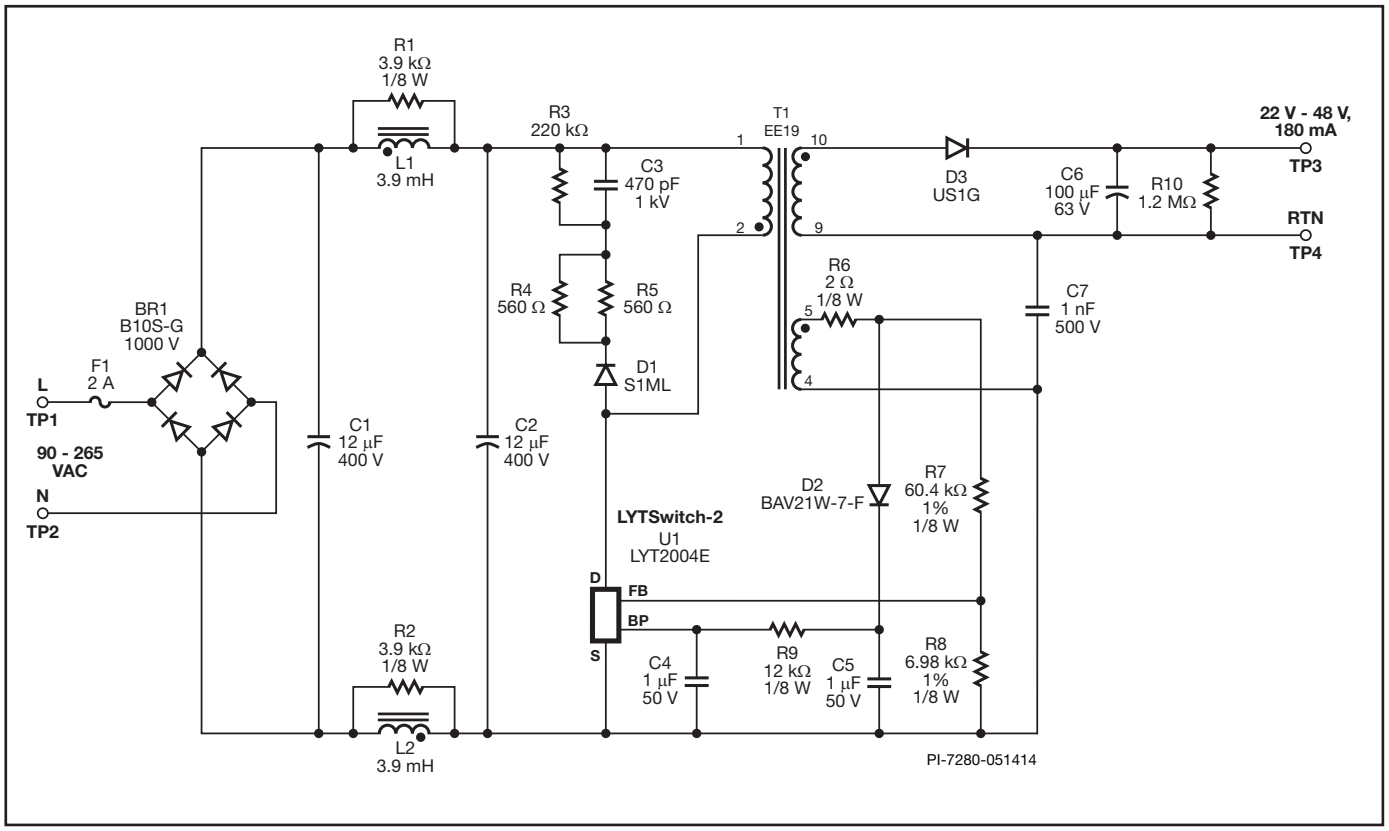


Figure 4. Energy Efficient 8.6 W LED Power Supply (>86 % Average Efficiency, <30 mW No-load Input Power).

Circuit Description

This circuit shown in Figure 4 is configured as a primary-side regulated flyback power supply utilizing the LYT2004E from the LYTSwitch-2 family of ICs. This type of LED driver design is typical for an external ballast application where safety isolation is required while power factor correction is not. The output can drive an LED load from 48 V to 22 V with a constant output current of 180 mA ±5% across input range of 90 VAC to 265 VAC and ambient temperature range of 0 ºC to 60 ºC. It has an average efficiency of >86% and <30 mW no-load input power measured at nominal input voltages (i.e. 115 VAC and 230 VAC). This design easily meets the most stringent current energy efficiency requirements.

Input Filter

AC input power is rectified by bridge diode BR1. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Inductor L1, L2, C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI. Resistors R1 and R2 placed across the inductors damp the Q to improve frequency noise filtering without reducing low frequency noise attenuation. A small value Y capacitor (C7) across the transformer was used to reducer common-mode noise currents. The fuse F1 provides protection against catastrophic failure. This can be replaced by a fusible resistor for cost reduction but should be suitably rated (and typically a wire wound type) to withstand the instantaneous dissipation experienced during input capacitor charging when first connected to the AC line.

LYT2004 Primary

The LYTSwitch-2 family (U1) incorporates the power switching device, oscillator, CC/CV control engine, start-up, and protection functions. The integrated 725 V power MOSFET provides a large drain voltage margin in universal input AC applications, increasing reliability and also reducing the output diode voltage stress by permitting the use of higher transformer turns ratios. The device is completely self-powered from the BYPASS pin and decoupling capacitor C4.

The optional bias supply formed by D2 and C5 and R6 provides operating current to U1 via resistor R9. This reduces the no-load consumption from 200 mW to less than 30 mW. The bias supply also increases light load efficiency.

The rectified and filtered input voltage is applied to one side of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated power MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D1, R3, R4, R5, and C3.

Output Rectification

The output from the transformer is rectified by D3, a 1 A, 400 V ultrafast recovery type diode (for higher efficiency), and filtered by C6. In this application C6 was sized to meet a (typical) ripple requirement of less than 10% without the need for an additional LC post filter.

A pre-load resistor R10 was employed to discharge the output capacitor and extinguish the LED light immediately after turn-off. The resistor will also keep the output from rising higher than the permitted maximum output voltage (usually determined by the output capacitor voltage rating) when the load is disconnected.

Output Regulation

The LYTSwitch-2 family regulates the output using ON/OFF control in the constant voltage (CV) regulation region of the output characteristic and frequency control for the constant current (CC) region. The feedback resistors (R7 and R8) were selected using standard 1% resistors to center both the nominal output voltage and constant current regulation thresholds. Resistor R6 acts as filter to limit the voltage spike (caused by the coupling of the bias winding to the primary winding), improving regulation.

Key Application Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power that can be obtained under the following assumed conditions:

1. The minimum DC bus voltage is 100 V at 90 VAC input. The value of the input capacitance should be made large enough to meet this requirement for AC input designs – typically 2-3 μF/W for low-line or universal input designs and 1-2 μF/W for high-line input designs.
2. The secondary output rectifier diode should withstand peak inverse voltage (PIV) for 55 V output voltage for open load condition.
3. Assume efficiency of >80%.
4. Discontinuous mode operation (K_P >1.3).
5. The LYTSwitch-2 part is either board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C, or (in the case of the E package) attached to a sufficiently sized heat sink to limit device temperature to below 110 °C.
6. Ambient temperature of less than 50 °C for open frame designs and an internal enclosure temperature of 60 °C for enclosed ballast-type designs.

Note: Higher output powers are achievable if an output CC tolerance > ±10% is acceptable, and allowing the device to be operated at a higher SOURCE pin temperature.

Output Tolerance

LYTSwitch-2 K and E package parts provides an overall CC mode output current tolerance of ±5% including line voltage, normal board-to-board component variation and across a temperature range of 0 °C to 110 °C. For the D package (SO-8) additional CC variance may occur due to stress caused by manufacturing (i.e. solder-wave immersion or I_R reflow). A sample power supply build is recommended to verify production tolerances for each design.

BYPASS Pin Capacitor Selection

A 1 μF BYPASS pin capacitor is recommended. The capacitor voltage rating should be greater than 7 V. The capacitor can be ceramic or electrolytic but tolerance of capacitor should be ≤ ±50%. The capacitor must be physically located close to the LYTSwitch-2 BYPASS pin for effective noise decoupling.

LYTSwitch-2 Layout Considerations

Circuit Board Layout

The LYTSwitch-2 family of ICs present a highly integrated power supply solution that integrates, both, the controller and the high-voltage power MOSFET onto a single die. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply. See Figures 5 and 6 for a recommended circuit board layout for LYTSwitch-2.

When designing a printed circuit board layout for the LYTSwitch-2 based power supply, it is important to follow these guidelines:

Single Point Grounding

Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LYTSwitch-2 SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.

Bypass Capacitor

The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins for effective noise decoupling.

Feedback Resistors

Place the feedback resistors (R7 and R8) very close to the FEEDBACK pin of the LYTSwitch-2 device. This minimizes noise coupling.

Thermal Considerations (D and K Package)

The copper area connected to the SOURCE pins provides heat sinking. A good estimate of expected power dissipation is to assume is that the LYTSwitch-2 will dissipate 5% of the output power. Provide enough copper area to keep the SOURCE pin temperature below 100 °C. Higher temperatures are allowable but output current (CC) tolerance will increase. In this case a maximum SOURCE pin temperature below 100 °C is recommended to provide margin for part-to-part $R_{DS(ON)}$ variation.

Secondary Loop Area

To minimize leakage inductance and EMI the area of the loop contained within the connections between the secondary winding (T1), the output diode (D3) and the output filter capacitor (C6) should be minimized. In addition, sufficient copper area should be to the rectifier diode for heat sinking preferably connected to the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

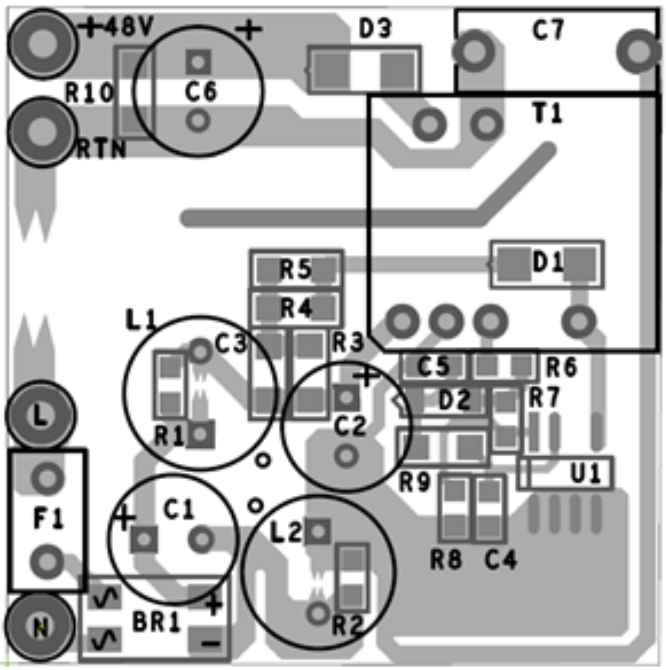


Figure 5. PCB Layout Example using SO-8C Package.

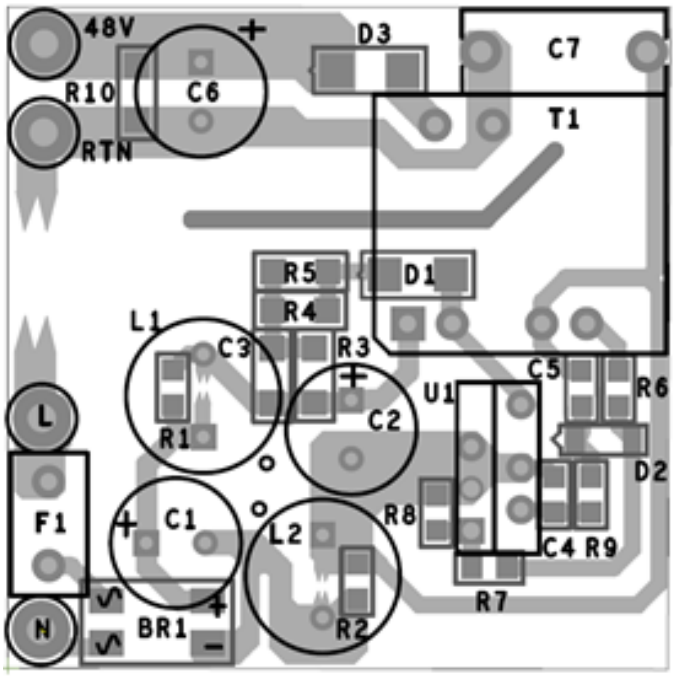


Figure 6. PCB Layout Example using eSIP Package.

Electrostatic Discharge Spark Gap

A trace is placed at one of the AC line inputs to form one electrode of a spark gap. The other electrode on the secondary is formed by the output return node. The spark gap directs most ESD energy from the secondary back to the AC input during a surge event. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent unwanted arcing occurring and possible circuit damage. If R1 and R2 are removed additional spark gaps across the EMI filter inductors (L1 and L2) to prevent excessive build-up of voltage across them during surge.

Drain Clamp Optimization

LYTSwitch-2 ICs use primary-side sensing to regulate the output. The voltage that appears on the primary winding is a reflection of the secondary winding voltage while the internal is off. Leakage inductance induced ringing can affect output regulation. Optimizing the drain clamp to minimize high frequency ringing will give the best regulation. Figure 7 shows the desired drain voltage waveform; while Figure 8 shows a large undershoot due to a leakage inductance induced ring. Ringing can be reduced (and hence regulation improved) by adjusting the value of the resistor in series with the primary clamp diode.

Addition of a Bias Circuit for Higher Light Load Efficiency and Lower No-load Input Power Consumption

The addition of a bias circuit can decrease the no-load input power from ~200 mW to less than 30 mW at 230 VAC input.

The power supply schematic shown in Figure 4 has the bias circuit incorporated. Diode D2, C5 and R9 form the bias circuit.

Diode D2 rectifies the output and C5 is the filter capacitor. A 1 µF capacitor is recommended to maintain the minimum bias voltage at low switching frequencies.

The recommended current into the BYPASS pin is equal to IC supply current (~0.5 mA) at the minimum bias winding voltage. The BYPASS pin current should not exceed 3 mA at the maximum bias winding voltage. The value of R9 is calculated according to $(V_{BIAS}-V_{BP})/I_{S2}$, where V_{BIAS} (10 V typical) is the voltage across C5, I_{S2} (0.5 mA typ.) is the IC supply current and V_{BP} (6.2 V typ.) is the BYPASS pin voltage.

The parameters I_{S2} and V_{BP} are provided in the parameter table of the LYTSwitch-2 data sheet. Diode D2 can be a low-cost type such as FR102, 1N4148 or BAV19/20/21.

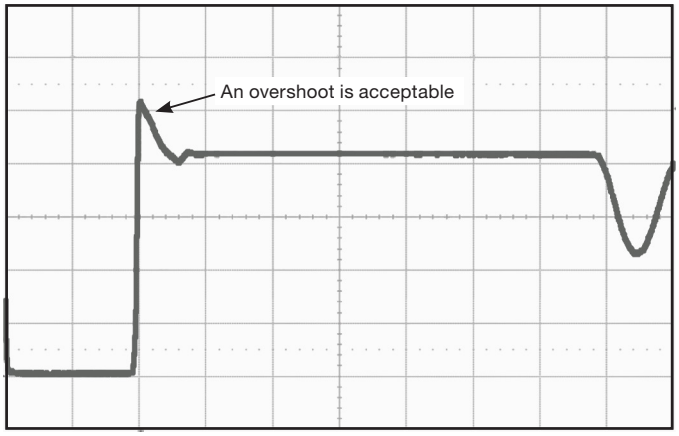


Figure 7. Desired Drain Voltage Waveform with Minimal Leakage Ringing Undershoot.

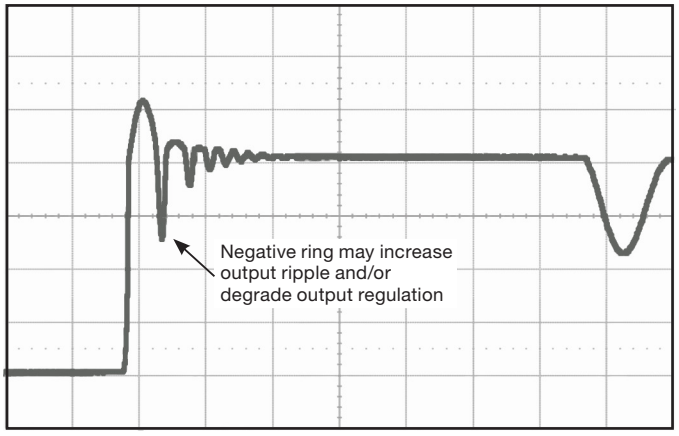


Figure 8. Undesirable Drain Voltage Waveform with Large Leakage Ring Undershoot.

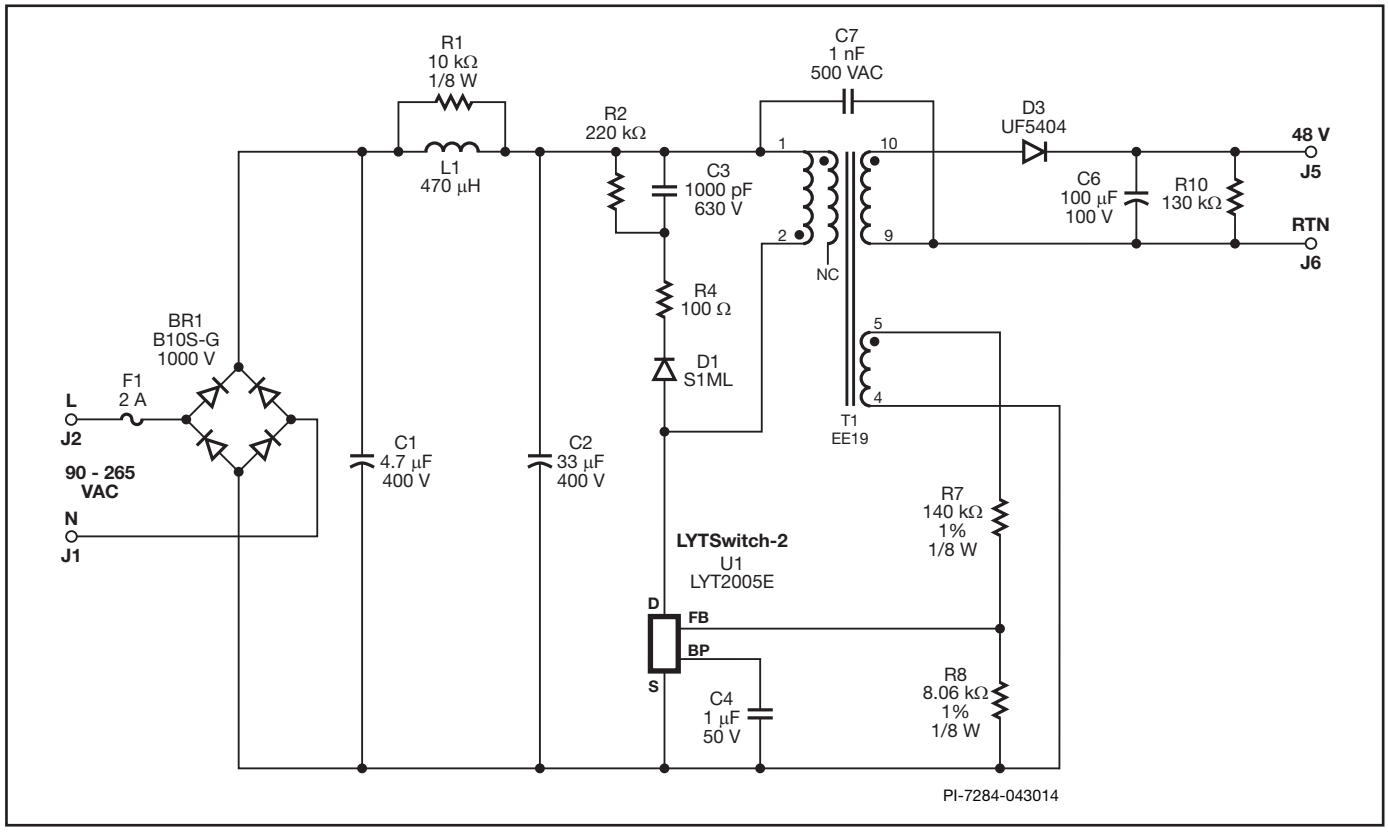


Figure 9. Example Schematic of LYTSwitch-2 Flyback Power Supply without Bias Supply.

Quick Design Checklist

As with any power supply design, all LYTSwitch-2 family designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following set of tests is strongly recommended:

1. Maximum drain voltage – Verify that the peak V_{DS} does not exceed 680 V at the highest input voltage and maximum output power.
2. Drain current – At maximum ambient temperature, maximum and minimum input voltage and maximum output load, review drain current waveforms at start-up for any signs of transformer saturation or excessive leading edge current spikes. LYTSwitch-2 devices have a leading edge blanking time to prevent premature termination of the ON-cycle, but limit leading edge spikes to less than the maximum time as specified in the data sheet.
3. Thermal check – At maximum output power, for both minimum and maximum input voltage and maximum ambient temperature; verify that temperature limits are not exceeded for LYTSwitch-2, transformer, output diodes and output capacitors. Thermal margin should be provided to allow for part-to-part variation in the $R_{DS(ON)}$ of the LYTSwitch-2 device. For optimum regulation, a SOURCE pin temperature of 90 ºC is recommended.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.power.com

Absolute Maximum Ratings[1,6]

DRAIN Voltage ..... -0.3 V to 725 V
DRAIN Pin Peak Current[5]: LYT2001 ..... 400 (600) mA[2]
LYT2002 ..... 504 (750) mA[2]
LYT2003 ..... 654 (980) mA[2]
LYT2004 .....686 (1029) mA[2]
LYT2005 ..... 784 (1176) mA[2]
Peak Negative Pulsed Drain Current ..... -100 mA[3]
FEEDBACK Pin Voltage ..... -0.3 to 9 V
FEEDBACK Pin Current..... 100 mA
BYPASS Pin Voltage ..... -0.3 to 9 V
Storage Temperature ……..... -65 to 150 °C
Operating Junction Temperature[4].....-40 to 150 °C
Lead Temperature[5].....260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Higher peak Drain current allowed while Drain to Source voltage does not exceed 400 V.
3. Duration not to exceed 2 ms.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for 5 seconds.
6. Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: D Package:
(θ_{JA}) .....100 °C/W[2], 80 °C/W[3]
(θ_{JC})[1] ..... 30 °C/W
E Package
(θ_{JA}) ..... 105 °C/W[4]
(θ_{JC}) ..... 2 °C/W[5]
K Package
(θ_{JA}) .....45 °C/W[6], 38 °C/W[7]
(θ_{JC}) ..... 2 °C/W[5]

Notes:
1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Free standing with no heat sink.
5. Measured at the back surface of tab.
6. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
7. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Programmable Maximum Frequency	f_{OSC}	T_J = 25 °C $t_{ON} \times I_{FB}$ = 1.4 mA-µs See Note A	$V_{FB} = V_{FBth}$			85	kHz
Minimum Operation Frequency	$f_{OSC(MIN)}$	T_J = 25 °C $V_{FB} = V_{FBth}$	LYT2001-2003	300	330	365	Hz
			LYT2004D/E/K	775	850	930	
			LYT2005	510	580	645	
Frequency Ratio (Constant Current)	$f_{RATIO(CC)}$	T_J = 25 °C Between V_{FB} = 1.0 V and V_{FB} = 1.6 V		1.550	1.593	1.635	
Frequency Ratio (Inductance Correction)	$f_{RATIO(IC)}$	Between $t_{ON} \times I_{FB}$ = 1.4 mA and $t_{ON} \times I_{FB}$ = 2 mA-µs		1.160	1.210	1.260	
Frequency Jitter		Peak-to-Peak Jitter Compared to Average Frequency, T_J = 25 °C			±7		%

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
Maximum Duty Cycle	DC_{MAX}	See Notes D, E			55		%
FEEDBACK Pin Voltage	$V_{FB(TH)}$	C_{BP} = 1 µF	T_J = 25 °C	1.915	1.940	1.965	V
			T_J = 100 °C See Note E	1.90	1.94	1.98	
FEEDBACK Pin Voltage at Turn-Off Threshold	$V_{FB(AR)}$			0.69	0.75	0.81	V
Minimum Switch ON-Time	$t_{ON(MIN)}$	See Note E			700		ns
FEEDBACK Pin Sampling Delay	t_{FB}	T_J = 25 °C		2.35	2.55	2.75	µs
DRAIN Pin Supply Current	I_{S1}	FB Voltage > V_{FBth} (MOSFET Not Switching)			320	370	µA
	I_{S2}	FB Voltage = V_{FBth} -0.1 V, Switch ON-Time = t_{ON} (MOSFET Switching at f_{OSC})	LYT2001		440		µA
			LYT2002		500	560	
			LYT2003		550	600	
			LYT2004		600	680	
			LYT2005		700	800	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V	LYT2001		-3.4		mA
			LYT2002	-7.0	-4.8	-2.5	
			LYT2003	-7.2	-5.8	-3.2	
			LYT2004	-8.5	-6.3	-3.2	
			LYT2005	-8.5	-6.3	-3.2	
	I_{CH2}	V_{BP} = 4 V	LYT2001		-2.3		
			LYT2002	-5.6	-3.2	-1.4	
			LYT2003	-5.6	-4.0	-2.0	
			LYT2004	-6.0	-4.4	-2.0	
			LYT2005	-6.0	-4.4	-2.0	
BYPASS Pin Voltage	V_{BP}			5.65	5.9	6.25	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.70	0.95	1.20	V
BYPASS Pin Shunt Voltage	V_{SHUNT}			6.2	6.4	6.8	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Current Limit	I_{LIMIT}	V_{BP} = 5.9 V T_J = 25 °C	LYT2001D di/dt = 60 mA/µs		250		mA
			LYT2002D di/dt = 80 mA/µs	293	315	337	
			LYT2003D di/dt = 100 mA/µs	363	390	417	
			LYT2004D di/dt = 105 mA/µs	390	420	450	
			LYT2004E/K di/dt = 125 mA/µs	460	495	530	
			LYT2005E/K di/dt = 135 mA/µs	511	550	589	
Minimum Current Limit Scale Factor	$I_{LIMIT(MIN)}$	T_J = 25 °C		0.28	0.32	0.39	
Normalized Output Current	I_O	T_J = 25 °C		0.975	1.000	1.025	
Leading Edge Blanking Time	t_{LED}	T_J = 25 °C See Note E		170	215		ns
Thermal Shutdown Temperature	T_{SD}	See Note E		135	142	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	See Note E			60		°C
Output							
ON-State Resistance	$R_{DS(ON)}$	LYT2001D I_D = 50 mA	T_J = 25 °C		24		Ω
			T_J = 100 °C		36		
		LYT2002D I_D = 63 mA	T_J = 25 °C		13	15.5	
			T_J = 100 °C		20	23.5	
		LYT2003D I_D = 78 mA	T_J = 25 °C		8	9.2	
			T_J = 100 °C		12	14	
		LYT2004D I_D = 84 mA	T_J = 25 °C		5	5.9	
			T_J = 100 °C		7.5	8.60	
		LYT2004E/K I_D = 99 mA	T_J = 25 °C		5	5.9	
			T_J = 100 °C		7.5	8.60	
		LYT2005E/K I_D = 110 mA	T_J = 25 °C		3.2	3.8	
			T_J = 100 °C		4.6	5.40	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Output (cont.)						
OFF-State Leakage	I_{DSS1}	V_{DS} = 560 V T_J = 125 °C, See Note C			50	µA
	I_{DSS2}	V_{DS} = 375 V T_J = 50 °C		15		
Breakdown Voltage	BV_{DSS}	T_J = 25 °C	725			V
DRAIN Pin Supply Voltage			50			V
Auto-Restart ON-Time	t_{AR-ON}	$t_{ON} \times I_{FB}$ = 1.4 mAµs f_{OSC} = 12 kHz V_{FB} = 0 See Notes A, E	100			ms
Auto-Restart OFF-Time	t_{AR-OFF}	See Note E	0.32			s
Open-Loop FEEDBACK Pin Current Threshold	I_{OL}	See Note E		-45		µA
Open-Loop ON-Time		See Note E		1.4		ms

NOTES:

A. Auto-restart on-time is a function of switching frequency programmed by t_{on}x I_{FB} and minimum frequency in CC mode.

B. The current limit threshold is compensated to cancel the effect of current limit delay. As a result the output current stays constant across the input line range.

C. I_{DSS1} is the worst-case off-state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 265 VAC) for no-load consumption calculations.

D. When the duty cycle exceeds DC_{MAX} the LYTSwitch-2 operates in on-time extension mode.

E. This parameter is derived from characterization.

Typical Performance Characteristics

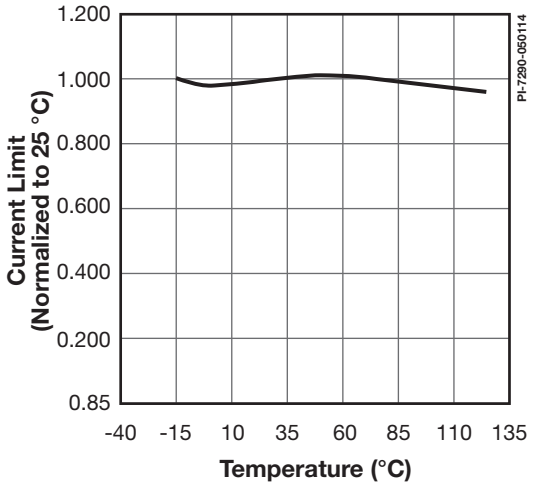


Figure 10. Current Limit vs. Temperature.

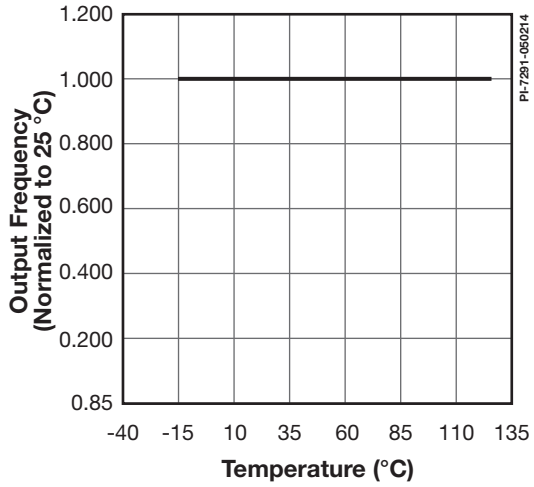


Figure 11. Output Frequency vs. Temperature.

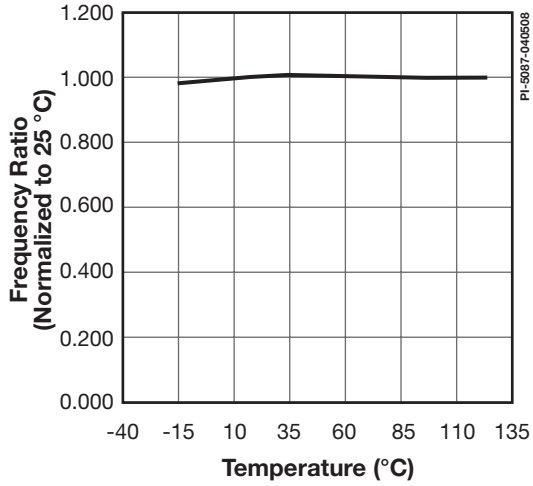


Figure 12. Frequency Ratio vs. Temperature (Constant Current).

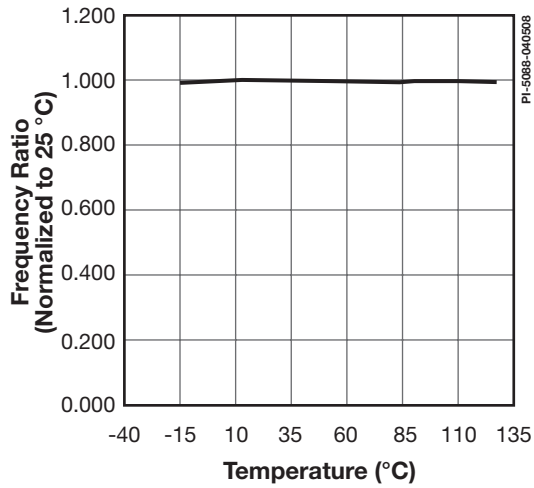


Figure 13. Frequency Ratio vs. Temperature (Inductor Current).

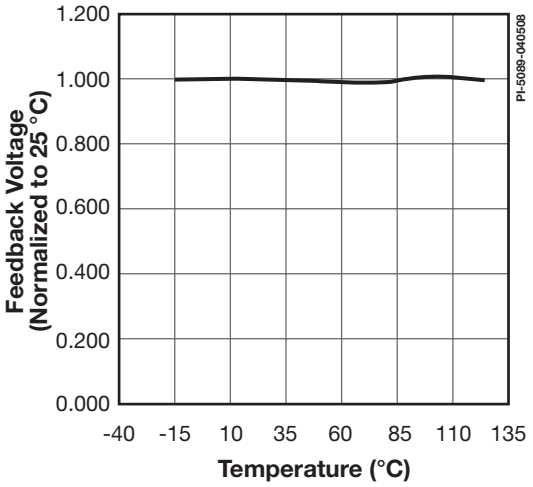


Figure 14. Feedback Voltage vs. Temperature.

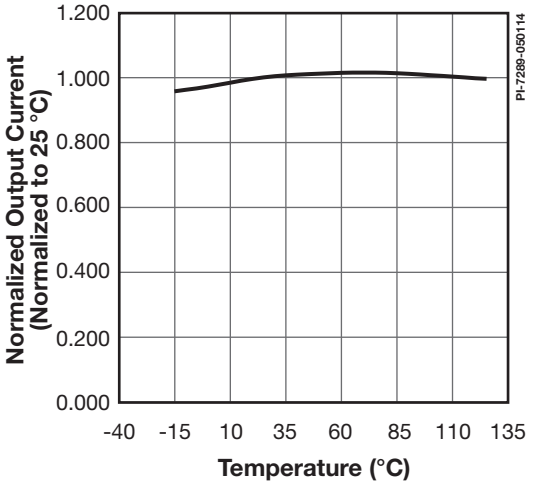


Figure 15. Normalized Output Current vs. Temperature.

Typical Performance Characteristics

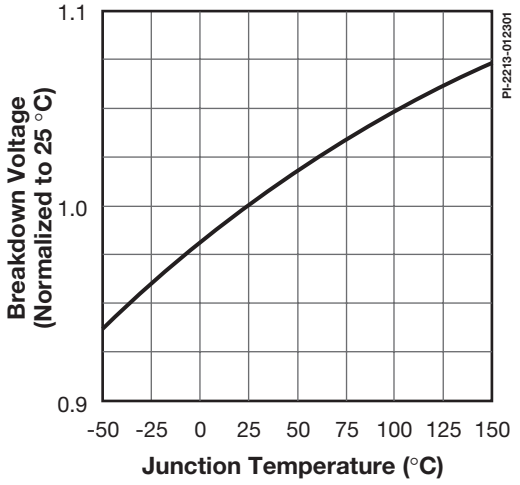


Figure 16. Breakdown vs. Temperature.

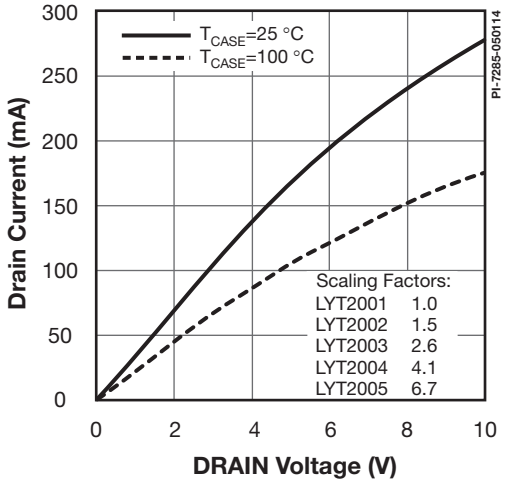


Figure 17. Output Characteristic.

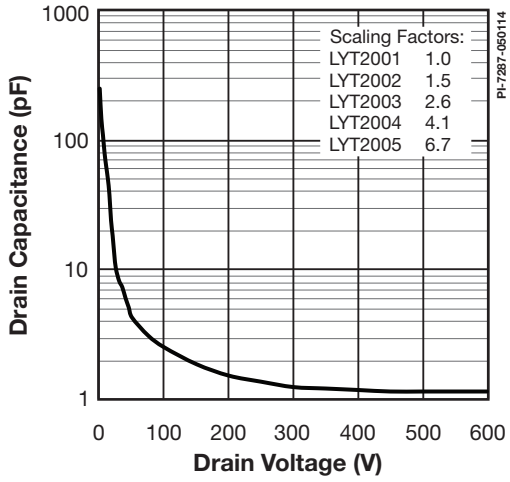


Figure 18. C_{OSS} vs. Drain Voltage.

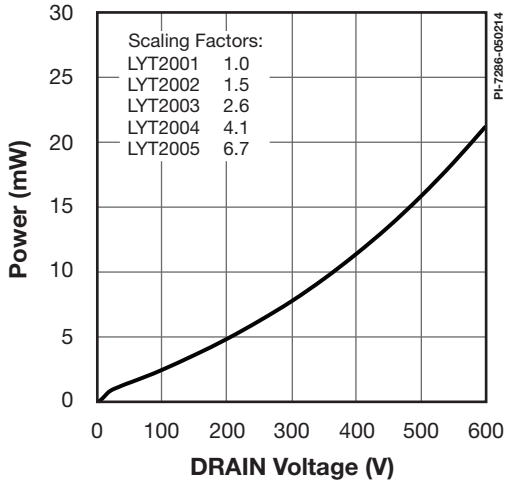
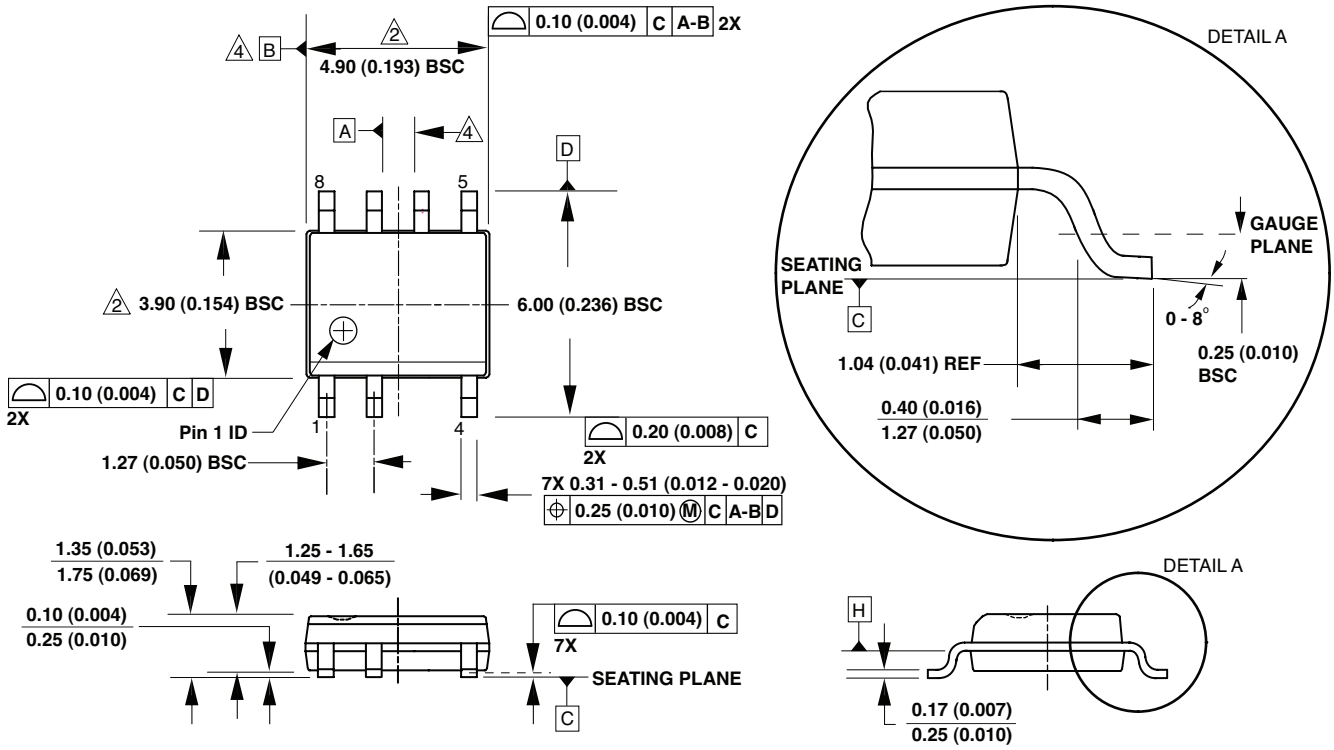


Figure 19. Drain Capacitance Power.

SO-8C (D Package)



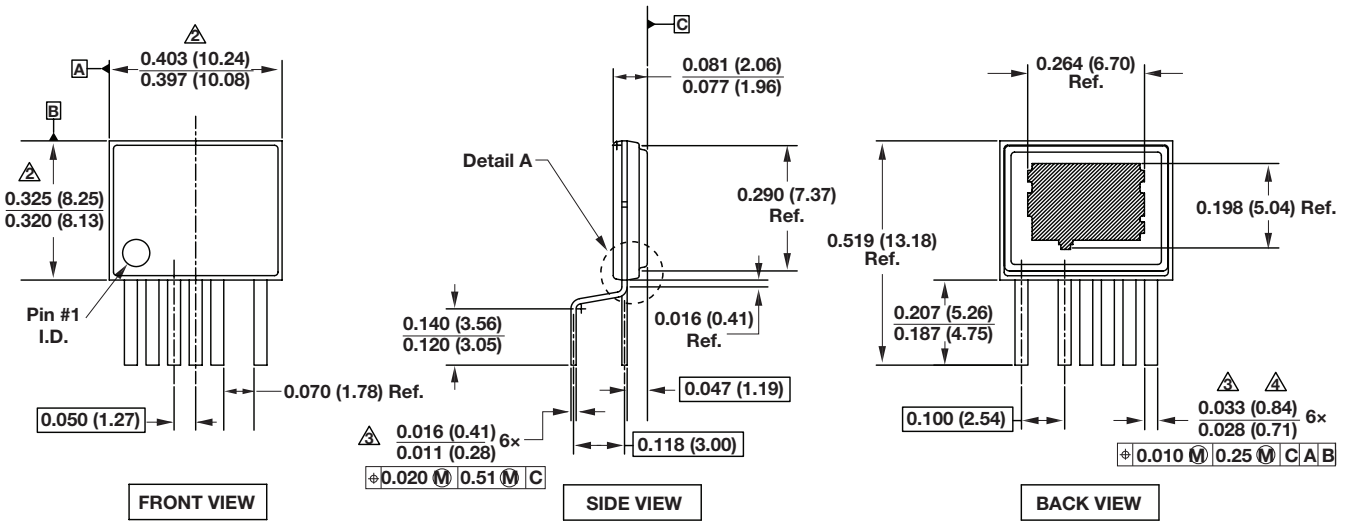
Notes:

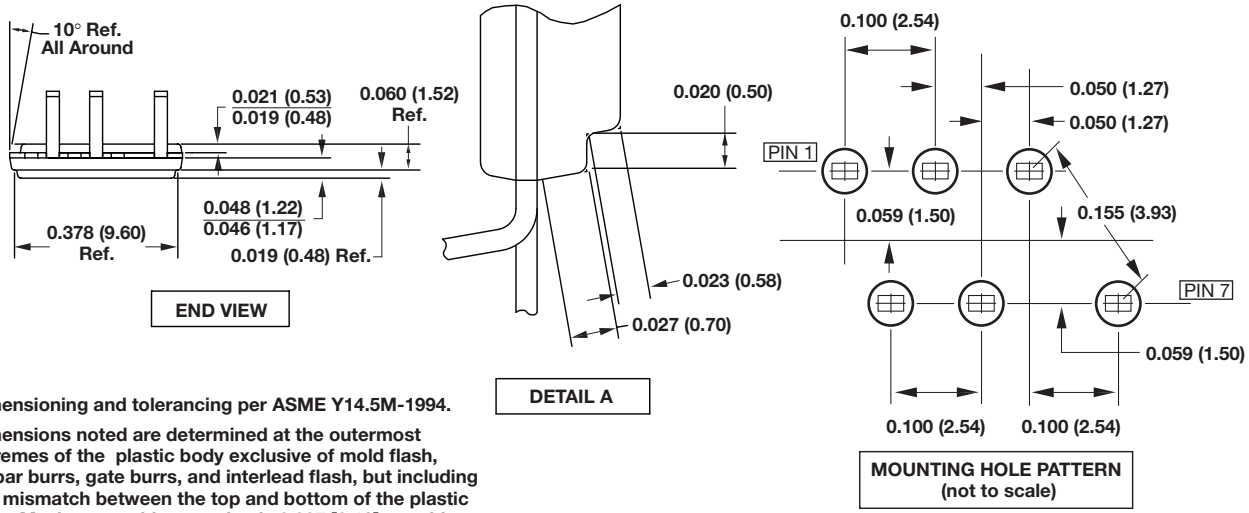
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040110

eSIP-7C (E Package)



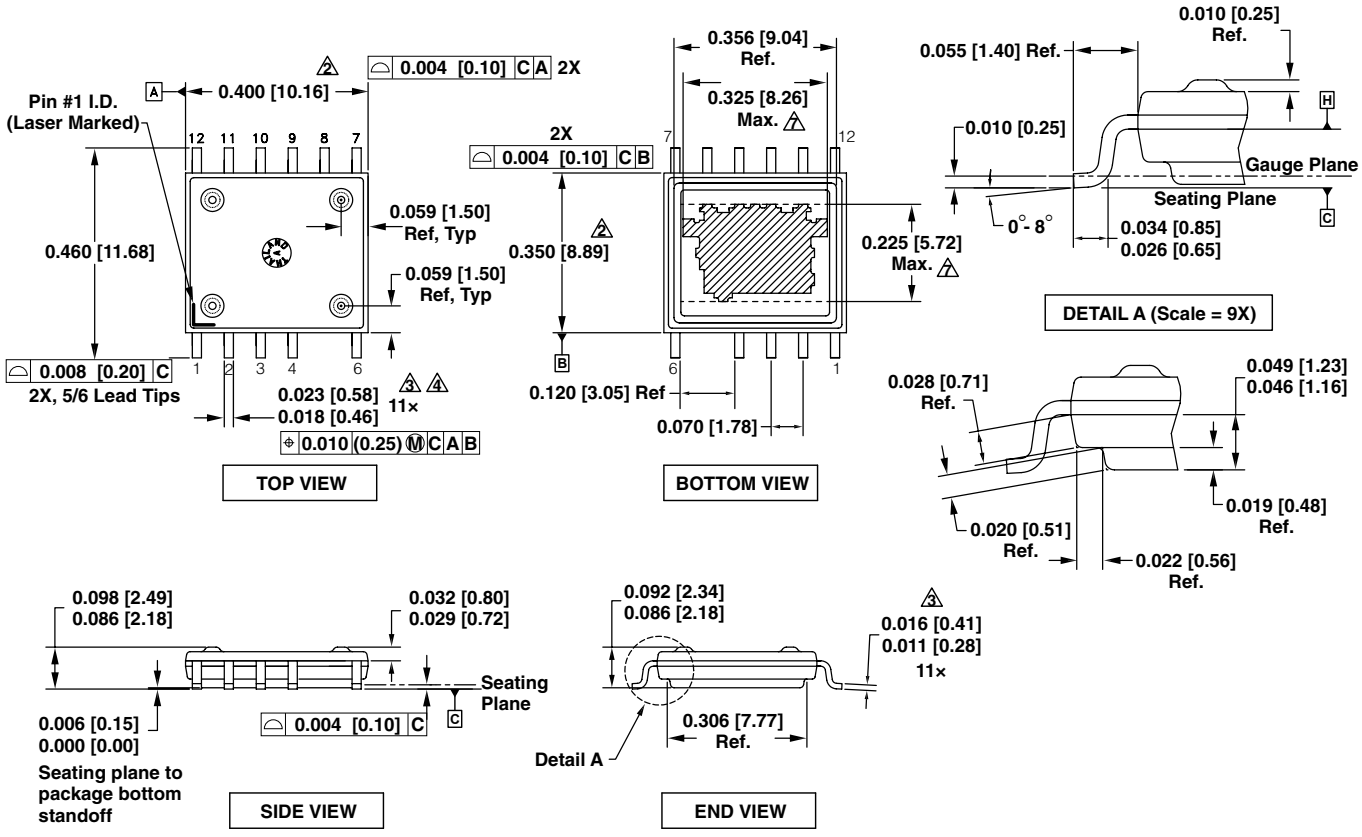


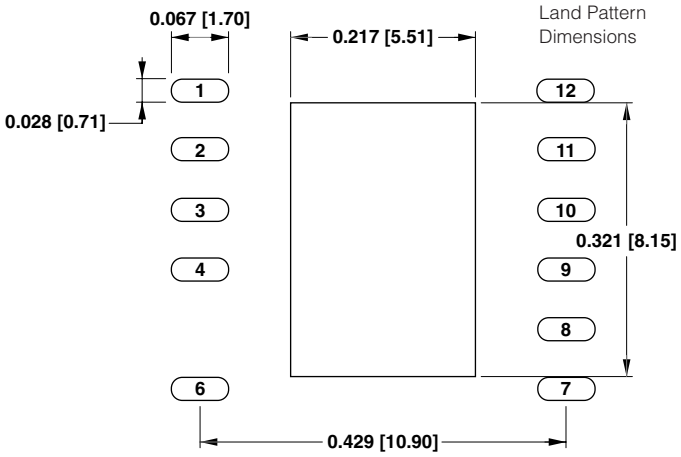
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-061510

eSOP-12B (K Package)



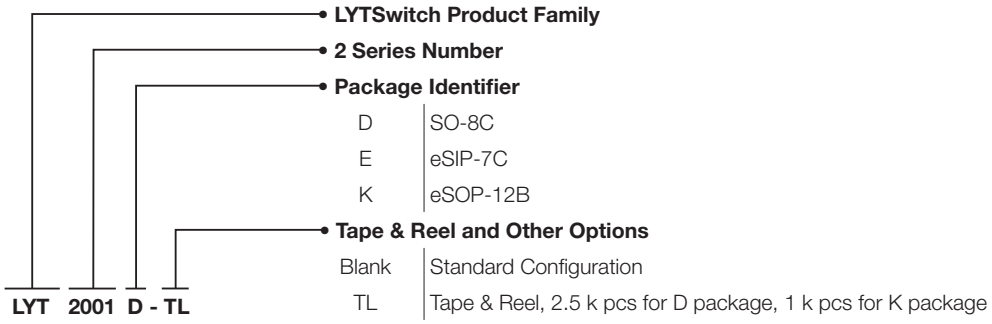


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5748a-100311

Part Ordering Information



Revision	Notes	Date
A	Code A.	05/19/14
A	Updated Figure 2.	06/12/14
A	Updated $V_{FB(TH)}$ parameter table information.	12/08/14

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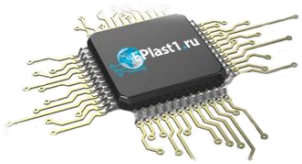

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