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January 2015

J109 / MMBFJ108 N-Channel Switch

Features

- This device is designed for digital switching applications where very low on resistance is mandatory.
- Sourced from process 58

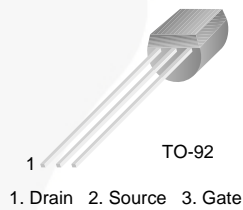


Figure 1. J109 Device Package

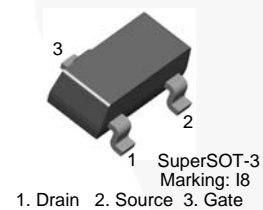


Figure 2. MMBFJ108 Device Package

Ordering Information

Part Number	Top Mark	Package	Packing Method
J109	J109	TO-92 3L	Bulk
J109_D26Z	J109	TO-92 3L	Tape and Reel
MMBFJ108	I8	SSOT 3L	Tape and Reel

Absolute Maximum Ratings^{(1), (2)}

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	-25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Notes:

1. These ratings are based on a maximum junction temperature of 150°C .
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.		Unit
		J109 ⁽³⁾	MMBFJ108 ⁽⁴⁾	
P_D	Total Device Dissipation	625	350	mW
	Derate Above 25°C	5.0	2.8	mW/ $^\circ\text{C}$
$R_{\theta\text{JC}}$	Thermal Resistance, Junction-to-Case	125		$^\circ\text{C/W}$
$R_{\theta\text{JA}}$	Thermal Resistance, Junction-to-Ambient	200	357	$^\circ\text{C/W}$

Notes:

- PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.
- Device mounted on FR-4 PCB 36mm x 18mm x 1.5mm; mounting pad for the collector lead minimum 6cm².

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
Off Characteristics						
$V_{(\text{BR})\text{GSS}}$	Gate-Source Breakdown Voltage	$I_G = -10 \mu\text{A}, V_{\text{DS}} = 0$	-25		V	
I_{GSS}	Gate Reverse Current	$V_{\text{GS}} = -15 \text{ V}, V_{\text{DS}} = 0$		-3.0	nA	
		$V_{\text{GS}} = -15 \text{ V}, V_{\text{DS}} = 0, T_A = 100^\circ\text{C}$		-200		
$V_{\text{GS(off)}}$	Gate-Source Cut-Off Voltage	$V_{\text{DS}} = 15 \text{ V}, I_D = 10 \text{ nA}$	MMBFJ108	-3.0	-10.0	V
			J109	-2.0	-6.0	
On Characteristics						
I_{DSS}	Zero-Gate Voltage Drain Current ⁽⁵⁾	$V_{\text{DS}} = 15 \text{ V}, V_{\text{GS}} = 0$	MMBFJ108	80		mA
			J109	40		
$r_{\text{DS(on)}}$	Drain-Source On Resistance	$V_{\text{DS}} \leq 0.1 \text{ V}, V_{\text{GS}} = 0$	MMBFJ108		8.0	Ω
			J109		12	
Small Signal Characteristics						
$C_{\text{dg(on)}}$ $C_{\text{sg(off)}}$	Drain-Gate & Source-Gate On Capacitance	$V_{\text{DS}} = 0, V_{\text{GS}} = 0, f = 1.0 \text{ MHz}$		85	pF	
$C_{\text{dg(off)}}$	Drain-Gate Off Capacitance	$V_{\text{DS}} = 0, V_{\text{GS}} = -10 \text{ V}, f = 1.0 \text{ MHz}$		15	pF	
$C_{\text{sg(off)}}$	Source-Gate Off Capacitance	$V_{\text{DS}} = 0, V_{\text{GS}} = -10 \text{ V}, f = 1.0 \text{ MHz}$		15	pF	

Note:

- Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Performance Characteristics

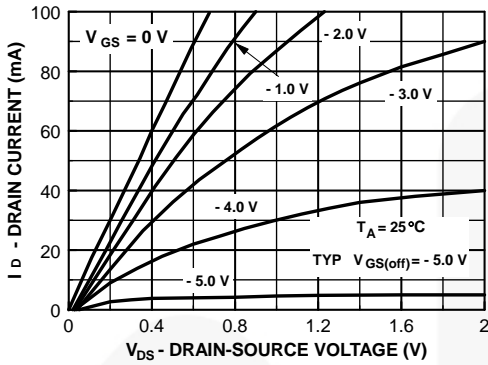


Figure 3. Common Drain-Source

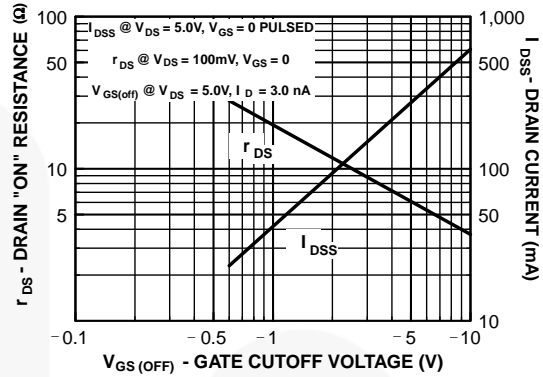


Figure 4. Parameter Interactions

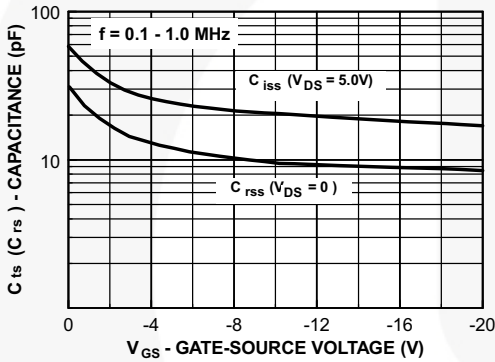


Figure 5. Common Drain-Source



Figure 6. Common Drain-Source

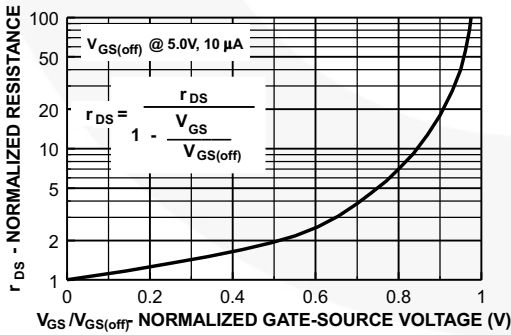


Figure 7. Normalized Drain Resistance vs. Bias Voltage

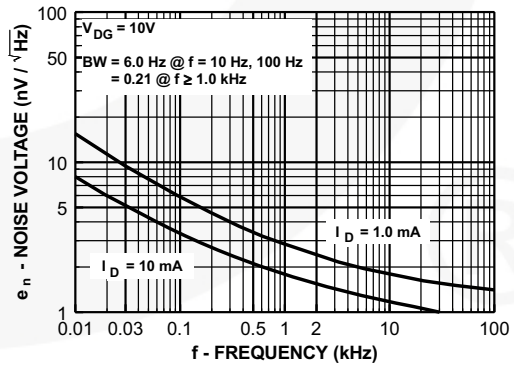


Figure 8. Noise Voltage vs. Frequency

Typical Performance Characteristics (Continued)

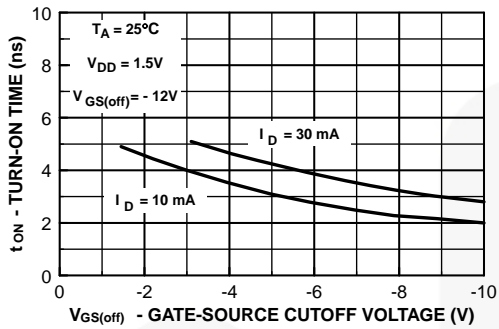


Figure 9. Switching Turn-On Time vs. Gate-Source Cut-Off Voltage

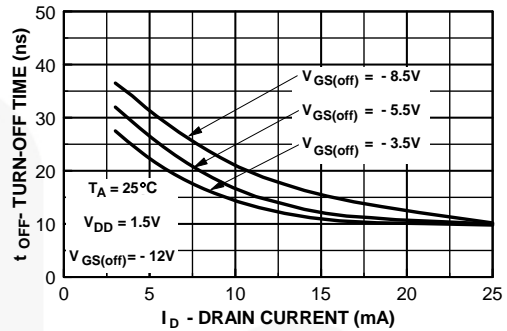


Figure 10. Switching Turn-Off Time vs. Drain Current

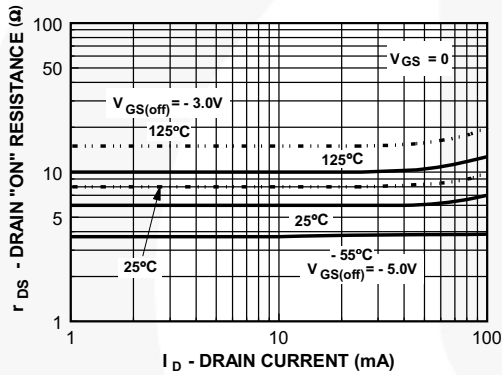


Figure 11. On Resistance vs. Drain Current

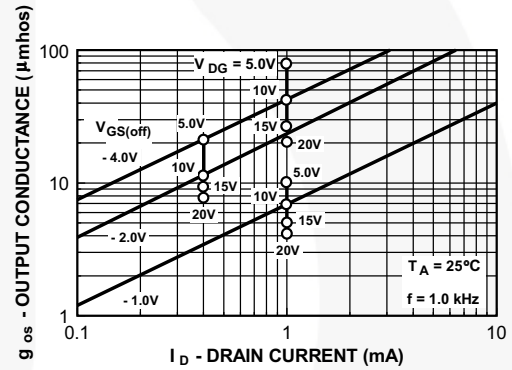


Figure 12. Output Conductance vs. Drain Current

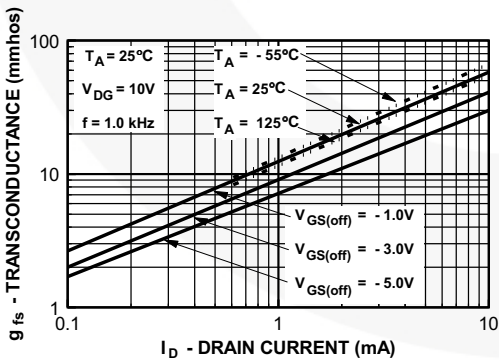


Figure 13. Transconductance vs. Drain Current

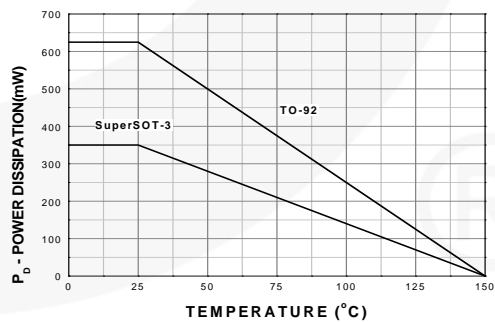


Figure 14. Power Dissipation vs. Ambient Temperature

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

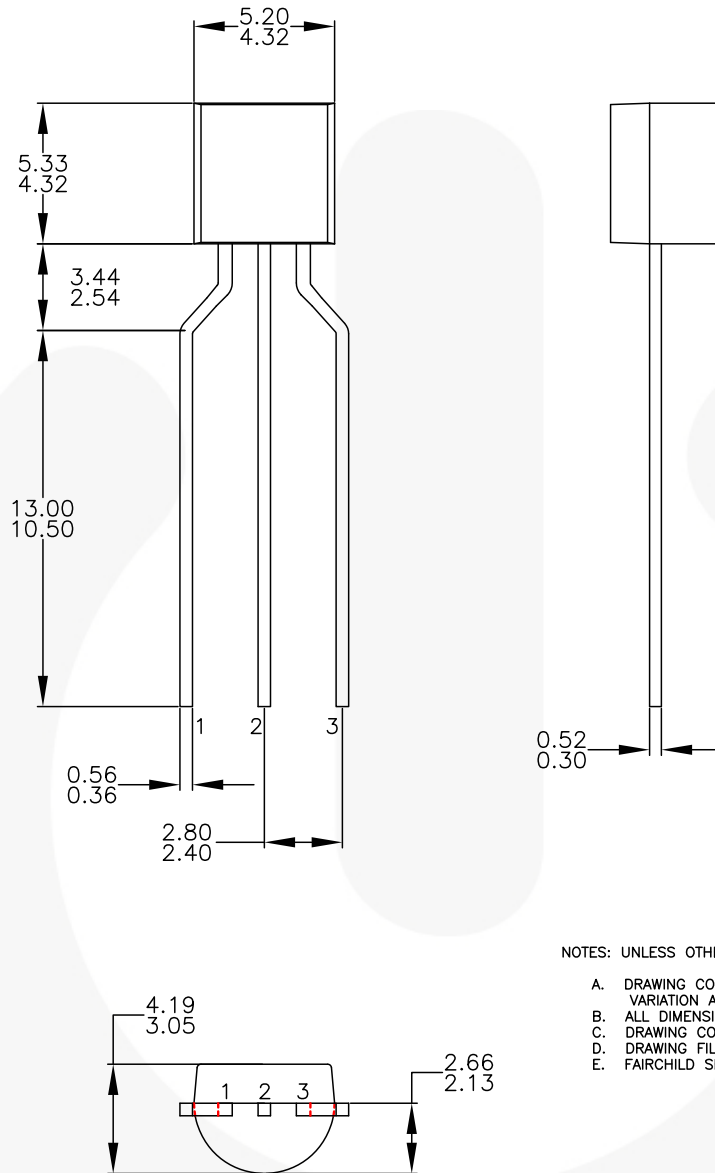
LEGEND:

- P - BIPOLAR
- F - JFET
- M - DMOS
- E - EMITTER
- B - BASE
- C - COLLECTOR
- D - DRAIN
- S - SOURCE
- G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 15. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type

Physical Dimensions (Continued)

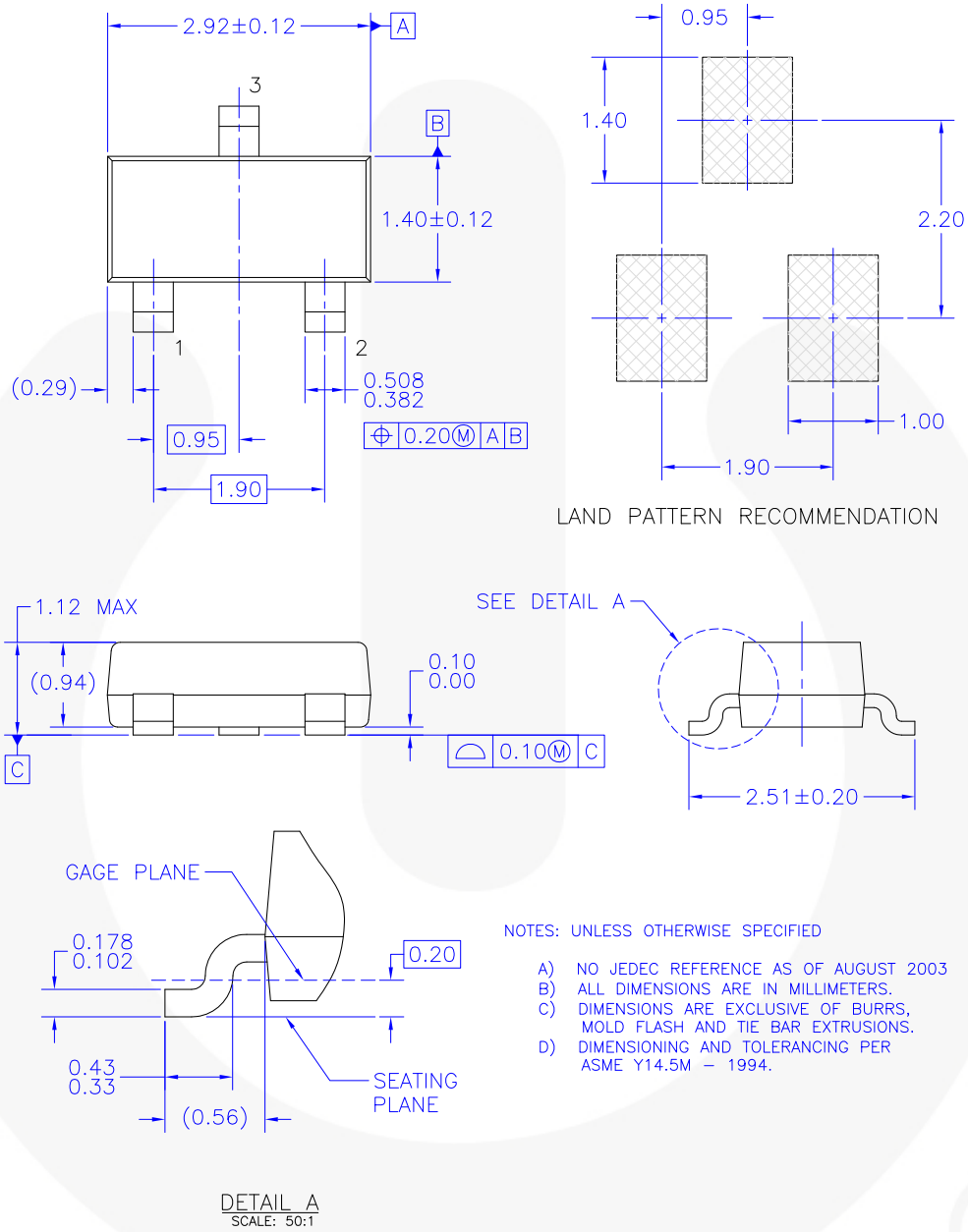


NOTES: UNLESS OTHERWISE SPECIFIED

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- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 16. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type

Physical Dimensions (Continued)



MA03BREV B

Figure 17. MOLDED PACKAGE, SUPERSOT, 3-LEAD





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