

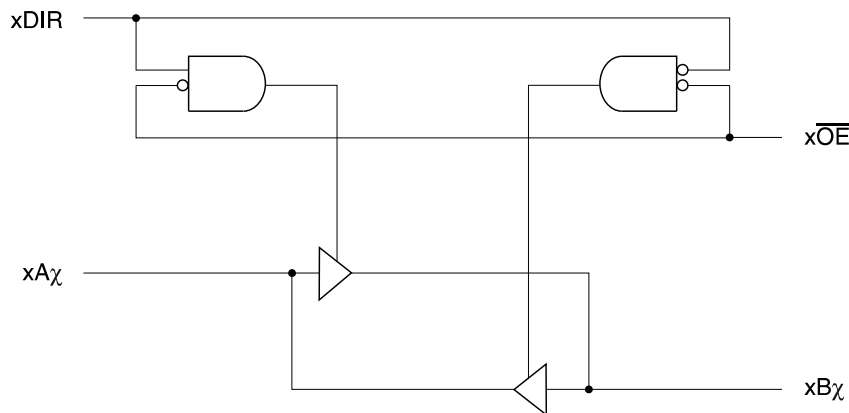
## Features

- Fastest Propagation Speeds in the Industry  $T_{PD}$  (F grade) = 2.5 ns,  $T_{PD}$  (G grade) = 2.0 ns
- Maximum Derating for Capacitive Loads 1.5ns/100pF (F grade) and 1.1ns/100pF (G grade)
- Very Low Ground Bounce <0.6V @  $V_{CC}=5.00$  V,  $T_a=25^\circ\text{C}$
- Excellent Noise Rejection
- Typical Output Skew  $\leq 0.25$ ns
- Bus Hold Circuitry to Retain Last Active State During Tri-State™
- Available in SSOP and TSSOP Packages

## Description

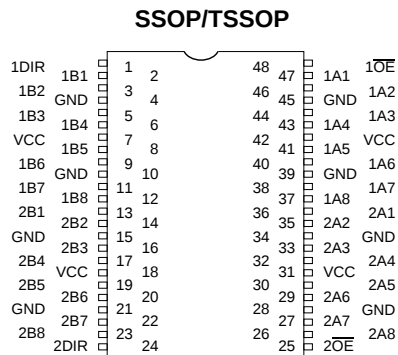
Atmel's new family of high speed CMOS transceivers offers the best of all worlds to the user requiring stability and ultra fast speeds. These transceivers, which can function as two 8-bit devices or one 16-bit device, are capable of improving processing efficiency as much as 6% by reducing the number of wait states required during memory access. In addition, this family of parts has been designed to minimize ground bounce on the outputs while rejecting input spikes of up to 1.8V and 1 ns wide. This combination of ultra high speed and low noise is the next step in high speed performance.

## Functional Block Diagram



## Pin Configurations

| Pin Names        | Descriptions                       |
|------------------|------------------------------------|
| $\overline{xOE}$ | Output Enable Input (Active Low)   |
| xDIR             | Direction Control Input            |
| $xA_\chi$        | Side A Inputs or Tri-State Outputs |
| $xB_\chi$        | Side B Inputs or Tri-State Outputs |



Top View

## AT16245<sup>TM</sup> Fast Logic<sup>TM</sup> Bi-Directional Transceiver

## AT16245F AT16245G

## Function Table

| Inputs           |           | Outputs             |
|------------------|-----------|---------------------|
| $\overline{xOE}$ | $xDIR$    |                     |
| L                | L         | Bus B Data to Bus A |
| L                | H         | Bus A Data to Bus B |
| H                | $X^{(1)}$ | High Z State        |

Note: 1. X = Don't Care

## Absolute Maximum Ratings\*

Operating Temperature ..... 0°C to +70°C  
Storage Temperature ..... -65°C to +150°C  
Voltage on any Pin  
with Respect to Ground..... -2.0 V to +7.0V<sup>(1)</sup>  
Maximum Operating Voltage..... 6.0V

NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is VCC +0.75V dc which may overshoot to +7.0V for pulses of less than 20 ns.

## 5.0 Volt DC Characteristics

Applicable over recommended operating range from Ta=0°C to +70°C, VCC=+5.0V ±5% (unless otherwise noted)

| Symbol                         | Parameter                           | Test Conditions                       | Min | Typ | Max  | Units |
|--------------------------------|-------------------------------------|---------------------------------------|-----|-----|------|-------|
| $\Delta I_{CC}$                | Quiescent Power Supply Current      | VCC=Max, VIN=3.4V                     |     | 0.8 | 1.2  | mA    |
| V <sub>IH</sub>                | Input High Voltage                  |                                       | 2.0 |     |      | V     |
| V <sub>IL</sub>                | Input Low Voltage                   |                                       |     |     | 0.8  | V     |
| I <sub>IH</sub>                | Input High Current (I/O Pins)       | VIN=VCC                               |     |     | ±15  | μA    |
| I <sub>IL</sub>                | Input Low Current (I/O Pins)        | VIN= GND                              |     |     | ±15  | μA    |
| I <sub>OZ</sub>                | Output Leakage Current              |                                       |     |     | ±10  | μA    |
| V <sub>OH</sub> <sup>(1)</sup> | Output High Voltage<br>F Grade only | VCC=4.75 V<br>I <sub>OH</sub> =-10 mA | 2.7 |     |      | V     |
| V <sub>OH</sub> <sup>(2)</sup> | Output High Voltage<br>G Grade only | VCC=4.75 V<br>I <sub>OH</sub> =-12 mA | 2.7 |     |      | V     |
| V <sub>OL</sub>                | Output Low Voltage (F Grade)        | I <sub>OL</sub> =10 mA                |     |     | 0.55 | V     |
| V <sub>OL</sub>                | Output Low Voltage (G Grade)        | I <sub>OL</sub> =12 mA                |     |     | 0.55 | V     |

Note: 1. F grade: At VCC(max), the value of V<sub>OH</sub>(max) = 3.75V and at VCC(min), V<sub>OH</sub>(max) = 3.25V  
2. G grade: At VCC(max), the value of V<sub>OH</sub>(max) = 3.75V and at VCC(min), V<sub>OH</sub>(max) = 3.35V

## AC Characteristics AT16245F

Applicable over recommended operating range from  $T_a=0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V} \pm 5\%$  (unless otherwise noted)

| Symbol                                     | Parameter                           | Test Conditions   | Min | Typ | Max | Units    |
|--------------------------------------------|-------------------------------------|-------------------|-----|-----|-----|----------|
| $t_{PHL}$<br>$t_{PLH}$                     | Propagation Delay                   | $CL=50\text{ pF}$ |     |     | 2.5 | ns       |
| $t_{PZH}$<br>$t_{PZL}$                     | Output Enable Time                  | $CL=50\text{ pF}$ |     |     | 6.0 | ns       |
| $t_{PHZ}$<br>$t_{PLZ}$                     | Output Disable Time                 | $CL=50\text{ pF}$ |     |     | 6.0 | ns       |
| $t_{SK}^{(1)}$                             | Output Skew                         | $CL=50\text{ pF}$ |     |     | 0.5 | ns       |
| $\Delta t_{PHL}^{(1)}$<br>$\Delta t_{PLH}$ | Propagation Delay vs Output Loading |                   |     | 1.3 | 1.5 | ns/100pF |

Note: 1. This parameter is guaranteed but not 100% tested.

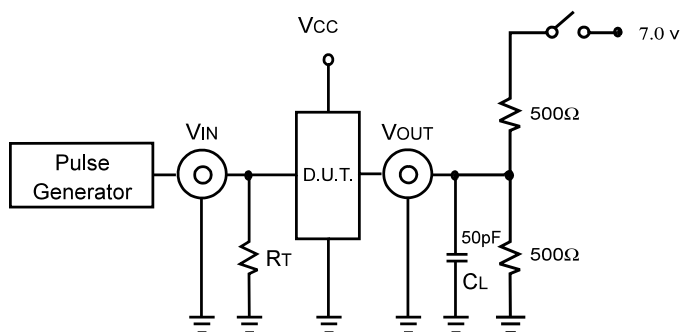
## AT16245G

Applicable over recommended operating range from  $T_a=0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC}=5.0\text{V} \pm 5\%$  (unless otherwise noted)

| Symbol                                     | Parameter                           | Test Conditions   | Min | Typ | Max | Units    |
|--------------------------------------------|-------------------------------------|-------------------|-----|-----|-----|----------|
| $T_{PHL}$<br>$T_{PLH}$                     | Propagation Delay                   | $CL=50\text{ pF}$ |     |     | 2.0 | ns       |
| $T_{PZH}$<br>$T_{PZL}$                     | Output Enable Time                  | $CL=50\text{ pF}$ |     |     | 6.0 | ns       |
| $T_{PHZ}$<br>$T_{PLZ}$                     | Output Disable Time                 | $CL=50\text{ pF}$ |     |     | 5.0 | ns       |
| $T_{SK}^{(1)}$                             | Output Skew                         | $CL=50\text{ pF}$ |     |     | 0.5 | ns       |
| $\Delta t_{PHL}^{(1)}$<br>$\Delta t_{PLH}$ | Propagation Delay vs Output Loading |                   |     | 0.9 | 1.1 | ns/100pF |

Note: 1. This parameter is guaranteed but not 100% tested.

## Test Circuits<sup>(1,2)</sup>



- Note:
1. Pulse Generator: Rate  $\leq 1.0\text{ MHz}$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  2. AC tests are done with a single bit switching, and timings need to be derated when multiple outputs are switching in the same direction simultaneously. This derating should not exceed 0.5 ns for 16 inputs switching simultaneously.

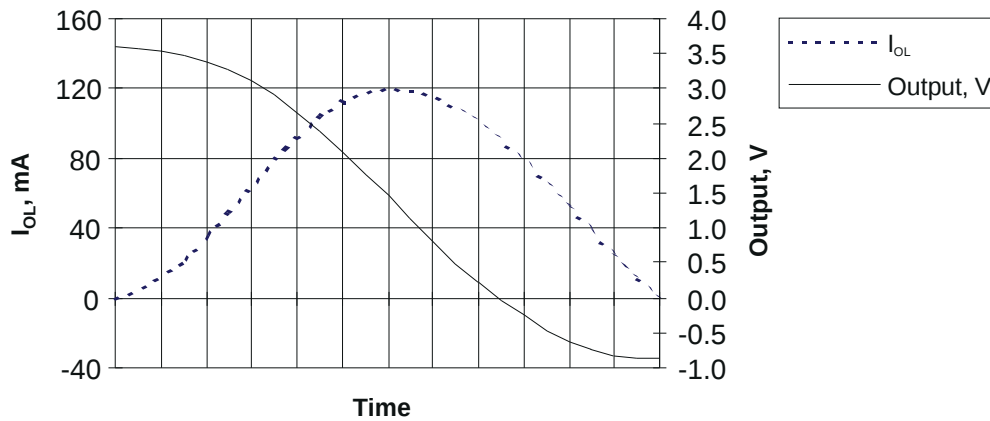
## Switch Position

| Test                                    | Switch |
|-----------------------------------------|--------|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests                         | Open   |

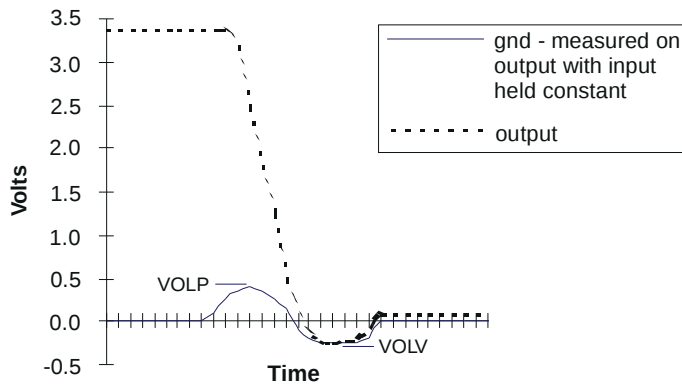
### Definitions:

- $C_L$  = Load capacitance; Includes jig and probe capacitance.  
 $R_T$  = Termination resistance; Should be equal to  $Z_{OUT}$  of the Pulse Generator.

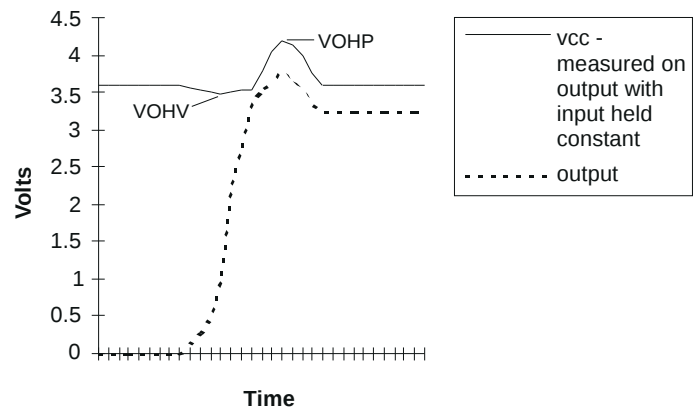
## IOL Pull Down Current



## Ground Bounce for High to Low Transitions<sup>(1)</sup>



## Supply Bounce for Low to High Transitions<sup>(2)</sup>

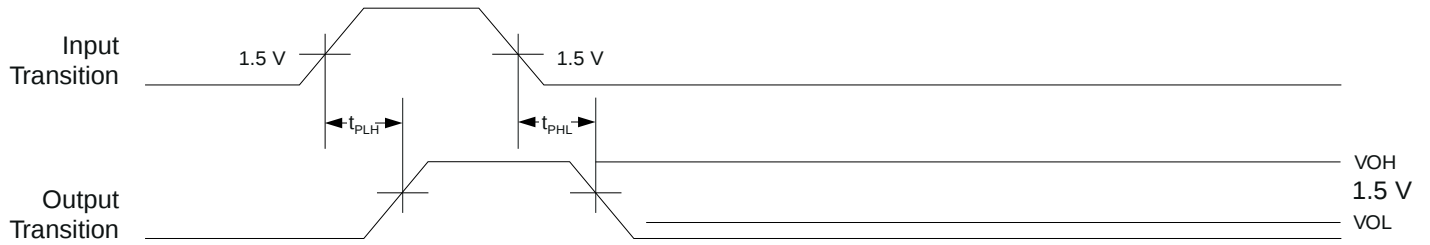


## Typical Values

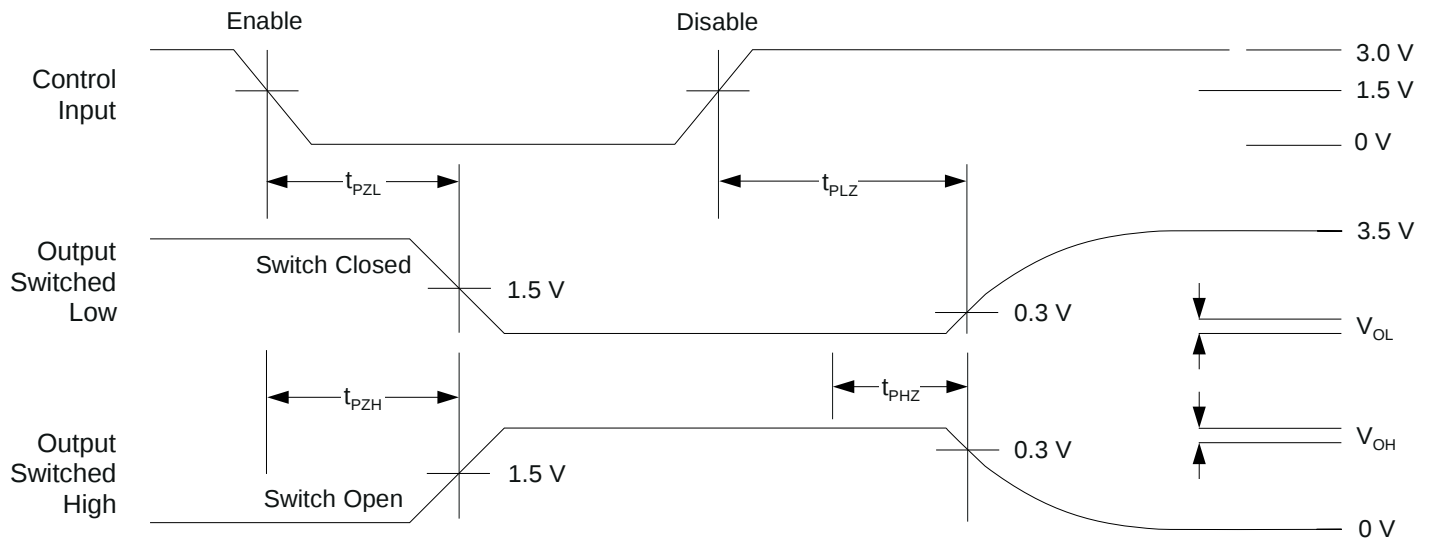
| Parameter | Value           | Units |
|-----------|-----------------|-------|
| $V_{OLP}$ | 0.4             | V     |
| $V_{OLV}$ | -0.26           | V     |
| $V_{OHV}$ | $V_{CC} - 0.13$ | V     |
| $V_{OHP}$ | $V_{CC} + 0.6$  | V     |

- Note:
1. When multiple outputs are switched at the same time, rapidly changing current on the ground and  $V_{CC}$  paths cause a voltage to develop across the parasitic inductance of the wire bond and package pins. This occurrence is called simultaneous switching noise. Atmel's AT16245 products have minimized this phenomenon as shown on the graph. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz. The ground data is measured on the one remaining output, which is set to logic low and will reflect any device ground movement.
  2. As on the graph for Ground Bounce, a similar condition occurs for low to high transitions. Output data is for 15 outputs switching simultaneously at a frequency of 1 MHz.  $V_{CC}$  droop is measured on the one remaining output pin, which is set to a logic high. This output will reflect any movement on the device  $V_{CC}$ .

## Propagation Delay Waveforms



## Enable and Disable Waveforms<sup>(1)</sup>



Note: 1. Enable and disable waveforms are the same for both  $\overline{xOE}$  and  $xDIR$  inputs.



## Ordering Information

| <b>T<sub>PD</sub></b> | <b>Ordering Code</b>               | <b>Package</b> | <b>Operation Range</b> |
|-----------------------|------------------------------------|----------------|------------------------|
| 2.5 ns                | AT16245F - 25YC<br>AT16245F - 25XC | 48Y<br>48X     | Commercial             |
| 2.0 ns                | AT16245G - 20YC<br>AT16245G - 20XC | 48Y<br>48X     | Commercial             |

| <b>Package Type</b> |                                                           |
|---------------------|-----------------------------------------------------------|
| <b>48X</b>          | 48 Pin, Plastic Thin Shrink Small Outline Package (TSSOP) |
| <b>48Y</b>          | 48 Pin, Plastic Shrink Small Outline Package (SSOP)       |



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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