SY88993AL

3.3V 3.2Gbps High-Speed Limiting Post Amplifier with High Input Sensitivity

General Description

The SY88993AL limiting post amplifier, with its wide bandwidth, is ideal for use as a post amplifier in fiber-optic receivers with data rates up to 3.2Gbps. Signals as small as $4mV_{PP}$ can be amplified to drive devices with CML inputs or AC-coupled PECL inputs. The SY88993AL generates a chatter-free Loss-of-Signal (LOS) open collector TTL output using an external resistor, as shown Figure 1.

The SY88993AL incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the /EN input of the device to maintain stability under loss of signal conditions. Using LOS_{LVL} pin the sensitivity of the level detect can be adjusted. The LOS_{LVL} voltage can be set by connecting a resistor divider between V_{CC} and V_{REF}, Figure 5.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

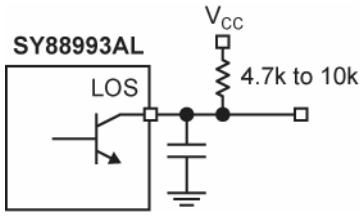


Figure 1. LOS_{LVL} resistor configuration

Features

- Up to 3.2Gbps operation
- Low noise CML data outputs
- Chatter-Free LOS generation
- Open Collector TTL LOS output
- TTL /EN Input
- Differential PECL inputs for data
- Single 3.3V power supply
- Available in a tiny 10-pin (3mm x 3mm) MSOP

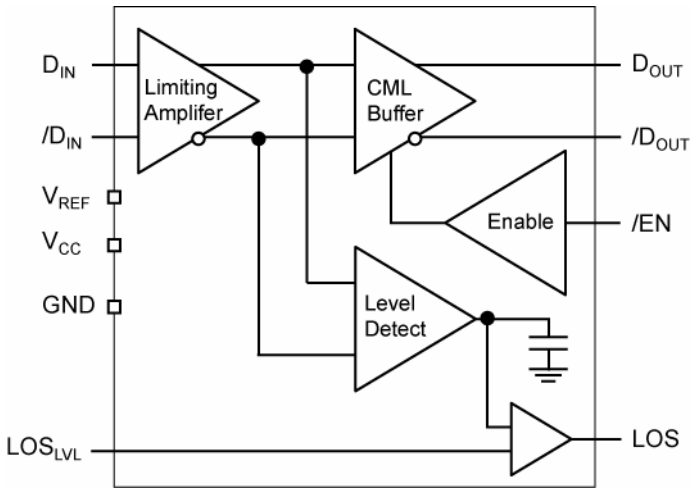
Applications

- PON
- SFP/SFF/GBIC optical transceivers
- Gigabit Ethernet
- 1X and 2X Fibre Channel
- SONET/SDH: OC 3/12/24/48 – STM 1/4/8/16
- Line driver and line receiver

Markets

- FTTX
- Datacom/Telecom

Block Diagram



Detailed Description

The SY88993AL is a high-sensitivity limiting post amplifier that operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as 4mV$_{PP}$ can be amplified. Figure 2 shows the allowed input voltage swing. The SY88993AL generates a LOS output. LOS$_{LVL}$ sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 3 shows a simplified schematic of the SY88993AL's input stage. The high-sensitivity of the input amplifier allows signals as small as 4mV$_{PP}$ to be detected and amplified. The input amplifier also allows input signals as large as 1800mV$_{PP}$. Input signals below 6mVpp are linearly amplified with a typical 38dB differential voltage gain. Since it is a limiting amplifier, the SY88993AL outputs typically 800mV$_{PP}$ voltage-limited waveforms for input signals that are greater than 10mV$_{PP}$. Applications requiring the SY88993AL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88993AL's input pins to ensure the best performance of the device.

Output Buffer

The SY88993AL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V$_{CC}$ for each output pin provides this. Figure 4 shows a simplified schematic of the output stage.

Loss-of-Signal

The SY88993AL generates a chatter-free LOS open-collector TTL output which requires an external pull-up resistor, as shown in Figure 1. LOS is used to determine that the input amplitude is large enough to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold sets by LOS$_{LVL}$ and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts the true output signal without removing the input signals. Typically, 5.6dB LOS hysteresis is provided to prevent chattering.

Loss-of-Signal Level Set

The SY88993AL incorporates a programmable level detect function to identify when the input signal has been lost. This information can be fed back to the /EN input of the device to maintain stability under loss of signal conditions. Using LOS$_{LVL}$ pin the sensitivity of the level detect can be adjusted. The LOS$_{LVL}$ voltage can be set by connection a resistor divider between V$_{CC}$ and V$_{REF}$, Figure 5.

Hysteresis

The SY88993AL typically provides 5.6dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88993AL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 5.6dB LOS hysteresis, a voltage factor of about 2 is required to assert or de-assert LOS.

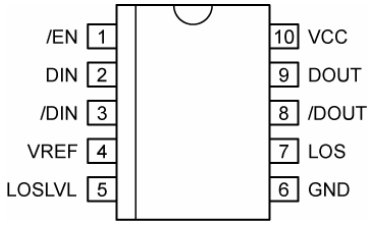
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88993ALKG	K10-1	Industrial	993L with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY88993ALKGTR[1]	K10-1	Industrial	993L with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Tape and reel.

Pin Configuration



10-Pin MSOP (K10-1)

Pin Description

Pin Number	Pin Name	Pin Function
1	/EN	TTL (Input): Output enable (Active Low).
2	DIN	Data (Input): Data input.
3	/DIN	Data (Input): Complementary data input.
4	VREF	Output: Reference voltage output for LOS Level Set (See Figure 3).
5	LOSLVL	Input: Loss-of-Signal Level Set
6	GND	Ground.
7	LOS	TTL Output (Open Collector): Loss-of-Signal indicator (Active High).
8	/DOUT	CML (Output): Inverting data output.
9	DOUT	CML (Output): Data output.
10	VCC	Power Supply: Positive power supply.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +4.0V
Input Voltage (DIN, /DIN) ..... 0V to V_{CC}
Lead Temperature (soldering, #sec.) ..... 260°C
Storage Temperature (T_s) ..... –55°C to +85°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance
MSOP (θ_{JA}) ..... 113°C/W
MSOP (ψ_{JB}) ..... 96°C/W

DC Electrical Characteristics

V_{CC} = +3.3V ±10%; R_{LOAD} = 50Ω to V_{CC}; T_A = -40°C to +85°C, unless noted. Typical values at Vcc = 3.3V, T_A = 25°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load.		40	55	mA
I_{OH}	LOS Output Leakage	V_{cc} = 3.6V			100	µA
LOS_{LVL}	LOSLVL Level		V_{REF}		V_{CC}	V
V_{OH}	Output HIGH Voltage		V_{CC}–20	V_{CC}–5	V_{CC}	mV
V_{OL}	Output LOW Voltage	Note 9	Vcc-350	V_{CC}–400	Vcc-475	mV
Z_O	Single-Ended Output Impedance	Note 10	40	50	60	Ω
V_{REF}	Reference Voltage		V_{CC}–1.38	V_{CC}–1.32	V_{CC}–1.26	V
$V_{OFFSEST}$	Differential Output Offset				±80	mV
V_{CMR}	Common Mode Range		GND ±2		V_{CC}–0.2	V

TTL DC Electrical Characteristics

V_{CC} = +3.3V ±10%; R_{LOAD} = 50Ω to V_{CC}; T_A = -40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	/EN Input HIGH Voltage		2.0			
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	-300			µA

Notes:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

AC Electrical Characteristics

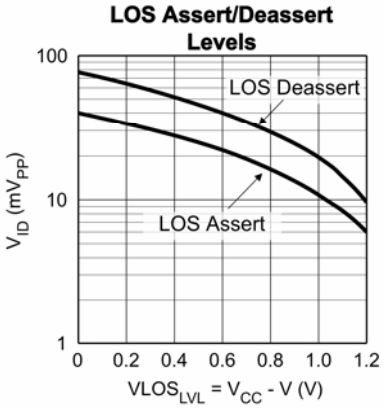
V_{CC} = +3.3V ±10%; R_{LOAD} = 50Ω to V_{CC}; T_A = -40°C to +85°C, unless noted.

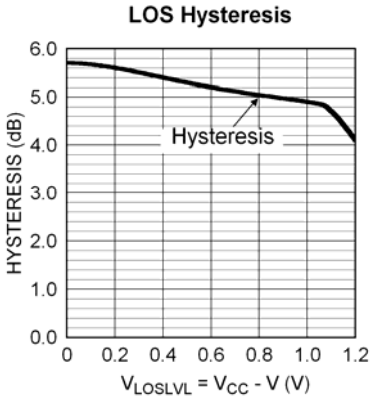
Symbol	Parameter	Condition	Min	Typ	Max	Units
LOS_{AH}	High LOS Assert Level	$V_{LOSLVL} = V_{CC}$	30	43		mV_{PP}
LOS_{DH}	High LOS De-assert Level	$V_{LOSLVL} = V_{CC}$		83	95	mV_{PP}
HYS_H	High LOS Hysteresis		2	5.6	8	dB
LOS_{AM}	Medium LOS Assert Level	$V_{LOSLVL} = V_{CC} - 400mV$	20	31		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	$V_{LOSLVL} = V_{CC} - 400mV$		55	65	mV_{PP}
HYS_M	Medium LOS Hysteresis		2	5.6	8	dB
LOS_{AL}	Low LOS Assert Level	$V_{LOSLVL} = V_{CC} - 800mV$	10	19		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	$V_{LOSLVL} = V_{CC} - 800mV$		31	45	mV_{PP}
HYS_L	Low LOS Hysteresis		2	5.6	8	dB
PSRR	Power Supply Rejection Ratio	Note 4		35		dB
t_{OFFL}	LOS Release Time Minimum Input	Note 5		0.1	0.5	µs
t_{OFFH}	LOS Release Time Maximum Input	Note 5		0.1	0.5	µs
t_{ONL}	LOS Assert Time	Note 5		0.2	0.5	µs
t_r, t_f	Differential Output Rise/Fall Time (20% to 80%)	Note 6		60	120	Ps
V_{ID}	Input Voltage Range		4		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	Note 7, 8, 9, 10	700	800	950	mV_{PP}
V_{SR}	LOS Sensitivity Range		4		50	mV_{PP}
$A_{V(Diff)}$	Differential Voltage Gain			38		DB
B_{-3dB}	3dB Bandwidth			2.5		GHz
S_{21}	Single-Ended Small Signal-Gain		26	32		dB

Notes:

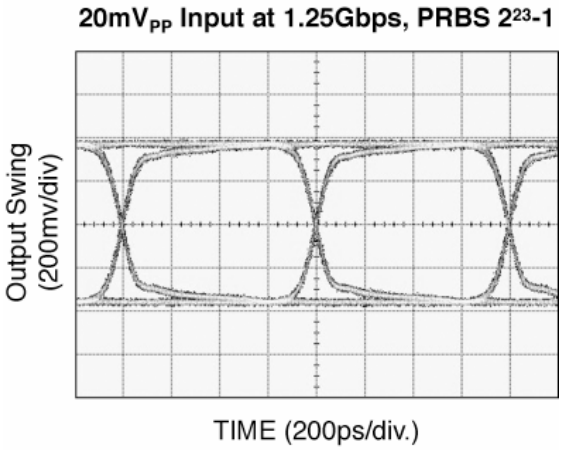
4. Input referred noise = RMS output noise/low frequency gain. Input referred, 55MHz.
5. Input is a 200MHz square wave, tr < 300ps.
6. With input signal V_{ID} > $50mV_{PP}$ with 50Ω load.
7. Input is a 200MHz square wave, tr < 300ps, 50Ω load.
8. VID > 10mVPP.
9. Output levels are based on 50Ω impedance. If the load impedance is different, the output level will be changed.
10. See output structure.

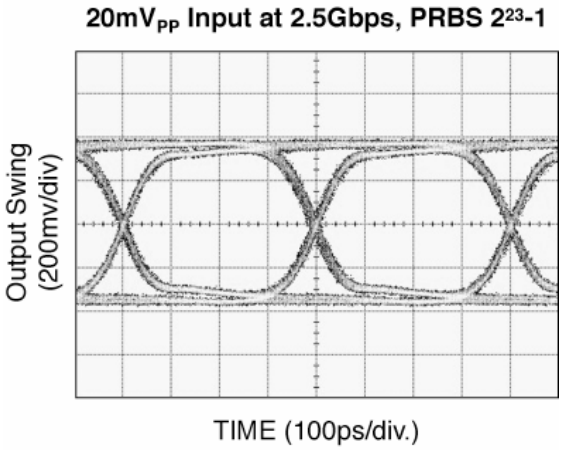
Typical Characteristics

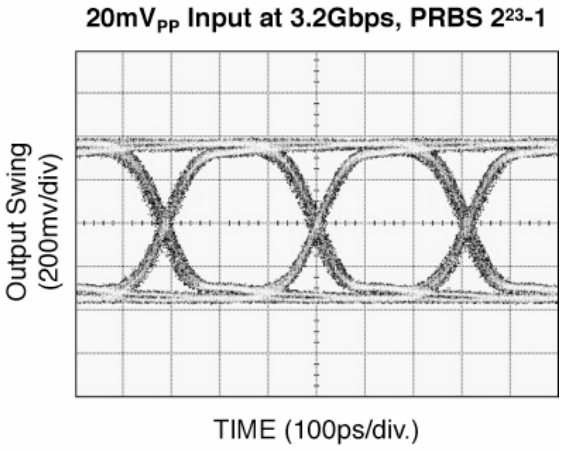


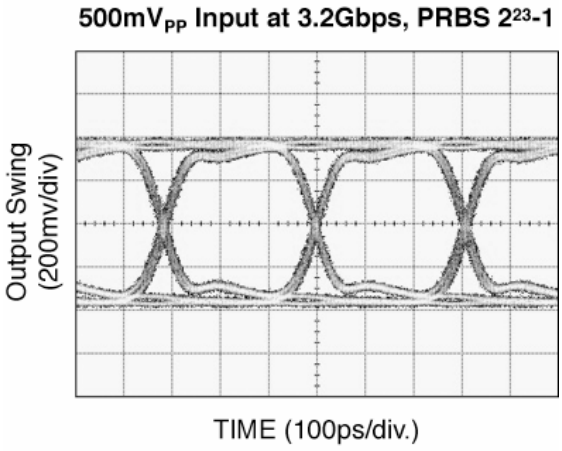


Functional Characteristics









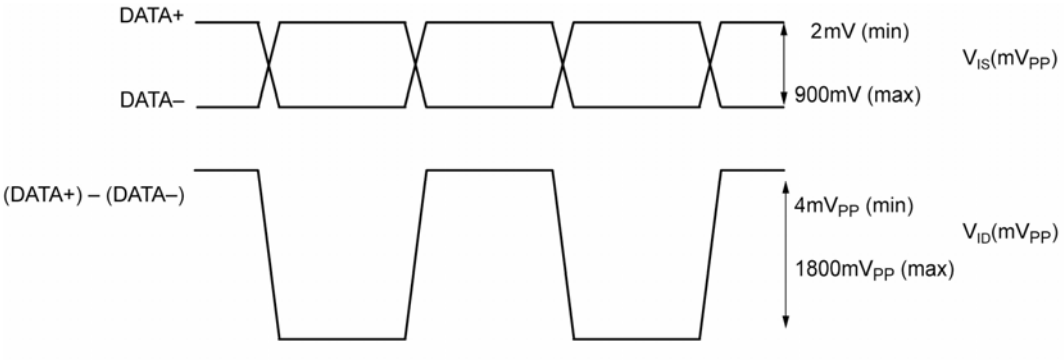


Figure 2. V_{IS} and V_{ID}

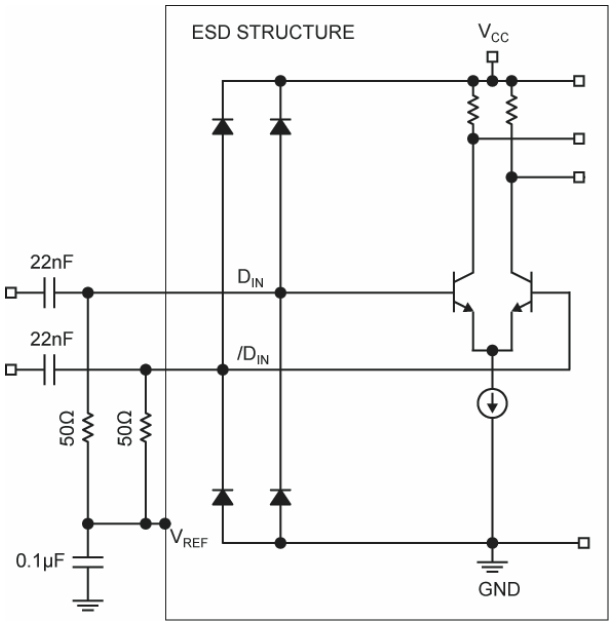


Figure 3. Differential Input Configuration

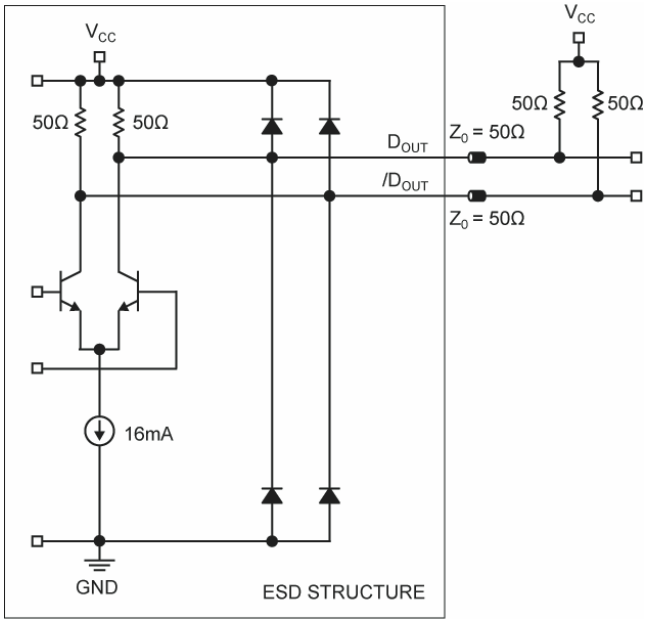


Figure 4. Differential Output Configuration

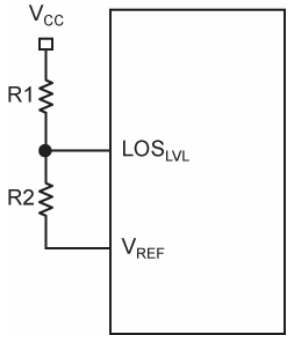
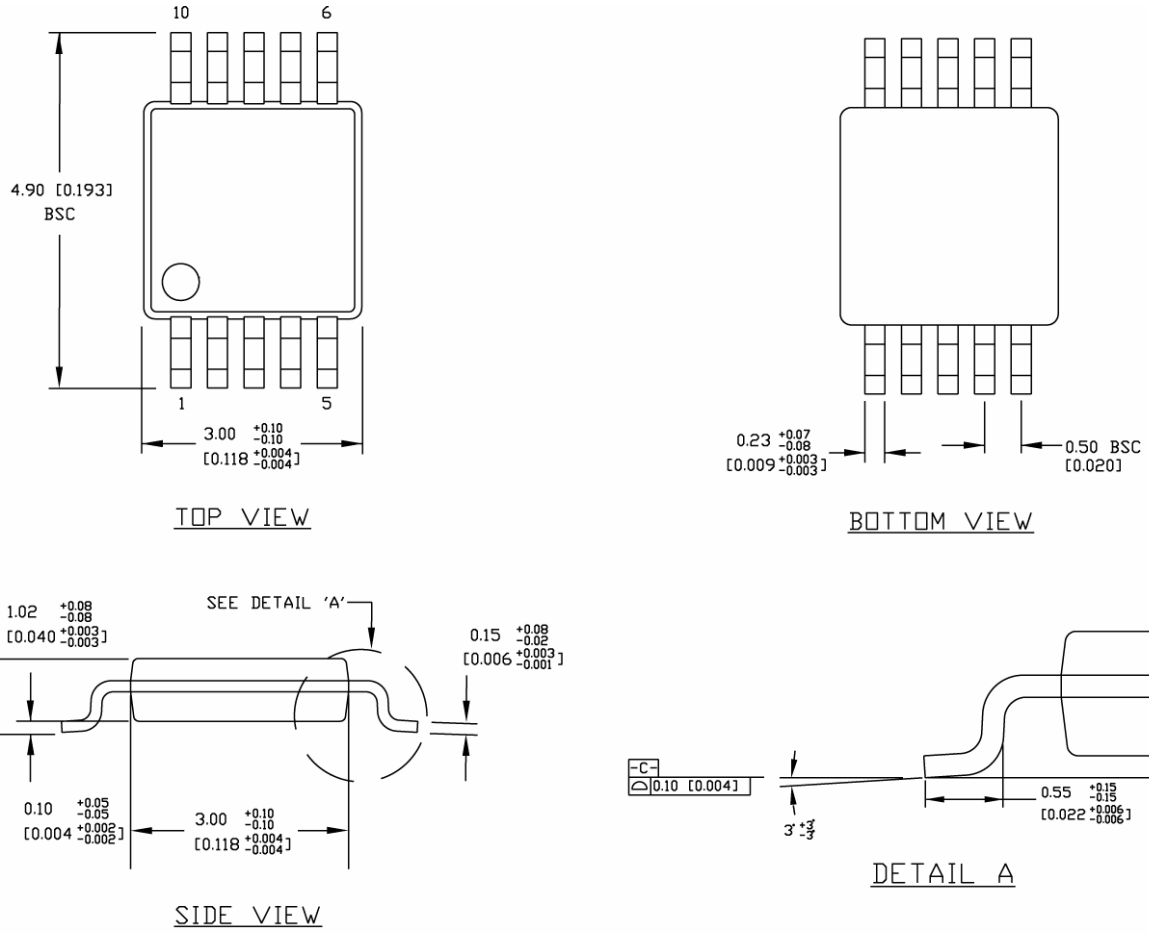


Figure 5. LOSLVL Circuit

Notes:

1. Resistor Divider = R2/ (R1 + R2)
2. R1 + R2 ≥ 5kΩ

Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

10-Pin MSOP (K10-1)

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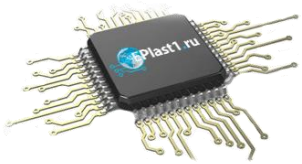

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