

FEATURES

- <0.5 pC charge injection over full signal range
- 2.5 pF off capacitance
- Low leakage; 0.6 nA maximum @ 85°C
- 120 Ω on resistance
- Fully specified at +12 V, ± 15 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 8-lead SOT-23 package

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio/video signal routing
- Communication systems

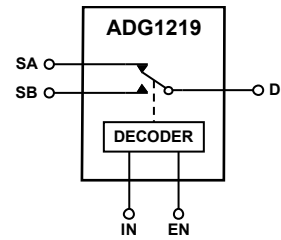
GENERAL DESCRIPTION

The ADG1219 is a monolithic *i*CMOS[®] device containing an SPDT switch. An EN input is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies. Each switch exhibits break-before-make switching action.

The *i*CMOS (industrial CMOS) modular manufacturing process combines high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and exceptionally low charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 0 INPUT

Figure 1.

06575-001

charge injection over the entire signal range of the device. *i*CMOS construction also ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

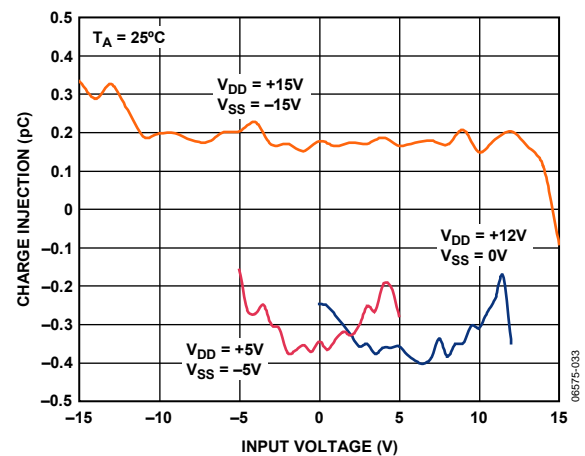


Figure 2. Charge Injection vs. Input Voltage

06575-033

Rev. A

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REVISION HISTORY

3/09—Rev. 0 to Rev. A

| | |
|--|----|
| Change to Power Requirements, I_{DD} Parameter, Table 1..... | 4 |
| Change to Power Requirements, I_{DD} Parameter, Table 2..... | 5 |
| Updated Outline Dimensions | 15 |

4/08—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

| Parameters | B Version ¹ | | | Unit | Test Conditions/Comments |
|---|------------------------|----------------|----------------------|-------------------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance, R_{ON} | 120 | | | Ω typ | $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 23 $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$ |
| | 200 | 240 | 270 | Ω max | |
| On Resistance Match Between Channels, ΔR_{ON} | 3.5 | | | Ω typ | |
| | 6 | 10 | 12 | Ω max | $V_S = -5\text{ V}$, 0 V , $+5\text{ V}$; $I_S = -1\text{ mA}$ |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 20 | | | Ω typ | |
| | 64 | 76 | 84 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.004 | | | nA typ | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24 |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.009 | | | nA typ | $V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24 |
| | ± 0.1 | ± 0.6 | ± 1 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.02 | | | nA typ | $V_S = V_D = \pm 10\text{ V}$; see Figure 25 |
| | ± 0.2 | ± 0.6 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | $V_{IN} = V_{INL}$ or V_{INH} |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | | μA typ | |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | | |
| Transition Time, $t_{TRANSITION}$ | 140 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 30 |
| | 170 | 200 | 230 | ns max | |
| t_{ON} (EN) | 85 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 30 |
| | 105 | 130 | 140 | ns max | |
| t_{OFF} (EN) | 105 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 30 |
| | 125 | 150 | 170 | ns max | |
| Break-Before-Make Time Delay, t_{BBM} | 40 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 31 |
| | | | 10 | ns min | |
| Charge Injection | 0.1 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | 77 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26 |
| Channel-to-Channel Crosstalk | 80 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27 |
| Total Harmonic Distortion + Noise | 0.15 | | | % typ | $R_L = 10\text{ k}\Omega$, 5 V rms , $f = 20\text{ Hz}$ to 20 kHz $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28 |
| -3 dB Bandwidth | 520 | | | MHz typ | |
| C_S (Off) | 2.5 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |
| | 3.3 | | | pF max | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |
| C_D (Off) | 4.3 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |
| | 5.1 | | | pF max | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |
| C_D , C_S (On) | 7.5 | | | pF typ | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |
| | 10 | | | pF max | $f = 1\text{ MHz}$; $V_S = 0\text{ V}$ |

ADG1219

| Parameters | B Version ¹ | | | Unit | Test Conditions/Comments |
|--------------------|------------------------|----------------|------------------|--|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| POWER REQUIREMENTS | | | | | $V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ |
| I_{DD} | 0.001 | | 1.0 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 0 V or V_{DD} |
| I_{DD} | 140 | | 190 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 5 V |
| I_{SS} | 0.001 | | 1.0 | $\mu\text{A typ}$ $\mu\text{A max}$ | Digital inputs = 0 V, 5 V or V_{DD} |
| V_{DD}/V_{SS} | | | $\pm 5/\pm 16.5$ | V min/max | $ V_{DD} = V_{SS} $ |

¹ Temperature range for B version is -40°C to +125°C.

² Guaranteed by design; not subject to production test.

SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameters | B Version ¹ | | | Unit | Test Conditions/Comments |
|---|------------------------|----------------|-----------------|--|--|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance, R_{ON} | 300 | | | $\Omega\text{ typ}$ | $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$; see Figure 23 |
| On Resistance Match Between Channels, ΔR_{ON} | 4.5 | 567 | 625 | $\Omega\text{ max}$ $\Omega\text{ typ}$ | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V to }10\text{ V}$, $I_S = -1\text{ mA}$ |
| On Resistance Flatness, $R_{FLAT(ON)}$ | 16 | 26 | 27 | $\Omega\text{ max}$ $\Omega\text{ typ}$ | $V_S = 3\text{ V, }6\text{ V, }9\text{ V}$, $I_S = -1\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | $V_{DD} = 13.2\text{ V}$ |
| Source Off Leakage, I_S (Off) | ± 0.006 | | | nA typ nA max | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24 |
| Drain Off Leakage, I_D (Off) | ± 0.006 | ± 0.6 | ± 1 | nA typ nA max | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24 |
| Channel On Leakage, I_D , I_S (On) | ± 0.02 | ± 0.6 | ± 1 | nA typ nA max | $V_S = V_D = 1\text{ V or }10\text{ V}$; see Figure 25 |
| Channel On Leakage, I_D , I_S (On) | ± 0.2 | ± 0.6 | ± 1 | nA typ nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.001 | | | $\mu\text{A typ}$ $\mu\text{A max}$ | $V_{IN} = V_{INL}$ or V_{INH} |
| Digital Input Capacitance, C_{IN} | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS ² | | | | | |
| Transition Time, $t_{TRANSITION}$ | 195 | | | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30 |
| t_{ON} (EN) | 120 | 300 | 340 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30 |
| t_{OFF} (EN) | 145 | 190 | 210 | ns typ ns max | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 30 |
| Break-Before-Make Time Delay, t_{BBM} | 70 | 220 | 255 | ns typ ns min | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 31 |
| Charge Injection | -0.8 | | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | 80 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26 |
| Channel-to-Channel Crosstalk | 80 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27 |
| -3 dB Bandwidth | 400 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28 |

| Parameters | B Version ¹ | | | Unit | Test Conditions/Comments |
|--------------------------------------|------------------------|----------------|-----------------|-----------|---|
| | 25°C | -40°C to +85°C | -40°C to +125°C | | |
| C _S (Off) | 2.9 | | | pF typ | f = 1 MHz; V _S = 6 V |
| | 3.7 | | | pF max | f = 1 MHz; V _S = 6 V |
| C _D (Off) | 5 | | | pF typ | f = 1 MHz; V _S = 6 V |
| | 5.8 | | | pF max | f = 1 MHz; V _S = 6 V |
| C _D , C _S (On) | 8.5 | | | pF typ | f = 1 MHz; V _S = 6 V |
| | 11 | | | pF max | f = 1 MHz; V _S = 6 V |
| POWER REQUIREMENTS | | | | | V _{DD} = 13.2 V |
| I _{DD} | 0.001 | | | μA typ | Digital inputs = 0 V or V _{DD} |
| | | | 1.0 | μA max | |
| I _{DD} | 140 | | | μA typ | Digital inputs = 5 V |
| | | | 190 | μA max | |
| V _{DD} | | | 5/16.5 | V min/max | V _{SS} = 0 V, GND = 0 V |

¹ Temperature range for B version is -40°C to +125°C.

² Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|--|
| V _{DD} to V _{SS} | 35 V |
| V _{DD} to GND | -0.3 V to +25 V |
| V _{SS} to GND | +0.3 V to -25 V |
| Analog Inputs ¹ | V _{SS} - 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to V _{DD} + 0.3 V or 30 mA, whichever occurs first |
| Peak Current, S or D | 100 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current per Channel, S or D | 30 mA |
| Operating Temperature Range Industrial (B Version) | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| 8-Lead SOT-23, θ _{JA} Thermal Impedance | 211.5°C/W |
| Reflow Soldering Peak Temperature, Pb Free | 260°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

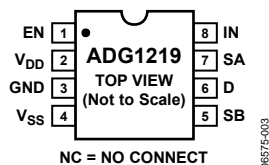


Figure 3. SOT-23 Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|--|
| 1 | EN | Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the IN logic input determines which switch is turned on. |
| 2 | V _{DD} | Most Positive Power Supply Potential. |
| 3 | GND | Ground (0 V) Reference. |
| 4 | V _{SS} | Most Negative Power Supply Potential. |
| 5 | SB | Source Terminal. Can be an input or output. |
| 6 | D | Drain Terminal. Can be an input or output. |
| 7 | SA | Source Terminal. Can be an input or output. |
| 8 | IN | Logic Control Input. |

Table 5. Truth Table

| EN | IN | Switch A | Switch B |
|----|----|----------|----------|
| 0 | X | Off | Off |
| 1 | 0 | On | Off |
| 1 | 1 | Off | On |

TYPICAL PERFORMANCE CHARACTERISTICS

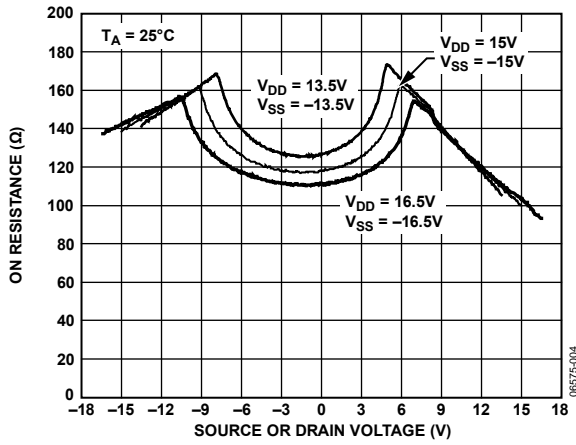


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

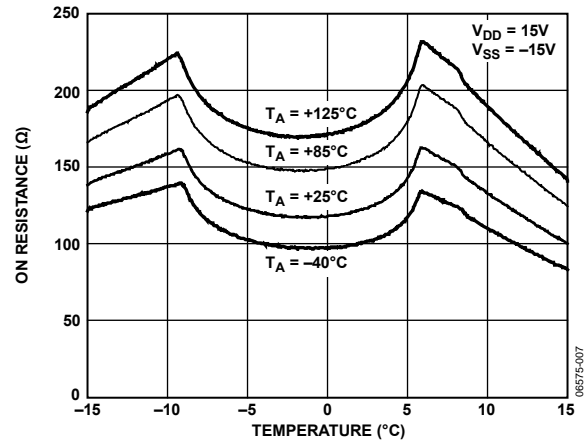


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

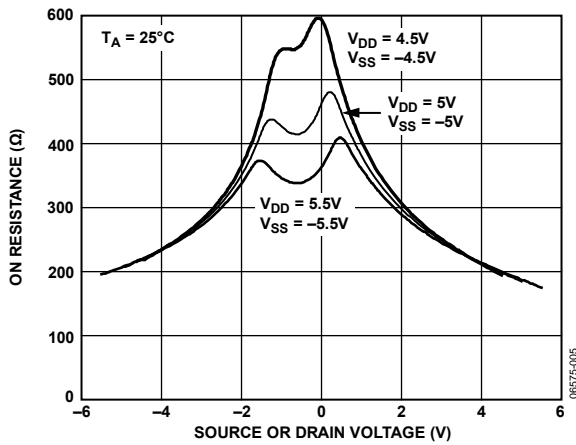


Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

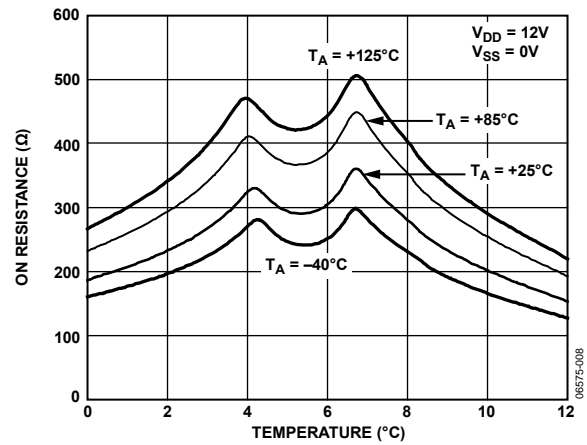


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

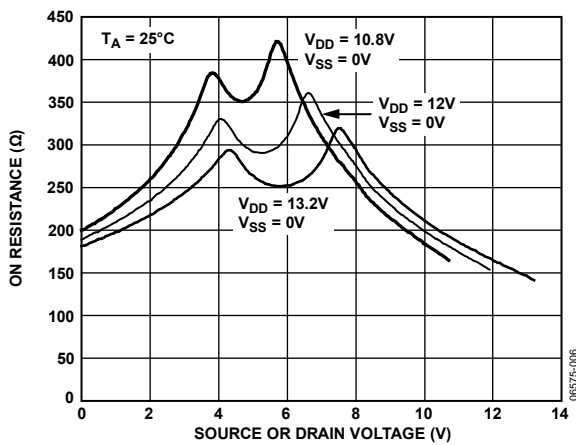


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

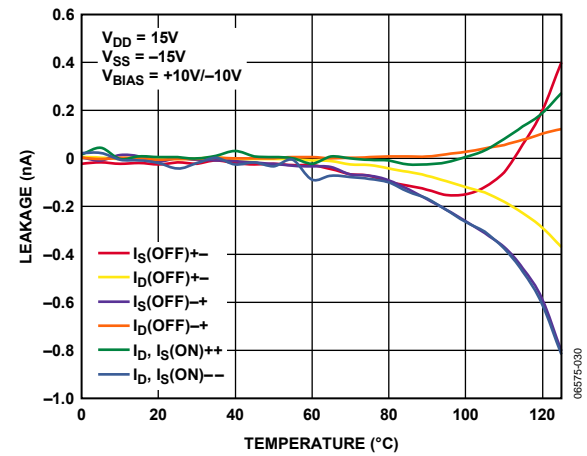


Figure 9. Leakage Currents as a Function of Temperature, 15 V Dual Supply

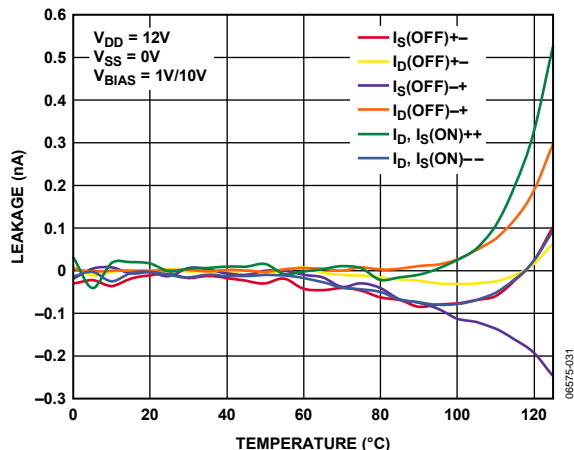


Figure 10. Leakage Currents as a Function of Temperature, 12 V Single Supply

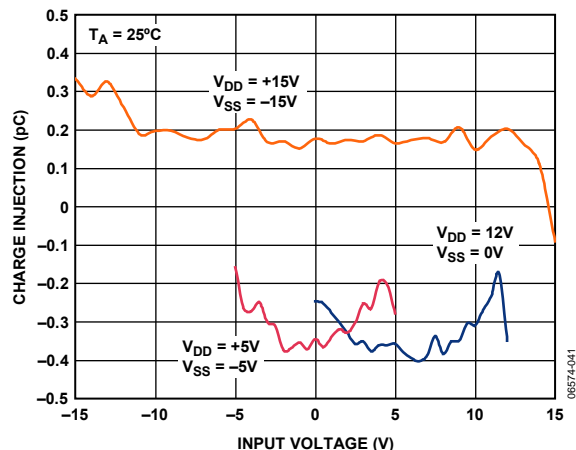


Figure 13. Charge Injection vs. Input Voltage

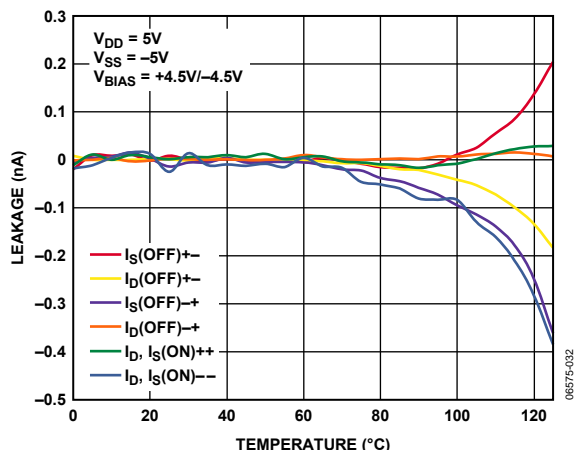


Figure 11. Leakage Currents as a Function of Temperature, 5 V Dual Supply

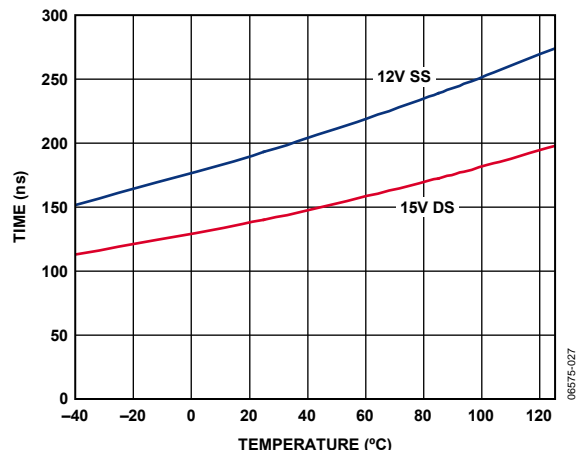


Figure 14. $t_{\text{TRANSITION}}$ Time vs. Temperature

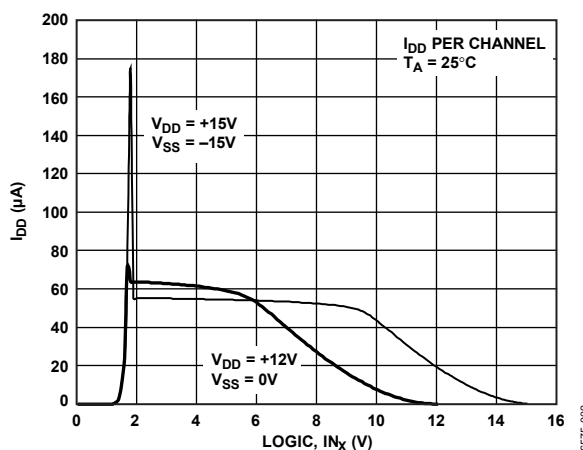


Figure 12. I_{DD} vs. Logic Level

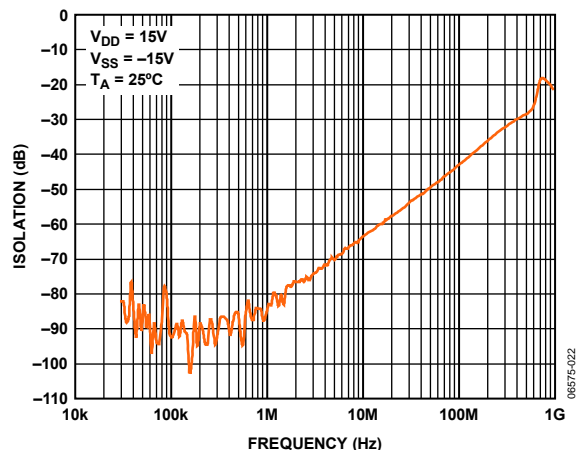


Figure 15. Off Isolation vs. Frequency

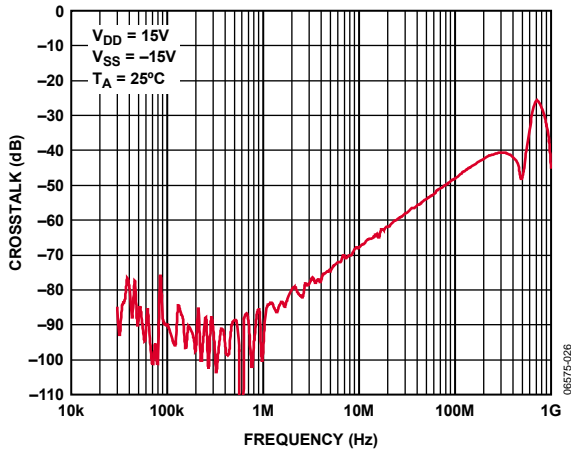


Figure 16. Crosstalk vs. Frequency

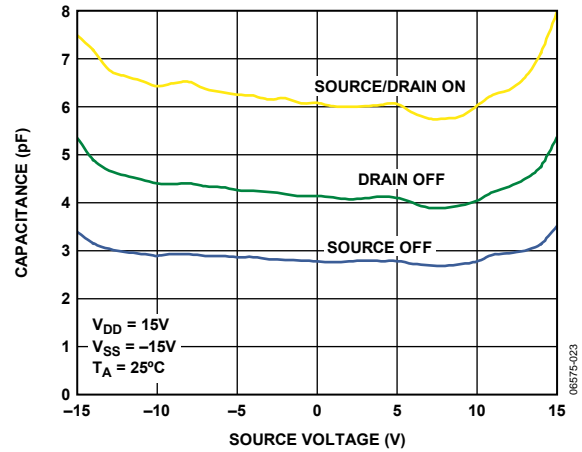


Figure 19. Capacitance vs. Source Voltage for Dual Supply

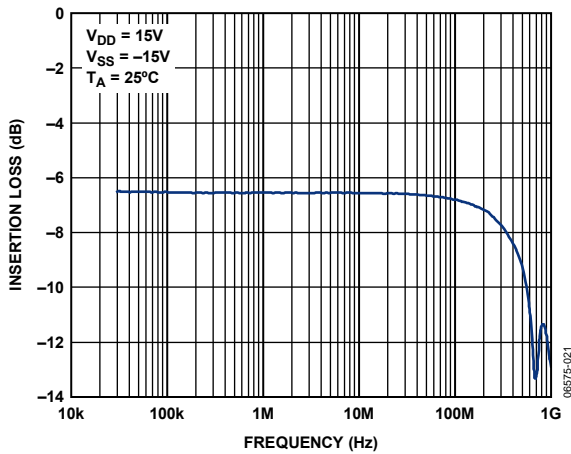


Figure 17. On Response vs. Frequency

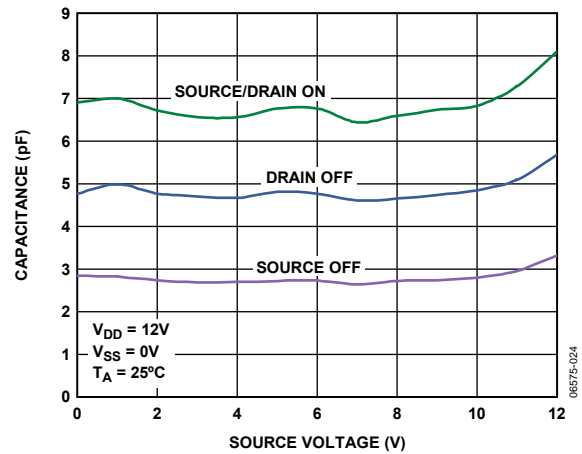


Figure 20. Capacitance vs. Source Voltage for Single Supply

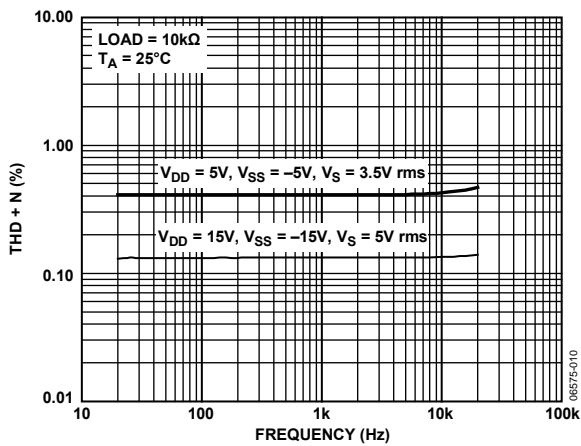


Figure 18. THD + N vs. Frequency

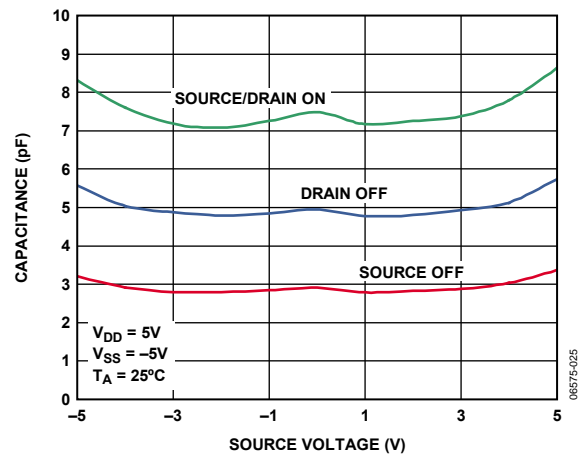


Figure 21. Capacitance vs. Source Voltage for Dual Supply

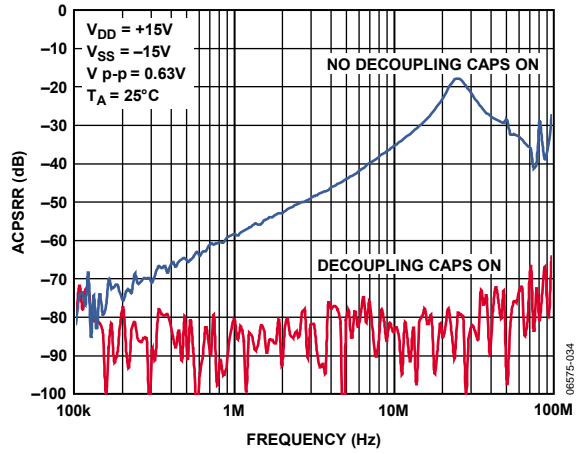


Figure 22. ACPSRR vs. Frequency

TEST CIRCUITS

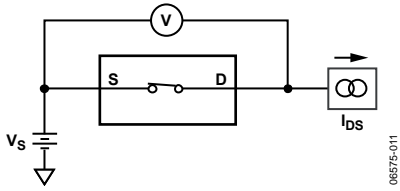


Figure 23. On Resistance

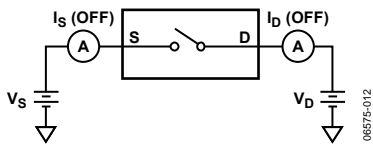


Figure 24. Off Leakage

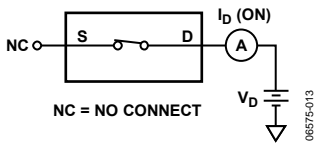
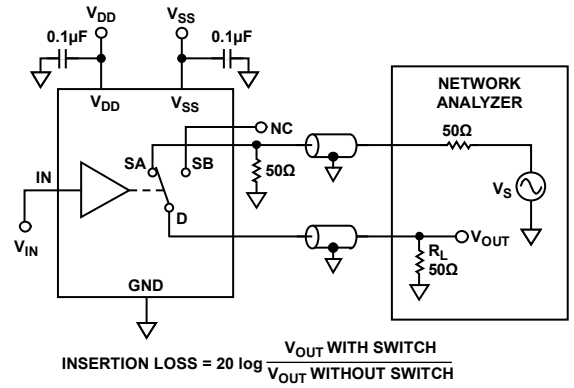
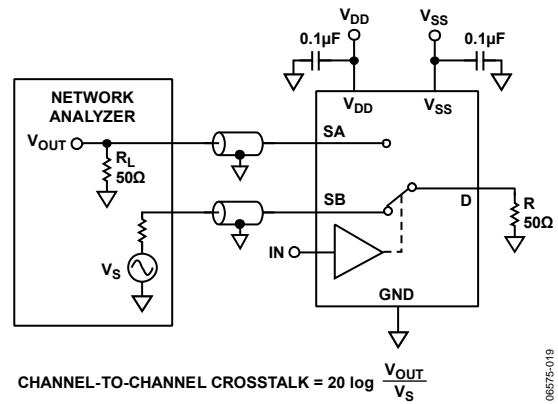


Figure 25. On Leakage



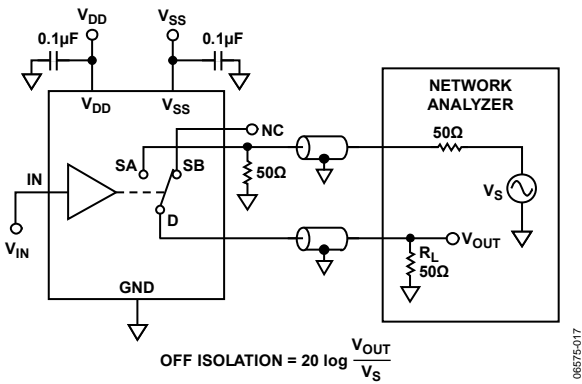
$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 27. Channel-to-Channel Crosstalk



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 28. Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

Figure 26. Off Isolation

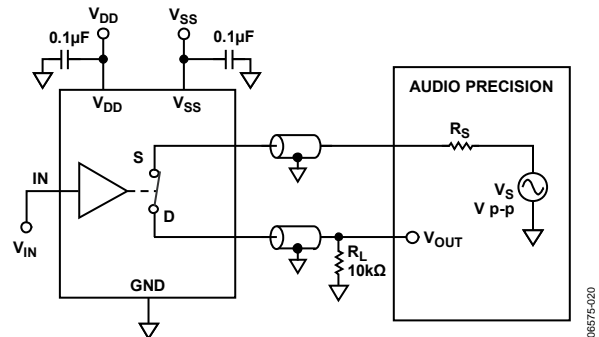


Figure 29. THD + Noise

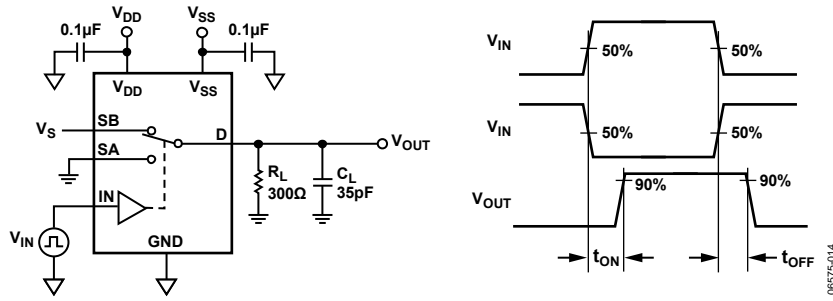


Figure 30. Switching Times

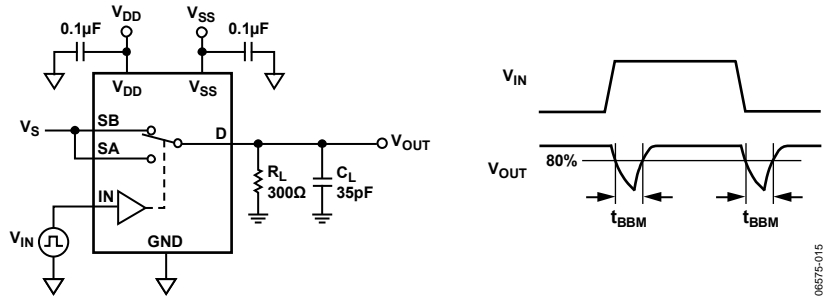


Figure 31. Break-Before-Make Time Delay

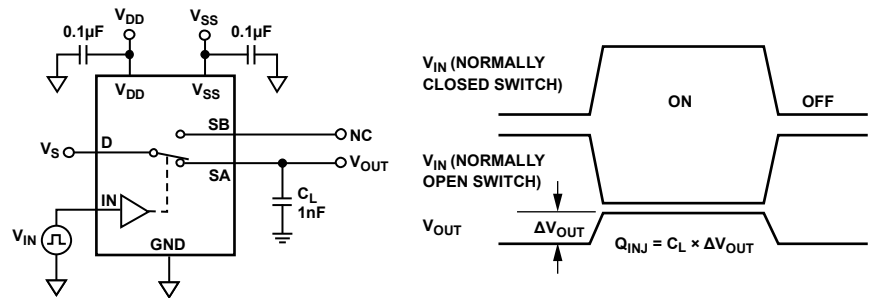


Figure 32. Charge Injection

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, measured with reference to ground.

C_D (Off)

The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON} (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANSITION}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

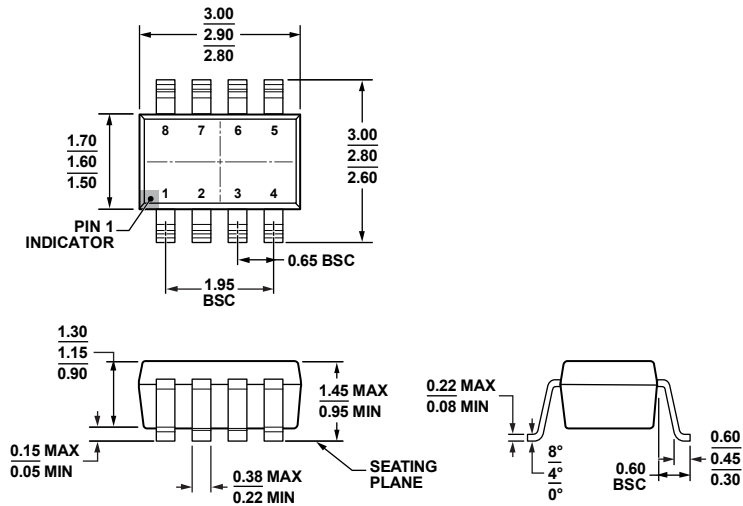
Total Harmonic Distortion (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 33. 8-Lead Lead Small Outline Transistor Package [SOT-23] (RJ-8)

Dimensions shown in millimeters

121608-A

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|-------------------------------|-------------------|---|----------------|----------|
| ADG1219BRJZ-R2 ¹ | -40°C to +125°C | 8-Lead Lead Small Outline Transistor Package [SOT-23] | RJ-8 | S24 |
| ADG1219BRJZ-REEL ¹ | -40°C to +125°C | 8-Lead Lead Small Outline Transistor Package [SOT-23] | RJ-8 | S24 |

¹ Z = RoHS Compliant Part.

ADG1219

NOTES



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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