

# 500mA, Low Quiescent Current, Ultra-Low Noise, High PSRR Low-Dropout Linear Regulator

Check for Samples: [TPS735xx](#)

## FEATURES

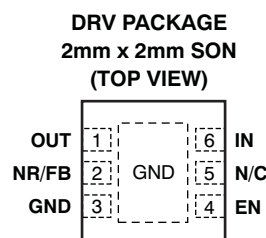
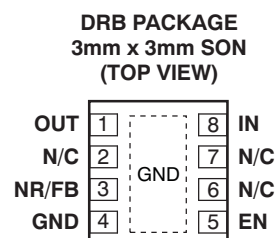
- 500mA Low Dropout Regulator with EN
- Low  $I_Q$ : 46 $\mu$ A
- Multiple Output Voltage Versions Available:
  - Fixed Outputs of 1.0V to 4.3V Using Innovative Factory EEPROM Programming
  - Adjustable Outputs from 1.25V to 6.0V
- High PSRR: 60dB at 1kHz
- Ultra-low Noise: 28 $\mu$ V<sub>RMS</sub>
- Fast Start-Up Time: 45 $\mu$ s
- Stable with a Low-ESR, 2.0 $\mu$ F Typical Output Capacitance
- Excellent Load/Line Transient Response
- 2% Overall Accuracy (Load/Line/Temp,  $V_{OUT} > 2.2V$ )
- Very Low Dropout: 280mV at 500mA
- 2mm × 2mm SON-6 and 3mm × 3mm SON-8 Packages

## APPLICATIONS

- WiFi, WiMax
- Printers
- Cellular Phones, SmartPhones
- Handheld Organizers, PDAs

## DESCRIPTION

The TPS735xx family of low-dropout (LDO), low-power linear regulators offers excellent ac performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 46 $\mu$ A (typical) ground current. The TPS735xx is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a typical dropout voltage of 250mV at 500mA output. The TPS735xx uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% ( $V_{OUT} > 2.2V$ ) over all load, line, process, and temperature variations. It is fully specified from  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  and is offered in low-profile, 2mm x 2mm SON and 3mm x 3mm SON packages that are ideal for wireless handsets, printers, and WLAN cards.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2011, Texas Instruments Incorporated



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TPS735xx yyy z	<b>XX</b> is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). <b>YYY</b> is package designator. <b>Z</b> is package quantity.

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Output voltages from 1.0V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted).<sup>(1)</sup>

PARAMETER	TPS735xx	UNIT
V <sub>IN</sub> range	–0.3 to +7.0	V
V <sub>EN</sub> range	–0.3 to V <sub>IN</sub> +0.3	V
V <sub>OUT</sub> range	–0.3 to V <sub>IN</sub> +0.3	V
V <sub>FB</sub> range	–0.3 to V <sub>FB</sub> (TYP) +0.3	V
Peak output current	Internally limited	
Continuous total power dissipation	See <a href="#">Thermal Information</a> table	
Junction temperature range, T <sub>J</sub>	–55 to +150	°C
Storage temperature range, T <sub>STG</sub>	–55 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS735xx <sup>(2)</sup>		UNITS
		DRB	DRV <sup>(3)</sup>	
		8 PINS	6 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(4)</sup>	47.8	50.2	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(5)</sup>	83	59	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(6)</sup>	N/A	N/A	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(7)</sup>	2.1	0.1	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(8)</sup>	17.8	30.1	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance <sup>(9)</sup>	12.1	8.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953A](#).

(2) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

- (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.  
ii. DRV: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array. Due to size limitation of thermal pad, 0.8-mm pitch array is used which is off the JEDEC standard.
- (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.  
ii. DRV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
- (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the [Power Dissipation](#) and [Estimating Junction Temperature](#) sections of this data sheet.

(3) Power dissipation may limit operating range.

(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(7) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain  $\theta_{JA}$  using a procedure described in JESD51-2a (sections 6 and 7).

(8) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain  $\theta_{JA}$  using a procedure described in JESD51-2a (sections 6 and 7).

(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$  or  $2.7\text{V}$ , whichever is greater;  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. For TPS73501,  $V_{OUT} = 3.0\text{V}$ . Typical values are at  $T_J = +25^{\circ}\text{C}$ .

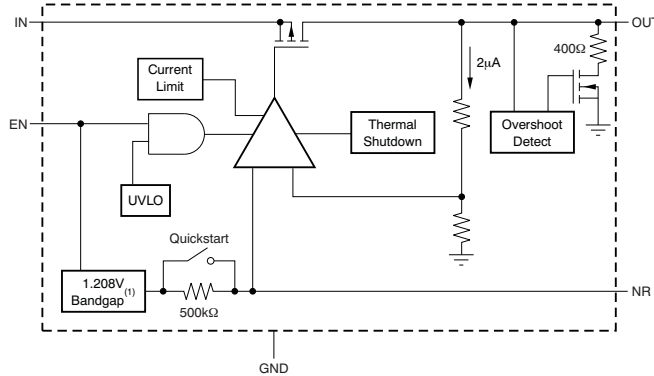
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IN</sub>	Input voltage range <sup>(1)</sup>			2.7		6.5	V
V <sub>FB</sub>	Internal reference (TPS73501)			1.184	1.208	1.232	V
V <sub>OUT</sub>	Output voltage range (TPS73501)			V <sub>FB</sub>		6.0	V
V <sub>OUT</sub>	Output accuracy	Nominal	T <sub>J</sub> = +25°C	−1.0		+1.0	%
V <sub>OUT</sub>	Output accuracy <sup>(1)</sup>	DRB package over V <sub>IN</sub> , I <sub>OUT</sub> , Temp	V <sub>OUT</sub> + 0.3V ≤ V <sub>IN</sub> ≤ V <sub>OUT</sub> > 6.5V 1mA ≤ I <sub>OUT</sub> ≤ 500mA, V <sub>OUT</sub> > 2.2V	−2.0	±1.0	+2.0	%
			V <sub>OUT</sub> + 0.3V ≤ V <sub>IN</sub> ≤ 6.5V 1mA ≤ I <sub>OUT</sub> ≤ 500mA, V <sub>OUT</sub> ≤ 2.2V	−3.0	±1.0	+3.0	%
		DRV package over V <sub>IN</sub> , I <sub>OUT</sub> , Temp	V <sub>OUT</sub> + 0.3V ≤ V <sub>IN</sub> ≤ V <sub>OUT</sub> + 3.0V, V <sub>IN</sub> ≤ 6.5V 1mA ≤ I <sub>OUT</sub> ≤ 500mA, V <sub>OUT</sub> > 2.2V	−2.0	±1.0	+2.0	%
			V <sub>OUT</sub> + 0.3V ≤ V <sub>IN</sub> ≤ V <sub>OUT</sub> + 3.0V, V <sub>IN</sub> ≤ 6.5V 1mA ≤ I <sub>OUT</sub> ≤ 500mA, V <sub>OUT</sub> ≤ 2.2V	−3.0	±1.0	+3.0	%
ΔV <sub>OUT</sub> %/ ΔV <sub>IN</sub>	Line regulation <sup>(1)</sup>		V <sub>OUT(NOM)</sub> + 0.3V ≤ V <sub>IN</sub> ≤ 6.5V		0.02		%/V
ΔV <sub>OUT</sub> %/ ΔI <sub>OUT</sub>	Load regulation		500μA ≤ I <sub>OUT</sub> ≤ 500mA		0.005		%/mA
V <sub>DO</sub>	Dropout voltage <sup>(2)</sup> (V <sub>IN</sub> = V <sub>OUT(NOM)</sub> − 0.1V)		I <sub>OUT</sub> = 500mA		280	500	mV
I <sub>CL</sub>	Output current limit		V <sub>OUT</sub> = 0.9 × V <sub>OUT(NOM)</sub> V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 0.9V, V <sub>IN</sub> ≥ 2.7V	800	1170	1720	mA
I <sub>GND</sub>	Ground pin current		500μA ≤ I <sub>OUT</sub> ≤ 500mA		45	65	μA
I <sub>SHDN</sub>	Shutdown current (I <sub>GND</sub> )		V <sub>EN</sub> ≤ 0.4V		0.15	1.0	μA
I <sub>FB</sub>	Feedback pin current (TPS73501)			−0.5		0.5	μA
PSRR	Power-supply rejection ratio V <sub>IN</sub> = 3.85V, V <sub>OUT</sub> = 2.85V, C <sub>NR</sub> = 0.01μF, I <sub>OUT</sub> = 100mA		f = 100Hz		60		dB
			f = 1kHz		56		dB
			f = 10kHz		41		dB
			f = 100kHz		28		dB
V <sub>N</sub>	Output noise voltage BW = 10Hz to 100kHz, V <sub>OUT</sub> = 2.8V		C <sub>NR</sub> = 0.01μF		11 x V <sub>OUT</sub>		μV <sub>RMS</sub>
			C <sub>NR</sub> = none		95 x V <sub>OUT</sub>		μV <sub>RMS</sub>
T <sub>STR</sub>	Startup time, V <sub>OUT</sub> = 0% to 90% V <sub>OUT</sub> = 2.85V, R <sub>L</sub> = 14Ω, C <sub>OUT</sub> = 2.2μF		C <sub>NR</sub> = none		45		μs
			C <sub>NR</sub> = 0.001μF		45		μs
			C <sub>NR</sub> = 0.01μF		50		μs
			C <sub>NR</sub> = 0.047μF		50		μs
V <sub>EN(HI)</sub>	Enable high (enabled)			1.2		V <sub>IN</sub>	V
V <sub>EN(LO)</sub>	Enable low (shutdown)			0		0.4	V
I <sub>EN(HI)</sub>	Enable pin current, enabled		V <sub>EN</sub> = V <sub>IN</sub> = 6.5V		0.03	1.0	μA
T <sub>SD</sub>	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		°C
T <sub>J</sub>	Operating junction temperature			−40		+125	°C
UVLO	Under-voltage lock-out		V <sub>IN</sub> rising	1.90	2.20	2.65	V
	Hysteresis		V <sub>IN</sub> falling		70		mV

(1) Minimum  $V_{IN} = V_{OUT} + V_{DO}$  or  $2.7\text{V}$ , whichever is greater.

(2)  $V_{DO}$  is not measured for devices with  $V_{OUT(NOM)} < 2.8\text{V}$  because minimum  $V_{IN} = 2.7\text{V}$ .

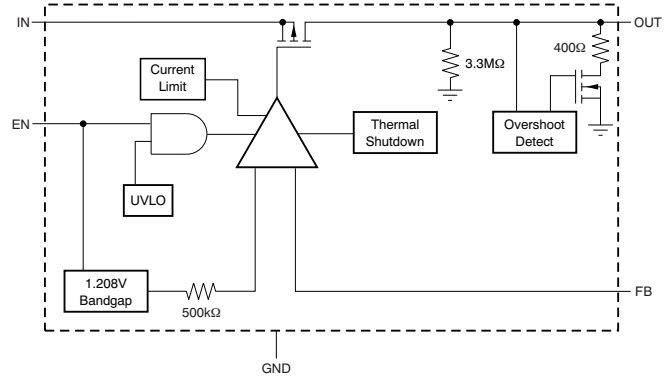
## DEVICE INFORMATION

### FUNCTIONAL BLOCK DIAGRAMS



NOTE (1): Fixed voltage versions between 1.0V to 1.2V have a 1.0V bandgap circuit instead of a 1.208V bandgap circuit.

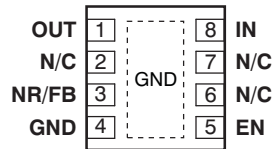
**Figure 1. Fixed Voltage Versions**



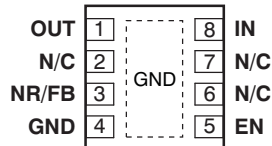
**Figure 2. Adjustable Voltage Versions**

## PIN CONFIGURATIONS

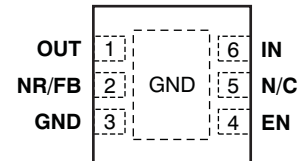
### DRB PACKAGE 3mm × 3mm SON-6 (TOP VIEW)



### DRB PACKAGE 3mm × 3mm SON-6 (TOP VIEW)



### DRV PACKAGE 2mm × 2mm SON-6 (TOP VIEW)



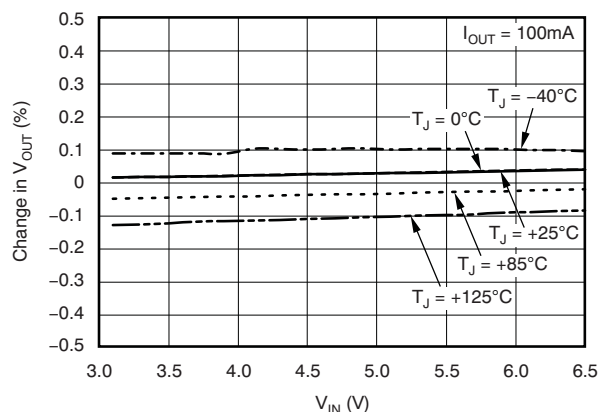
## PIN DESCRIPTIONS

TPS735xx			DESCRIPTION
NAME	DRV	DRB	
IN	6	8	Input supply.
GND	3, Pad	4	Ground. The pad must be tied to GND.
EN	4	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	2	3	Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels.
FB	2	3	Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	1	1	Output of the regulator. A small capacitor (total typical capacitance $\geq 2.0\mu\text{F}$ ceramic) is needed from this pin to ground to assure stability.
N/C	5	2, 6, 7	Not internally connected. This pin must either be left open, or tied to GND.

## TYPICAL CHARACTERISTICS

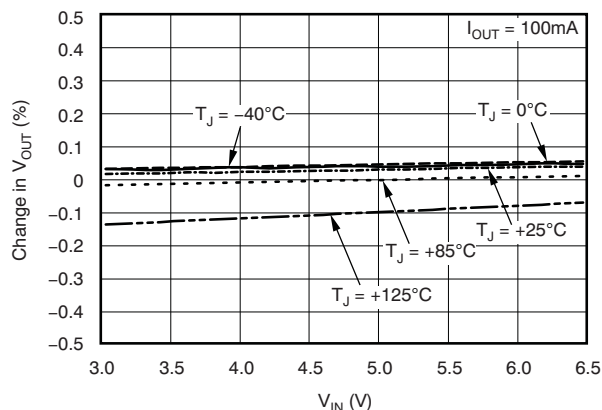
Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$  or  $2.7\text{V}$ , whichever is greater;  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. For TPS73501,  $V_{OUT} = 2.8\text{V}$ . The TPS73525 is used as the evaluation target of the fixed-voltage option in this datasheet. However, this voltage option may not be released. Check the Package Option Addendum at the end of this document for the availability of the 2.5V version. Typical values are at  $T_J = +25^\circ\text{C}$ .

**TPS73501 LINE REGULATION**



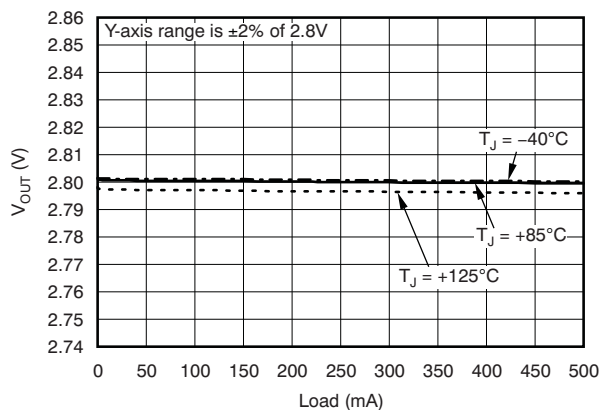
**Figure 3.**

**TPS73525 LINE REGULATION**



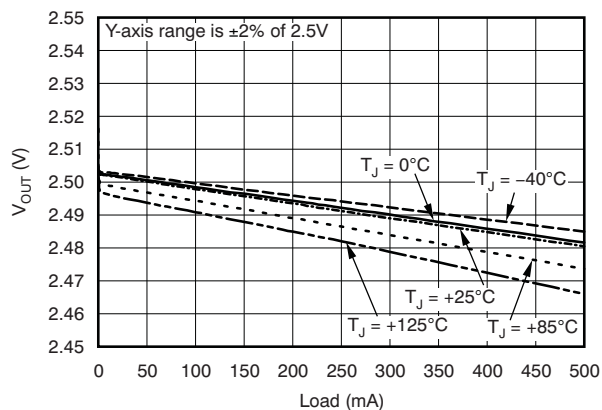
**Figure 4.**

**TPS73501 LOAD REGULATION**



**Figure 5.**

**TPS73525 LOAD REGULATION**



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$  or  $2.7\text{V}$ , whichever is greater;  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. For TPS73501,  $V_{OUT} = 2.8\text{V}$ . The TPS73525 is used as the evaluation target of the fixed-voltage option in this datasheet. However, this voltage option may not be released. Check the Package Option Addendum at the end of this document for the availability of the 2.5V version. Typical values are at  $T_J = +25^\circ\text{C}$ .

**TPS73525 GROUND PIN CURRENT vs  
OUTPUT CURRENT**

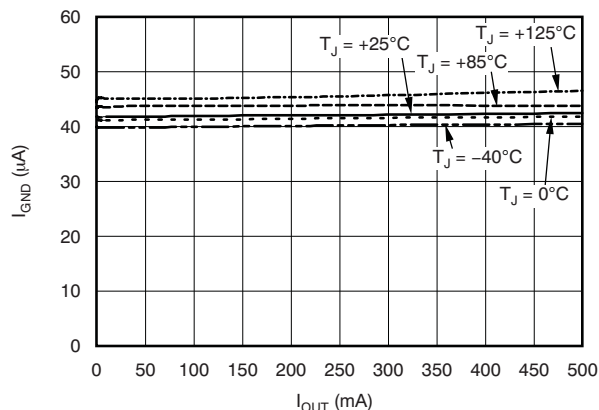


Figure 7.

**TPS73525 GROUND PIN CURRENT (DISABLE) vs  
TEMPERATURE**

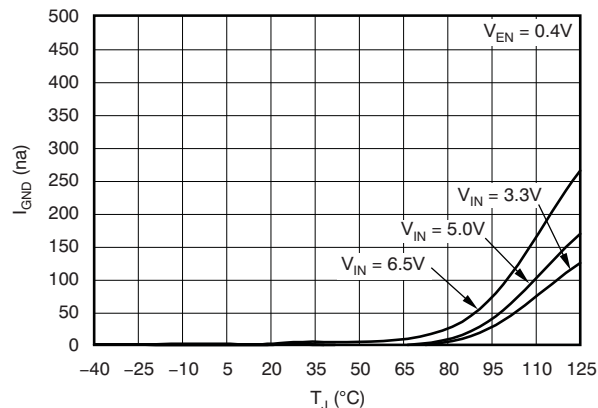


Figure 8.

**TPS73501 DROPOUT VOLTAGE vs  
OUTPUT CURRENT**

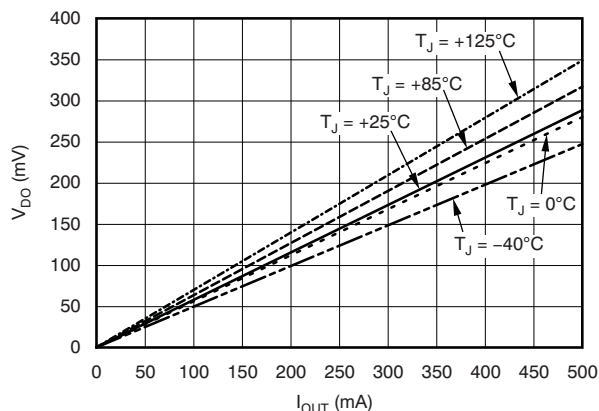


Figure 9.

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY  
( $V_{IN} - V_{OUT} = 1.0\text{V}$ )**

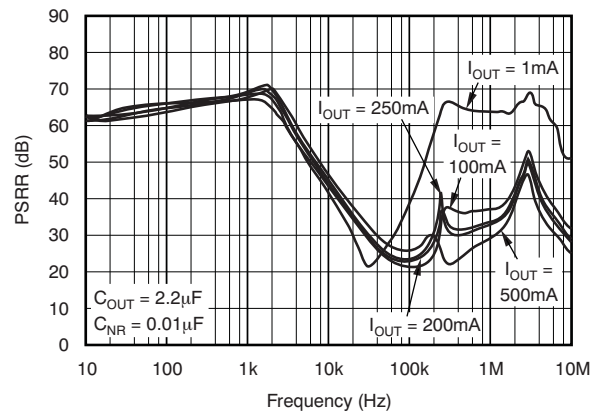


Figure 10.

### TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$  or  $2.7\text{V}$ , whichever is greater;  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. For TPS73501,  $V_{OUT} = 2.8\text{V}$ . The TPS73525 is used as the evaluation target of the fixed-voltage option in this datasheet. However, this voltage option may not be released. Check the Package Option Addendum at the end of this document for the availability of the 2.5V version. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY**  
( $V_{IN} - V_{OUT} = 0.5\text{V}$ )

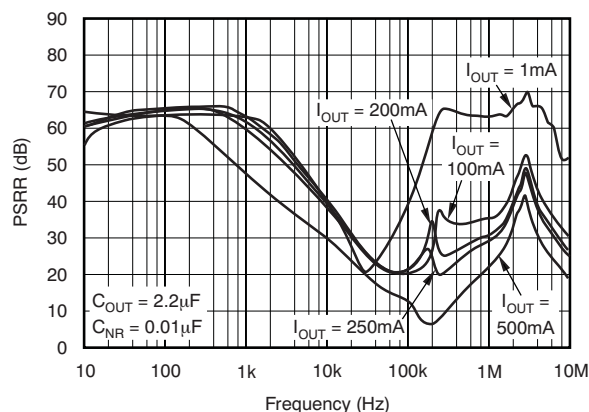


Figure 11.

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY**  
( $V_{IN} - V_{OUT} = 0.3\text{V}$ )

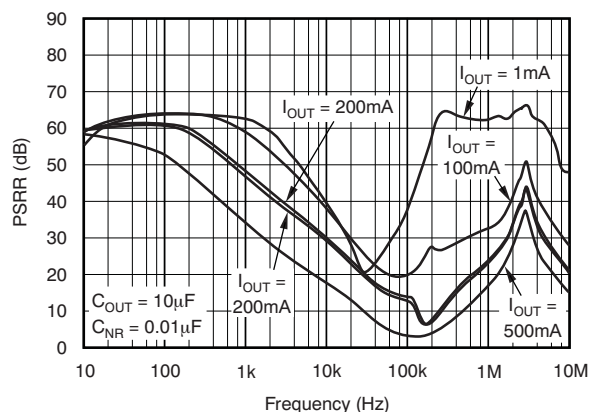


Figure 12.

**TPS73525**  
**TOTAL NOISE vs  $C_{NR}$**

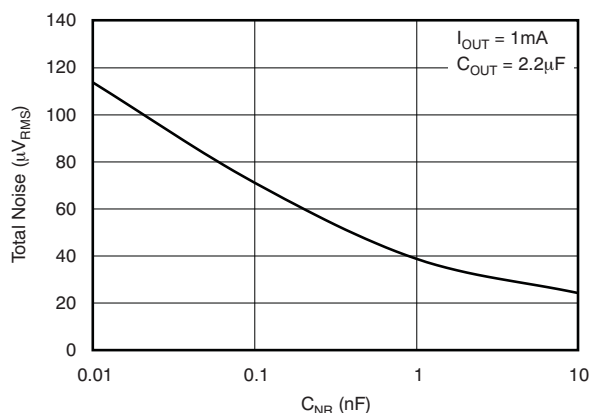


Figure 13.

**TPS73525**  
**TOTAL NOISE vs  $C_{OUT}$**

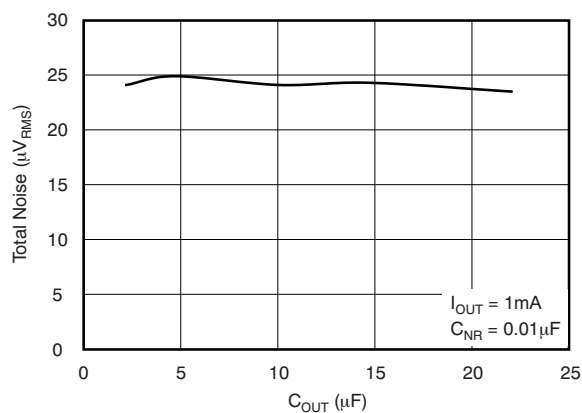


Figure 14.



## TYPICAL CHARACTERISTICS (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$  or  $2.7\text{V}$ , whichever is greater;  $I_{OUT} = 1\text{mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 2.2\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. For TPS73501,  $V_{OUT} = 2.8\text{V}$ . The TPS73525 is used as the evaluation target of the fixed-voltage option in this datasheet. However, this voltage option may not be released. Check the Package Option Addendum at the end of this document for the availability of the 2.5V version. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

**TPS73525**  
**TURN-ON RESPONSE**  
( $V_{IN} = V_{EN}$ )

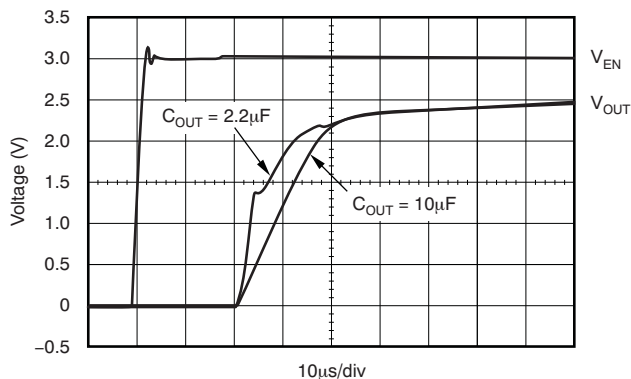


Figure 15.

**TPS73525**  
**EN RESPONSE OVER STABLE  $V_{IN}$**

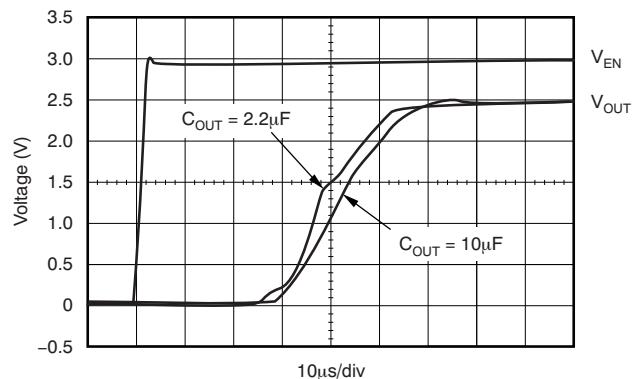


Figure 16.

**TPS73525**  
**POWER-UP/POWER-DOWN**  
( $V_{IN} = V_{EN}$ )

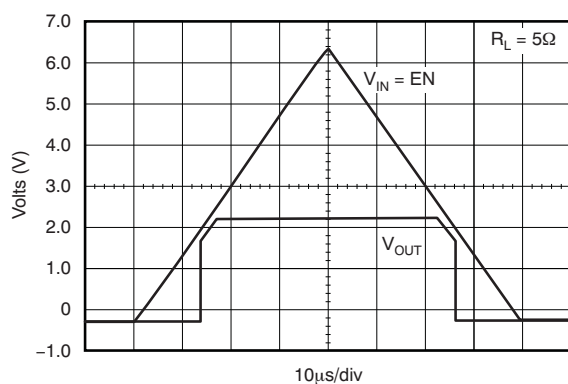


Figure 17.

**TPS73525 LOAD TRANSIENT RESPONSE**

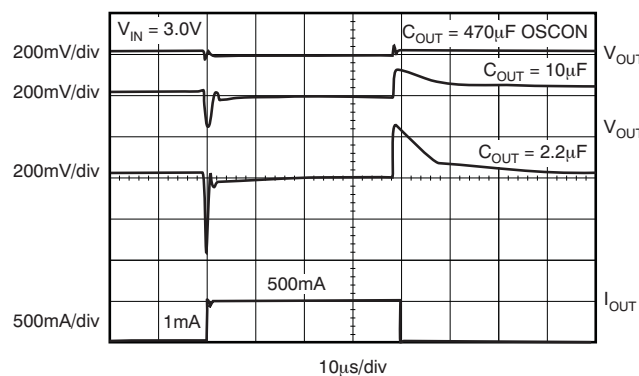


Figure 18.

**TPS73525 LINE TRANSIENT RESPONSE**

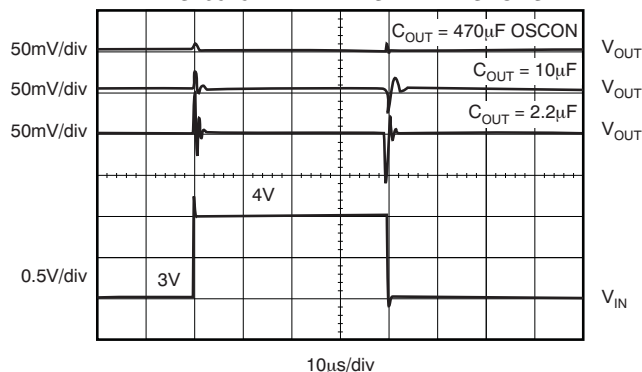
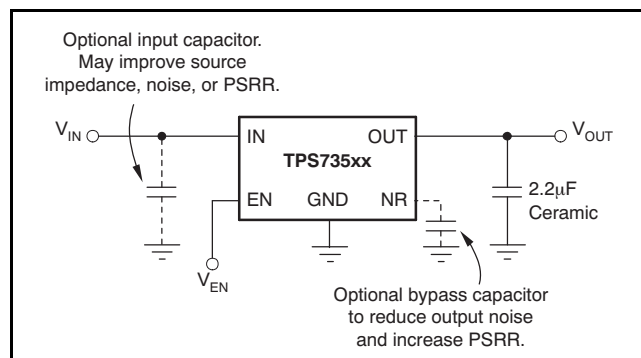


Figure 19.

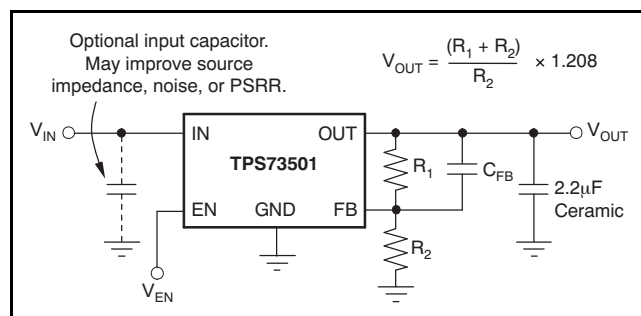
## APPLICATION INFORMATION

The TPS735xx family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom ( $V_{IN} - V_{OUT}$ ). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS735xx an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Figure 20 shows the basic circuit connections for fixed voltage models. Figure 21 gives the connections for the adjustable output version (TPS73501).  $R_1$  and  $R_2$  can be calculated for any output voltage using the formula in Figure 21.



**Figure 20. Typical Application Circuit for Fixed Voltage Versions**



**Figure 21. Typical Application Circuit for Adjustable Voltage Versions**

### Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a  $0.1\mu\text{F}$  to  $1\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of  $0.1\mu\text{F}$  is enough in this condition. When it is difficult to place these two ground points close together, a  $1\mu\text{F}$  capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a  $0.1\mu\text{F}$  input capacitor may be necessary to ensure stability.

The TPS735xx is designed to be stable with standard ceramic output capacitors of values  $2.2\mu\text{F}$  or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be  $< 1.0\Omega$ , so output capacitor type should be either ceramic or conductive polymer electrolytic.

### Feedback Capacitor Requirements (TPS73501 only)

The feedback capacitor,  $C_{FB}$ , shown in Figure 21 is required for stability. For a parallel combination of  $R_1$  and  $R_2$  equal to  $250\text{k}\Omega$ , any value from  $3\text{pF}$  to  $1\text{nF}$  can be used. Fixed voltage versions have an internal  $30\text{pF}$  feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below  $5\text{pF}$  should be used to ensure fast startup; values above  $47\text{pF}$  can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS73501 is stable in unity-gain configuration (OUT tied to FB) without  $C_{FB}$ .

### Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor ( $C_{NR}$ ) is used with the TPS735xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a  $0.01\mu\text{F}$  noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives  $2\mu\text{A}$  of divider current has the same noise performance as a fixed voltage version. To further

optimize noise, equivalent series resistance of the output capacitor can be set to approximately  $0.2\Omega$ . This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with  $C_{NR} = 0.01\mu\text{F}$ , total noise is given approximately by [Equation 1](#):

$$V_N = \frac{11\mu\text{V}_{\text{RMS}}}{V} \times V_{\text{OUT}} \quad (1)$$

The TPS73501 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

### Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

### Internal Current Limit

The TPS735xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS735xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

### Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

### Dropout Voltage

The TPS735xx uses a PMOS pass transistor to achieve low dropout. When  $(V_{\text{IN}} - V_{\text{OUT}})$  is less than the dropout voltage ( $V_{\text{DO}}$ ), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the  $R_{\text{DS, ON}}$  of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout,  $V_{\text{DO}}$  approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{\text{IN}} - V_{\text{OUT}})$  approaches dropout. This effect is shown in the [Typical Characteristics](#) section.

### Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS735xx use a quick-start circuit to fast-charge the noise reduction capacitor,  $C_{NR}$ , if present (see the [Functional Block Diagrams](#)). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage  $C_{NR}$  capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup,  $V_{\text{IN}}$  should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the [Typical Characteristics](#) section. The quick-start switch is closed for approximately  $135\mu\text{s}$ . To ensure that  $C_{NR}$  is fully charged during the quick-start time, a  $0.01\mu\text{F}$  or smaller capacitor should be used.

### Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding  $C_{\text{FB}}$  between OUT and FB improves stability and transient response. The transient response of the TPS735xx is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a  $400\Omega$  resistor to ground.

### Undervoltage Lock-Out (UVLO)

The TPS735xx utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than  $50\mu\text{s}$  duration.

### Minimum Load

The TPS735xx is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of  $500\mu\text{A}$  is required. Below  $500\mu\text{A}$  at junction temperatures near  $+125^\circ\text{C}$ , the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately  $50\mu\text{A}$ . In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

## Thermal Information

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS735xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS735xx into thermal shutdown degrades device reliability.

### Package Mounting

Solder pad footprint recommendations for the TPS735xx are available from the Texas Instruments web site at [www.ti.com](http://www.ti.com).

### Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

**Note:** When the device is used in a condition of higher input and lower output voltages with the DRV and DRB packages,  $P_D$  exceeds the package rating at room temperature. This equation shows an example of the DRB package:

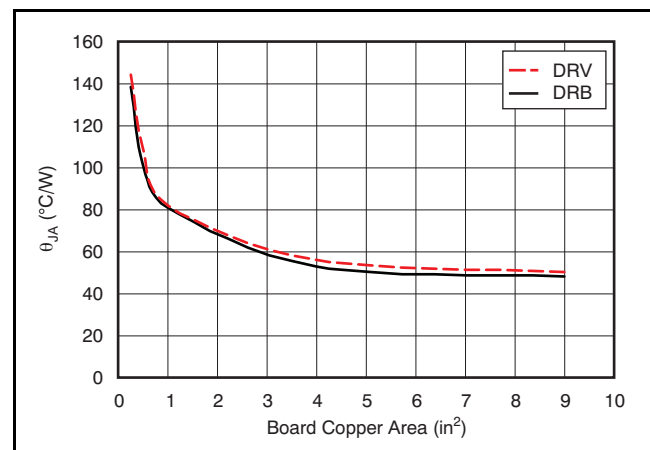
$$P_D = (6.5V - 1.0V) \times 500mA = 2.75W, \text{ which is greater than } 2.5W \text{ at } +25^\circ C.$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On both SON (DRB) and SON (DRV) packages, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using [Equation 3](#):

$$R_{\theta JA} = \frac{(+125^\circ C - T_A)}{P_D} \quad (3)$$

Knowing the maximum  $R_{\theta JA}$ , the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using [Figure 22](#).



Note:  $\theta_{JA}$  value at board size of 9in<sup>2</sup> (that is, 3in × 3in) is a JEDEC standard.

**Figure 22.  $\theta_{JA}$  vs Board Size**

[Figure 22](#) shows the variation of  $\theta_{JA}$  as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

**NOTE:** When the device is mounted on an application PCB, it is strongly recommended to use  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the [Estimating Junction Temperature](#) section.

## ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in [Equation 4](#)). For backwards compatibility, an older  $\theta_{JC,Top}$  parameter is listed as well.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

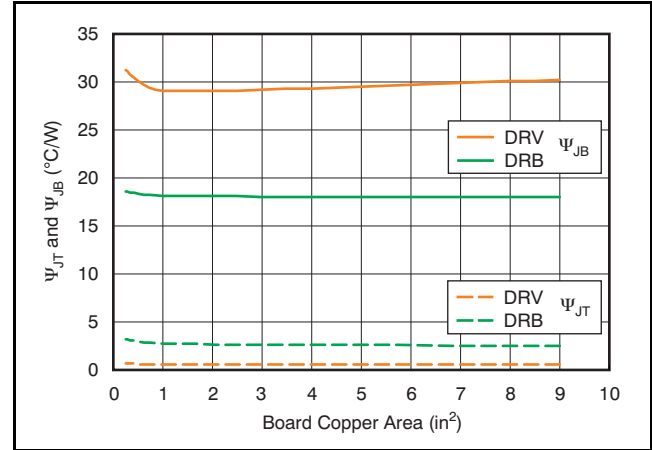
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D \quad (4)$$

Where  $P_D$  is the power dissipation shown by [Equation 2](#),  $T_T$  is the temperature at the center-top of the IC package, and  $T_B$  is the PCB temperature measured 1mm away from the IC package on the PCB surface (as [Figure 24](#) shows).

**NOTE:** Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

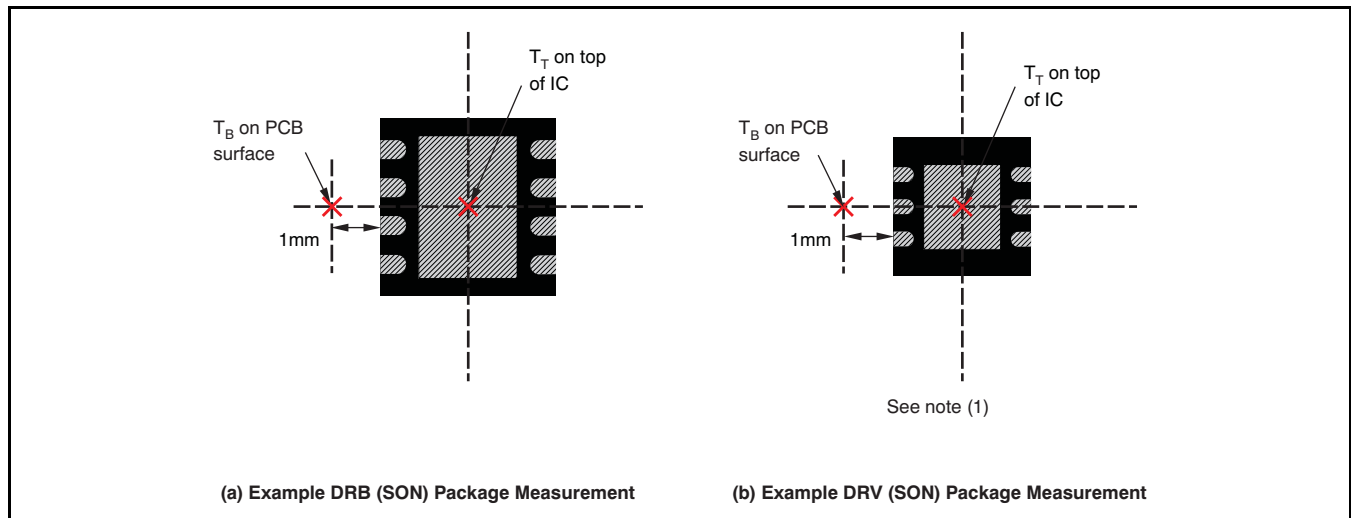
For more information about measuring  $T_T$  and  $T_B$ , see the application note [SBVA025, Using New Thermal Metrics](#), available for download at [www.ti.com](http://www.ti.com).

By looking at [Figure 23](#), the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with [Equation 4](#) is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.



**Figure 23.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size**

For a more detailed discussion of why TI does not recommend using  $\theta_{JC(top)}$  to determine thermal characteristics, refer to application report [SBVA025, Using New Thermal Metrics](#), available for download at [www.ti.com](http://www.ti.com). For further information, refer to application report [SPRA953, IC Package Thermal Metrics](#), also available on the TI website.



(1) Power dissipation may limit operating range. Check [Thermal Information](#) table.

**Figure 24. Measuring Points for  $T_T$  and  $T_B$**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

---

Changes from Revision I (April, 2011) to Revision J	Page
---	------

---

- |  |    |
|--|----|
| • Replaced the <i>Dissipation Ratings</i> table with the <i>Thermal Information</i> table .....                | 3  |
| • Revised conditions for Typical Characteristics to include statement about TPS73525 device availability ..... | 6  |
| • Updated <a href="#">Power Dissipation</a> section .....  | 12 |
| • Added <a href="#">Estimating Junction Temperature</a> section .....  | 13 |
- 

Changes from Revision H (November, 2009) to Revision I	Page
--	------

---

- |  |   |
|--|---|
| • Corrected typo in <a href="#">Electrical Characteristics</a> table for $V_{OUT}$ specification, DRV package test conditions, $V_{OUT} \leq 2.2V$ ..... | 4 |
|--|---|
-



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS73501DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK	<a href="#">Samples</a>
TPS73501DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBK	<a href="#">Samples</a>
TPS73501DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDR	<a href="#">Samples</a>
TPS73501DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDR	<a href="#">Samples</a>
TPS73512DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT	<a href="#">Samples</a>
TPS73512DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QTT	<a href="#">Samples</a>
TPS73515DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH	<a href="#">Samples</a>
TPS73515DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QWH	<a href="#">Samples</a>
TPS73525DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	<a href="#">Samples</a>
TPS73525DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	<a href="#">Samples</a>
TPS73525DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	<a href="#">Samples</a>
TPS73525DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CBM	<a href="#">Samples</a>
TPS73525DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSW	<a href="#">Samples</a>
TPS73525DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NSW	<a href="#">Samples</a>
TPS73527DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK	<a href="#">Samples</a>
TPS73527DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAK	<a href="#">Samples</a>
TPS735285DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAW	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS735285DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAW	<a href="#">Samples</a>
TPS73533DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY	<a href="#">Samples</a>
TPS73533DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CVY	<a href="#">Samples</a>
TPS73533DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVY	<a href="#">Samples</a>
TPS73533DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CVY	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

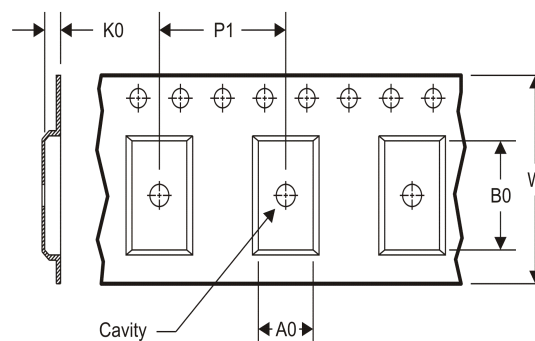
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73501DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73501DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73501DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73512DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73512DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73515DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73525DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73525DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73527DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73527DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS735285DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73533DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73533DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73533DRVR	SON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS73533DRVT	SON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

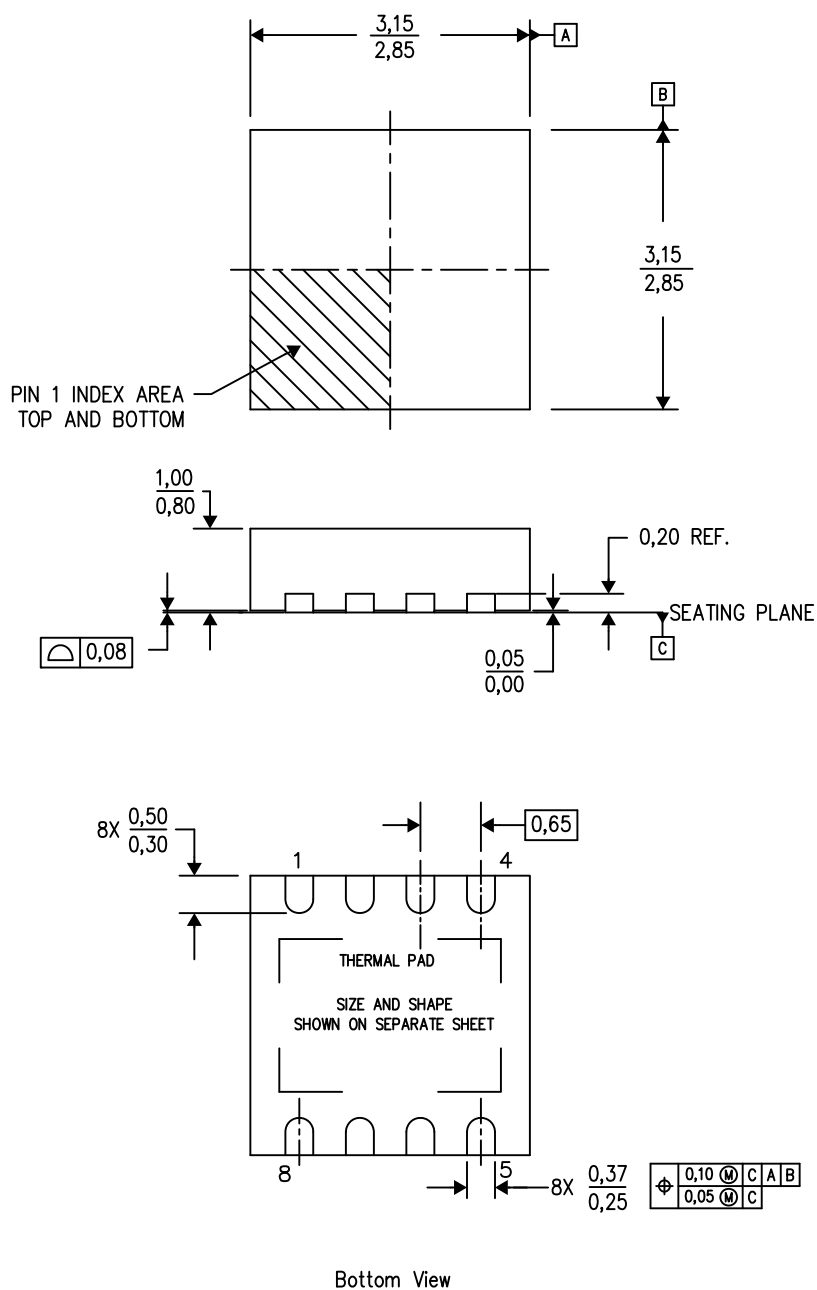
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73501DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73501DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73501DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS73501DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS73512DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73512DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73515DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73515DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73525DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73525DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73525DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS73525DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS73527DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS73527DRVT	SON	DRV	6	250	203.0	203.0	35.0
TPS735285DRVR	SON	DRV	6	3000	203.0	203.0	35.0

---

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS735285DRV	SON	DRV	6	250	203.0	203.0	35.0
TPS73533DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73533DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73533DRVR	SON	DRV	6	3000	203.0	203.0	35.0
TPS73533DRV	SON	DRV	6	250	203.0	203.0	35.0

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4203482-2/K 06/12

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

DRB (S-PVSON-N8)

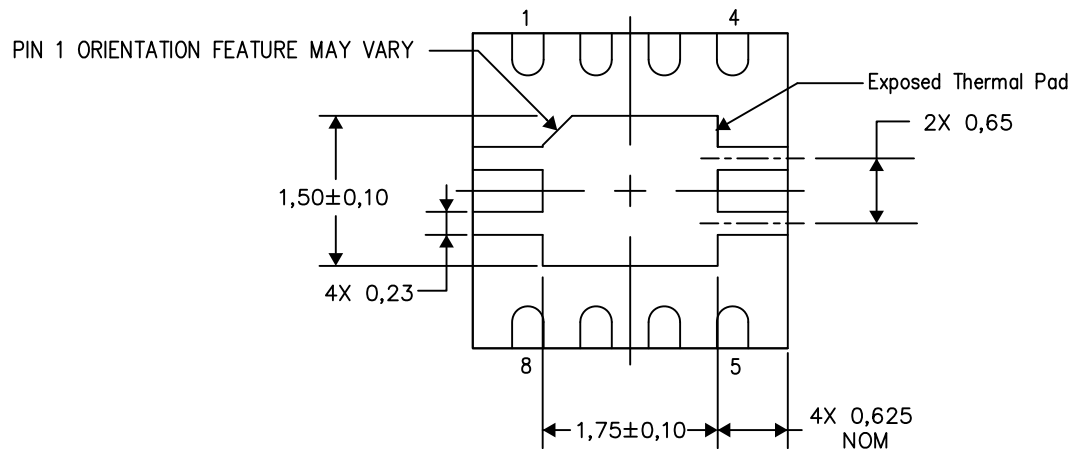
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

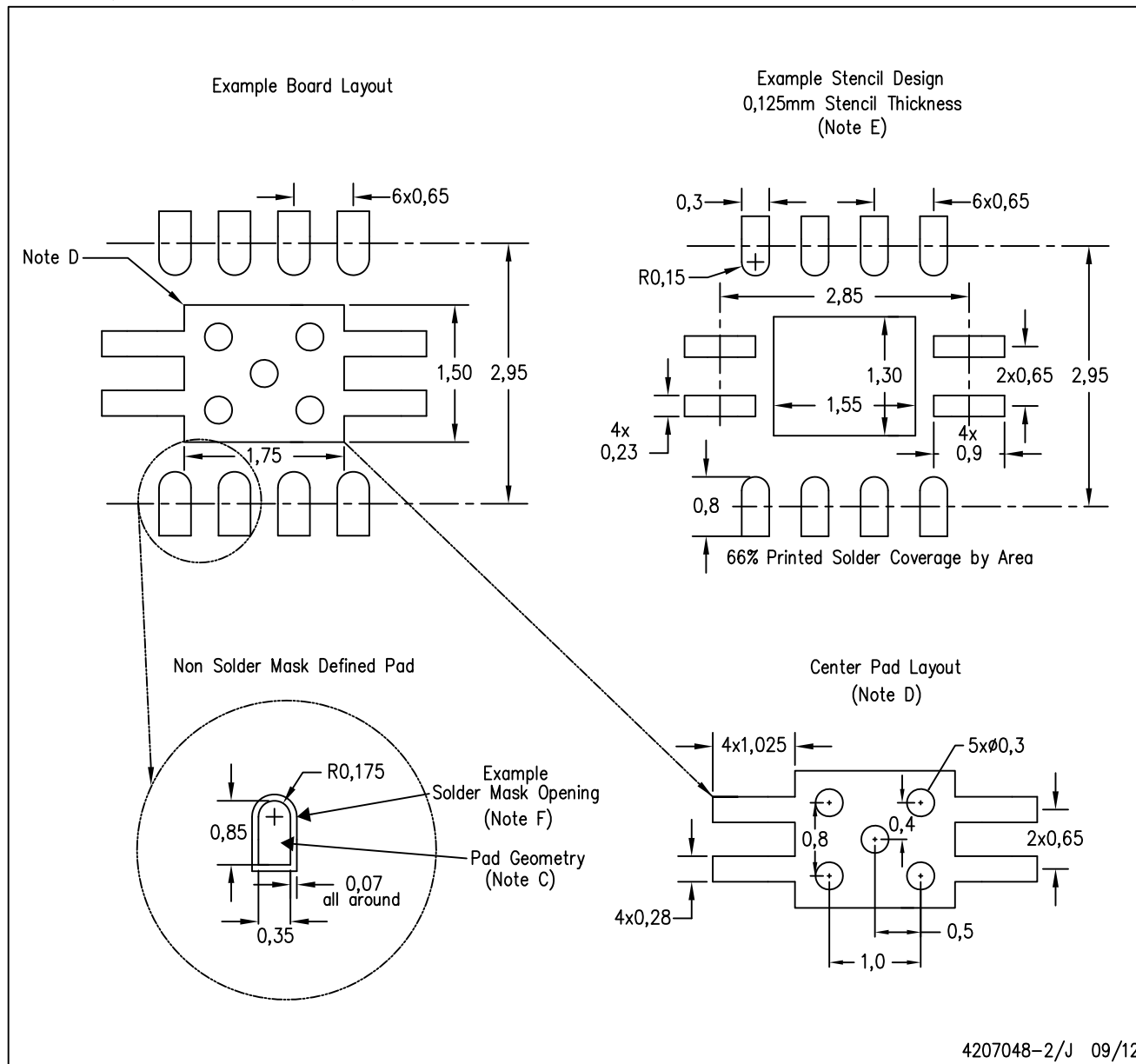
Exposed Thermal Pad Dimensions

4206340-2/N 09/12

NOTE: All linear dimensions are in millimeters

DRB (S-PVSON-N8)

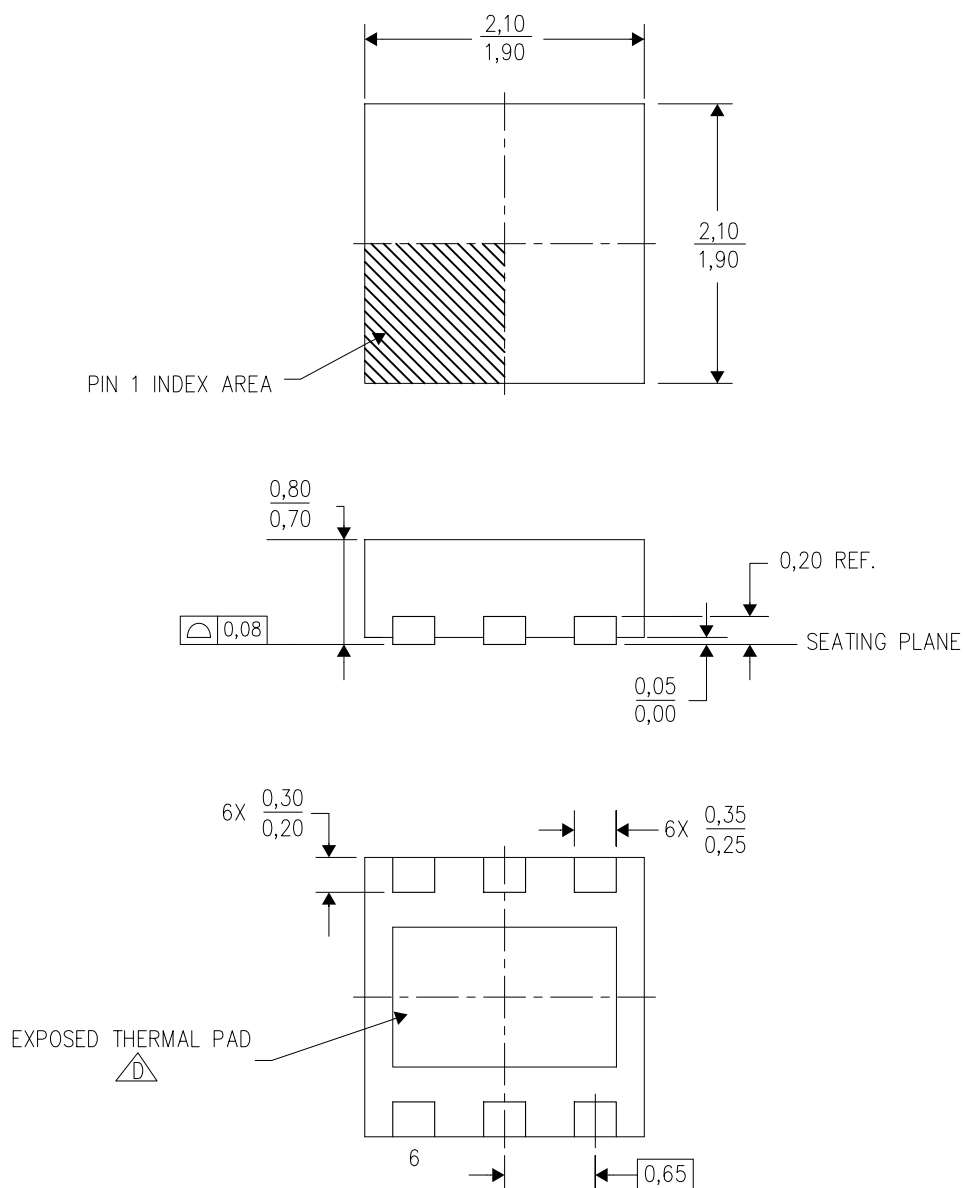
PLASTIC SMALL OUTLINE NO-LEAD




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



## THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

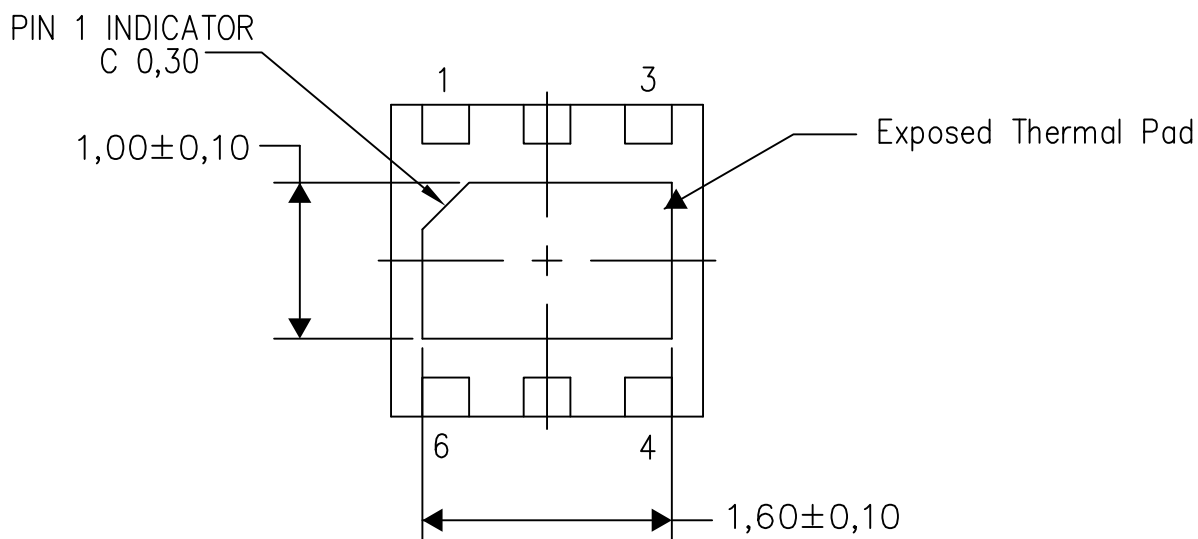
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

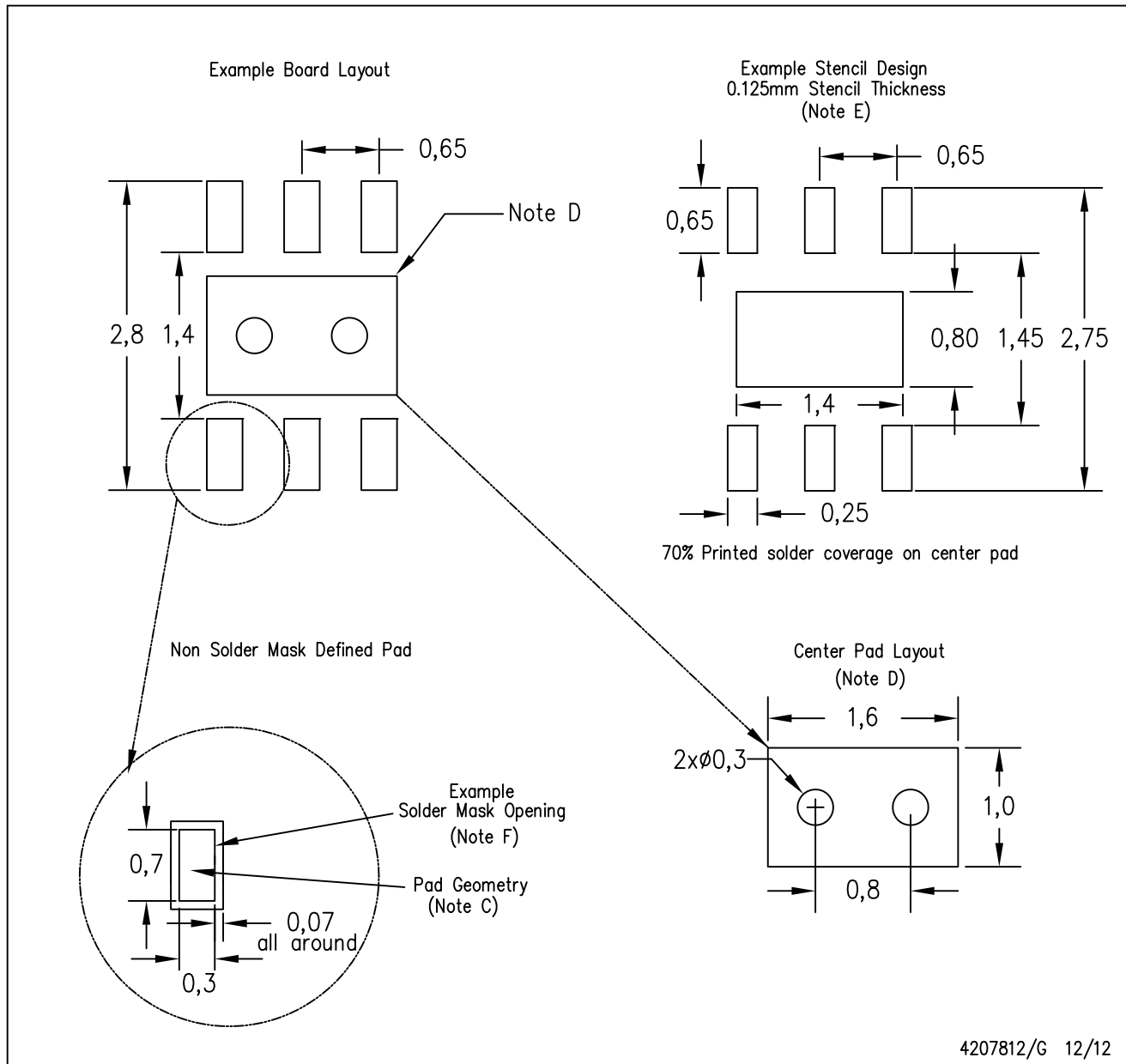
Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.