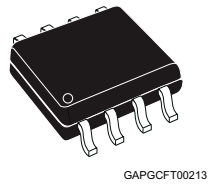
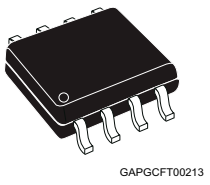
L4988

Automotive low drop voltage regulator

Datasheet - production data



SO-8



SO-20

Features

Max DC supply voltage	V_S	40V
Max output voltage tolerance	ΔV_o	+/-2%
Max dropout voltage	V_{dp}	500 mV
Output current	I_o	200 mA
Quiescent current	I_{qn}	75 µA(1)

1. Typical value with watchdog disabled.

- AEC-Q100 qualified
- Operating DC supply voltage range 5.6 V to 31 V
- Reset circuit sensing the output voltage down to 1V
- Programmable reset pulse delay with external capacitor
- Watchdog
- Programmable watchdog timer with external capacitor
- Enable input for enabling/disabling the watchdog functionality
- Thermal shutdown and short circuit protection
- Wide temperature range (Tj = -40°C to 150°C)

Description

The L4988 is a monolithic integrated 5V voltage regulator with a low drop voltage at currents up to 200mA. The output voltage regulating element consists in a p-channel MOS and the regulation is performed regardless of input voltage transients up to 40V. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. The L4988 is protected against short circuit and an over-temperature protection switches off the device in case of extremely high power dissipation. The L4988 is active when the Enable is high. State of the art features like reset and watchdog make this device particularly suitable to supply microprocessor systems in automotive applications.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
SO8	L4988D	L4988DTR
SO20 (16+2+2)	L4988MD	

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1 Block diagram and pin configuration

Figure 1.Block diagram

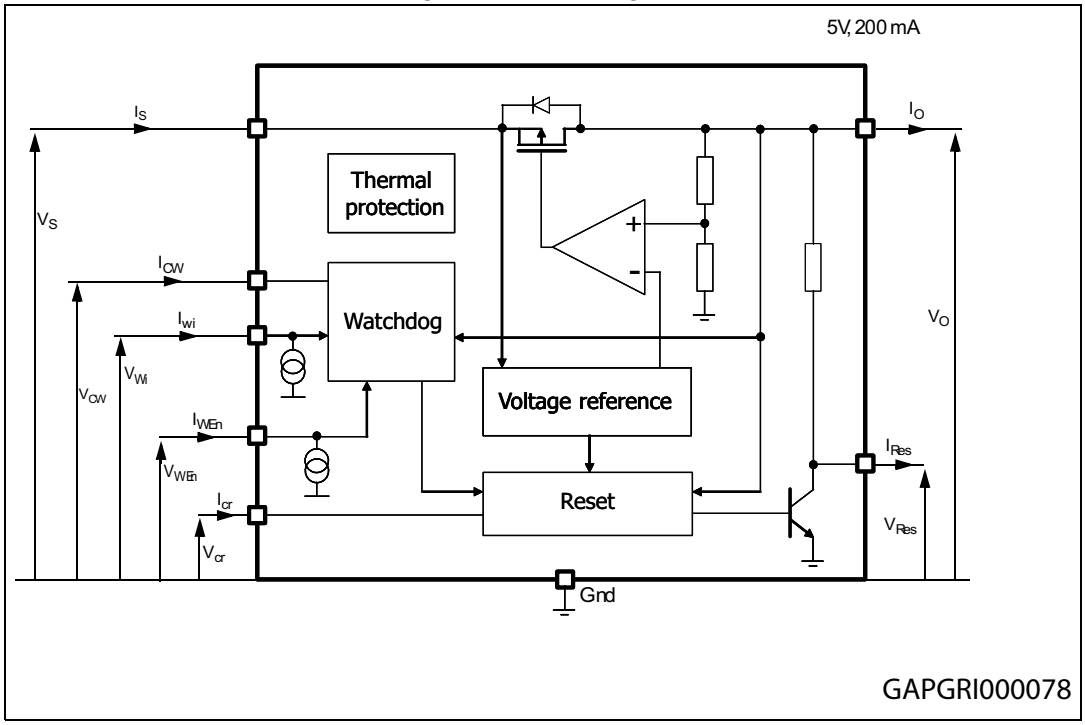
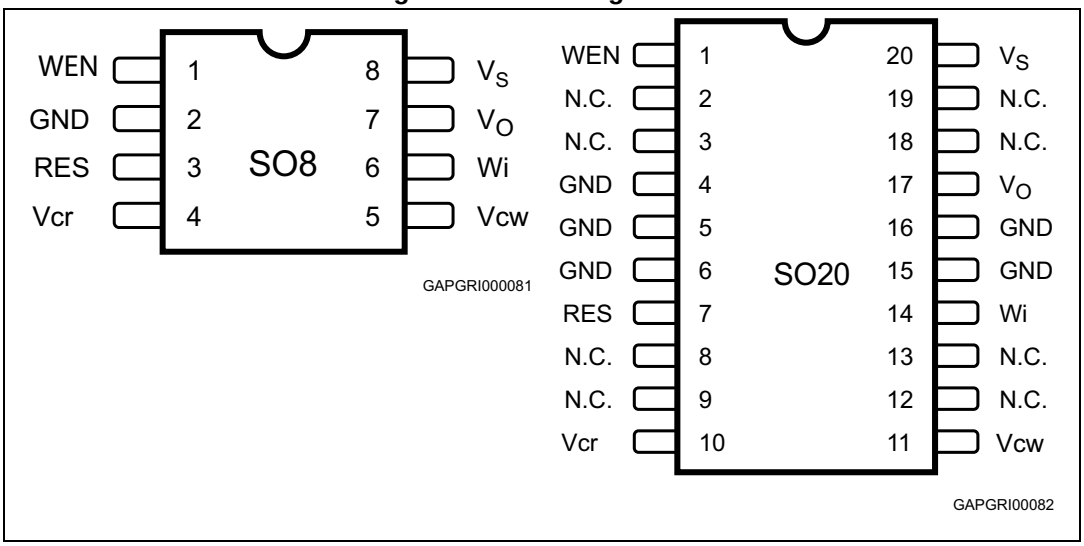


Table 2. Pins description

Pin name	SO8(D)	S020(MD)	Function
WEn	1	1	Watchdog Enable input If high watchdog functionality is active
Gnd	2	4	Ground reference
Gnd		5, 6, 15, 16	Ground. Connected these pins to a heat spreader ground
Res	3	7	Reset output. It is pulled down when output voltage goes below Vo_th or frequency at Wi is too low.
Vcr	4	10	Reset timing adjust. A capacitor between Vcr pin and gnd, sets the reset delay time (trd)
Vcw	5	11	Watchdog timer adjust A capacitor between Vcw pin and gnd, sets the time response of the watchdog monitor.
Wi	6	14	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
Vo	7	17	Voltage regulator output Block to ground with a capacitor >100nF (needed for regulator stability)
Vs	8	20	Supply voltage Block to ground directly at IC pin with a capacitor
N.C.		2, 3, 8, 9, 12, 13, 18, 19	Not connected

Figure 2.Pins configuration



2 Electrical specifications

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{Vsdc}	DC supply voltage	-0.3 to 40	V
I_{Vsdc}	Input current	Internally limited	
V_{Vo}	DC output voltage	-0.3 to 6(1)	V
I_{Vo}	DC output current	Internally limited	
V_{Wi}	Watchdog input voltage	-0.3 to V_{Vo} + 0.3	V
V_{od}	Open Drain output voltage	-0.3 to V_{Vo} + 0.3	V
I_{od}	Open Drain output current	Internally limited	
V_{cr}	Reset delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{cw}	Watchdog delay voltage	-0.3 to V_{Vo} + 0.3	V
V_{WEn}	Watchdog Enable input voltage	-0.3 to V_{Vo} +0.3	V
T_j	Junction temperature	-40 to 150	“C
V_{ESD}	ESD voltage level (HBM-MIL STD 883C)	±2	kV
V_{ESD}	ESD voltage level (CDM AEC-Q100-011)	750	V

1. Using the typical application schematic with Cout= 10 µF and Iout=0 A, when the regulator is switched-on, an overshoot exceeding 6 V could occur.This behavior does not impact the reliability of the regulator.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	S08	S016+2+2	Unit
$R_{th\text{-}jamb}$	Thermal resistance junction to ambient	130(1)	51(2)	°C/W

1. With copper area 2 cm^2 ; for details see *Figure 29*.
2. With copper area 6 cm^2 ; for details see *Figure 33*.

2.3 Electrical characteristics

V_S =5.6V to 31V, T_j= -40°C to +150°C unless otherwise specified.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Vo	V_{o_ref}	Output voltage	Vs = 6 to 31V Io = 1 to 200mA	4.9	5.0	5.1	V
Vo	I_{short}	Short circuit current	Vs = 13.5V(1)	200	280	500	mA
Vo	I_{lim}(2)	Output current limitation	Vs = 13.5V(1)	200	350	600	mA
Vs, Vo	V_{line}	Line regulation voltage	Vs = 6 to 31V Io = 1 to 200mA			25	mV
Vo	V_{load}	Load regulation voltage	Io = 1 to 200mA			25	mV
Vs, Vo	V_{dp}(3)	Drop voltage	Io = 200mA		270	500	mV
Vs, Vo	V_{dp}(3)	Drop voltage	Io = 150mA		200	400	mV
Vs, Vo	SVR	Ripple rejection	fr = 100 Hz(4)		60		dB
Vs, Vo	I_{qn_200}	Quiescent current	Vs=13.5V, Io=200mA, WEn = high		1.9	2.5	mA
Vs, Vo	I_{qn_50}	Quiescent current	Vs=13.5V, Io= 50mA, WEn = high		500	700	µA
Vs, Vo	$I_{q\_1\_we}$	Quiescent current	Vs=13.5V, Io< 1mA, WEn = high		93	200	µA
Vs, Vo	$I_{q\_1\_wd}$	Quiescent current	Vs=13.5V, Io< 1mA, WEn = low		75	150	µA
	Tw	Thermal protection temperature		150		190	°C
	Tw_hy	Thermal protection temperature hysteresis			10		°C

1. See *Figure 3*.
2. Measured output current when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.
3. Vs-Vo measured when the output voltage has dropped 100mV from its nominal value obtained at Vs=13.5V and Io= 75mA.
4. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Res	Vres_l	Reset output low voltage	R_{ext} = 5 kΩ to Vo, Vo > 1 V			0.4	V
Res	I_{Res_h}	Reset output high leakage current	V_{Res} = 5 V			1	µA
Res	R_p_u	Pull up internal resistance	With respect to Vo	12	25	50	kΩ
Res	Vo_th	Vo out of regulation threshold	Vs = 6 to 31V, Io = 1 to 200mA	6%	8%	10%	Below V_{o_ref}
Vcr	Vrlth	Reset timing low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcr	Vrhth	Reset timing high threshold	Vs =13.5V	44%	47%	50%	V_{o_ref}
Vcr	Icr	Charge current	Vs = 13.5V	8	17.6	30	µA
Vcr	Idr	Discharge current	Vs = 13.5V	8	17.6	30	µA
Res	Trr_2	Reset reaction time(1)	Vo = V_{o_th} -100mV	100	275	1000	µs
Res	Trd	Reset delay time	Vs = 13.5V, Ctr = 1nF	65		150	ms

1. When Vo becomes lower than 4V, the reset reaction time decreases down to 2µs assuring a faster reset condition in this particular case.

Table 7. Watchdog

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Wi	Vih	Input high voltage	Vs = 13.5V	3.5			V
Wi	Vil	Input low voltage	Vs = 13.5V			1.5	V
Wi	Vih	Input hysteresis	Vs = 13.5V		500		mV
Wi	Ii	Pull down current	Vs = 13.5V		10	20	µA
Vcw	Vwhth	High threshold	Vs = 13.5V	44%	47%	50%	V_{o_ref}
Vcw	Vwlth	Low threshold	Vs = 13.5V	10%	13%	16%	V_{o_ref}
Vcw	Icwc	Charge current	Vs = 13.5V, Vcw = 0.1V	4	8	14	µA
Vcw	Icwd	Discharge current	Vs = 13.5V, Vcw = 2.5V	1.0	2.1	4.5	µA
Vcw	Twop	Watchdog period	Vs = 13.5V, Ctw = 47nF	25	50	90	ms
Res	twol	Watchdog output low time	Vs = 13.5V, Ctw = 47nF	6	10.5	22	ms

Table 8. Watchdog Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
WEn	V_{En_l}	Enable input low voltage				1	V
WEn	V_{En_h}	Enable input high voltage		3			V
WEn	V_{En_hy}	Enable input hysteresis		500	800	1100	mV
WEn	I_leak	Pull down current	WEn = 5V	2	8	20	µA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs. Tj

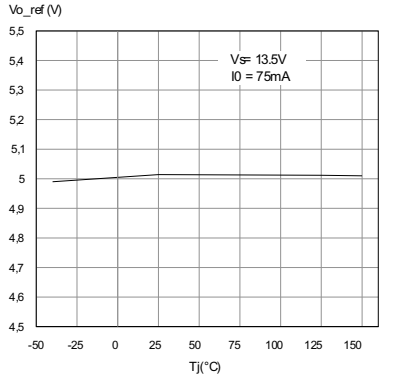


Figure 4. Output voltage vs. Vs

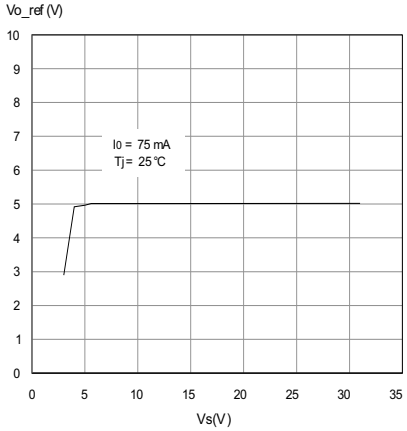


Figure 5. Drop Voltage vs. Output Current

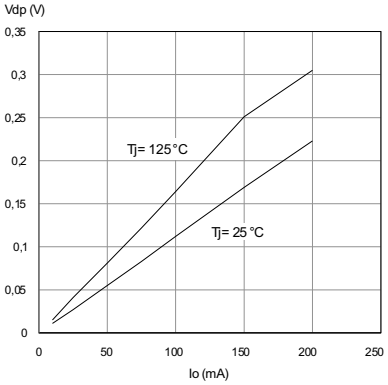


Figure 6. Current consumption vs. Output Current

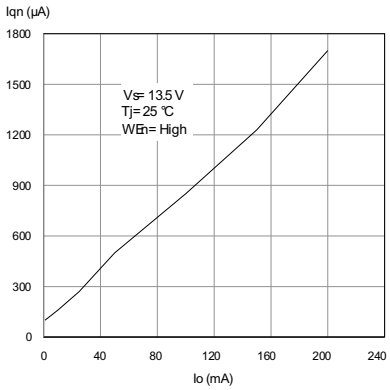


Figure 7. Current consumption vs. Input Voltage

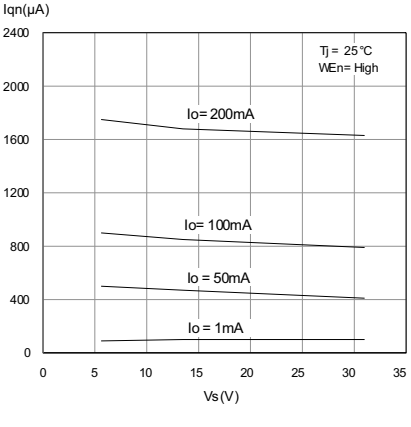


Figure 8. Current limitation vs. Tj

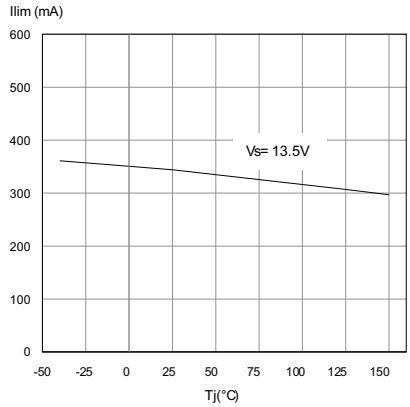


Figure 9. Current limitation vs. Input Voltage

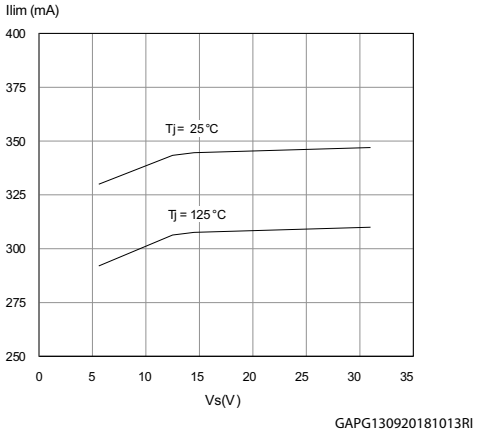


Figure 10. Short Circuit Current vs. Tj

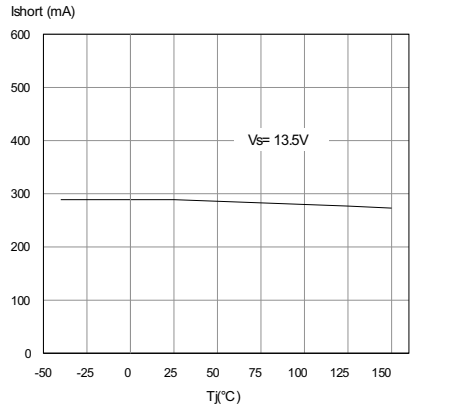


Figure 11. Short Circuit Current vs. Input Voltage

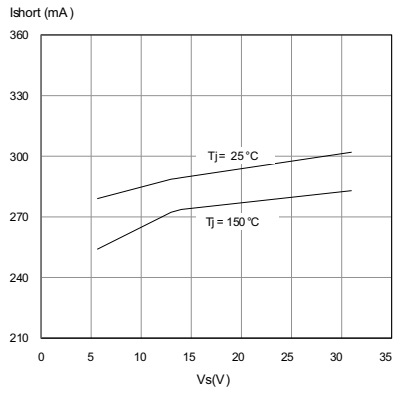


Figure 12. V_{WEn_high} vs. Tj

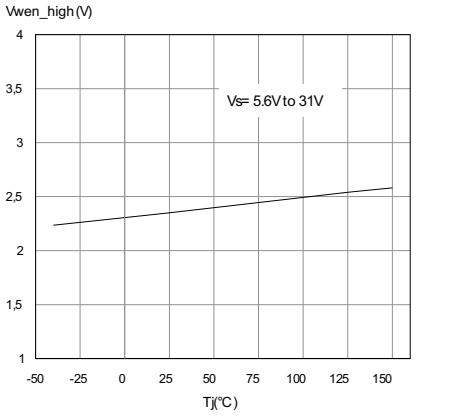


Figure 13. V_{WEN_LOW} vs. Tj

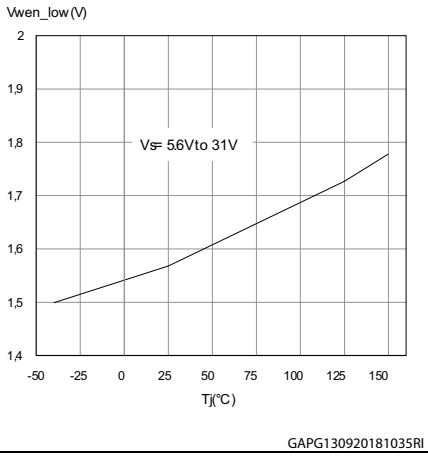


Figure 14. Vrhth vs. Tj

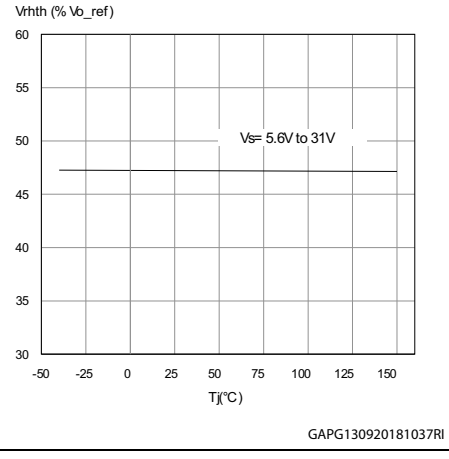


Figure 15. Vrlth vs.Tj

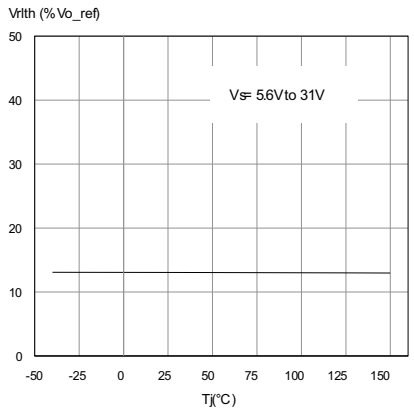


Figure 16. Vwhth vs. Tj

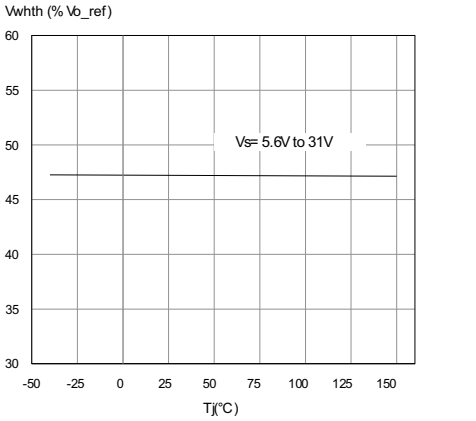


Figure 17. Vwlth vs. T_j

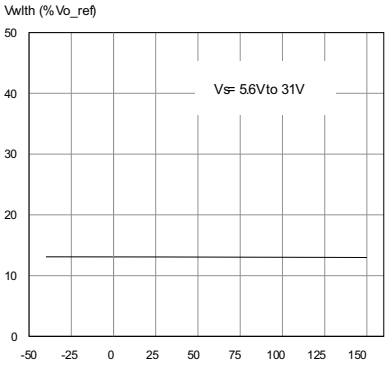


Figure 18. Icr & Icwc vs. T_j

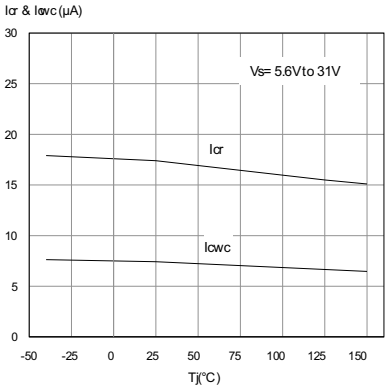


Figure 19. Idr & Icwd vs.T_j

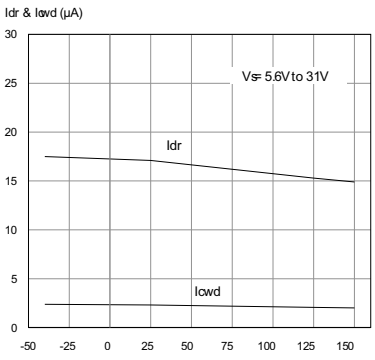


Figure 20. Twop vs. T_j

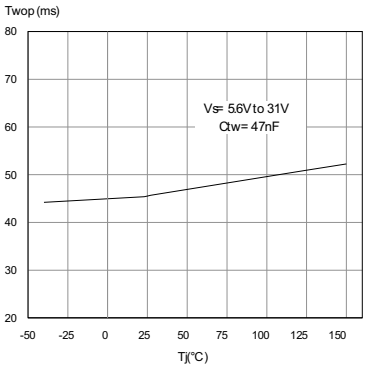
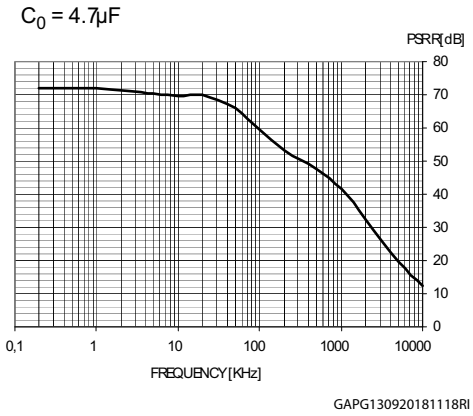


Figure 21. PSRR



2.5 Test circuit and waveforms plot

2.5.1 Load regulation

Figure 22. Load regulation test circuit

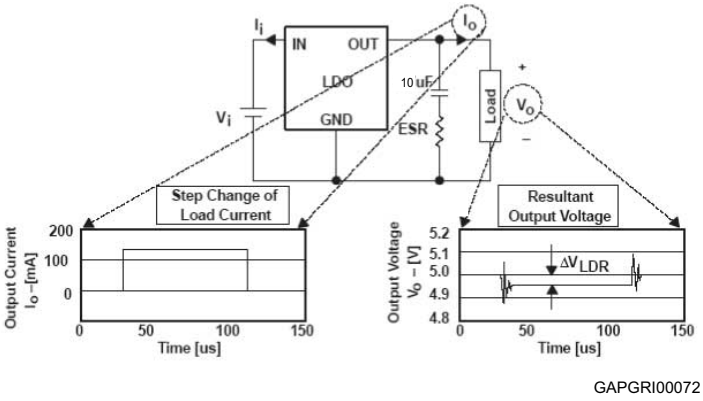
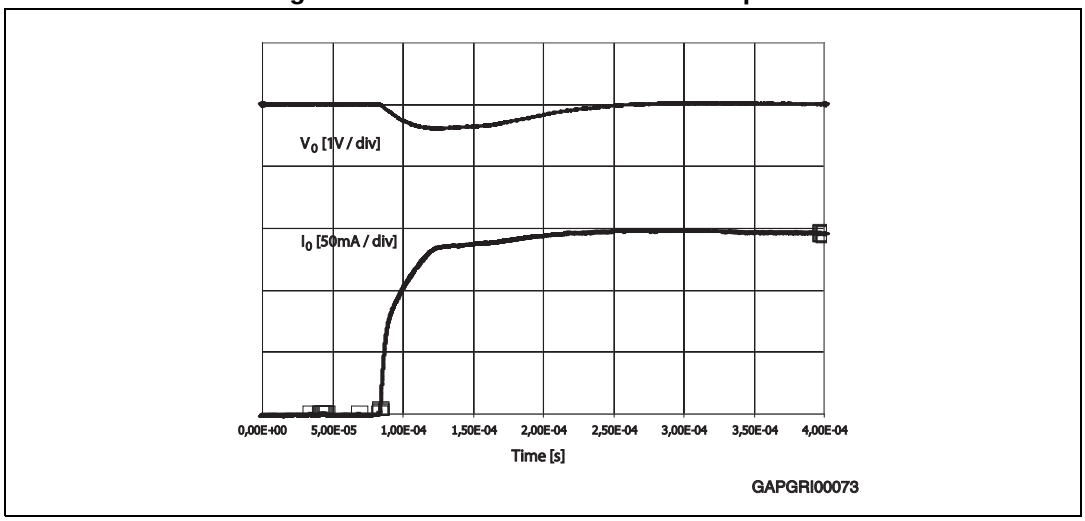
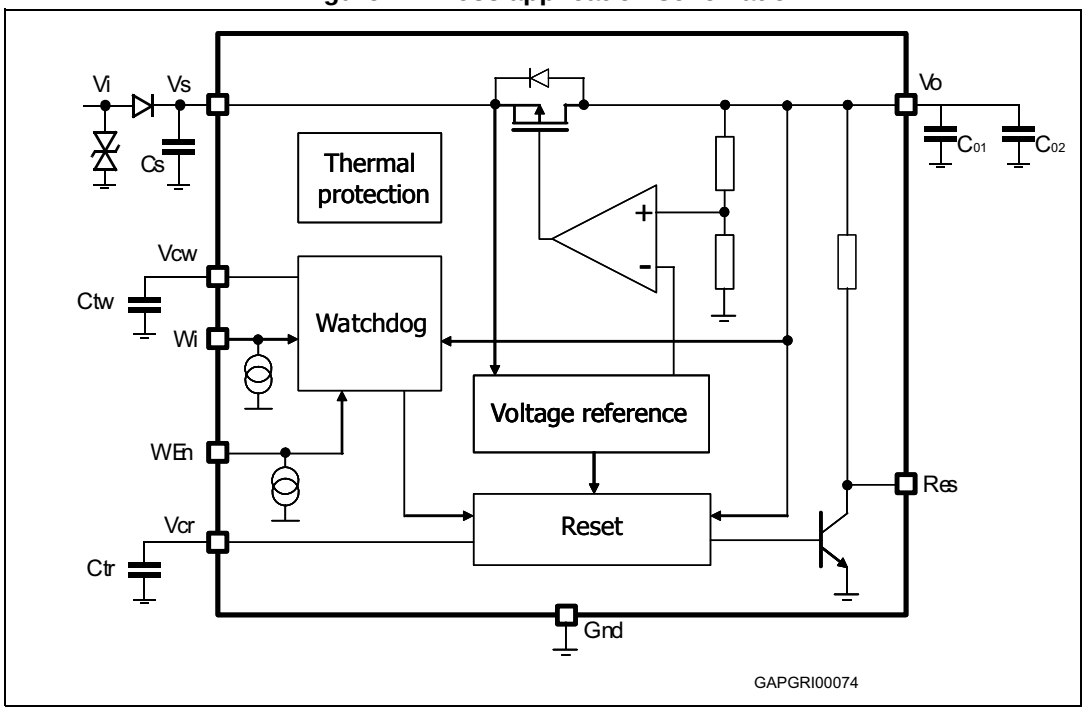


Figure 23.Maximum load variation response



3 Application information

Figure 24.L4988 application schematic

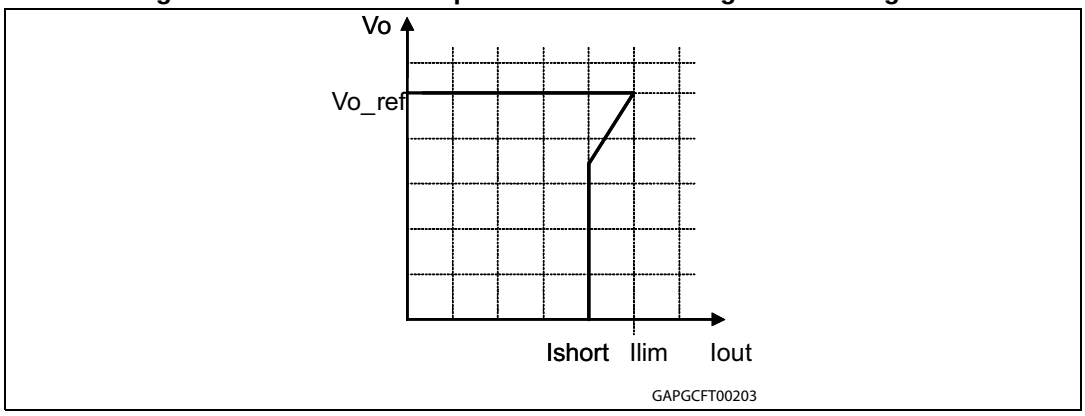


Note: The input capacitor Cs > 200nF is necessary for the smoothing of line disturbances. The output capacitor Co1 > 100nF is necessary for the stability of the regulation loop. In order to damp output voltage oscillations during high load current surges, it is recommended to put an additional electrolytic capacitor Co2 > 10µF at the output pin.

3.1 Voltage regulator

Voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at currents up to 200mA is obtained. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. A short circuit protection to GND is provided.
The high precision of the output voltage is obtained with a pre-trimmed reference voltage.

Figure 25.Behavior of output current versus regulated voltage Vo



3.2 Reset

The reset circuit supervises the output voltage Vo. The Vo_th reset threshold is defined with the internal reference voltage and a resistor output divider. If the output voltage becomes lower than Vo_th then Res goes low with a reaction time trr. The reset low signal is guaranteed for an output voltage Vo greater than 1V.

When the output voltage becomes higher than Vo_th then Res goes high with a delay trd. This delay is obtained by an internal oscillator.

The oscillator period is given by:

Tosc = [(Vrhth-Vrlth) x Ctr] / Icr + [(Vrhth-Vrlth) x Ctr] / Idr

where:

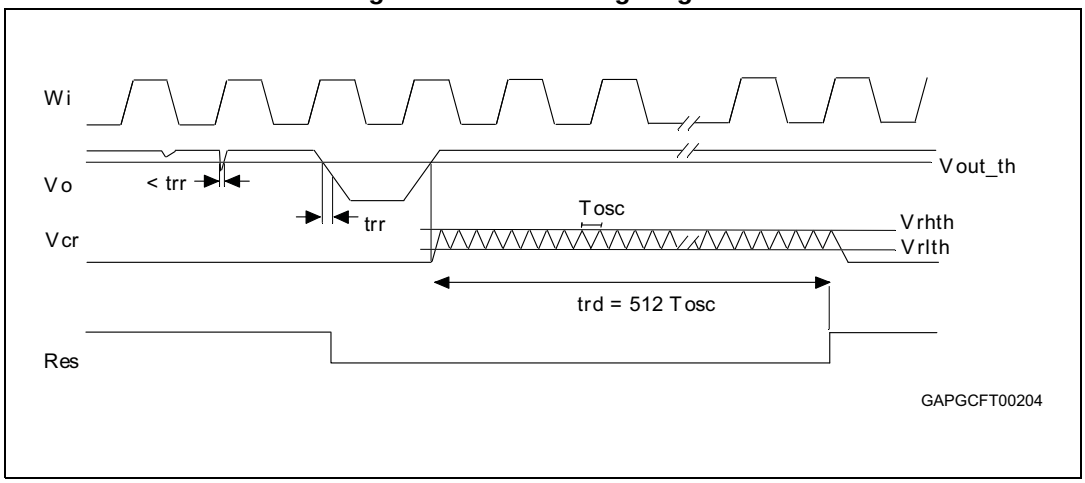
Icr:	is an internally generated charge current
Idr:	is an internally generated discharge current
Vrhth, Vrlth:	are two voltages defined with the output voltage and a resistor output divider
Ctr:	is an external capacitance.

trd is given by:

trd = 512 x Tosc

Reset is active when En is high.

Figure 26.Reset timing diagram



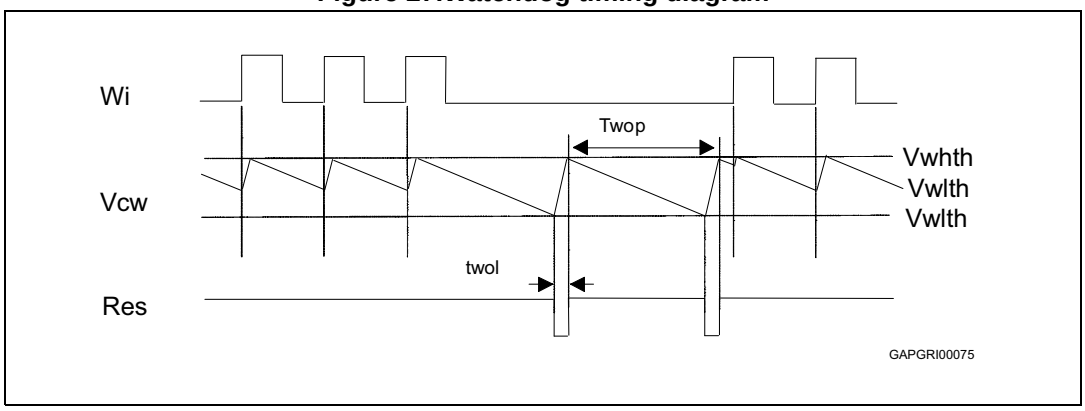
3.3 Watchdog

A connected microcontroller is monitored by the watchdog input Wi. If pulses are missing, the Reset output pin is set to low. The pulse sequence time can be set within a wide range with the external capacitor, C_{tw}. The watchdog circuit discharges the capacitor C_{tw}, with the constant current I_{cwd}. If the lower threshold V_{wlth} is reached, a watchdog reset is generated. To prevent this the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold V_{wlth}. In order to calculate the minimum time t, during which the micro-controller must output the positive edge, the following equation can be used:

$$(V_{whth}-V_{wlth}) \times C_{tw} = I_{cwd} \times t$$

Every Wi positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, V_{whth}, the current switches from charging to discharging. The result is a saw-tooth voltage at the watchdog timer capacitor C_{tw}.

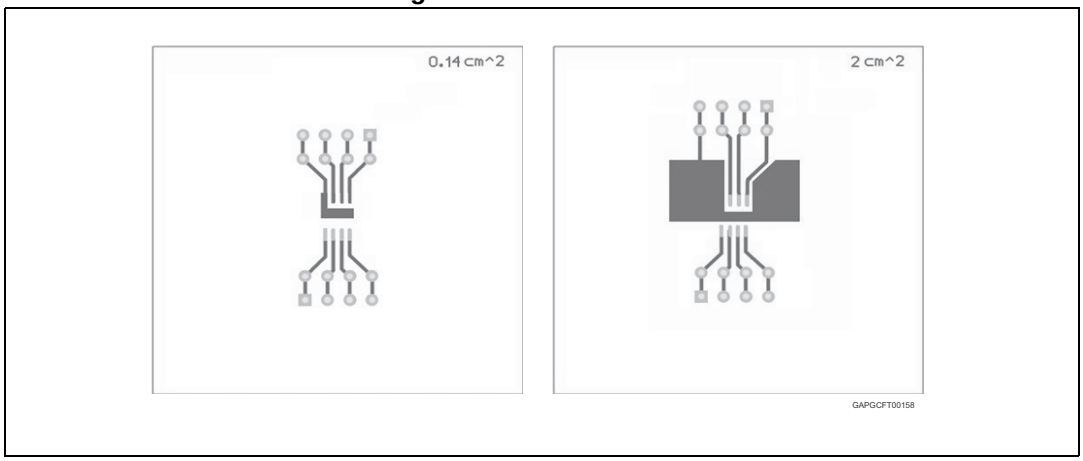
Figure 27.Watchdog timing diagram



4 Package and PCB thermal data

4.1 SO-8 thermal data

Figure 28.SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness = 2mm, Cu thickness = 35µm , Copper areas: from minimum pad lay-out to 8cm^2)

Figure 29.SO-8 $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

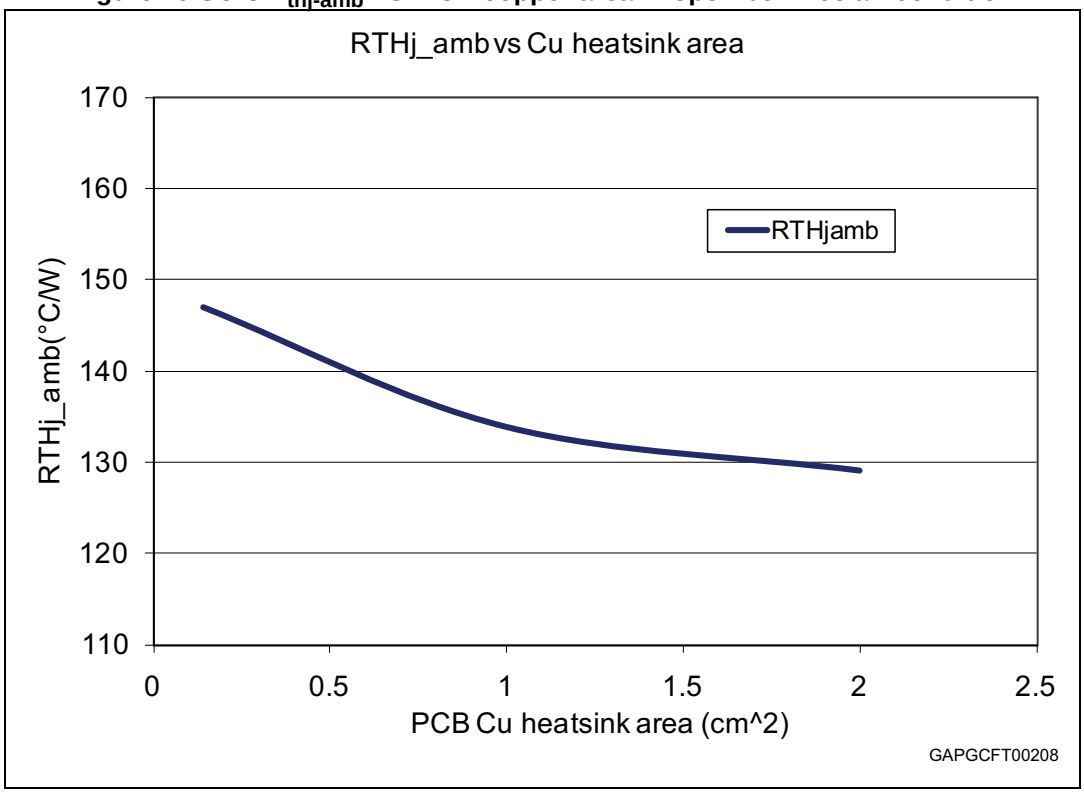
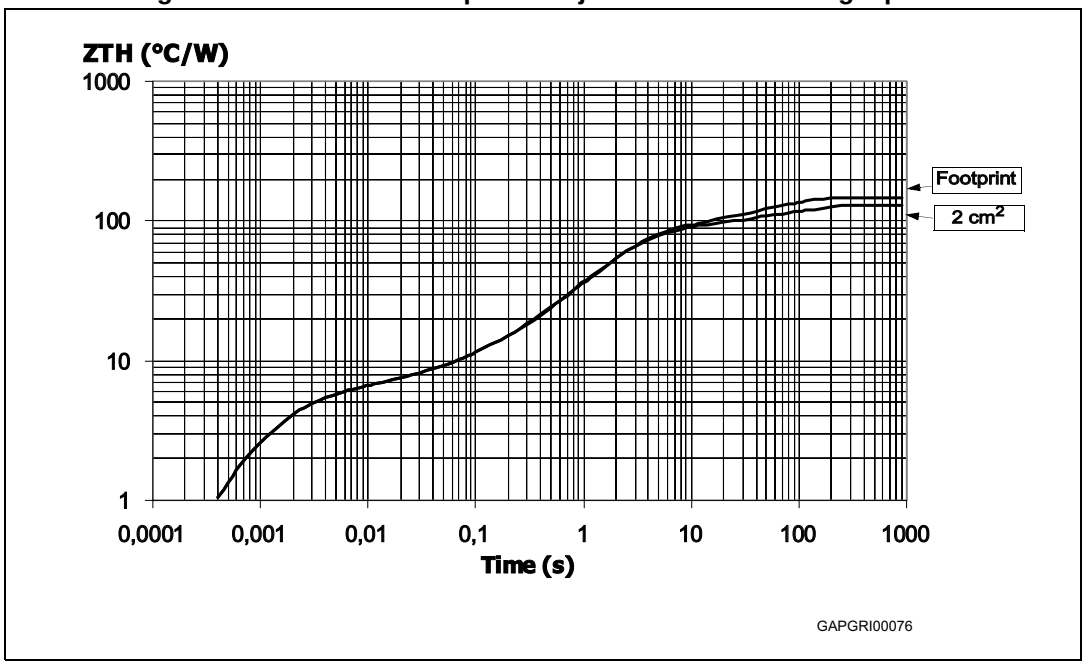


Figure 30.SO-8 thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 31.SO-8 thermal fitting model of a single channel

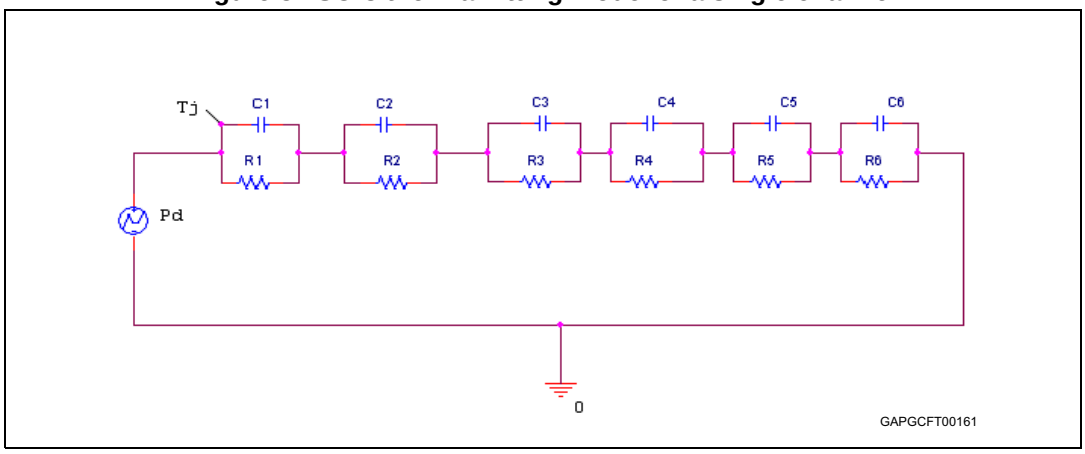
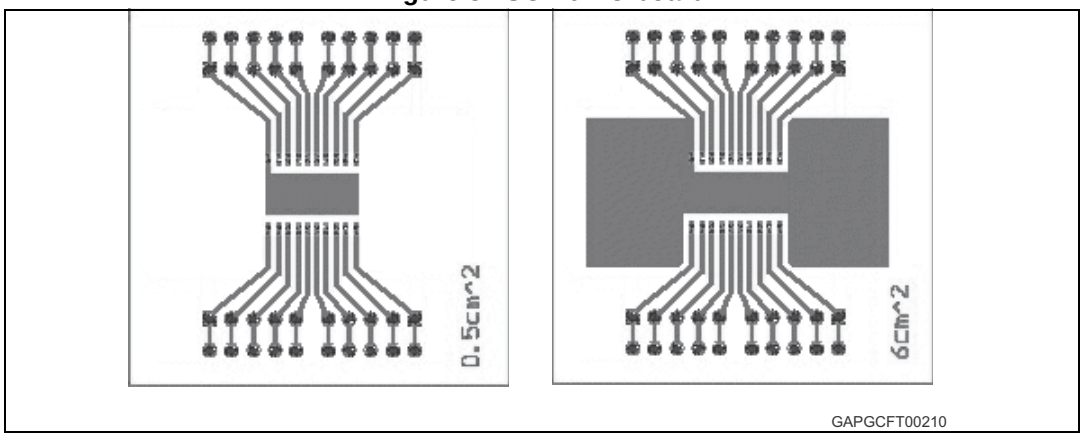


Table 9. SO-8 thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2	
R4 (°C/W)	41	
R5 (°C/W)	40	
R6 (°C/W)	58	40
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.03	
C4 (W.s/°C)	0.04	
C5 (W.s/°C)	0.1	
C6 (W.s/°C)	1.05	2

4.2 SO-20 thermal data

Figure 32.SO-20 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm,PCB thickness = 2mm, Cu thickness=35µm , Copper areas: from minimum pad lay-out to 8cm^2).

Figure 33.SO-20 $R_{thj\text{-}amb}$ Vs. PCB copper area in open box free air condition

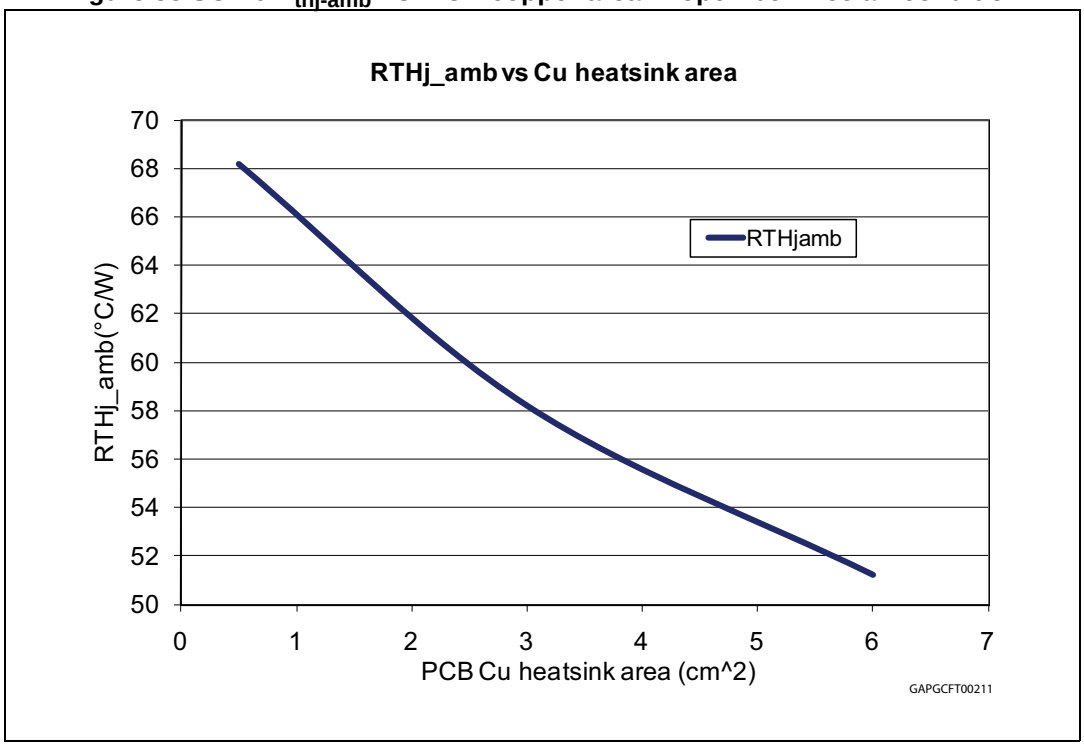
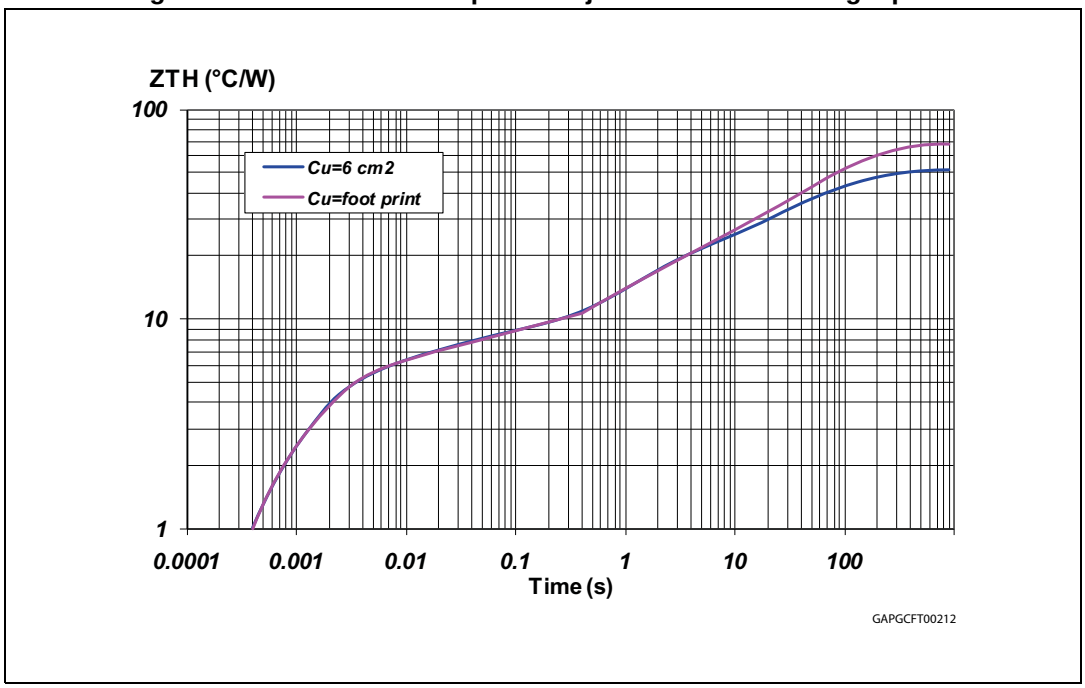


Figure 34.SO-20 thermal impedance junction ambient single pulse



Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Figure 35. SO-20 thermal fitting model of a single channel

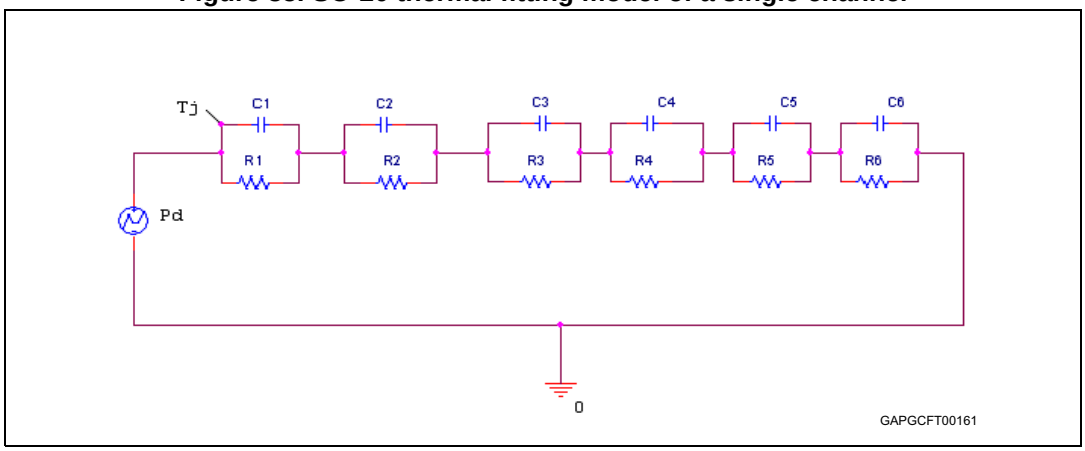


Table 10. SO-20 thermal parameter

Area/island (cm^2)	Footprint	2
R1 (°C/W)	4.21	
R2 (°C/W)	2.11	
R3 (°C/W)	2.2	
R4 (°C/W)	10	
R5 (°C/W)	15	
R6 (°C/W)	35	18
C1 (W.s/°C)	0.00029	
C2 (W.s/°C)	0.0024	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.15	
C5 (W.s/°C)	1.5	
C6 (W.s/°C)	4	7

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.2 SO-8 package information

Figure 36.SO-8 package dimensions

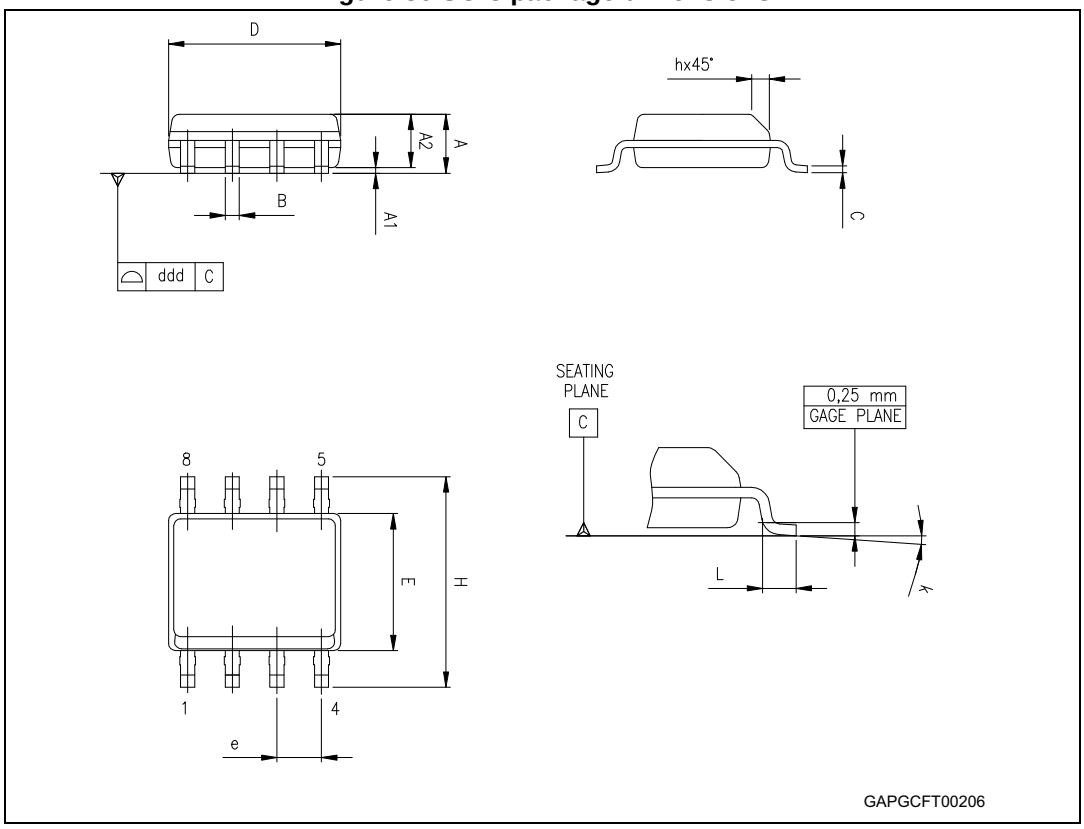


Table 11. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D(1)	4.80	4.90	5.00
E	5.80	6.00	6.20
E1(2)	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm in total (both side).
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

5.3 SO-20 package information

Figure 37.SO-20 package dimensions

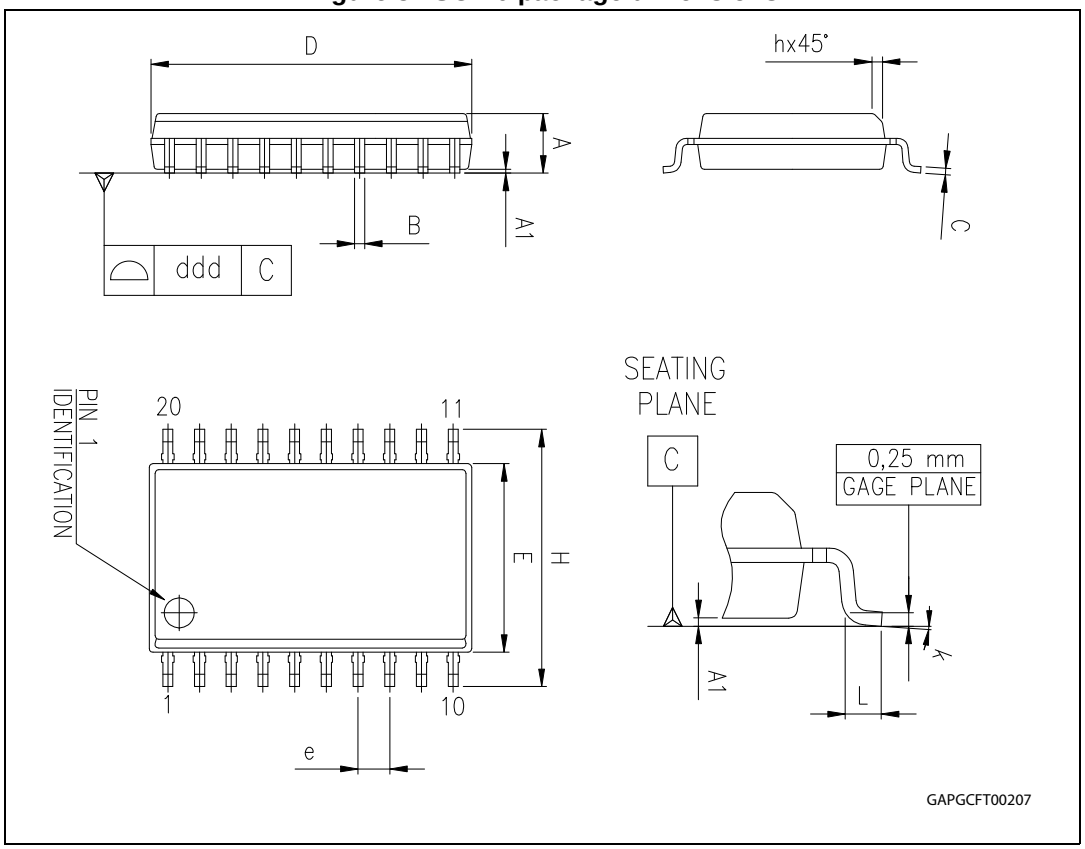


Table 12. SO-20 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D(1)	12.60		13.00
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27

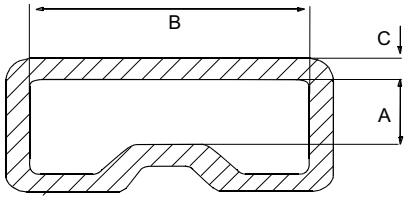
Table 12. SO-20 mechanical data (continued)

Symbol	Millimeters		
	Min.	Typ.	Max.
k	0°		8°
ddd			0.10

1. “D” dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

5.4 SO-8 packing information

Figure 38.SO-8 tube shipment (no suffix)



Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

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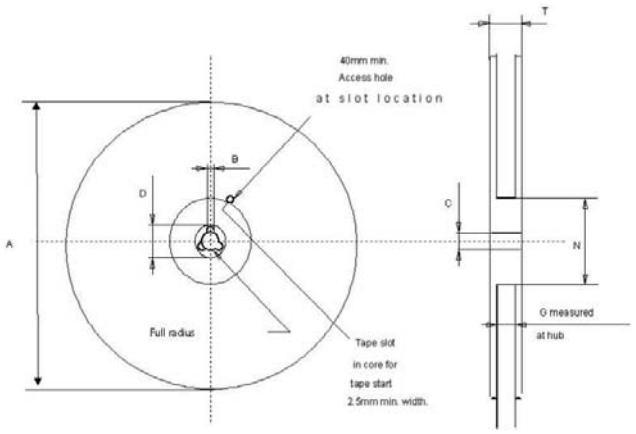
Figure 39.SO-8 tape and reel shipment (suffix “TR”)



REEL DIMENSIONS

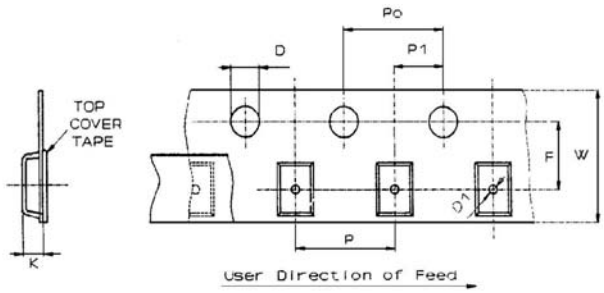
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

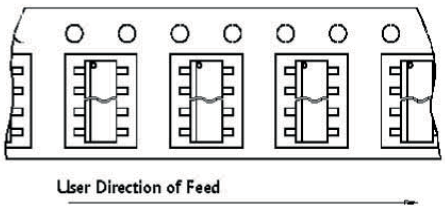
All dimensions are in mm.

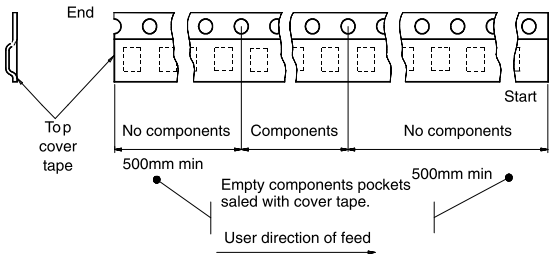
TAPE DIMENSIONS
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (+ 0.1/-0)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.05)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2

All dimensions are in mm.







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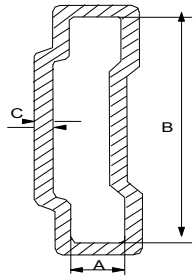
5.5 SO-20 packing information

Figure 40.SO-20 tube shipment (no suffix)



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Base Q.ty	40
Bulk Q.ty	800
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Jun-2007	1	Initial release
30-Aug-2007	2	Added features table. Added list of tables and figures. Updated *Section 2.3: Electrical characteristics*. Added *Section 4: Package and PCB thermal data*. Added *SO-8 packing information* and *SO-20 packing information*.
13-Feb-2008	3	Update *Section 2.3: Electrical characteristics*.
04-Jun-2008	4	Document restructured. Changed *Figure 1: Block diagram*. Updated features table on cover page: changed quiescent current value from 80 to 75 µA. Updated *Table 5: General*: – changed I_{short} typical value from 250 to 280 mA – changed I_{qn_50} typical value from 550 to 500 µA – changed $I_{q\_1\_we}$ typical value from 130 to 93 µA – changed $I_{q\_1\_wd}$ typical value from 80 to 75 µA. Updated *Table 7: Watchdog*: – changed Vwlth values in V_{o_ref} percentages – changed Vwhth values in V_{o_ref} percentages. Added *Figure 24: L4988 application schematic*. Added *Section 2.4: Electrical characteristics curves*. Added *Section 2.5: Test circuit and waveforms plot*.
05-Apr-2012	5	Update *Table 3: Absolute maximum ratings*.
20-Sep-2013	6	Updated disclaimer.
13-Sep-2018	7	Updated title and *Features*. Minor text changes.
18-Sep-2018	8	Typo errors.

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- Консультации по применению компонента;
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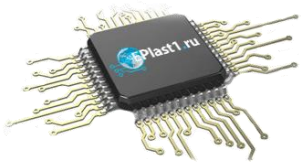
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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