DSC1101/21

Low-Jitter Precision CMOS Oscillator

Features

- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±10 ppm, ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive: –55°C to +125°C
  - Ext. Industrial: –40°C to +105°C
  - Industrial: –40°C to +85°C
  - Commercial: –20°C to +70°C
- High Supply Noise Rejection: –50 dBc
- Wide Freq. Range: 2.3 MHz to 170 MHz
- Small Industry Standard Footprints
  - 2.5 mm x 2.0 mm, 3.2 mm x 2.5 mm, 5.0 mm x 3.2 mm, and 7.0 mm x 5.0 mm
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25 to 3.6V
- Standby and Output Enable Function
- Lead-Free and RoHS Compliant

Applications

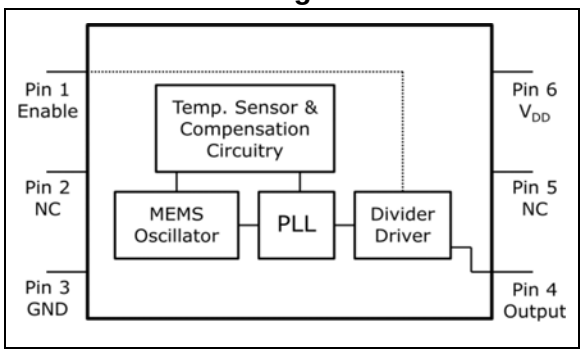
- Storage Area Networks
  - SATA, SAS, Fibre Channel
- Passive Optical Networks
  - EPON, 10G-EPON,V GPON, 10G-PON
- Ethernet
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video and Surveillance
- PCI Express
- Display Port

General Description

The DSC1101 and DSC1121 series of high performance oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1101 has a standby feature that allows it to completely power-down when EN pin is pulled low; whereas for DSC1121, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 4-pin CMOS quartz crystal oscillators.

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} .....–0.3V to V_{DD} + 0.3V
Supply Voltage .....–0.3V to +4.0V
ESD Protection On All Pins .....4000V HBM, 1500V CDM (max.)

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: 1000+ years of data retention on internal memory.

TABLE 1-1: DC CHARACTERISTICS

Electrical Characteristics						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.6	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSC1101, EN pin low, output is disabled
		—	20	22		DSC1121, EN pin low, output is disabled
		—	31	35		Output enabled, C_L = 15 pF, F_0 = 100 MHz
Frequency Stability (Including frequency variations due to initial tolerance, temp. and power supply voltage.)	Δf	—	—	±10	ppm	Ext Comm. & Ind. only
				±20		All temp ranges
		—	—	±25		All temp ranges
		—	—	±50		All temp ranges
Aging	Δf	—	—	±5	ppm	1 year @ 25°C
Startup Time (Note 2)	t_{SU}	—	—	5	ms	T = 25°C
Input Logic Levels Input Logic High Input Logic Low	V_{IH}	0.75×V_{DD}	—	—	V	—
	V_{IL}	—	—	0.1×V_{DD}		
Output Disable Time (Note 3)	t_{DS}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSC1101
		—	—	20	ns	DSC1121
Enable Pull-up Resistor (Note 4)	—	—	40	—	kΩ	Pull-up Resistor Exist
CMOS Output						
Output Logic Levels Output Logic High Output Logic Low	V_{OH}	0.9×V_{DD}	—	—	V	I = ±6 mA
	V_{OL}	—	—	0.1×V_{DD}		

Note 1: Pin 6 V_{DD} should be filtered with 0.1 µF capacitor.
2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.
3: Output Waveform and Test Circuit figures define the parameters.
4: Output is enabled if pad is floated or not connected.

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TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Transition Time Rise Time Fall Time	t_R	—	1.1	2	ns	20% to 80% C_L = 15 pF
	t_F	—	1.3	2		
Frequency	f_0	2.3	—	170	MHz	C_L = 15 pF, –20°C to +70°C and –40°C to +85°C
		3.3	—	170		C_L = 15 pF, –40°C to +105°C and –55°C to +125°C
Output Duty Cycle	SYM	45	—	55	%	—
Period Jitter	J_{PER}	—	3	—	ps_{RMS}	F_{OUT} = 125 MHz
Integrated Phase Noise	J_{PH}	—	0.3	—	ps_{RMS}	200 kHz to 20 MHz @ 125 MHz
		—	0.38	—		100 kHz to 20 MHz @ 125 MHz
		—	1.7	2		12 kHz to 20 MHz @ 125 MHz

Note 1: Pin 6 V_{DD} should be filtered with 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures define the parameters.

4: Output is enabled if pad is floated or not connected.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range (T)	T_A	–20	—	+70	°C	Ordering Option E
	T_A	–40	—	+85	°C	Ordering Option I
	T_A	–40	—	+105	°C	Ordering Option L
	T_A	–55	—	+125	°C	Ordering Option M
Junction Operating Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_A	–40	—	+150	°C	—
Soldering Temperature Range	T_S	—	—	+260	°C	40 sec. max

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 NOMINAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

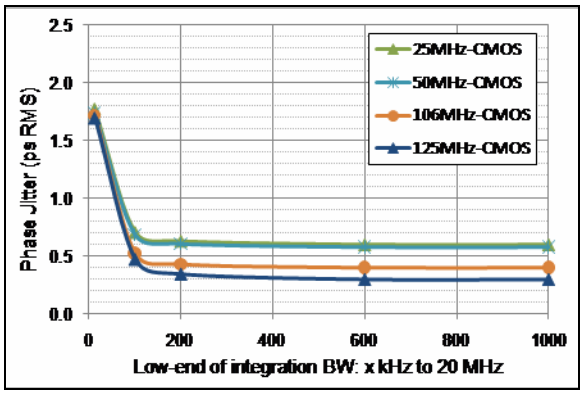

FIGURE 2-1: *Phase Jitter (Integrated Phase Noise).*

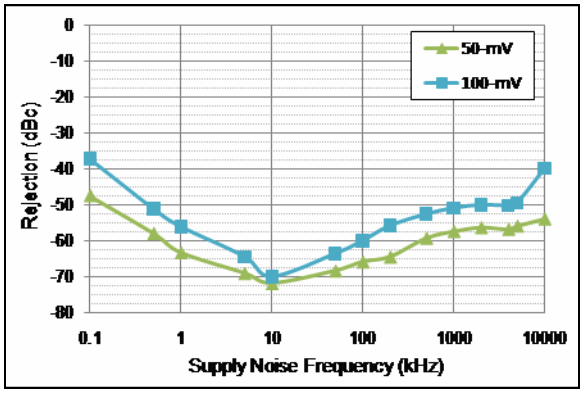

FIGURE 2-2: *Power Supply Rejection Ratio.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1. Pin order and descriptions apply across all package types.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number 7x5 w/ Pad	Pin Number 7x5 w/o Pad	Pin Number 5x3.2	Pin Number 3.2x2.5	Pin Number 2x2.5	Pin Name	Description
1	1	1	1	1	EN	Enable.
2	2	2	2	2	NC	Do not connect.
3	3	3	3	3	GND	Ground.
4	4	4	4	4	OUT	Output.
5	5	5	5	5	NC	Do not connect.
6	6	6	6	6	V_{DD}	Supply voltage.
PAD	—	—	—	—	PAD	Tie to ground.

TABLE 3-2: OUTPUT ENABLE MODES

EN Pin	DSC1101	DSC1121
High	Output Active	Output Active
NC	Output Active	Output Active
Low	Standby	Output Disabled

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4.0 OUTPUT WAVEFORM

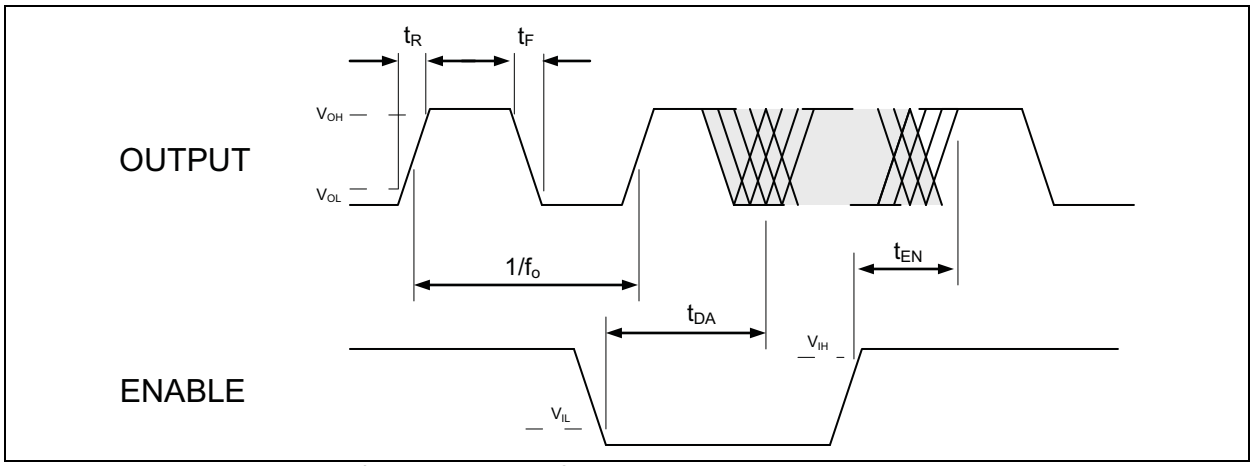

FIGURE 4-1: *DSC1101/21 Output Waveform.*

5.0 TYPICAL TERMINATION SCHEME

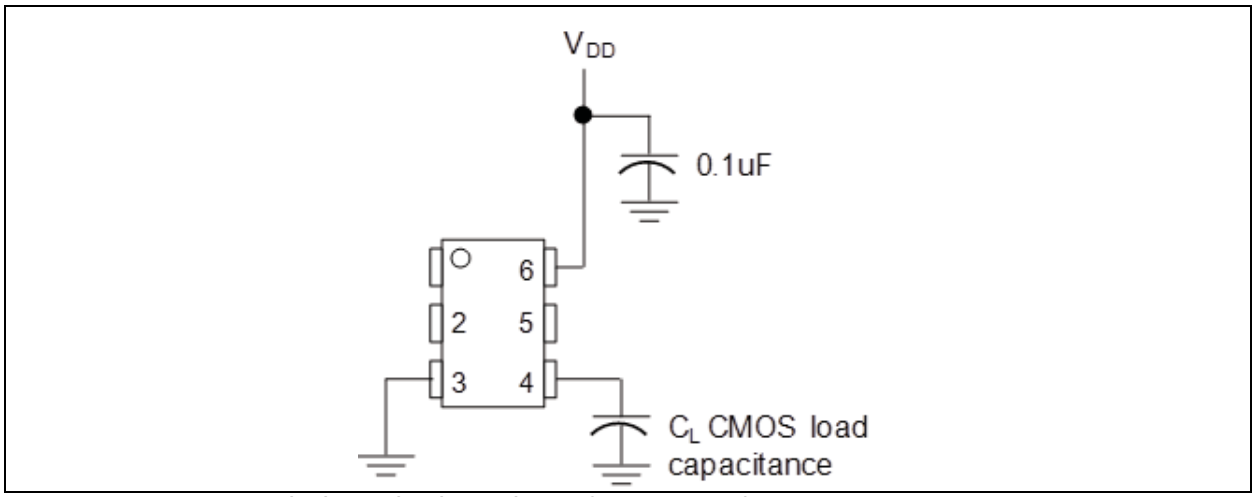

FIGURE 5-1: *Typical Termination Scheme for DSC1101/21.*

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6.0 BOARD LAYOUT (RECOMMENDED)

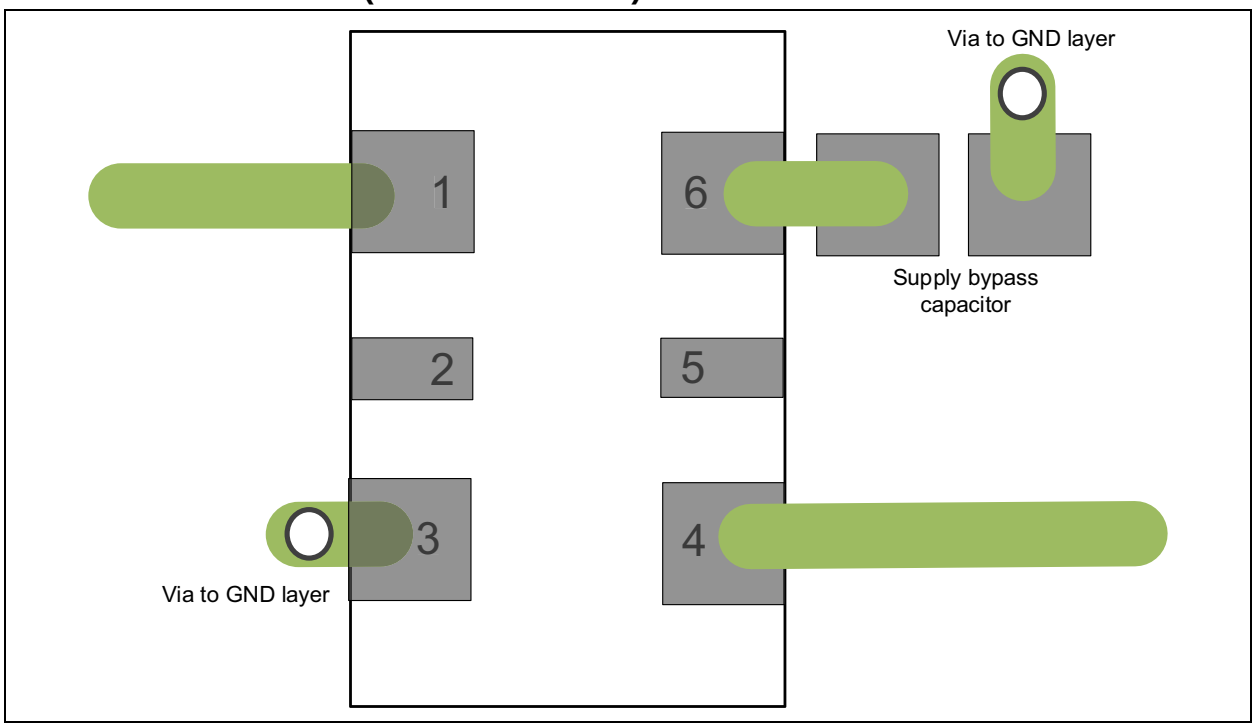
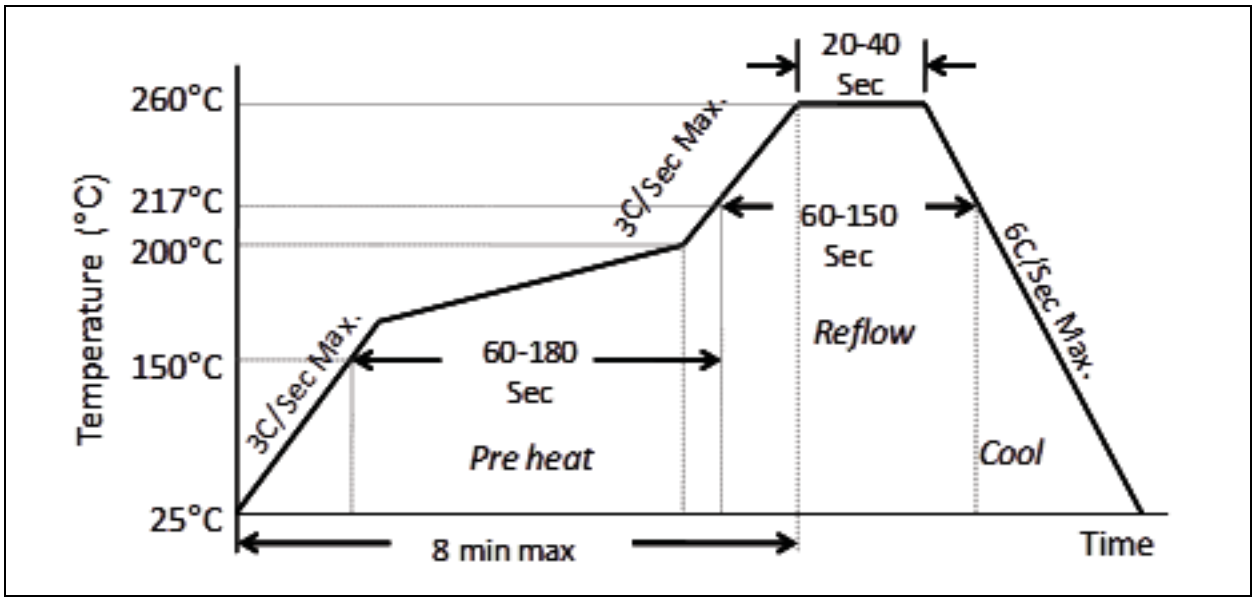


FIGURE 6-1: *DSC1101/21 Recommended Board Layout.*

7.0 SOLDER REFLOW PROFILE



MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec. Max.
Preheat Time 150°C to 200°C	60-180 Sec.
Time Maintained Above 217°C	60-150 Sec.
Peak Temperature	255-260°C
Time within 5°C of Actual Peak	20-40 Sec.
Ramp-Down Rate	6°C/Sec. Max.
Time 25°C to Peak Temperature	8 minute Max.

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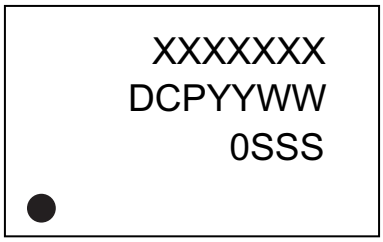
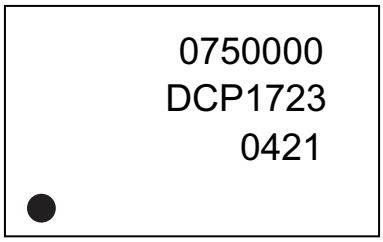
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

6-Pin CDFN/VDFN*



Example

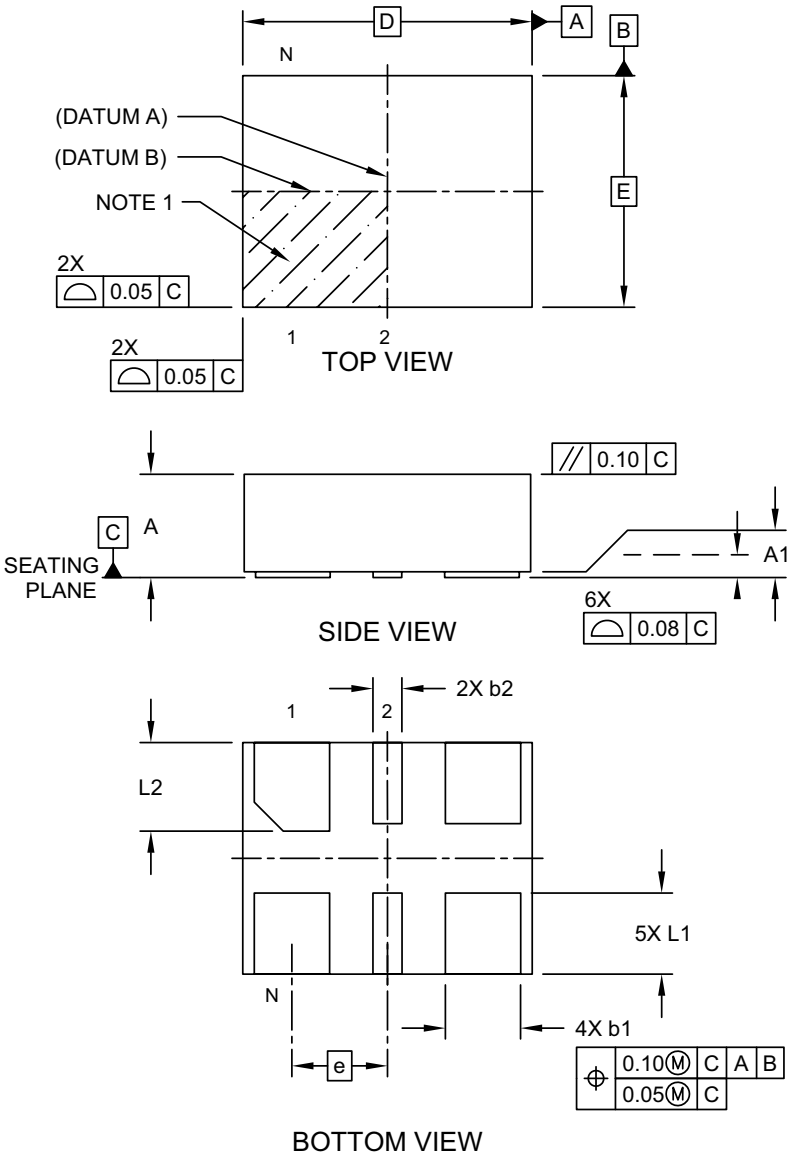


Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	SSS	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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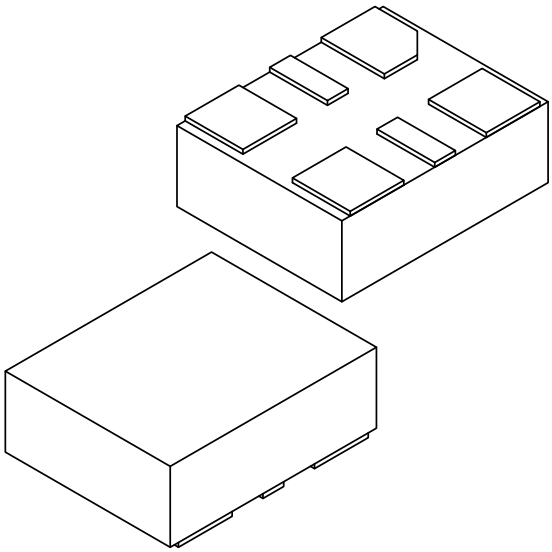
6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.825 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	2.50 BSC		
Overall Width	E	2.00 BSC		
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

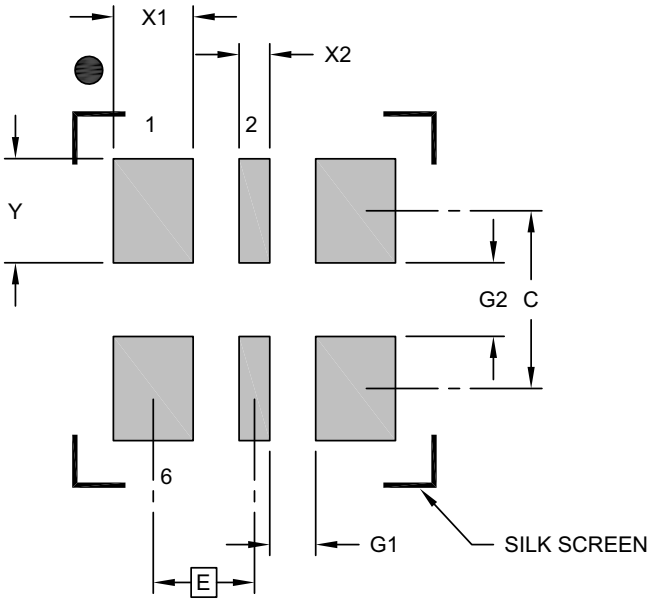
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005A Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.825 BSC		
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3005A

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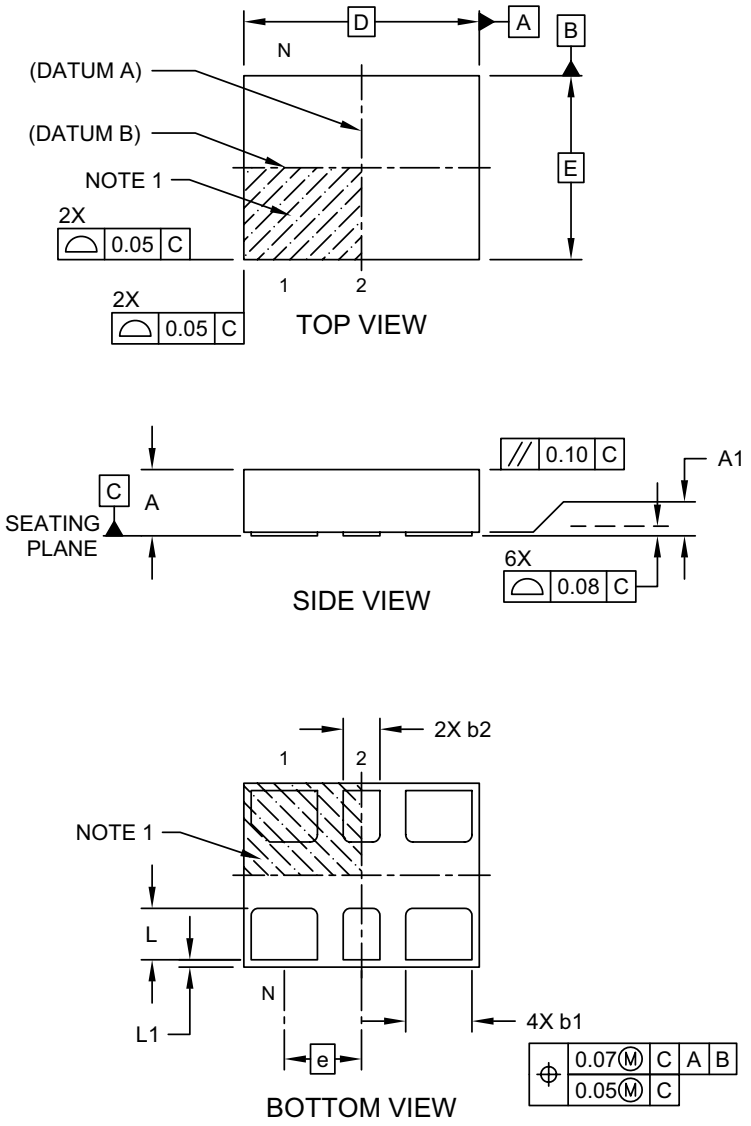
6-Lead VDFN 3.2 mm x 2.5 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

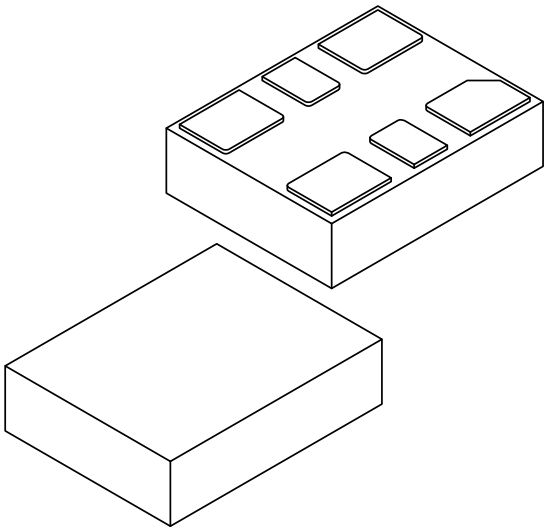
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1007A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	1.05 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	3.20 BSC		
Overall Width	E	2.50 BSC		
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Length	L	0.65	0.70	0.75
Terminal Pullback	L1	0.10 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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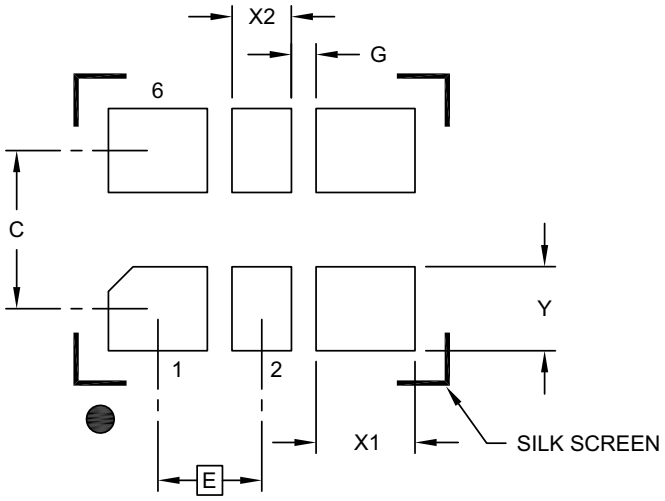
6-Lead Very Thin Plastic Dual Flatpack No-Lead (H5A) - 3.2x2.5 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.05 BSC	
Contact Pad Spacing	C		1.60	
Contact Pad Width (X4)	X1			1.00
Contact Pad Width (X2)	X2			0.60
Contact Pad Length (X6)	Y			0.85
Space Between Contacts (X4)	G1	0.25		

Notes:

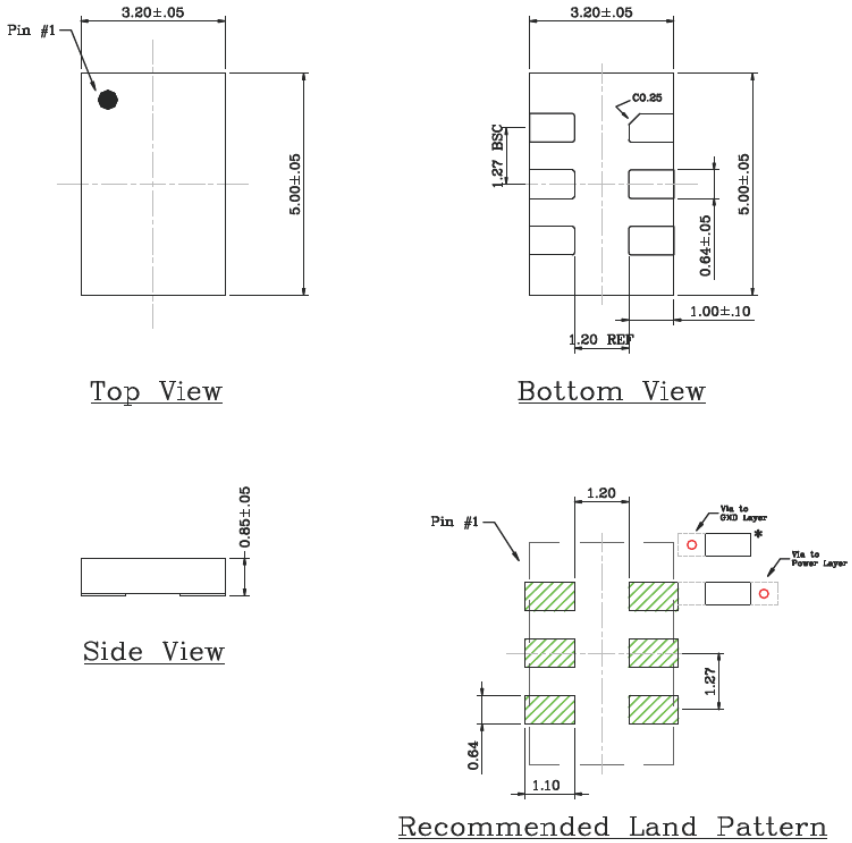
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3007A

6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	CDFN5032-6LD-PL-1	UNIT	MM



NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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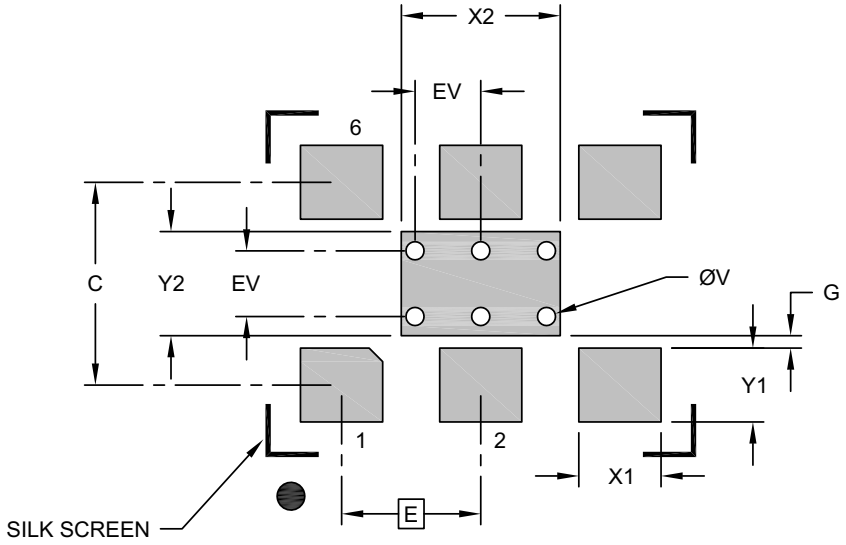
6-Lead VDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.54 BSC		
Optional Center Pad Width	X2			2.90
Optional Center Pad Length	Y2			1.90
Contact Pad Spacing	C		3.70	
Contact Pad Width (X6)	X1			1.50
Contact Pad Length (X6)	Y1			1.35
Contact Pad to Center Pad (X2)	G	0.20		
Thermal Via Diameter (X6)	V		0.33	
Thermal Via Pitch	EV		1.20	

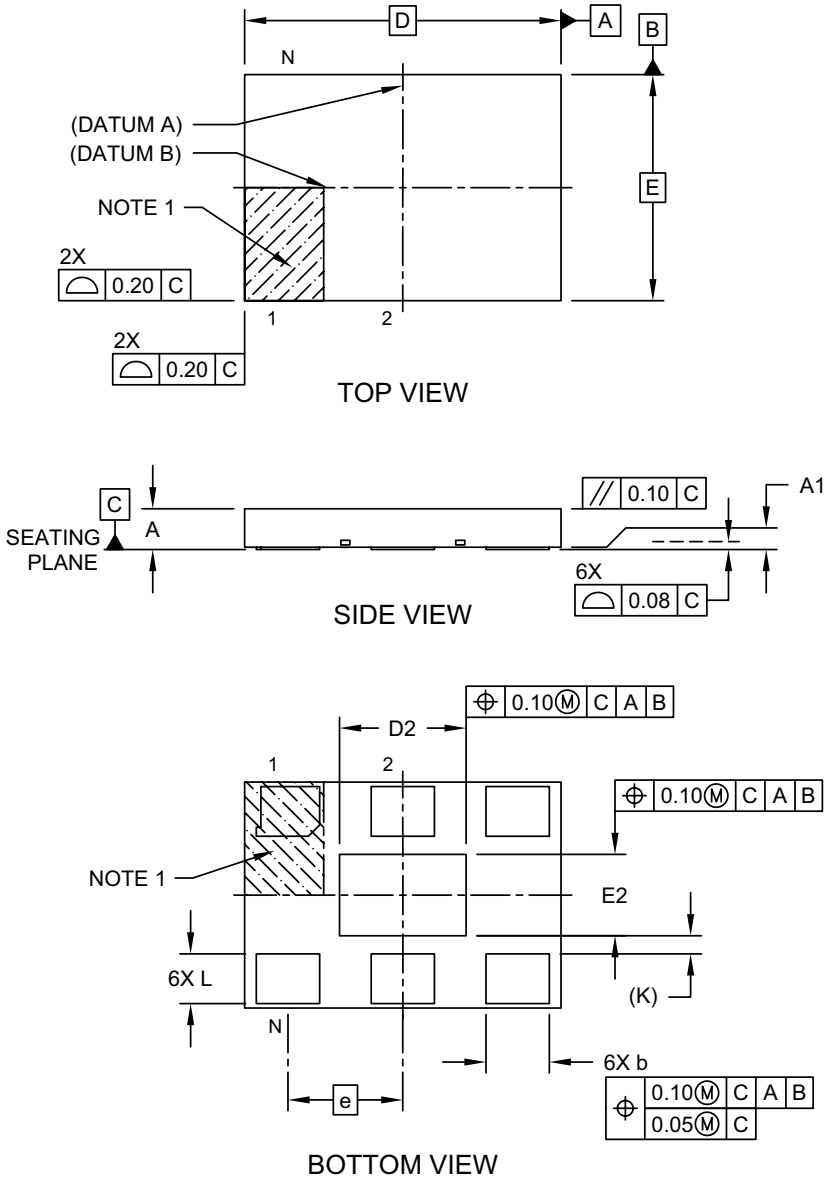
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3010A

6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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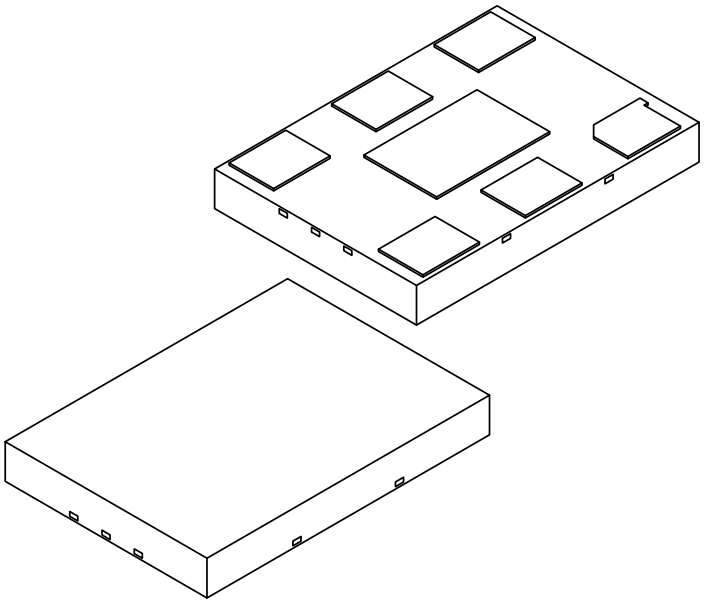
6-Lead Very Thin Plastic Quad Flat, No Lead Package (H8A) - 7x5 mm Body [VDFN] With 2.8x1.8 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	2.54		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D	7.00 BSC		
Exposed Pad Length	D2	2.70	2.80	2.90
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	1.70	1.80	1.90
Terminal Width	b	1.35	1.40	1.45
Terminal Length	L	1.00	1.10	1.20
Terminal-to-Exposed-Pad	K	0.20 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

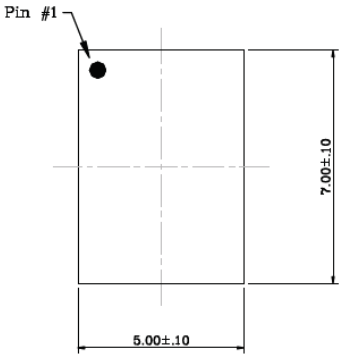
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1010A Sheet 2 of 2

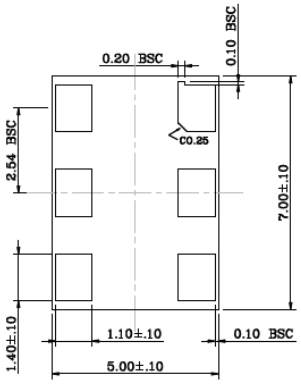
6-Lead CDFN 7.0 mm x 5.0 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 7.0x5.0mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	CDFN75-6LD-PL-1	UNIT	MM

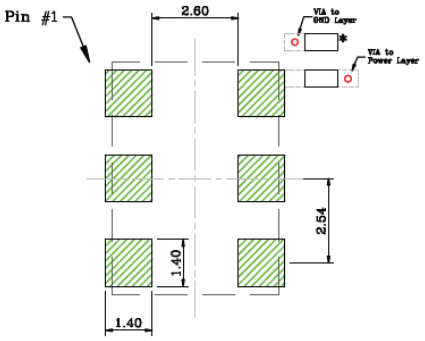


Top View



Bottom View

Side View



Recommended Land Pattern

NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (August 2017)

- Initial creation of document DSC1101/21 to Microchip data sheet template DS20005613A.
- Minor text changes throughout.

Revision B (December 2017)

- Military temperature range changed to Automotive in Features and Product Identification System.
- Supply Current values updated in Table 1-1.
- Test Circuit section removed.
- Updated Figure 6-1, Recommended Board Layout.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XXX.XXXX	X
Device	Package	Temperature Range	Stability	Frequency	Packaging Option

Device:	DSC1101:	Low-Power Precision CMOS Oscillator with Standby	
	DSC1121:	Low-Power Precision CMOS Oscillator	
Package:	A	=	6-Lead 7.0 mm x 5.0 mm VDFN
	B	=	6-Lead 5.0 mm x 3.2 mm CDFN
	C	=	6-Lead 3.2 mm x 2.5 mm VDFN
	D	=	6-Lead 2.5 mm x 2.0 mm VDFN
	N	=	6-Lead 7.0 mm x 5.0 mm CDFN (no center pad)
Temperature Range:	E	=	–20°C to +70°C (Extended Commercial)
	I	=	–40°C to +85°C (Industrial)
	L	=	–40°C to +105°C (Extended Industrial)
	M	=	–55°C to +125°C (Automotive)
Stability:	1	=	±50 ppm
	2	=	±25 ppm
	3	=	±20 ppm
	5	=	±10 ppm
Frequency:	xxx.xxxx	=	2.3 MHz to 170 MHz (user-defined)
Packing Option:	<blank>	=	110/Tube
	T	=	1,000/Reel

Examples:

a) DSC1101AM1-010.0000T:
Low-Power Precision CMOS Oscillator with Standby, 6-LD 7.0X5.0 VDFN, Automotive Temperature Range, ±50 ppm, 10 MHz Output Frequency, 1,000/Reel

b) DSC1101BL2-030.0000:
Low-Power Precision CMOS Oscillator with Standby, 6-LD 5.0X3.2 CDFN, Extended Industrial Temperature Range, ±25 ppm, 30 MHz Output Frequency, 110/Tube

c) DSC1101DE5-150.0000:
Low-Power Precision CMOS Oscillator with Standby, 6-LD 2.5X2.0 VDFN, Extended Commercial Temperature Range, ±10 ppm, 150 MHz Output Frequency, 110/Tube

d) DSC1101AI2-075.0000T:
Low-Power Precision CMOS Oscillator with Standby, 6-LD 7.0X5.0 VDFN, Industrial Temperature Range, ±25 ppm, 75 MHz Output Frequency, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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