AAT2610

7-Channel PMU for Digital Still Cameras

General Description

The AAT2610 is a highly integrated power management solution specifically suited for Digital Still Camera (DSC) systems, featuring seven DC-DC switching regulators for maximum operating efficiency.

The input operating voltage range is 1.6 to 5.5V, making the device an ideal solution for 1-cell Li-ion batteries, 2-cell alkaline batteries, and USB and regulated AC-DC wall adapters. All seven DC-DC switching regulators feature high efficiency light load operating mode to extend battery life while in low power standby state.

Three different DC-DC building blocks provide maximum design flexibility: a boost (step-up) DC-DC controller with an output voltage range of 3.0V to 5.5V and a current mode control buck (step-down) or boost (step-up) DC-DC controller with an output voltage range of 2.5V to the step-up converter (SU) output voltage and buck output range of 0.6V to V_{IN}. Dual current mode control synchronous buck regulators provide low voltage, low noise outputs required for system logic and memory. Output voltage range is 0.6V to V_{IN}. The Auxiliary 1 boost (step-up) is ideally suited for LCD backlight and can drive 1-6 white LEDs with ±10% accuracy. PWM input controls LED dimming across the frequency range from 10% to 100% duty cycle. The integrated OVP and SCF feature protects the device from open-circuit LED conditions.

The Auxiliary 2 boost (step-up) and Auxiliary 3 buck-boost (inverting) output provide low noise (≤30mVpp) +15V and -7.5V outputs for CCD loads. An expensive transformer is not required.

No external MOSFETs and low profile TQFN55-40L package are ideal to save space for DSC solution. Integrated, low $R_{DS(ON)}$ power MOSFETs provide output voltages from 0.6V to 16VDC and an inverting output up to -10V. The high switching frequency ensures small external filtering components. Internal compensation is provided for optimum transient performance and minimum application design effort.

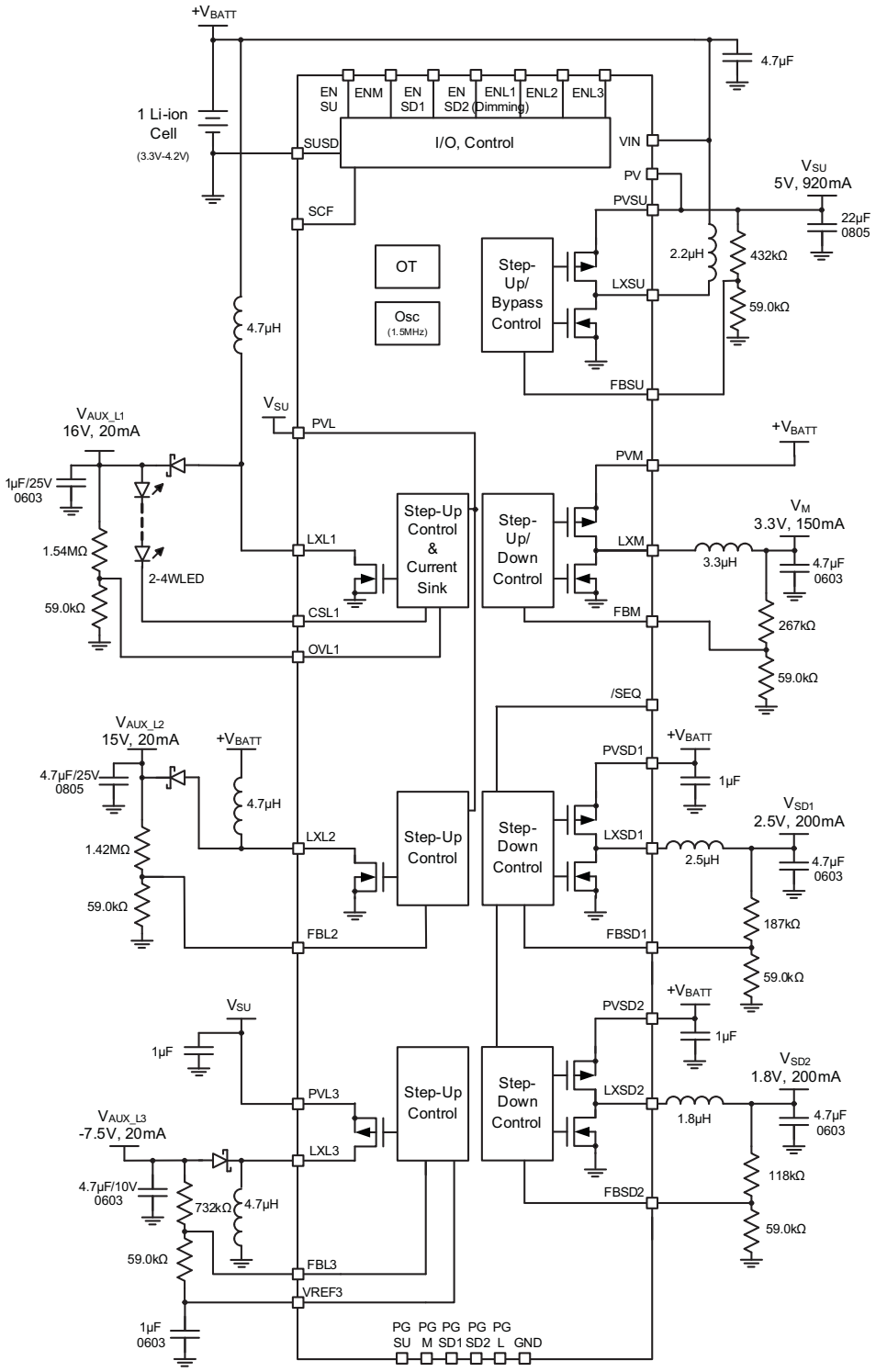
Features

- Input Voltage Range 1.6 to 5.5V
  - 1-Cell Li-ion, 2-Cell Alkaline
  - Adapter or USB Inputs
- 7 Channel up to 96% High Efficiency DC/DCs
  - Adjustable Output
  - 4 Channel Synchronous Rectification
  - Light Load Mode for High Efficiency
- <1µA Total Quiescient Current
- Current Mode Control
  - Fast, Stable Transient Response
  - No External Compensation
  - Current Limit for Internal MOSFET Protection
- High Frequency 1.5MHz System Clock
- High Voltage Series LED Driver
  - 1 to 6 White LEDs
  - External Schottky Diode
  - ±10% Accuracy Current Sink
  - Integrated OVP
  - PWM Dimming: 1k to 30kHz, 10 to 100% Duty Cycle
- Step-Up and Inverting Outputs for CCD
  - Low Noise Outputs
  - Transformerless Inverter Output
- Flexible Sequencing Implementation
  - Independent Enable Control
  - 10ms Pre-Programmed Buck or Boost Delay
- Integrated Soft-Start
- Over-Voltage and Over-Temperature Protection
- Pb-free TQFN55-40L Package
- Temperature Range: -40°C to +85°C

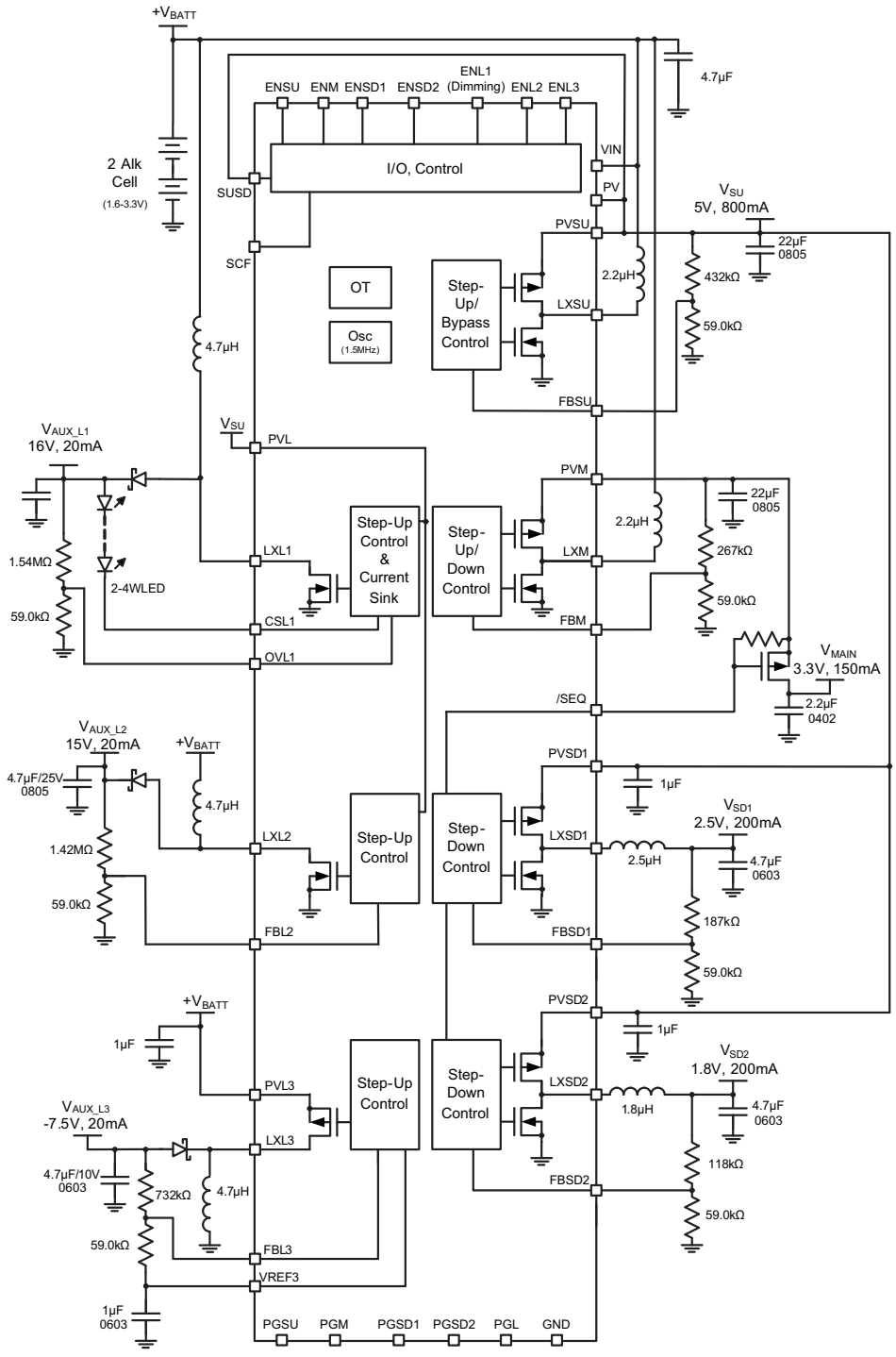
Applications

- DSCs and DVCs
- MP3 Players
- PMP

Typical Applications



1. Single Cell Li-ion Battery Input, 5V Motor.



2. Dual Cell Alkaline Battery Input, 5V Motor.

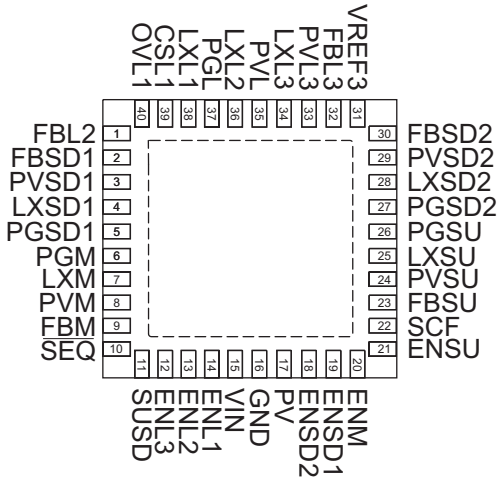
Pin Descriptions

Number	Symbol	Description
1	FBL2	Auxiliary 2 (AUX_L2) boost converter feedback pin. This pin is high impedance when the AUX2 controller is disabled. Connect an external resistor divider between this pin and AUX2 output and GND to set the AUX2 output voltage with 0.6V.
2	FBSD1	Step-down 1 (SD1) buck converter feedback pin. This pin is high impedance when the SD1 controller is disabled. Connect an external resistor divider between this pin and SD1 output and GND to set the SD1 output voltage with 0.6V.
3	PVSD1	Step-down 1 (SD1) buck converter input pin. Bypass to GND plane with a 1µF ceramic capacitor.
4	LXSD1	Step-down 1 (SD1) buck converter switching node. Connect this pin to an external inductor. This pin is high impedance when the SD1 converter is disabled.
5	PGSD1	Step-down 1 (SD1) buck converter power ground. Tie this pin to ground plane.
6	PGM	Main (SUD) converter power ground. Tie this pin to ground plane.
7	LXM	If is SUSD pulled high, the Main is a boost (step-up) converter and the pin functions as the Main converter switching node. In this case, connect this pin to the external inductor. If SUSD is pulled low, the Main is a buck (step-down) converter and the pin functions as the Main converter switching node. In this case, connect this pin to the external inductor. In either case, LXM is high impedance when the Main converter is disabled.
8	PVM	If SUSD is pulled high, the Main is a boost (step-up) converter and this pin functions as the Main converter output. In this case, connect a ceramic capacitor to GND plane from this pin. If SUSD is pulled low, the Main is a buck (step-down) converter and this pin functions as the Main converter input voltage. In this case, connect this pin to the external inductor.
9	FBM	Main (M) buck or boost converter feedback pin. This pin is high impedance when the Main controller is disabled. Connect an external resistor divider between this pin and Main output and GND to set the Main output voltage with 0.6V.
10	$\overline{SEQ}$	Main (M) converter open-drain output sequencing pin. This pin is internally pulled low after both SD1 and SD2 converters completed soft-start and achieved output regulation. This pin can provide gate drive to external P-channel MOSFETs which disconnect the load during start-up. This pin is open-circuit during shut-down, overload or during OT trip conditions.
11	SUSD	Main converter configuration pin. Tie this pin to high to configure the Main output as a boost (step-up) converter, or tie this pin to low to configure the Main output as a buck (step-down) converter. This pin cannot be toggled during operation.
12	ENL3	Auxiliary 3 (AUX_L3) buck-boost (inverting) converter active high enable pin. The AUX_L3 output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. The pin has an internal 330kΩ pull-down resistor.
13	ENL2	Auxiliary 2 (AUX_L2) boost converter active high enable pin. The AUX_L2 output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. The pin has an internal 330kΩ pull-down resistor.
14	ENL1	Auxiliary 1 (AUX_L1) boost converter active high enable pin. The Main output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. The pin has an internal 330kΩ pull-down resistor. This pin also functions as PWM input for the LED dimming feature. The input PWM frequency is logic level high and low within 1kHz to 30kHz frequency. PWM dimming input duty cycle (ON-time/TOTAL-time) range is from 10% to 100%.
15	VIN	Input voltage. Tie this pin to the input of step-up (SU).
16	GND	Chip ground. Tie this pin to ground plane.
17	PV	Power input for the PMIC. Connect this pin directly to the PVSU pin.
18	ENSD2	Step-down 2 (SD2) buck converter active high enable pin. The SD2 output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. This pin has an internal 330kΩ pull-down resistor.
19	ENSD1	Step-down 1 (SD1) buck converter active high enable pin. The SD1 output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. This pin has an internal 330kΩ pull-down resistor.
20	ENM	Main buck or boost converter active high enable pin. However, the Main output remains disabled until 2,048 clock cycles after Step-Up (SU) output has reached regulation. This pin has an internal 330kΩ pull-down resistor.
21	ENSU	Step-up (SU) boost converter active high enable pin. This pin has an internal 330kΩ pull-down resistor.

Pin Descriptions

Number	Symbol	Description
22	SCF	Open drain, active low, short circuit flag output. SCF goes open when overload protection or AUX_L1 open circuit occur during abnormal operation or during startup. SCF can drive P-channel MOSFETs to disconnect a given output from the load.
23	FBSU	Step-up (SU) boost converter feedback pin. This pin is high impedance when the SU controller is disabled. Connect an external resistor divider between this pin and SU output and GND to set the SU output voltage with 0.6V.
24	PVSU	Step-up (SU) boost converter input.
25	LXSU	Step-up (SU) boost converter switching node. Connect this pin to the external inductor and anode of the Schottky rectifying diode. This pin is high impedance when the SU converter is disabled.
26	PGSU	Step-up (SU) boost converter power ground. Tie this pin to ground plane.
27	PGSD2	Step-down 2 (SD2) buck converter power ground pin. Tie this pin to ground plane.
28	LXSD2	Step-down 2 (SD2) buck converter switching node. Connect this pin to an external inductor. This pin is high impedance when the SD2 converter is disabled.
29	PVSD2	Step-down 2 (SD2) buck converter input pin. Bypass this pin to GND plane with a 1µF ceramic capacitor.
30	FBSD2	Step-down 2 (SD2) buck converter feedback pin. This pin is high impedance when the SD2 controller is disabled. Connect an external resistor divider between this pin and SD2 output and GND to set the SD2 output voltage with 0.6V.
31	VREF3	Auxiliary 3 (AUX_L3) buck/boost (inverting) reference voltage pin. Bypass VREF3 to GND with a 1µF or greater capacitor. Connect an external resistor divider between this pin and L3 output and FBL with 0.6V.
32	FBL3	Auxiliary 3 (AUX_L3) boost converter feedback pin. The pin is high impedance when the AUX_L3 controller is disabled. Connect an external resistor divider between this pin and AUX_L3 output and VREF3 pin to set the AUX_L3 negative buck/boost (inverting) output voltage with 0V.
33	PVL3	Auxiliary 3 (AUX_L3) buck/boost (inverting) input node. Connect this pin to the input ceramic capacitor.
34	LXL3	Auxiliary 3 (AUX_L3) buck/boost (inverting) switching node. Connect this pin to the cathode of the external Schottky diode and buck/boost inductor.
35	PVL	Power input for auxiliary (AUX_L1, AUX_L2, AUX_L3) channels' power FET driver. Tie this pin to PVSU.
36	LXL2	Auxiliary 2 (AUX_L2) boost (step-up) switching node. Connect this pin to the anode of the external Schottky diode and boost inductor.
37	PGL	Power ground for auxiliary (AUX_L1, AUX_L2, AUX_L3) channels' power FET driver. Tie this pin to ground plane.
38	LXL1	Auxiliary 1 (AUX_L1) boost (step-up) switching node. Connect this pin to the anode of the external Schottky diode and boost inductor.
39	CSL1	Auxiliary 1 (AUX_L1) boost converter current sink pin. The pin is high impedance when the AUX_L1 controller is disabled. Connect this pin to the cathode of the bottom LED in the string to ensure DC current flow. Current level is programmed by the internal RSET resistor from 1 to 20mA.
40	OVL1	Auxiliary 1 (AUX_L1) boost (step-up) over-voltage protection pin. Connect an external resistor divider between this pin and AUX_L1 output voltage and GND to set the AUX_L1 over-voltage threshold with 0.6V.
EP		Exposed pad (bottom). Connect to ground directly beneath the package for thermal dissipation.

Pin Configuration



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
	All other pins to GND/PGND	-0.3 to 6.0	V
	Voltage from LXL1, LXL2 to GND/PGND	-0.3 to 30.0	V
	Voltage from LXL3 to GND/PGND	-8.0 to 6.0	V
	Operating Junction Temperature Range	-40 to 150	°C
	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information[2]

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation[3]	2.0	W
θ_{JA}	Maximum Thermal Resistance	25.0	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on 1.6mm thick FR4 circuit board.
3. Derate 40mW/°C above 2°C ambient temperature

Electrical Characteristics[1]

Unless otherwise noted V_{PVSU} = V_{PVM}= V_{PVSD1} = V_{PVSD2} = 3.6V, T_A =-40°C to +85°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
General						
V_{IN}	Operating Input Voltage Range	I_{LOAD} ≤ Full Load (see Tables 1 and 2)	1.6		5.5	V
I_{SHDN}	Shutdown Supply Current	EN_SU = EN_M = EN_SD1 = EN_SD2 = 0V, EN_DL1 = EN_DL2 = EN_DL3 = 0V		0.01	10	µA
I_Q	Quiescient Current into PV Pin with SU Enabled	EN_SU = 3.6V, FBSU = 1.5V (does not include switching losses)		300	450	µA
	Quiescient Current into PV Pin with SU/SD1/SD2 Enabled	EN_SU = EN_SD1 = EN_SD2 = 3.6V, FBSU = FBSD1 = FBSD2 = 1.5V, EN_M = EN_DL1 = EN_DL2 = EN_DL3 = 0V (does not include switching losses)		600	900	µA
	Quiescient Current into PV Pin with SU/SUD Enabled	EN_SU = EN_M = 3.6V, FBSU = FBSUD = 1.5V, EN_SD1 = EN_SD2 = EN_DL1 = EN_DL2 = EN_DL3 = 0 (does not include switching losses)		450	700	µA
	Quiescient Current into PV Pin with	EN_SU = EN_DL1 = 3.6V, FBSU = FBL1 = 1.5V, EN_M = EN_SD1 = EN_SD2 = EN_DL1 = EN_DL2 = EN_DL3 = 0(does not include switching losses)		400	650	µA
Oscillator						
F_{OSC}	Oscillator Frequency Range		1.2	1.5	1.8	MHz
SU DC-DC Boost (Step-Up) Converter						
$V_{UVLO(SU)}$	SU Under-Voltage Threshold	Rising edge	1.6	1.8	2.0	V
$V_{UVLO(SU),HYS}$	SU Under-Voltage Threshold Hysteresis	Falling edge		400		mV
$V_{OUT(SU)}$	Step-Up Output Voltage Range		3.0		5.5	V
$V_{IN(BP-ENTER)}$	Enter Bypass Mode	V_{IN} Rising edge	4.625	4.750	4.900	V
$V_{IN-HYS(BP-EXIT)}$	Exit Bypass Mode - Hysteresis	V_{IN} Falling edge	100	112	125	mV
t_{DELAY}	Start-Up Delay of SUSD, SD1, SD2, AUX_L1, AUX_L2, AUX_L3 after VSU in Regulation			512		OSC Cyc
V_{FBSU}	FBSU Reference Voltage	T_A = 25°C	0.588	0.600	0.612	V
$I_{MODE(SU)}$	SU Light Load Mode Current Threshold			200		mA
$D_{MAX(SU)}$	Step-Up Maximum Duty Cycle	1.6 ≤ V_{PVSU} ≤ 5.0V, V_{FBSU} = 0.60V	85	95		%
$I_{LEAK(FBSU)}$	FBSU Pin Leakage Current	V_{FBSU} = 0.60V	-100	0.01	+100	nA
$I_{LEAK(PVSU)}$	PVSU Pin Leakage Current	V_{LXSU} = 0V, V_{PVSU} = 5.5V		0.1	5	µA
$I_{LEAK(LXSU)}$	LXSU Pin Leakage Current	V_{LXSU} = $V_{OUT(SU)}$ = 5.5V		0.1	5	µA
R_{DSON}	N-Channel			50		mΩ
	P-Channel			130		mΩ
I_{LIMIT}	N-Channel Current Limit		4.1	4.8		A
I_{OFF}	P-Channel Turn-Off Current			20		mA
$I_{STARTUP}$	Startup Current Limit	V_{PVSU} = 1.8V		750		mA
$T_{OFF(STARTUP)}$	Startup Off-Time	V_{PVSU} = 1.8V		700		ns
$F_{OSC(STARTUP)}$	Startup Frequency	V_{PVSU} = 1.8V		200		kHz

1. The AAT2610 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Electrical Characteristics[1]

Unless otherwise noted V_{PVSU}=V_{PVM}= V_{PVSD1}= V_{PVSD2} =3.6V, T_A=-40°C to +85°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Main DC-DC Buck (Step-Down) or Boost (Step-Up) Converter						
$V_{OUT(M)}$	Main Output Step-Up Voltage Range	V_{SUSD} = V_{PVSU}	3.0		5.5	V
	Main Output Step-Down Voltage Range	V_{SUSD} = GND; V_{PVM} must be greater than $V_{OUT(M)}$	1.0		V_{IN}	V
V_{FBM}	FBM Reference Voltage	T_A = 25°C	0.59	0.60	0.61	V
$I_{LIMIT(M)}$	Step-Up Mode Current Limit	V_{SUSD} = V_{PVSU}	1.5	1.75		A
	Step-Down Mode Current Limit	V_{SUSD} = GND	0.7	0.85		A
$I_{MODE(M)}$	Step-Up Light Load Mode Current Threshold	V_{SUSD} = V_{PVSU}		200		mA
	Step-Down Light Load Mode Current Threshold	V_{SUSD} = GND		100		mA
$D_{MAX(M)}$	Step-Up Maximum Duty Cycle	1.6 ≤ V_{IN} ≤ 5.0V, V_{SUSD} = V_{PVSU}	80	95		%
	Step-Down Maximum Duty Cycle	1.6 ≤ V_{IN} ≤ 5.0V, V_{SUSD} = GND	100			
$I_{LEAK(FBM)}$	FBM Pin Leakage Current	V_{FBSU} = 0.6V	-100	0.01	+100	nA
$I_{LEAK(LXM)}$	LXM Pin Leakage Current	V_{LXSU} = $V_{OUT(M)}$ = 5.5V		0.1	5	µA
R_{DSON}	N-Channel			75		mΩ
	P-Channel			120		mΩ
$I_{OFF(M)}$	Step-Up Mode N-Channel Turn-Off Current	V_{SUSD} = V_{PVSU}		20		mA
	Step-Down Mode N-Channel Turn-Off Current	V_{SUSD} = GND		20		
$t_{SOFT-START}$	Soft-Start Interval			2,048		OSC Cyc
T_{SEQ}	Sequencing Time Delay	SD1/SD2 Regulation to $V_{SEQ(L)}$ Transition		10,000		OSC Cyc
$I_{LEAK(SEQ)}$	SEQ Pin Leakage Current	EN_SU = V_{PVSU}, FBSU = 1.5V		0.1	1	µA
$V_{SEQ(L)}$	SEQ Low Output Voltage	0.1mA into SEQ pin		0.01	0.1	V
SD1/2 DC-DC Step-Down (Buck) Converters						
$V_{OUT(SD1/SD2)}$	SD1/SD2 Step-Down Output Voltage Range		0.60		V_{IN}	V
$V_{FB(SD1/SD2)}$	FBSD1, FBSD2 Reference Voltage	T_A = 25°C	0.59	0.60	0.61	V
$I_{LIMIT(SD1/SD2)}$	P-Channel Current Limit		0.6	0.7		A
$I_{MODE(SD1/SD2)}$	SD1 Light Load Mode Current Threshold			100		mA
$D_{MAX(SD1/SD2)}$	Maximum Duty Cycle	1.6 ≤ V_{PVSU} ≤ 5.0V, $V_{SD1/2}$ = 0.60V	100			%
$I_{LEAK(FBSD1/SD2)}$	FBSD1, FBSD2 Pin Leakage Current	$V_{FBSD1/SD2}$ = 0.6V	-100	0.01	+100	nA
$I_{LEAK(LXSD1/SD2)}$	LXSD1, LXSD2 Pin Leakage Current	$V_{LXSD1/SD2}$ = 0 to 3.6V		0.1	5	µA
$R_{DSON(SD1)}$	N-Channel			500		mΩ
	P-Channel			650		mΩ
$R_{DSON(SD2)}$	N-Channel			250		mΩ
	P-Channel			450		mΩ
I_{OFF}	N-Channel Turn-Off Current			20		mA
$T_{SOFTSTART}$	Soft-Start Interval			2,048		OSC Cyc

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Electrical Characteristics[1]

Unless otherwise noted V_{PVSU}=V_{PVM}= V_{PVSD1}= V_{PVSD2} =3.6V, T_A=-40°C to +85°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
AUX L1/L2 DC-DC Boost (Step-Up) Converters						
$V_{OUT(AUX_L1/L2)}$	AUX_L1/L2 Step-Up Output Voltage Range[2]		5.0		20.0	V
I_{CSL1}	CSL1 Current Sink Accuracy	T_A = 25°C	18.0	20.0	22.0	mA
V_{FBL2}	FBL2 Reference Voltage	T_A = 25°C	0.59	0.60	0.61	V
V_{OVL1}	OVL1 Reference Voltage	T_A = 25°C	0.59	0.60	0.61	V
$I_{LIMIT(AUX_L1)}$	N-Channel Current Limit		0.60	0.70		A
$I_{LIMIT(AUX_L2)}$	N -Channel Current Limit		0.60	0.70		A
$I_{MODE(AUX_L1/L2)}$	AUX_L1/L2 Light Load Mode Current Threshold			100		mA
$D_{MAX(L1/L2)}$	Maximum Duty Cycle		95			%
$I_{LEAK(FBL2)}$	FBL2 Pin Leakage Current		-100	0.01	+100	nA
$R_{DSON(AUX_L1)}$	N-Channel			1000		mΩ
$R_{DSON(AUX_L2)}$	N-Channel			1000		mΩ
$T_{SOFTSTART(AUX_L2)}$	AUX_L2 Soft-Start Interval			2,048		OSC Cyc
AUX L3 DC-DC Buck/Boost (Inverter) Converters						
V_{REF3}	REF3 Reference Voltage	T_A = 25°C, I_{REF} = 20µA	0.59	0.60	0.61	V
V_{FBL3}	FBL3 Inverter Reference Voltage	T_A = 25°C	-0.01	0.00	0.01	V
$I_{LIMIT(AUX_L3)}$	P-Channel Current Limit			1.5		A
$I_{MODE(AUX_L3)}$	SD1 Light Load Mode Current Threshold			100		mA
$I_{LEAK(REF3,FBL3)}$	REF3, FBL3 Pin Leakage Current		-100	0.01	+100	nA
R_{DSON}	P-Channel			1000		mΩ
$t_{SOFTSTART}$	Soft-Start Interval			2,048		OSC Cyc
Overload Protection						
$t_{DELAY(\overline{SCF})}$	Overload Fault Delay			100,000		OSC Cyc
$I_{LEAK(\overline{SCF})}$	$\overline{SCF}$ Pin Leakage Current	EN_SU = V_{PVSU}, FBSU = 1.5V		0.1	1	µA
$V_{L(\overline{SCF})}$	$\overline{SCF}$ Low Output Voltage	0.1mA into SCF pin		0.01	0.1	V
Thermal Protection						
T_{SD}	Over-Temperature Shutdown			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

1. The AAT2610 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. The Step-Up converter operates in startup mode until this voltage is reached. Do not apply full load current during startup.

Electrical Characteristics[1]

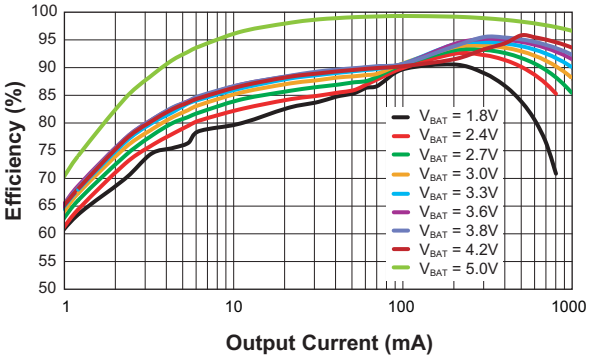
Unless otherwise noted V_{PVSU}=V_{PVM}= V_{PVSD1}= V_{PVSD2} =3.6V, T_A=-40°C to +85°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Logic Inputs						
$V_{L(EN_SU)}$	EN_SU Logic Low Threshold	1.1V < V_{PVSU} < 1.8V			0.2	V
		1.8V ≤ V_{PVSU} < 2.5V			0.4	V
		2.5V ≤ V_{PVSU} < 5.5V			0.5	V
$V_{H(EN_SU)}$	EN_SU Logic High Threshold	1.1V < V_{PVSU} < 1.8V	(V_{PVSU} - 0.2)			V
		1.8V < V_{PVSU} < 5.5V	1.6			V
$V_{EN_x(L)}$, $V_{SUSD(L)}$	EN_x, SUSD Logic Low Threshold	2.7V < V_{PVSU} < 5.5V			0.5	V
$V_{EN_x(H)}$, $V_{SUSD(H)}$	EN_x, SUSD Logic Low Threshold	2.7V < V_{PVSU} < 5.5V	1.6			V
$I_{LEAK(SUSD)}$	SUSD Pin Leakage Current			0.1	1	µA
R_{ENx}	ENx Input Impedance			330		kΩ
$T_{EN_L1(L)}$	Disable Low Time	Dimming state: EN low to LED Disable; 2.7V < V_{IN} < 5V	2	3	4	µs
$T_{EN_L1(H)}$	Enable High Time	Dimming state: EN high to LED Regulation; 2.7V < V_{IN} <5V	2	3	4	µs
$T_{EN_L1(DIS-L)}$	Disable Low Time	Disables Dimming state: Soft-start enabled on subsequent EN transition; 2.7V < V_{IN} < 5V	1000		1200	µs

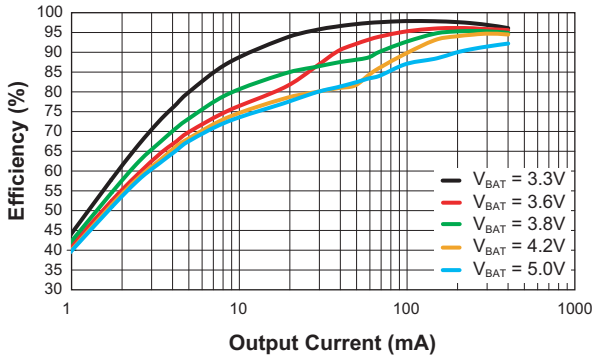
1. The AAT2610 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

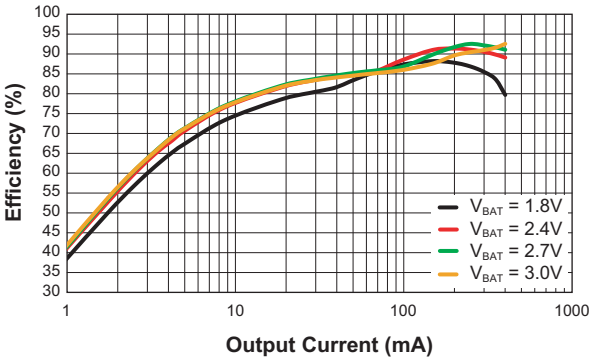
SU Efficiency vs. Output Current
(V_{SU} = 5V; L = 2.2µH; C_{OUT} = 22µF)



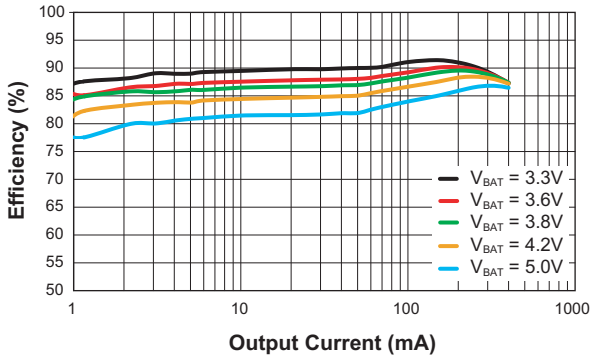
MSD Efficiency vs. Output Current
(V_{PVM} = V_{BAT}; V_{MSD}= 3.3V; L = 3.3µH; C_{OUT} = 4.7µF)



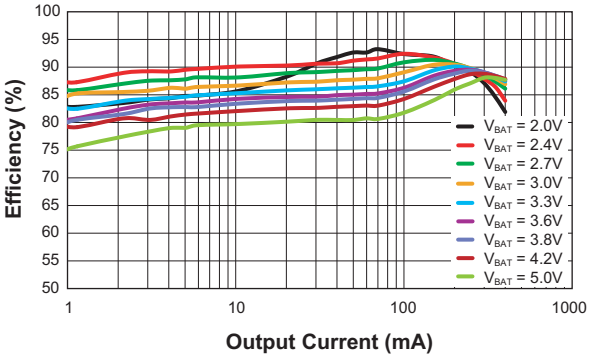
MSU Efficiency vs. Output Current
(V_{MSU} = 3.3V; L = 2.2µH; C_{OUT} = 10µF)



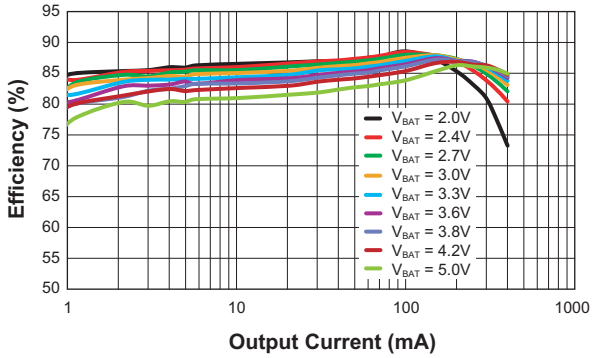
SD1 Efficiency vs. Output Current
(V_{PVSD1} = V_{BAT}; V_{SD1} = 2.5V; L = 2.2µH; C_{OUT} = 10µF)



SD2 Efficiency vs. Output Current
(V_{PVSD2} = V_{BAT}; V_{SD2} = 1.8V; L = 2.2µH; C_{OUT} = 4.7µF)

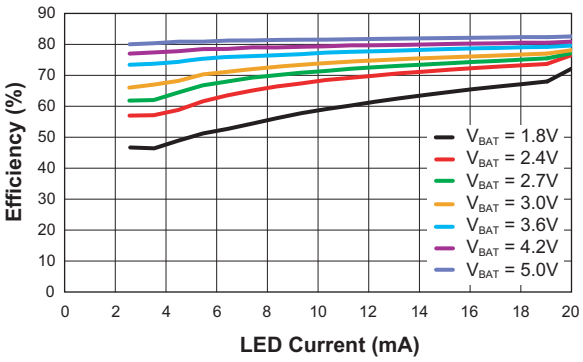


SD2 Efficiency vs. Output Current
(V_{SD2} = 1.2V; L = 2.2µH; C_{OUT} = 4.7µF)

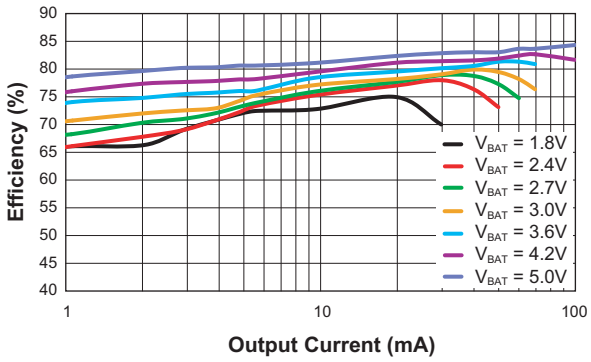


Typical Characteristics

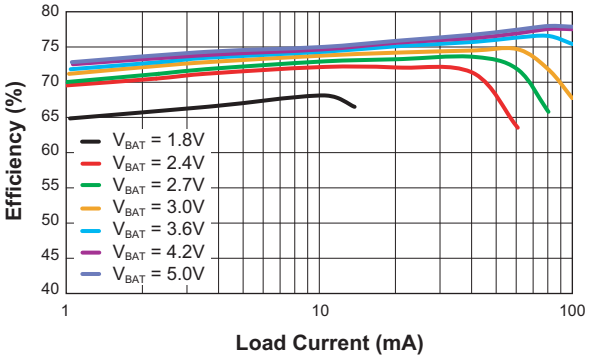
AUX1 Efficiency vs. PWM Duty Cycle
(4 WLEDs; L = 4.7µH; C_{OUT} = 1µF; 10kHz PWM Control)



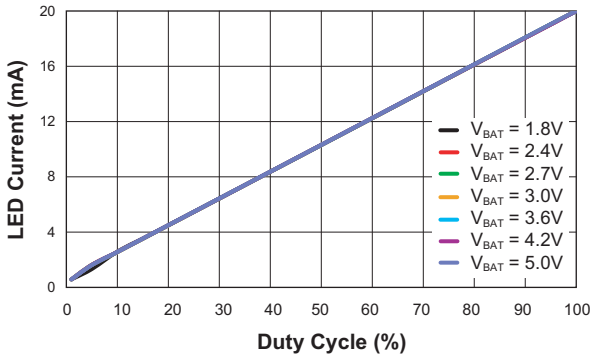
AUX2 Efficiency vs. Output Current
(V_{AUX2} = +15V; L = 4.7µH; C_{OUT} = 4.7µF)



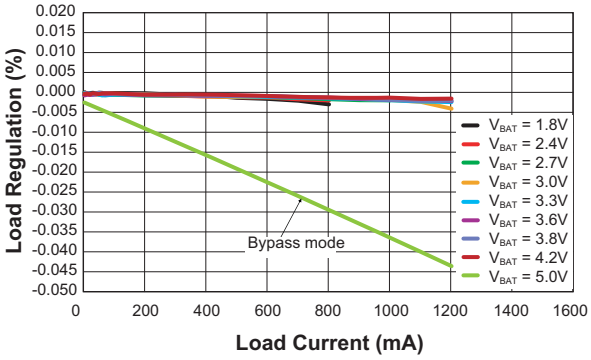
AUX3 Efficiency vs. Output Current
(V_{AUX3} = -7.5V; L = 4.7µH; C_{OUT} = 4.7µF)



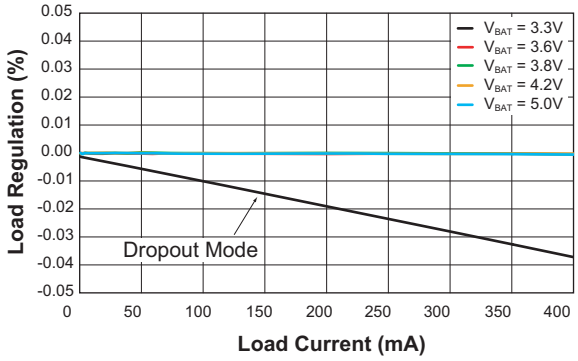
AUX1 PWM Duty Cycle vs. LED Current
(4 WLEDs; L = 4.7µH; C_{OUT} = 1µF; 10kHz PWM Control)



SU Load Regulation vs. Output Current
(V_{SU} = 5V; L = 2.2µH; C_{OUT} = 22µF)

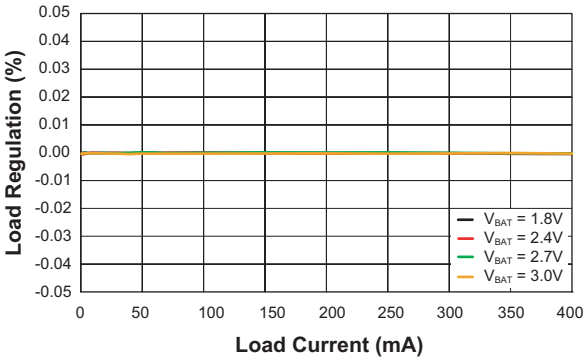


Main SD Load Regulation vs. Output Current
(V_{PVM} = V_{BAT}; V_{MSD} = 3.3V; L = 3.3µH; C_{OUT} = 4.7µF)

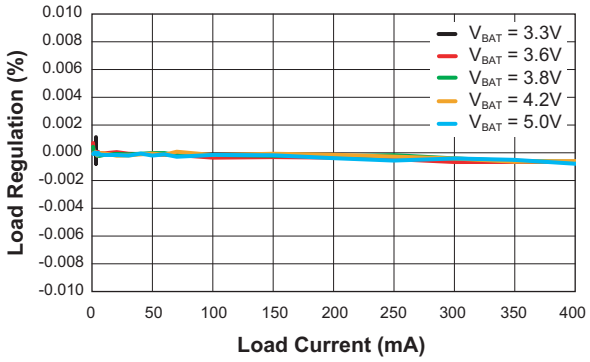


Typical Characteristics

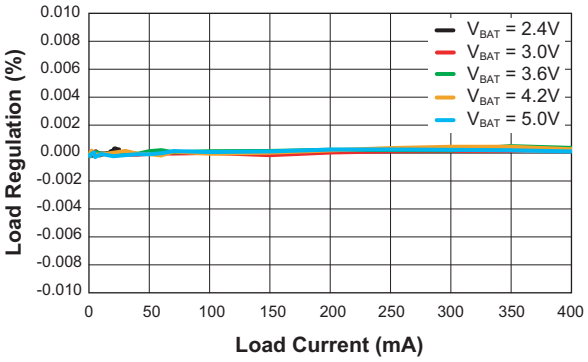
Main SU Load Regulation vs. Output Current
(V_{MSU} = 3.3V; L = 2.2µH; C_{OUT} = 10µF)



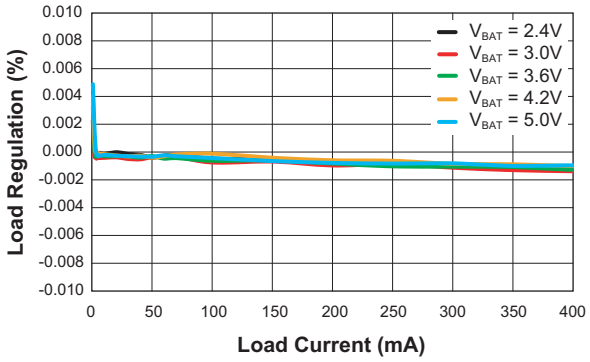
SD1 Load Regulation vs. Output Current
(V_{PVSD1} = V_{BAT}; V_{SD1} = 2.5V: L = 2.2µH; C_{OUT} = 10µF)



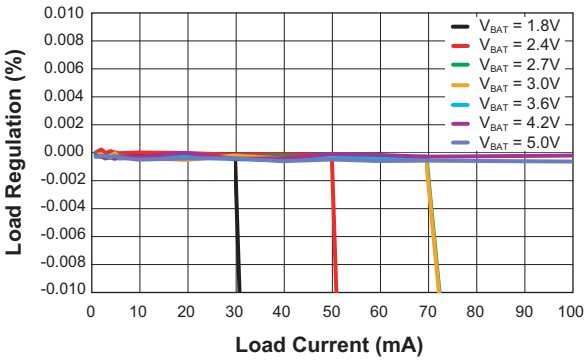
SD2 Load Regulation vs. Output Current
(V_{PVSD2} = V_{BAT}; V_{SD2} = 1.8V: L = 2.2µH; C_{OUT} = 4.7µF)



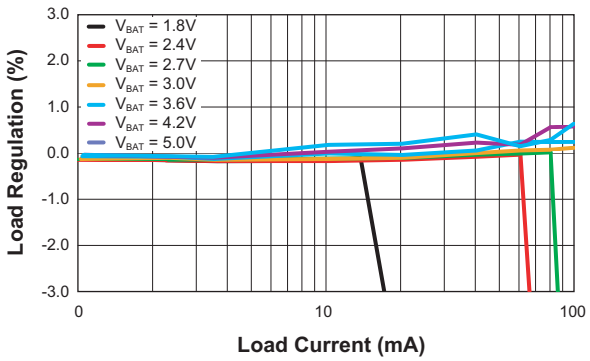
SD2 Load Regulation vs. Output Current
(V_{SD2} = 1.2V: L = 2.2µH; C_{OUT} = 4.7µF)



AUX2 Load Regulation vs. Output Current
(V_{AUX2} = +15V; L = 4.7µH; C_{OUT} = 4.7µF)

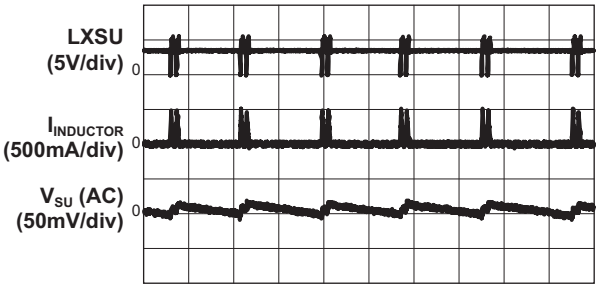


AUX3 Load Regulation vs. Output Current
(V_{AUX3} = -7.5V; L = 4.7µH; C_{OUT} = 4.7µF)



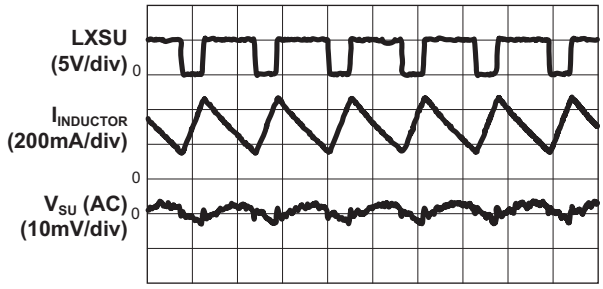
Typical Characteristics

SU Output Ripple
(V_{BAT} = 3.6V; V_{SU} = 5V; C_{OUT} = 22µF; 10mA Load)



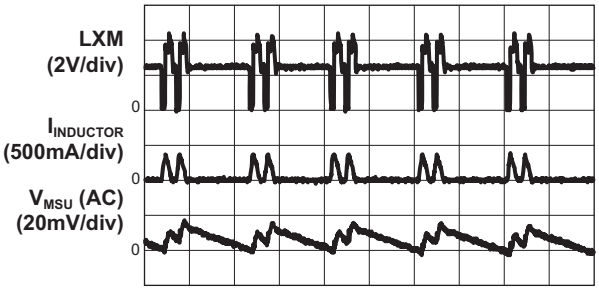
Time (10µs/div)

SU Output Ripple
(V_{BAT} = 3.6V; V_{SU} = 5V; L = 2.2µH;
C_{OUT} = 22µF; 200mA Load)



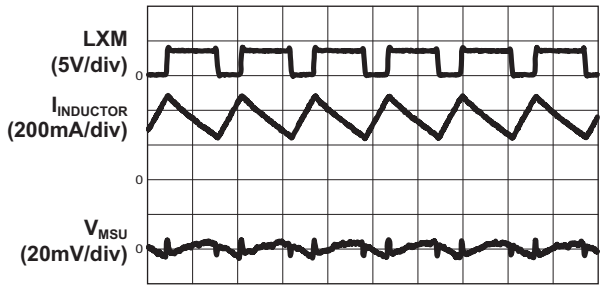
Time (400ns/div)

Main SU Output Ripple
(V_{BAT} = 2.4V; V_{MSU} = 3.3V; L = 2.2µH;
C_{OUT} = 10µF; 10mA Load)



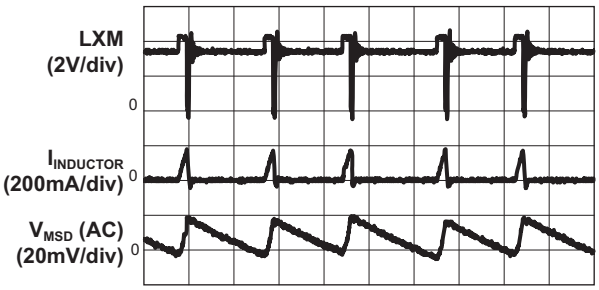
Time (4µs/div)

Main SU Output Ripple
(V_{BAT} = 2.4V; V_{MSU} = 3.3V; L = 2.2µH;
C_{OUT} = 10µF; 200mA Load)



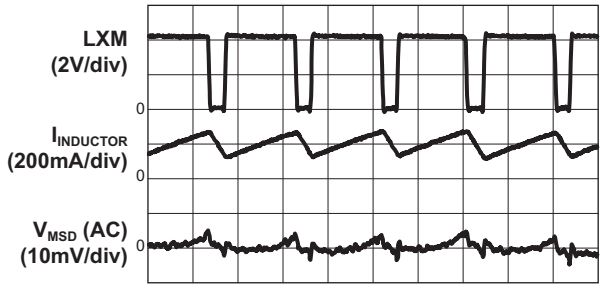
Time (400ns/div)

Main SD Output Ripple
(V_{PVM} = V_{BAT} = 4.2V; V_{MSD} = 3.3V; L = 3.3µH;
C_{OUT} = 4.7µF; 10mA Load)



Time (4µs/div)

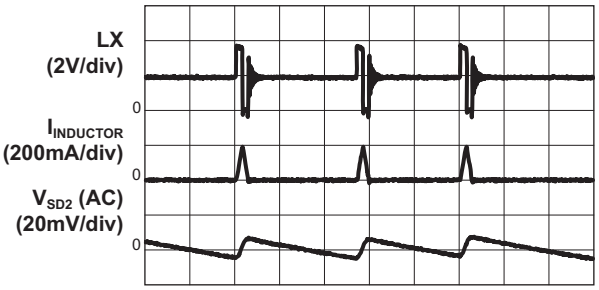
Main SD Output Ripple
(V_{PVM} = V_{BAT} = 4.2V; V_{MSD} = 3.3V; L = 3.3µH;
C_{OUT} = 4.7µF; 200mA Load)



Time (4µs/div)

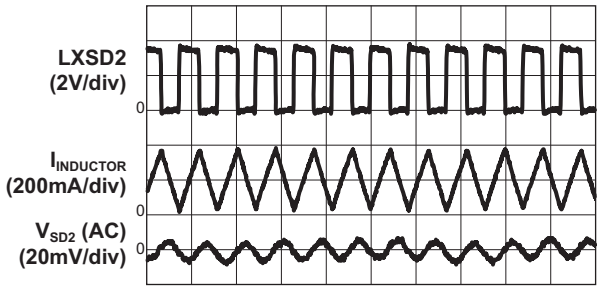
Typical Characteristics

SD Output Ripple
(V_{PSD2} = V_{BAT} = 3.6V; V_{SD2} = 1.8V; L = 2.2µH;
C_{OUT} = 4.7µF; 10mA Load)



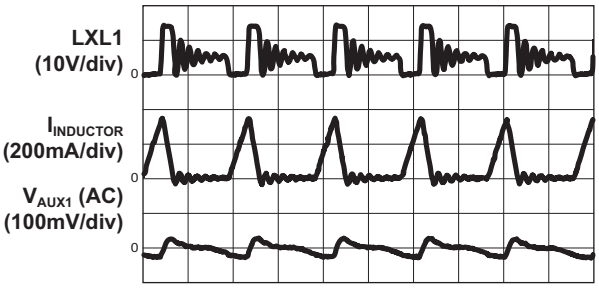
Time (2µs/div)

SD Output Ripple
(V_{PVSD2} = V_{BAT} = 3.6V; V_{SD2} = 1.8V; L = 2.2µH;
C_{OUT} = 4.7µF; 200mA Load)



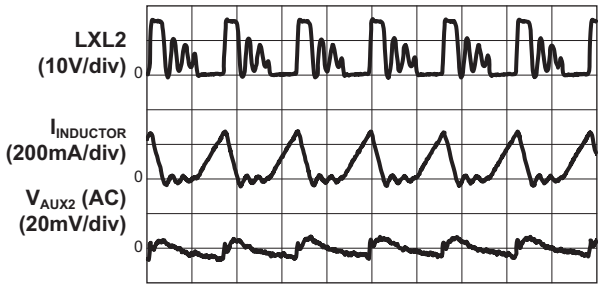
Time (800ns/div)

AUX1 Output Ripple
(V_{BAT} = 3.6V; C_{OUT} = 1µF; L = 4.7µH;
4 WLED with 20mA Load)



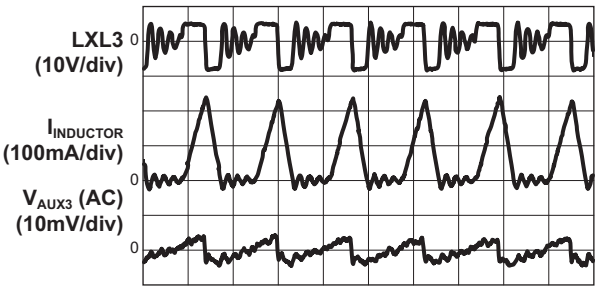
Time (400ns/div)

AUX2 Output Ripple
(V_{BAT} = 3.6V; V_{AUX2} = 15V; C_{OUT} = 4.7µF/25V;
L = 4.7µH; 20mA Load)



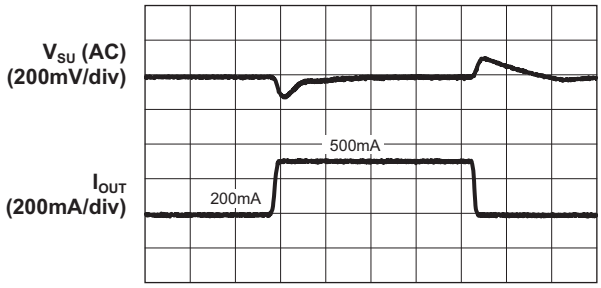
Time (400ns/div)

AUX3 Output Ripple
(V_{BAT} = 3.6V; V_{AUX3} = -7.5V; C_{OUT} = 4.7µF/10V;
L = 4.7µH; 20mA Load)



Time (400ns/div)

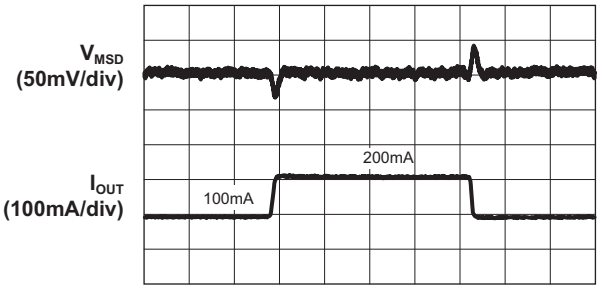
SU Channel Load Transient Response
(V_{BAT} = 3.6V; V_{SU} = 5V; L = 2.2µH; C_{OUT} = 22µF;
Transient Slew Rate 0.1A/µs)



Time (40µs/div)

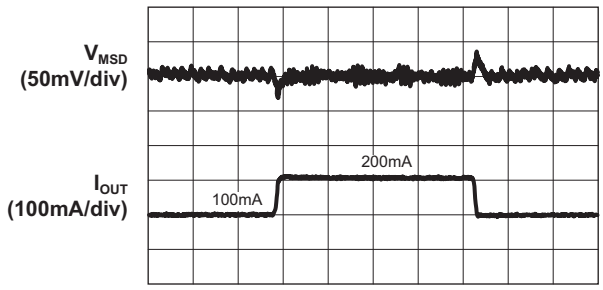
Typical Characteristics

Main SD Load Transient Response
(V_{BAT} = V_{PVM} = 3.6V; V_{MSD} = 3.3V; L = 3.3µH;
C_{OUT} = 4.7µF; Transient Slew Rate = 0.1A/µs)



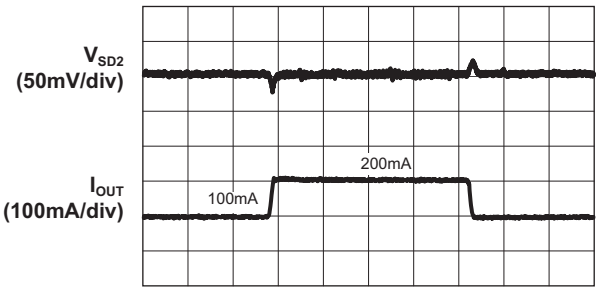
Time (40µs/div)

SD1 Load Transient Response
(V_{BAT} = V_{PVSD1} = 3.6V; V_{SD1} = 2.5V; L = 2.2µH;
C_{OUT} = 10µF; Transient Slew Rate = 0.1A/µs)



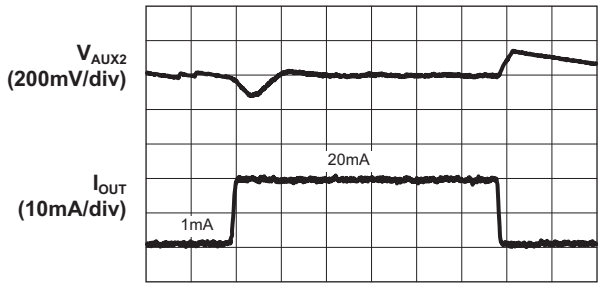
Time (40µs/div)

SD2 Load Transient Response
(V_{BAT} = V_{PVSD2} = 3.6V; V_{SD2} = 1.8V; L = 2.2µH;
C_{OUT} = 4.7µF; Transient Slew Rate = 0.1A/µs)



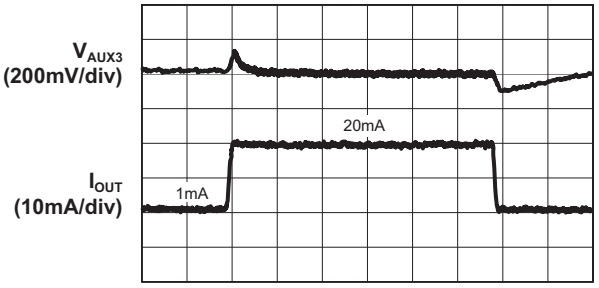
Time (40µs/div)

AUX2 Load Transient Response
(V_{BAT} = 3.6V; V_{AUX2} = 15V; L = 4.7µH;
C_{OUT} = 4.7µF/25V; Transient Slew Rate = 0.1A/µs)



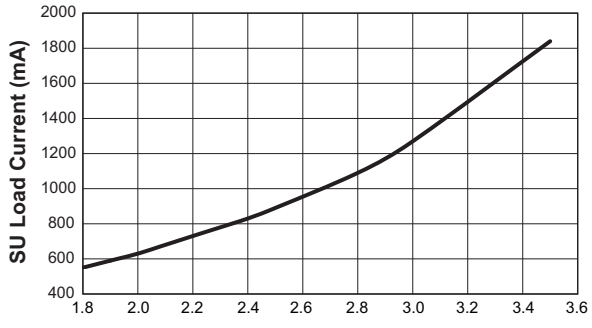
Time (40µs/div)

AUX3 Load Transient Response
(V_{BAT} = V_{PVL3} = 3.6V; V_{AUX3} = -7.5V; L = 4.7µH;
C_{OUT} = 4.7µF/10V; Transient Slew Rate = 0.1A/µs)



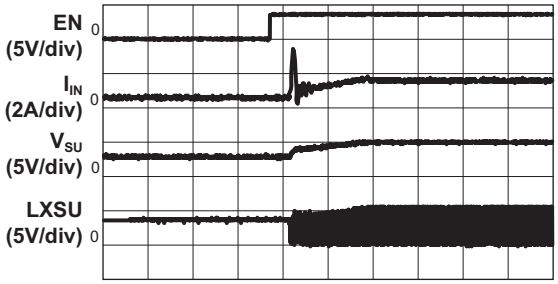
Time (40µs/div)

Mininum Start-up Voltage vs. Load Current
(V_{SU} = 5V)



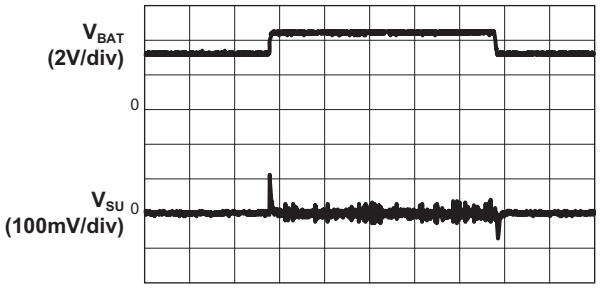
Typical Characteristics

SU Start-up
(V_{BAT} = 3.6V; V_{SU} = 5V; C_{OUT} = 22µF; 1A Load)



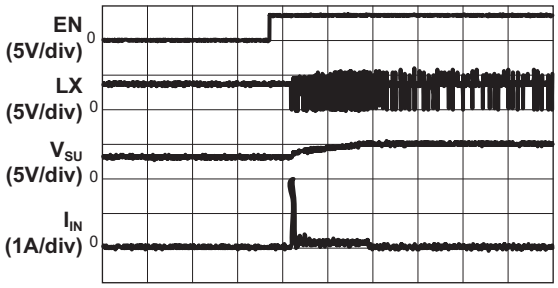
Time (200µs/div)

Line Transient Response
(V_{BAT} = 3.6V to 4.2V; V_{SU} = 5V; L = 2.2µH;
C_{OUT} = 22µF; 200mA Load)



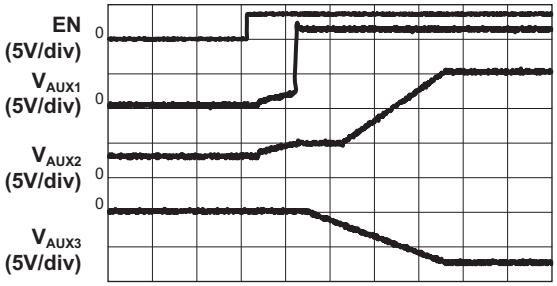
Time (1ms/div)

SU Start-up Sequence
(V_{BAT} = 3.6V; All Seven Channels Enabled;
V_{SU} = 5V; SU = 10mA Load)



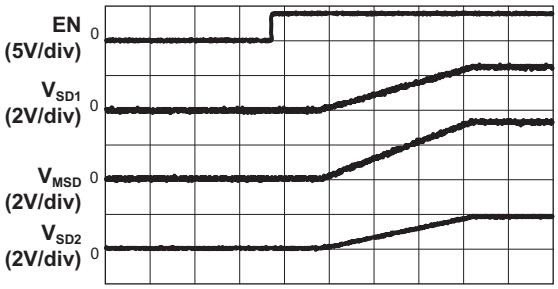
Time (200µs/div)

AUX1, AUX2, AUX3 Start-up Sequence
(V_{BAT} = 3.6V; AUX1 = 4 WLEDs; V_{SU} = 5V; V_{AUX2} = 15V;
V_{AUX3} = -7.5V; AUX2, AUX3 = 10mA Load)



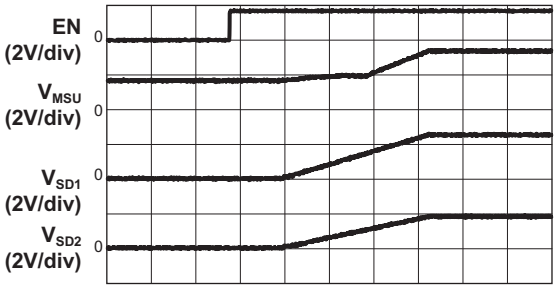
Time (400µs/div)

MSD, SD1, SD2 Startup Sequence
(V_{BAT} = 3.6V; V_{SU} = 5V; V_{MSD} = 3.3V;
V_{SD2} = 1.8V; 10mA Load)



Time (400µs/div)

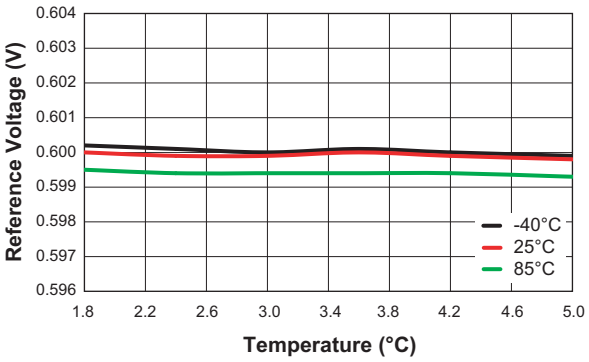
MSU, SD1, SD2 Startup Sequence
(V_{BAT} = 1.8V; V_{SU} = 5V; V_{MSU} = 3.3V; V_{SD1} = 2.5V;
PVSD1 = PVSD2 = PVSU; 10mA Load)



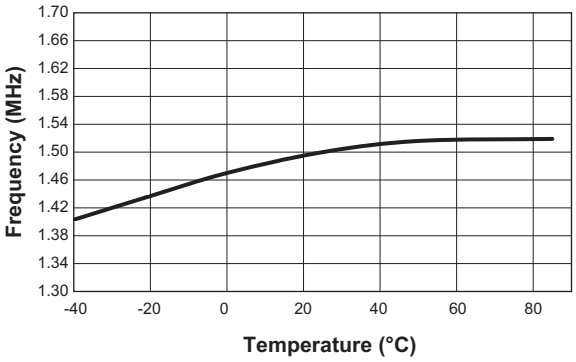
Time (400µs/div)

Typical Characteristics

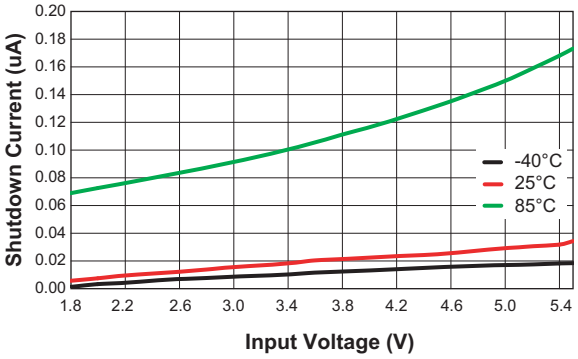
Reference Voltage vs. Temperature



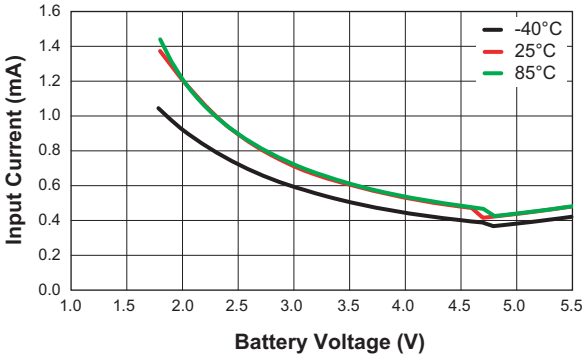
Switching Frequency vs. Temperature



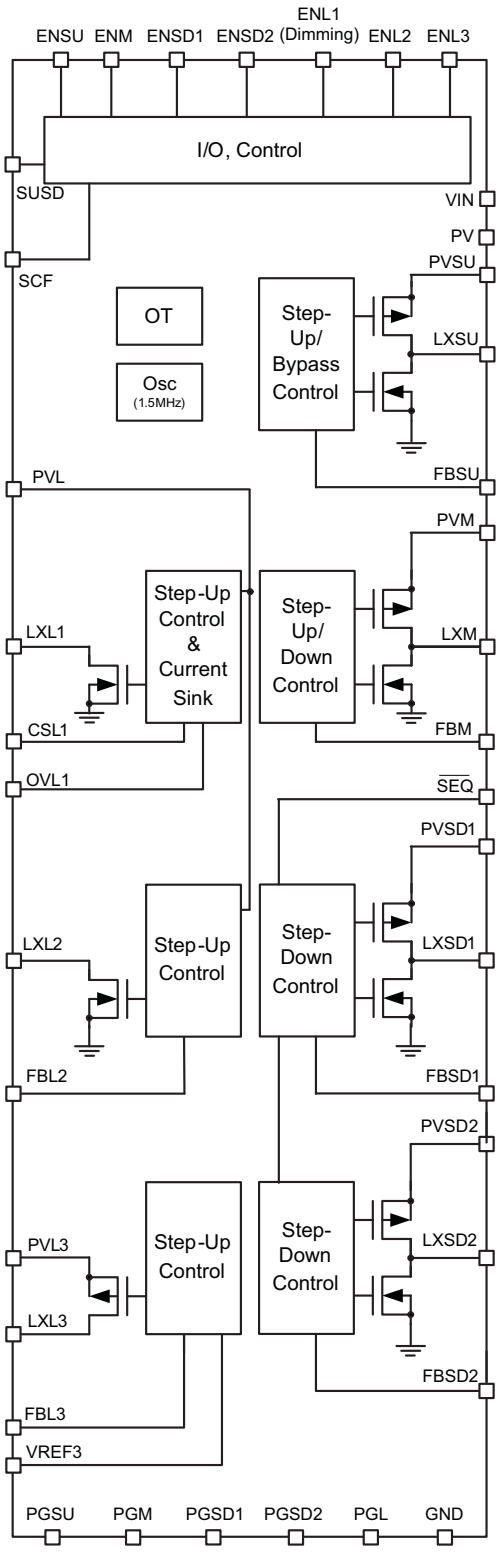
Shutdown Current vs. Input Voltage



Input Current vs. Input Voltage
(Only SU Enabled, V_{SU} = 5V, L = 2.2µH, C_{OUT} = 22µF)



Functional Block Diagram



Functional Description

The AAT2610 PMIC is targeted for single cell Li-ion battery or dual cell Alkaline battery applications. It includes seven integrated step-up and step-down converters, including one synchronous step-up converter (SU), two synchronous step-down converters (SD1, SD2), one synchronous step-up or step-down converter (Main), two non-synchronous step-up converters (AUX1, AUX2) and one non-synchronous buck-boost (inverting) converter (AUX3).

The SU converter is the key channel. Its output powers all internal control and reference circuits when the output voltage is above 2.7V. The AUX1 converter is specially designed for 1 to 6 white LED serial backlight applications. Its current sink pin (CSL1) is suitable to control WLED current to up to 20mA. AUX3 is a transformerless inverting converter which controls the internal P-channel MOSFET to regulate negative voltage.

The AAT2610 uses a fixed-frequency peak current control architecture. Light load mode is used to enhance light load efficiency. Compensation is integrated to reduce the number of external components and achieve excellent transient response and load and line regulation.

The ideal 1.5MHz switching frequency allows the use of smaller output filter components for improved power density, reduced external component size, and optimized output voltage ripple. The output voltages can be programmed by an external divider.

The AAT2610 has seven separate enable pins to control each converter's startup. A 1.4ms startup delay is employed to guarantee that the key SU converter is already in regulation and the internal control and the reference have been normally biased before the other six converters start up.

Synchronous Step-Up DC to DC Converter

The AAT2610 has one synchronous step-up DC-DC converter. It utilizes internal power MOSFETs to achieve high efficiency over the full load current range. The external feedback can program the output voltage between 3.0V to 5.5V. Its "bypass" mode automatically connects the input to the output when the input voltage is higher than the bypass mode threshold. In shutdown, the enable pin (ENSU) is pulled low, the SU converter output is equal to the input voltage minus a voltage drop across the parasitical body diode, and all other channels are shut down regardless of their enable setting.

Start-Up

The AAT2610's major control circuitries adopt power from the SU converter output and do not function at less than 2.7V. To ensure the PMIC can start up at V_{IN} as low as 1.8V, the step-up converter employs a startup oscillator with a typical 200kHz frequency. The startup oscillator drives the internal N-channel MOSFET at LXSU until the SU converter output voltage reaches 2.7V, at which point the current-mode PWM circuitry takes over. A startup current limit (750mA) and NMOSFET off time (700ns) decrease the startup inrush current. At low input voltages, the AAT2610 may have difficulty starting up with heavy loads.

Under-Voltage Lockout

Independent UVLO (Under-Voltage Lockout) circuitry guarantees the sufficient input power and proper operation of all internal circuitry. When input voltage at V_{IN} rises above 1.8V, the AAT2610 leaves UVLO status and enters the startup process. Once in regulation, the V_{IN} power can be as low as 1.6V before the AAT2610 enters UVLO status.

Bypass Mode

When the SU converter input voltage increases above the bypass mode threshold (typically 4.75V), the step-up converter enters "bypass" mode, which automatically connects the input to the output. In this mode, P-channel synchronous MOSFET is always ON and N-channel MOSFET is always off. The output voltage follows input voltage in the mode and overload protection is disabled.

Synchronous Step-Up / Step-Down DC to DC Converter

The AAT2610 has one synchronous step-up/step-down DC-DC converter which is ideally designed for 2AA/Li-ion applications. The SUSD pin is used to set the operation mode. When SUSD is set to logic high, the step-up converter setting is selected. N-channel switch transistor current is sensed for current loop control to regulate the output over the complete load range; when SUSD is pulled low, the step-down converter type is set and the P-channel switch transistor current is sampled for the current control loop. In both converter types, soft-start is employed to suppress the startup inrush current and eliminate the output voltage overshoot.

In shutdown with the enable pin (ENM) pulled low, if the step-down converter is selected, the converter is forced into a non-switching state and the output voltage drops to zero. When the step-up converter is selected, the output voltage is equal to the input voltage minus a voltage

drop across the parasitical body diode. If true load disconnection is required, an external PMOSFET controlled by SEQ can be adopted.

Synchronous Step-Down DC to DC Converter

The AAT2610 has two synchronous step-down DC-DC converters. Their output voltages can be programmed from 0.6V to V_{IN} by an external resistor divider.

At dropout, the converter's duty cycle equals 100% and the output voltage tracks the input voltage minus the voltage drop across the P-channel MOSFET. At low input supply voltage, the $R_{DS(ON)}$ of the P-channel MOSFET increases, and the efficiency of the converter decreases.

The two step-down converters adopt soft-start to eliminate output voltage overshoot when the enable or input voltage is applied. When the ENSD1 and ENSD2 are pulled low, the outputs of the two SD converters are down to zero and its shutdown current is below 1μA.

Non-Synchronous Step-Up and Buck/Boost (Inverting) DC to DC Converters

Two non-synchronous step-up converters are targeted for LCD backlight and CCD positive loads. The controllers regulate the output voltage by modulating the pulse width of the internal NMOSFET. External schottky diode and power inductor are required to set up the boost. The output voltage can be programmed from 5V to 20V by external divider.

Auxiliary 1 is ideally designed for driving typical 4 serial white LEDs. The maximum current flowing through the WLED string is sensed at CSL1 and set to 20mA by the internal ballast resistor with ±10% accuracy. The industry standard PWM (Pulse Width Modulation) controlling technology is adopted to program the WLED current. Applying a 10% ~100% duty cycle PWM signal with the frequency range 1kHz to 30kHz at ENL1 can get 2mA to 20mA WLED current. If an open circuit occurs, the internal over-voltage protection circuit prevents damage to the converter within 67ms, then shuts down all channels.

Auxiliary 2 is designed for +15V CCD bias. Soft-start is adopted to eliminate the output voltage overshoot and decrease the effect on the input voltage.

Auxiliary 3 is non-synchronous buck-boost (inverting) DC to DC converter which is targeted for negative CCD loads with low noise. Soft-start is adopted to limit the inrush current at startup.

Light Load Mode and Normal PWM Control

The AAT2610 uses light load mode to enhance the efficiency at light load. In light load mode, if the error amplifier output signal is lower than a given level at a certain clock point, the switch pulse is skipped to reduce dominant switching losses.

In normal PWM mode to the buck converter, the current through the P-channel (high side) is sensed for current loop control. The P-channel current limit is used to prevent internal power PMOSFET overstress or damage by the high power. To the boost converter, the current though the N-channel (low side) is sensed for the control loop and its current limit also protects the main MOSFET.

The error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. The internal fixed slope compensation is employed to eliminate the sub-harmonic oscillation and keep regulation stable when the duty cycle is over 50%.

Fault Protection

Short-Circuit and Overload Protection

When any of the converters' output voltage is lower than the programmed value for a certain period of time (100,000 clock cycles, typically 66.7ms), the central control circuits treat it as an overload situation; all seven channels will be turned off and SCF will be pulled low until the IC is restarted either by SU enable pin (ENSU) reset or re-application of the input voltage. During overload period, the peak current limit prevents the main switch (NMOSFET of step-up converter and PMOSFET of step-down converter) from overstress and damage, and also avoids saturation of the external inductor. For synchronous step-up (SU) channels, overload protection function is disabled in "bypass" mode.

Over-Temperature Protection

Thermal protection completely disables power MOSFET switching when internal power dissipation becomes excessive. Only reference and internal clock are still active in this condition. Once the over-temperature condition is removed, the output voltages automatically recover. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

Application Information

Setting the Output Voltage

Step-Down Converter

An external resistor divider is used to program the step-down converter's output voltage from 0.6V to V_{IN}. Resistors R1 and R2 in Figure 1 program the output to regulate at voltages higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output voltages with R2 set to 59kΩ.

The AAT2610 has 3 step-down converters: SD1, SD2 and Main SD. The external resistor sets the output voltage according to the following equations:

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R1}{R2}\right)$$

$$R1 = \left(\frac{V_{OUT}}{0.6V} - 1\right) \cdot R2$$

Table 1 shows the resistor selection for different output voltage settings. 1% accuracy metal-film resistors are strongly recommended to get accurate output voltages.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)
1.2	59
1.5	88.7
1.8	118
2.5	187
3.0	237
3.3	267

Table 1: Resistor Select for Step-Down Converter Output Voltage Setting.

Step-Up Converter

Similar to the step-down converter, the step-up regulators also use an external resistor divider to program the output voltage. The AAT2610 has 4 step-up converters: SU, Main SU, AUX1 and AUX2. The equation for external resistors setting the output voltage is same as for the step-down converter. Figure 2 shows the synchronous (SU and Main SU) and non-synchronous (AUX1 and AUX2) step-up converter application connections. Table 2 shows resistor selection for different output voltage settings. 1% accuracy metal-film resistors are strongly recommended to get accurate output voltages.

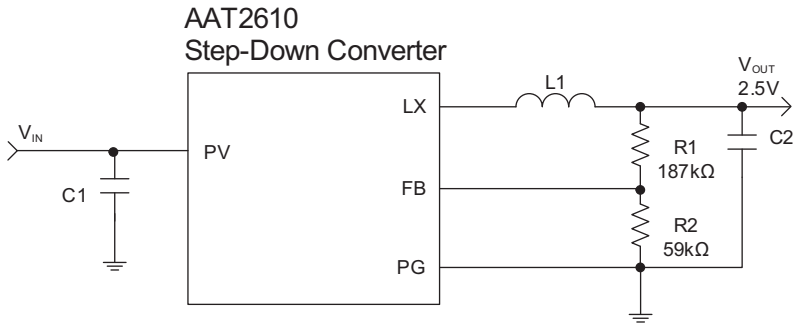
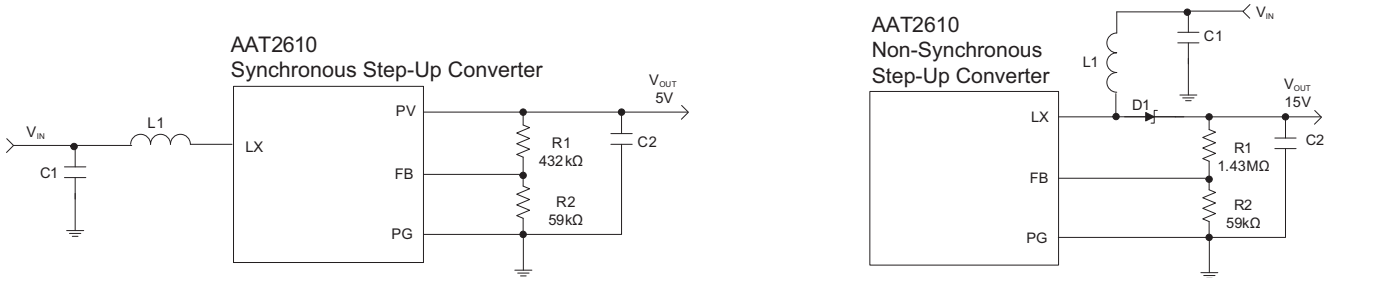


Figure 1: Step-Down Converter with Output Voltage Programmed by External Resistor Divider.



(a) Synchronous step-up converter

(b) Non-synchronous step-up converter

Figure 2: Step-Up Converter with Output Voltage Programmed by External Resistor Divider.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)
3.3	267
3.8	316
4.2	357
5.0	432
15	1420

Table 2: Resistor Select for Step-up Converter Output Voltage Setting.

Buck-Boost (Inverting) Converter

The AAT2610 has one inverting converter, AUX3. Figure 3 shows an AUX3 application circuit. Its programmed output voltage can be set by the following equations:

$$V_{OUT} = \frac{-0.6V}{R2} \cdot R1$$

$$R1 = \frac{V_{OUT}}{-0.6V} \cdot R2$$

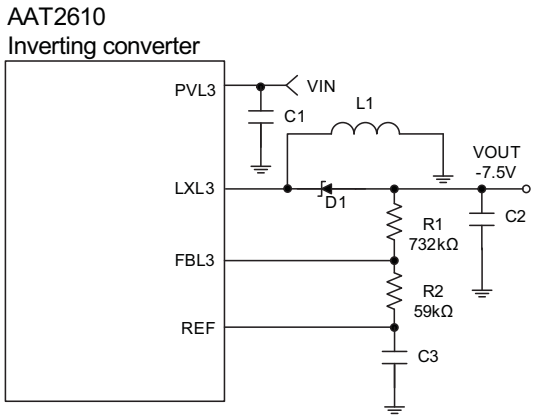


Figure 3: Buck/Boost (Inverting) Converter with Output Voltage Programmed by External Resistor Divider.

Inductor Selection

The AAT2610 can utilize small surface mount inductors due to its fast 1.5MHz switching frequency. Optimized inductor values for each channel keeps the seven channels stable, and achieves reduced output voltage ripple at smaller output capacitor size. See Table 3 for recommended inductors for each channel. A greater inductance value will allow greater output current capability by reducing inductor ripple current. Increasing the inductance above 4.7µH will increase size to get enough saturation current rating. The following equations show the minimum saturation current of the selected inductors.

Manufacturer	Part Number	Inductance (µH)	Max DC Current (A)	DCR (mΩ)	Size (mm) LxWxH	Type	Suit for Channel
Sumida	CDRH4D22/HP	2.2	3.2	35.4	4.5x4.5x2.4	shielded	SU
	CDRH8D28	2.5	4.5	12	8.3x8.3x3	shielded	SU
	CDRH2D09	2.5	0.53	120	3.2x3.2x1.0	shielded	Main SD, SD1, SD2
		2.2	0.60	115	3.2x3.2x1.0	shielded	Main SD, SD1, SD2
		1.8	0.65	105	3.2x3.2x1.0	shielded	SD2
	CDRH2D09C	3.3	0.50	139	3.2x3.2x1.0	shielded	Main SU
	CDRH2D14	4.7	1.0	135	3.2x3.2x1.55	shielded	AUX1, AUX2, AUX3
	CDRH2D11/HP	4.7	0.75	190	3.2x3.2x1.2	shielded	
	CDRH2D18/HP	2.2	1.6	48	3.2x3.2x2.0	shielded	Main SD, SD1, SD2
	CDRH2D18/HP	4.7	1.2	110	3.2x3.2x2.0	shielded	AUX1, AUX2, AUX3
Cooper	SD3110	2.2	1.0	149	3.1x3.1x1.0	shielded	Main SD, SD1, SD2
	SD3110	3.3	0.81	195	3.1x3.1x1.0	shielded	Main SU, SD1, SD2
	SD3112	4.7	0.80	246	3.1x3.1x1.2	shielded	AUX1, AUX2, AUX3
Murata	LQH32PN2R2NN0	2.2	1.6	76	3.2x2.5x1.55	unshielded	Main SD, SD1, SD2
	LQH32PN3R3NN0	3.3	1.2	120	3.2x2.5x1.55	unshielded	Main SU, SD1, SD2
	LQH32PN4R7NN0	4.7	1.0	180	3.2x2.5x1.55	unshielded	AUX1, AUX2, AUX3

Table 3: Suggested Inductor Selection Information.

To step-up converter,

$$I_{L_SAT} > \frac{I_{OUT_MAX}}{1 - D} + \frac{V_{IN} \cdot D}{2 \cdot f \cdot L}$$

Among it,

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

To step-down converter,

$$I_{L_SAT} > I_{OUT_MAX} + \frac{(V_{IN} - V_{OUT}) \cdot D}{2 \cdot f \cdot L}$$

Among it,

$$D = \frac{V_{OUT}}{V_{IN}}$$

Input and Output Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. The following equations show the minimum capacitance under the required output voltage ripple for step-up and step-down converters. In actual application, capacitance usually decreases a lot as its DC bias increases. So when selected output capacitors, not only calculating the output capacitor minimum values are necessary according to the equations, but the actual capacitance must be carefully considered to get expected output voltage ripple. X5R and X7R dielectric materials of ceramic capacitors are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

To step-up converter,

$$C_{OUT} \geq \frac{D \cdot I_{OUT}}{\Delta V_{OUT} \cdot f}$$

To step-down converter,

$$C_{OUT} \geq \frac{V_{OUT}}{8 \cdot f^2 \cdot L \cdot \Delta V_{OUT}} \cdot (1 - D)$$

For example, to step-up converter, when V_{IN} = 3.6V, I_{OUT} = 900mA, and f = 1.5MHz, output ripple requires below 30mV. According to the equation above, the calculated C_{OUT} should be higher than 5.6µF. If use Sumida 22µF/6.3V 0805 ceramic capacitor, its capacitance at 5V DC bias is 8.0µF which can meet the ripple requirements.

Input capacitors for input decoupling should be located as close as possible to the device to get better input power filtering effect. Select 1µF to 4.7µF X5R or X7R ceramic capacitors for the inputs. Table 4 shows suggested capacitor part numbers.

Output Diode

A Schottky diode is suitable in the three non-synchronous step-up channels for its low forward voltage and fast recovery time. 20V rated Schottky diodes are recommended for outputs less than 10V, while 30V rated Schottky diodes are recommended for outputs greater than 10V. Table 5 shows suggested diode part numbers.

Using $\overline{SEQ}$ for Power Sequence

Power sequence delay is designed to connect the loads to Main channel output after its normal startup. Use the $\overline{SEQ}$ output signal to control an external PMOSFET connected between Main output and loads. The $\overline{SEQ}$ output is high impedance lasted for 10ms when startup, then pulled low after both the SD1 and SD2 converters completed soft-start and achieved output regulation. When SD1 and SD2 are disabled, $\overline{SEQ}$ is also pulled low after 10ms when Main channel achieves regulation.

Using SCF for Full-Load Startup

SCF goes high (high impedance, open drain) when overload protection occurs. Under normal operation, SCF pulls low. It can be used to drive a P-channel MOSFET switch that turns off the load of a selected supply in the event of an overload. Or, it can remove the load until the supply reaches regulation, effectively allowing full load startup.

Thermal Considerations

Thermal design is an important aspect of power management IC applications and PCB layout. The AAT2610 TQFN55-40L package can provide up to 2W of power dissipation when it is properly soldered onto a printed circuit board with thermal vias. The package has a maximum thermal resistance of 25°C/W. The maximum power dissipation in a given ambient condition can be calculated:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)
θ_{JA} = Package Thermal Resistance (°C/W)
$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C) [150°C]
T_A = Ambient Temperature (°C)

The power dissipation for the synchronous buck channel in CCM (Continuous Conduction Mode) can be calculated by the following equation:

$$P_{Syn\text{-}BUCK} = I_{OUTBUCK}^2 \cdot \left(R_{DS(ON)P} \cdot \frac{V_{INBUCK}}{V_{OUTBUCK}} + R_{DS(ON)N} \cdot \left[1 - \frac{V_{INBUCK}}{V_{OUTBUCK}} \right] \right)$$

Where:

$P_{Syn\text{-}BUCK}$ = Synchronous Buck Channel Power Dissipation
$I_{OUTBUCK}$ = Synchronous Buck Channel Output Current
$V_{OUTBUCK}$ = Synchronous Buck Channel Output Voltage
V_{INBUCK} = Synchronous Buck Channel Input Voltage
$R_{DS(ON)x}$ = Synchronous Buck Channel PMOS or NMOS Drain-Source On Resistance

The power dissipation for the synchronous boost channel in CCM can be calculated by the following equation:

$$P_{Syn\text{-}BOOST} = I_{INBOOST}^2 \cdot \left(R_{DS(ON)P} \cdot \frac{V_{INBOOST}}{V_{OUTBOOST}} + R_{DS(ON)N} \cdot \left[1 - \frac{V_{INBOOST}}{V_{OUTBOOST}} \right] \right)$$

Where:

$P_{Syn\text{-}BOOST}$ = Synchronous Boost Channel Power Dissipation
$I_{INBOOST}$ = Synchronous Boost Channel Input Current
$V_{OUTBOOST}$ = Synchronous Boost Channel Output Voltage
$V_{INBOOST}$ = Synchronous Boost Channel Input Voltage
$R_{DS(ON)x}$ = Synchronous Boost Channel PMOS or NMOS Drain-Source On Resistance

The power dissipation for the non-synchronous boost channel can be calculated by the following equation:

$$P_{Nonsyn\text{-}BOOST} = I_{INBOOST}^2 \cdot \left(R_{DS(ON)N} \cdot \left[1 - \frac{V_{INBOOST}}{V_{OUTBOOST}} \right] \right)$$

Where:

$P_{Nonsyn\text{-}BOOST}$ = Non-Synchronous Boost Channel Power Dissipation
$I_{INBOOST}$ = Non-Synchronous Boost Channel Input Current
$V_{OUTBOOST}$ = Non-Synchronous Boost Channel Output Voltage
$V_{INBOOST}$ = Non-Synchronous Boost Channel Input Voltage
$R_{DS(ON)N}$ = Non-Synchronous Boost Channel internal NMOS Drain-Source On Resistance

The power dissipation for the inverting channel in CCM can be calculated by the following equation:

$$P_{Nonsyn\text{-}BUCKBOOST} = I_{IN\text{-}BUCKBOOST}^2 \cdot R_{DS(ON)P} \cdot \frac{V_{OUT\text{-}BUCKBOOST}}{V_{IN\text{-}BUCKBOOST} - V_{OUT\text{-}BUCKBOOST}}$$

Where:

$P_{Nonsyn\text{-}BUCKBOOST}$ = Non-Synchronous Buck/Boost Channel Power Dissipation
$I_{IN\text{-}BUCKBOOST}$ = Non-Synchronous Buck/Boost Channel Input Current
$V_{OUT\text{-}BUCKBOOST}$ = Non-Synchronous Buck/Boost Channel Output Voltage
$V_{IN\text{-}BUCKBOOST}$ = Non-Synchronous Buck/Boost Channel Input Voltage
$R_{DS(ON)P}$ = Non-Synchronous Buck/Boost Channel internal PMOS Drain-Source On Resistance

Layout Guidance

When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the AAT2610:

1. The exposed pad (EP) must be reliably soldered to the GND plane for better power dissipation. A PGND pad below EP is required.
2. The power traces, including the GND trace, the LX trace and the IN trace should be kept short, direct and wide to allow large current flow. Each inductor of the seven channels should be connected to the LX pins as short as possible. Use several VIA pads when routing between layers to decrease the conduction resistance.
3. The input filter capacitor of each channel should connect as closely as possible to IN (Pins 3, 8, 15, 29, 33 and 35) and GND (Pins 5, 6, 26, 27 and 37) to get good power filtering.
4. Keep the switching node, LX (Pins 4, 7, 25, 29, 34, 36 and 38), away from the sensitive FB node.
5. The feedback trace should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. The external feedback resistors should be placed as closely as possible to the FB pin (Pin 1, 2, 9, 23, 30, 32 and 40) to minimize the length of the high impedance feedback trace.
6. It is recommended to connect the external feedback resistor divider to the signal ground (Pin 16). The signal ground and power ground should be connected at a single point to alleviate the power ground noise affecting the feedback voltage.
7. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

Figure 4 and 5 show the AAT2610 evaluation board layout with 4 layers.

Manufacturer	Value (µF)	Voltage (V)	Case Size	Part Number	Channel / Capacitor Position
Murata	1	25	0603	GRM188R61E105K	AUX1 / output
	1	10	0603	GRM185R61A105K	SD1, SD2, AUX1, AUX2, AUX3 / input
	3.3	10	0603	GRM188R61A335K	AUX3 / output
	4.7	25	0805	GRM21BR61E475K	AUX2 / output
	4.7	6.3	0603	GRM188R60J475K	SU, Main / input Main SD, SD1, SD2 / output
	10	6.3	0805	GRM219R60J106KE19	Main SU, SD1, SD2
	22	6.3	0805	GRM21BR60J226M	SU, Main SU / output

Table 4: Suggested Input and Output Capacitor Selection Information.

Manufacturer	Part Number	Rated Forward Current (A)	Non-Repetitive Peak Surge Current (A)	Rated Voltage (V)	Thermal Resistance ($R_{\theta JA}$, °C/W)	Package
ON Semi	MBR0530T	0.5	5.5	30	206	SOD-123
	MBR0520LT	0.5	5.5	20	206	SOD-123
Diodes	BAT42W	0.2	4	30	500	SOD-123
Zetex	ZHCS350	0.35	4.2	40	330	SOD-523
Central Semi	CMDSH2-3	0.2	1.0	30	500	SOD-323

Table 5: Suggested Schottky Diode Selection Information.

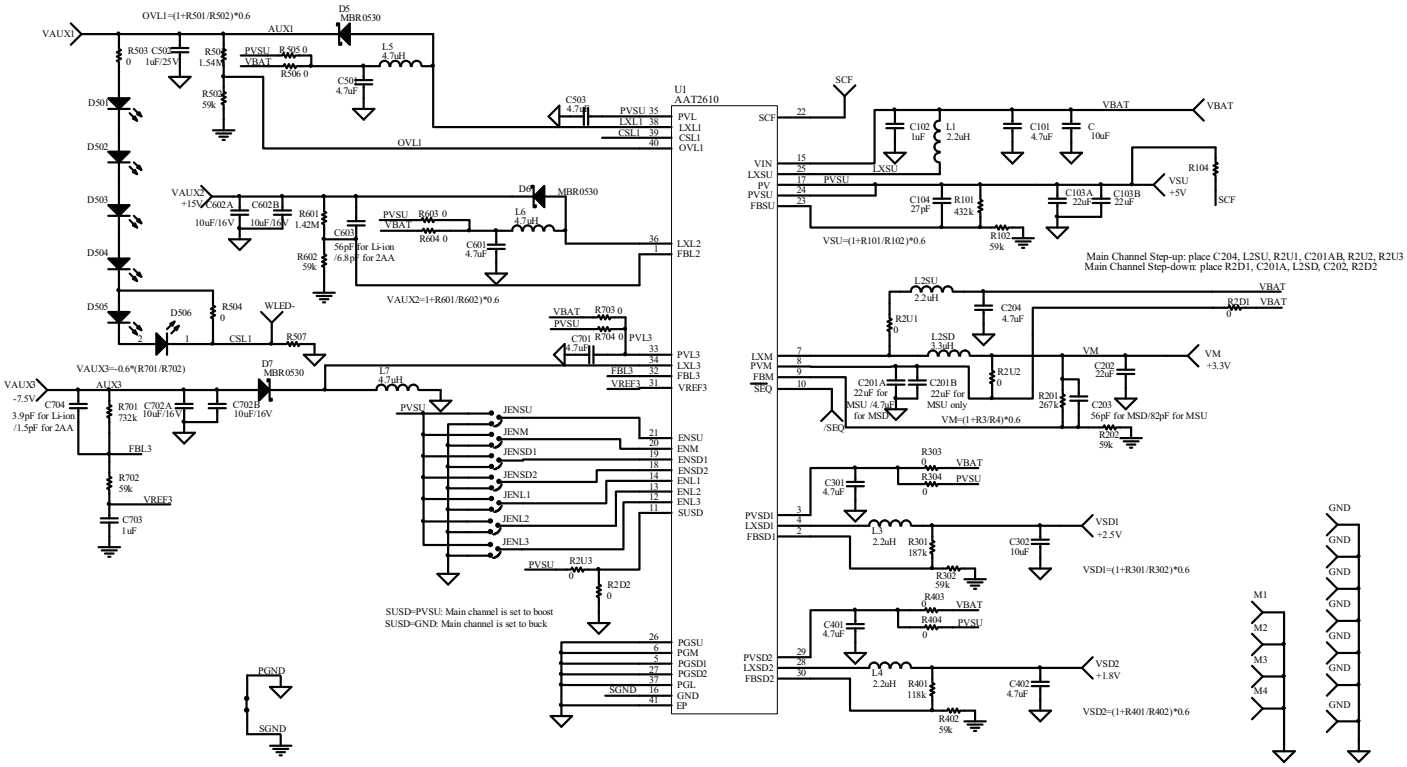
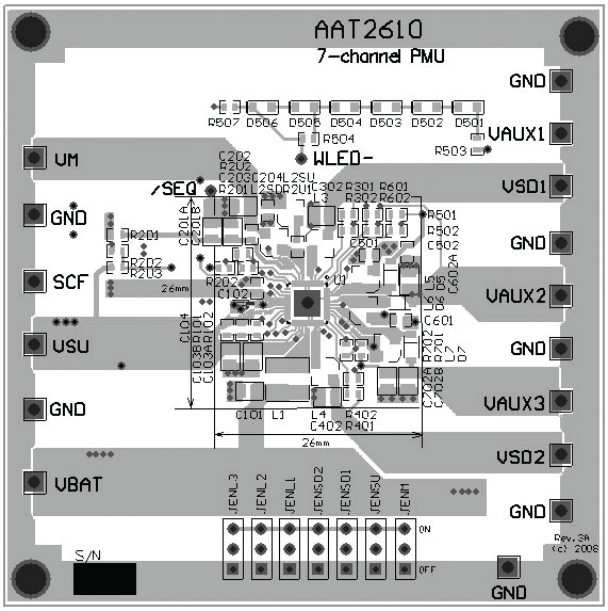
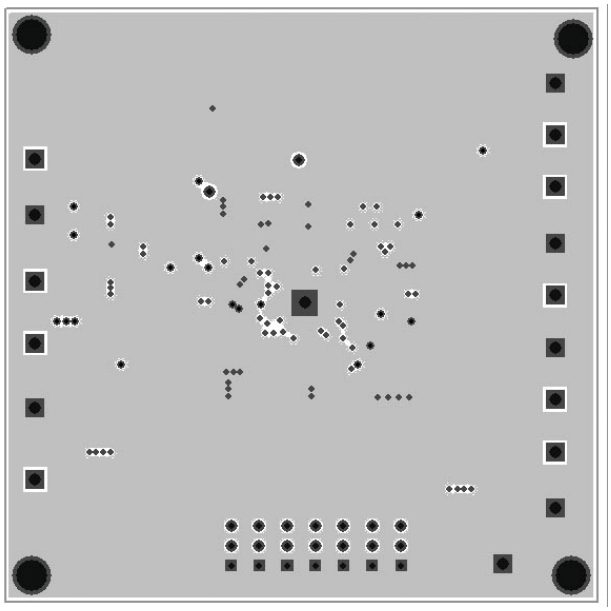


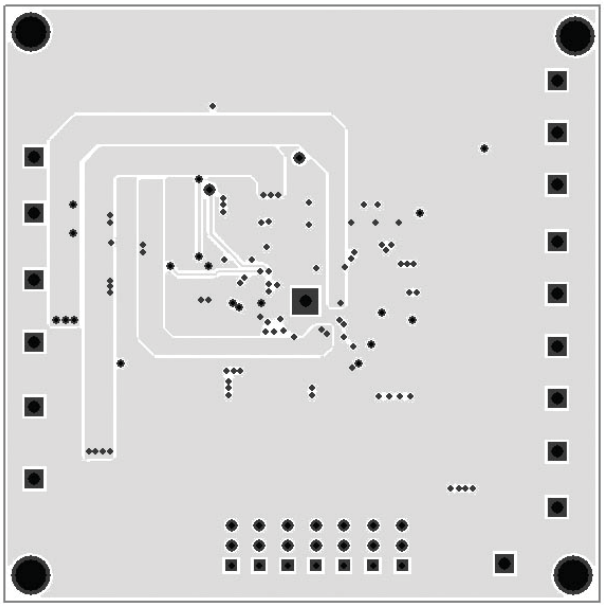
Figure 4: AAT2610 Evaluation Board Schematic.



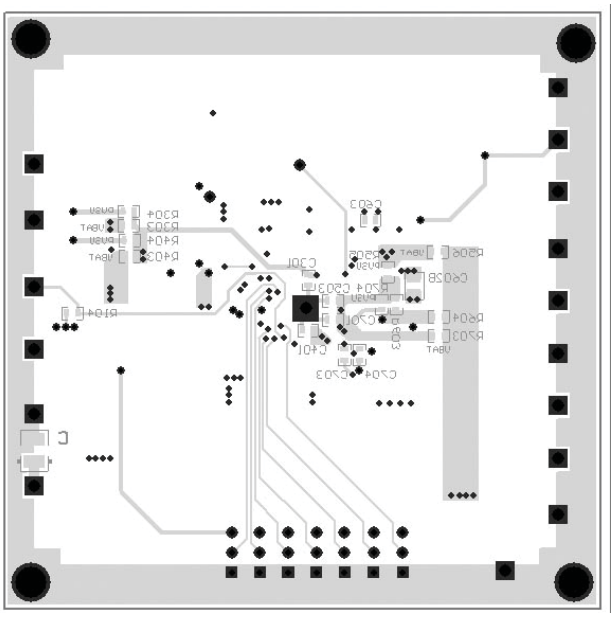
(a) Top Layer



(b) Internal GND Layer



(c) Internal Signal Layer



(d) Bottom Layer

Figure 5: AAT2610 Evaluation Board PCB Layout.

Designation	Part Number	Description	Manufacturer
IC Device			
U1	AAT2610IIC	Seven-Channel High Efficiency Power Management Unit	AnalogicTech
Capacitor			
C	T494B106M010AS	CAP TAN 10µF B 10V 20%	KEMET
C101	GRM21BR61C475K	CAP Ceramic 4.7µF 0805 X5R 16V 10%	Murata
C102, C703	GRM185R61A105K	CAP Ceramic 1µF 0603 X5R 10V 10%	
C103A, C103B, C202	GRM21BR60J226M	CAP Ceramic 22µF 0805 X5R 6.3V 20%	
C104	GRM1885C1H270J	CAP Ceramic 27pF 0603 C0G 50V 5%	
C201A, C301, C401, C402, C501, C503, C601, C701	GRM188R60J475K	CAP Ceramic 4.7µF 0603 X5R 6.3V 10%	
C203, C603	GRM1885C1H560J	CAP Ceramic 56pF 0603 C0G 50V 5%	
C302	GRM188R60J106M	CAP Ceramic 10µF 0603 X5R 6.3V 20%	
C303, C403	GRM1885C1H100J	CAP Ceramic 10pF 0603 C0G 50V 5%	
C502	GRM188R61E105K	CAP Ceramic 1µF 0603 X5R 25V 10%	
C602A, C602B, C702A, C702B	GRM21BR61C106K	CAP Ceramic 10µF 0805 X5R 16V 10%	
C704	GRM1885C1H3R9D	CAP Ceramic 3.9pF 0603 C0G 50V ±0.5pF	
Inductor			
L1	CDRH4D22/HP-2R2NC	Power Inductor 2.2µH 3.2A SMD	Sumida
L2SD	CDRH2D14-3R3NC	Power Inductor 3.3µH 1.2A SMD	
L3, L4	CDRH2D18/HPNP-2R2NC	Power Inductor 2.2µH 1.6A SMD	
L5, L6, L7	CDRH2D14 NP-4R7NC	Power Inductor 4.7µH 1.0A SMD	
Resistor			
R2D1, R2D2, R303 R403, R503, R504, R506, R604, R703	RC0603FR-070RL	RES 0Ω 1/10W 1% 0603 SMD	Yageo
R101	RC0603FR-07432KL	RES 432KΩ 1/10W 1% 0603 SMD	
R102, R202, R302 R402, R502, R602, R702	RC0603FR-0759KL	RES 59KΩ 1/10W 1% 0603 SMD	
R201	RC0603FR-07267KL	RES 267KΩ 1/10W 1% 0603 SMD	
R301	RC0603FR-07187KL	RES 187KΩ 1/10W 1% 0603 SMD	
R401	RC0603FR-07118KL	RES 118KΩ 1/10W 1% 0603 SMD	
R501	RC0603FR-071M54L	RES 1.54MΩ 1/10W 1% 0603 SMD	
R601	RC0402FR-071M42L	RES 1.42MΩ 1/16W 1% 0402 SMD	
R701	RC0603FR-07732KL	RES 732KΩ 1/10W 1% 0603 SMD	
Other			
D501, D502, D503, D504	RS-0805	20mA White LED 0805	Realstar
D5, D6, D7	MBR0530	Diode Schottky 0.5A 30V SOD-123	International Rectifier

Table 6: AAT2610 Li-ion Application Demo Board Bill of Materials (BOM).

Designation	Part Number	Description	Manufacturer
IC Device			
U1	AAT2610IIC	Seven-Channel High Efficiency Power Management Unit	AnalogicTech
Capacitor			
C	T494B106M010AS	CAP TAN 10µF B 10V 20%	KEMET
C101	GRM21BR61C475K	CAP Ceramic 4.7µF 0805 X5R 16V 10%	Murata
C102, C703	GRM185R61A105K	CAP Ceramic 1µF 0603 X5R 10V 10%	
C103A, C201A, C201B, C302	GRM21BR60J226M	CAP Ceramic 22µF 0805 X5R 6.3V 20%	
C203	GRM1885C1H820J	CAP Ceramic 82pF 0603 C0G 50V 5%	
C204, C301, C401, C402, C501, C503, C601, C701	GRM188R60J475K	CAP Ceramic 4.7µF 0603 X5R 6.3V 10%	
C303	GRM1885C1H150J	CAP Ceramic 15pF 0603 C0G 50V 5%	
C403	GRM1885C1H5R6D	CAP Ceramic 5.6pF 0603 C0G 50V ±0.5pF	
C502	GRM21BR61E475KA	CAP Ceramic 4.7µF 0805 X5R 25V 10%	
C602A,C602B, C702A, C702B	GRM21BR61C106K	CAP Ceramic 10µF 0805 X5R 16V 10%	
C603	GRM1885C1H6R8D	CAP Ceramic 6.8pF 0603 C0G 50V ±0.5pF	
C704	GRM1885C1H1R5D	CAP Ceramic 1.5pF 0603 C0G 50V ±0.5pF	
Inductor			
L1	CDRH4D22/HP-2R2NC	Power Inductor 2.2µH 3.2A SMD	Sumida
L2SU, L3, L4	CDRH2D18/HPNP-2R2NC	Power Inductor 2.2µH 1.6A SMD	
L5,	CDRH2D14 NP-4R7NC	Power Inductor 4.7µH 1.0A SMD	
L6, L7	CDRH2D18/HP-100	Power Inductor 10µH 0.85A SMD	
Resistor			
R2U1, R2U2, R2U3 R303, R404, R503, R504, R506, R604, R704	RC0603FR-070RL	RES 0Ω 1/10W 1% 0603 SMD	Yageo
R101	RC0603FR-07432KL	RES 432KΩ1/10W 1% 0603 SMD	
R102, R202, R301, R302, R402, R502, R602	RC0603FR-0759KL	RES 59KΩ1/10W 1% 0603 SMD	
R201	RC0603FR-07267KL	RES 267KΩ1/10W 1% 0603 SMD	
R401	RC0603FR-07187KL	RES 187KΩ 1/10W 1% 0603 SMD	
R501	RC0603FR-071M54L	RES 1.54MΩ 1/10W 1% 0603 SMD	
R601	RC0603FR-071M2L	RES 1.2MΩ 1/10W 1% 0603 SMD	
R701	RC0603FR-07732KL	RES 732KΩ 1/10W 1% 0603 SMD	
R702	RC0603FR-0751KL	RES 51KΩ 1/10W 1% 0603 SMD	
Other			
D501, D502, D503, D504	RS-0805	20mA White LED 0805	Realstar
D5, D6, D7	MBR0530	Diode Schottky 0.5A 30V SOD-123	International Rectifier

Table 7: AAT2610 2AA Application Demo Board Bill of Material (BOM).

Additional Applications

The auxiliary AUX1 channel can drive higher current levels by adding an external resistor at the CSL1 pin. As an example, a 220Ω is connected between CSL1 and GND to get a maximum 25mA led current as shown in Figure 6; a 73Ω is used to get maximum 35mA led current as shown in Figure 7.

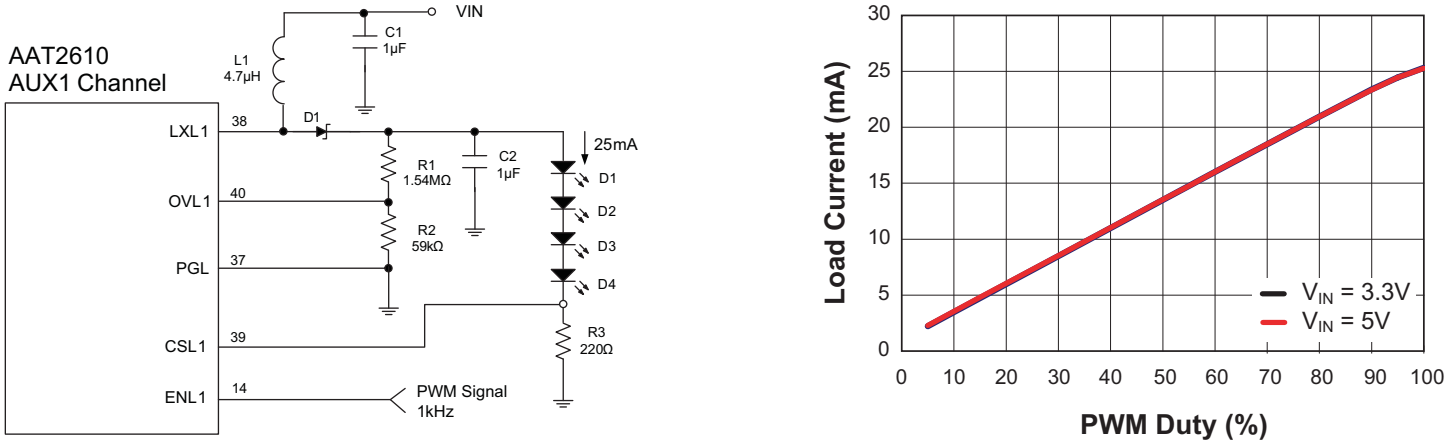


Figure 6: AUX1 Channel Application Example Driving 4 WLEDs with Maximum 25mA Led Current.

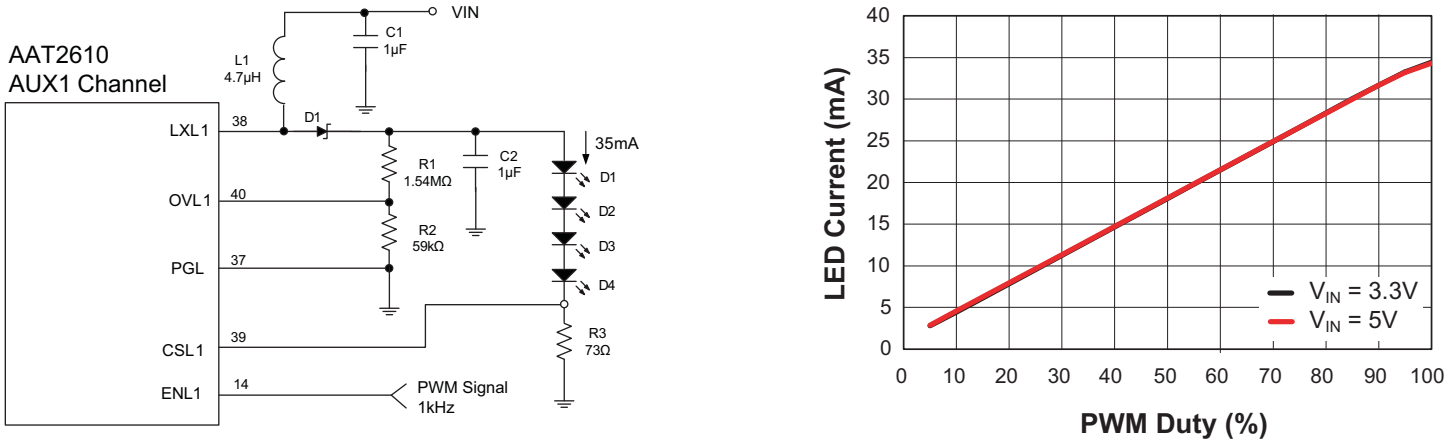


Figure 7: AUX1 Channel Application Example of Driving 4 WLEDs with Maximum 35mA Led Current.

Ordering Information

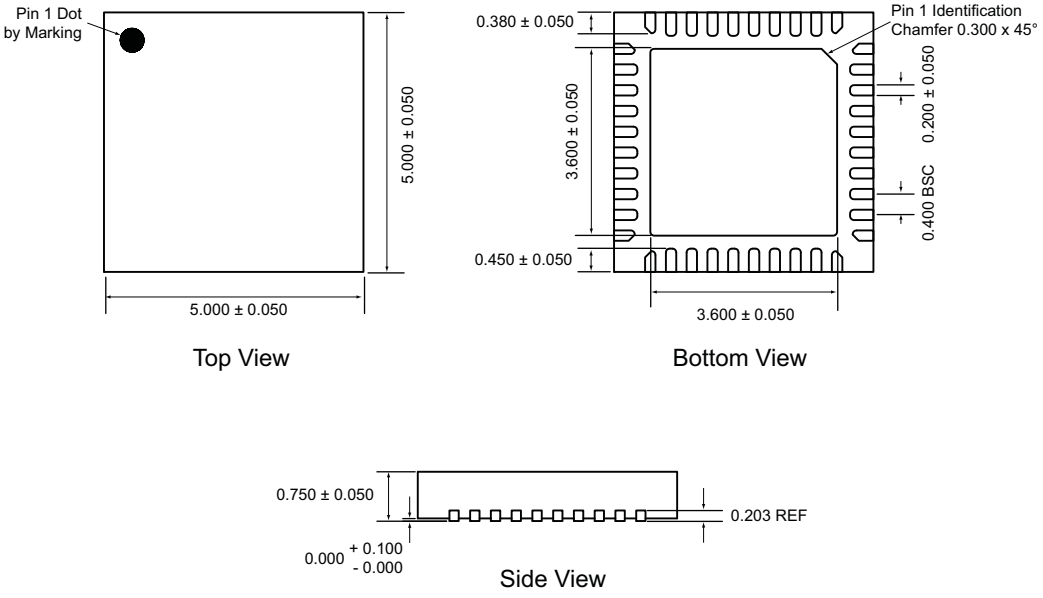
Output Voltage	Package	Marking[1]	Part Number(Tape & Reel)[2]
Adj. 0.6V	TQFN55-40L	3GXYY	**AAT2610IIC**

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All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/about/quality.aspx.

Package Information

TQFN55-40L[3]



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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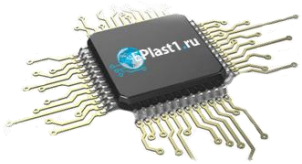
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