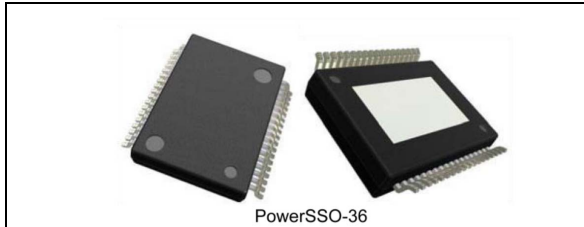


Quad-channel high-side driver with 16-bit SPI interface for automotive applications


Datasheet - production data



- Undervoltage shutdown
- Overvoltage clamp
- Latch-off or programmable time limited auto restart (power limitation and overtemperature shutdown)
- Load dump protected
- Protection against loss of ground

Features

| Channel | V _{CC} | R _{ON(typ)} | I _{LIMH(typ)} |
|---------|-----------------|----------------------|------------------------|
| 0-1 | 28 V | 35 mΩ | 35 A |
| 2-3 | 28 V | 9 mΩ | 80 A |

- AEC-Q100 qualified 
- General
 - 16-bit ST-SPI for full diagnostic with 8 bits Short Frame option
 - Programmable Bulb/LED mode for ch. 0-1
 - Advanced limp home functions for robust fail-safe system
 - Very low standby current
 - Optimized electromagnetic emissions
 - Very low electromagnetic susceptibility
 - Control through direct inputs and / or SPI
 - Compliant with European directive 2002/95/EC
- Diagnostic functions
 - Multiplex proportional load current sense
 - Synchronous diagnostic of over load and short to GND, output shorted to V_{CC} and OFF-state open-load
 - Programmable case overtemperature warning
- Protection
 - Two levels load current limitation
 - Self limiting of fast thermal transients

Description

The VNQ7004SY is a device made using STMicroelectronics® VIPower® technology. It is intended for driving resistive or inductive loads directly connected to ground. The device is protected against voltage transient on V_{CC} pin.

An 8 bit short frame access to output control registers is provided allowing PWM control through SPI with high granularity.

An analog current feedback for each channel is connected to the CURRENT-SENSE pin via a multiplexer. The device detects open-load in OFF-state conditions.

Real time diagnostic is available through the SPI bus (open-load, output short to V_{CC}, overtemperature, communication error, power limitation or latch off).

Output current limitation protects the device in an over load condition. The device can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or programmable time limited auto restart.

The device enters a limp home mode in case of loss of digital supply (V_{DD}), reset of digital memory or watchdog monitoring time-out event. In this mode states of channel 0, 1, 2 or 3 are respectively controlled by four dedicated pins IN0, IN1, IN2 and IN3. Channel 0 and 1 can be programmed via SPI for load type (BULB/ LED mode).

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1 Block diagram and pin description

Figure 1. Block diagram

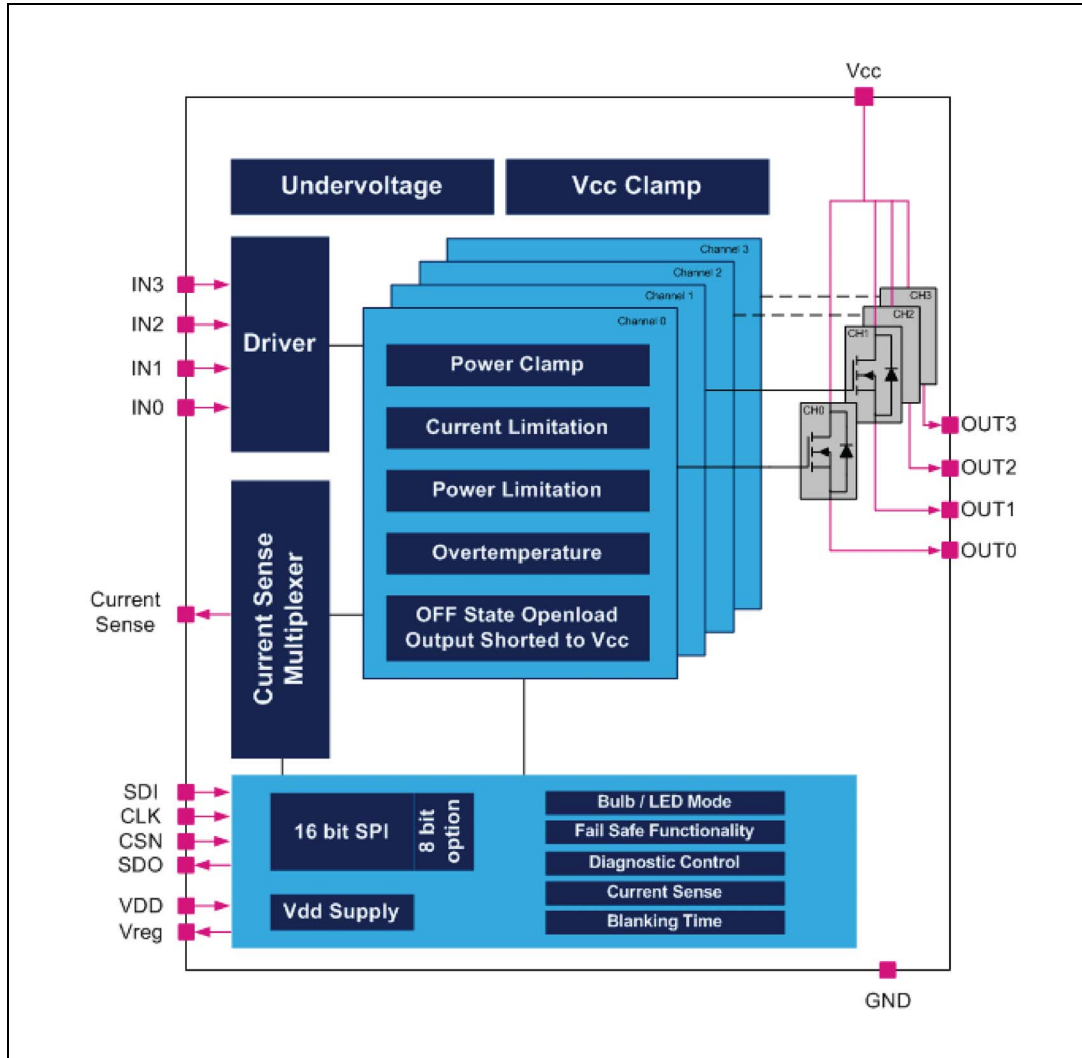
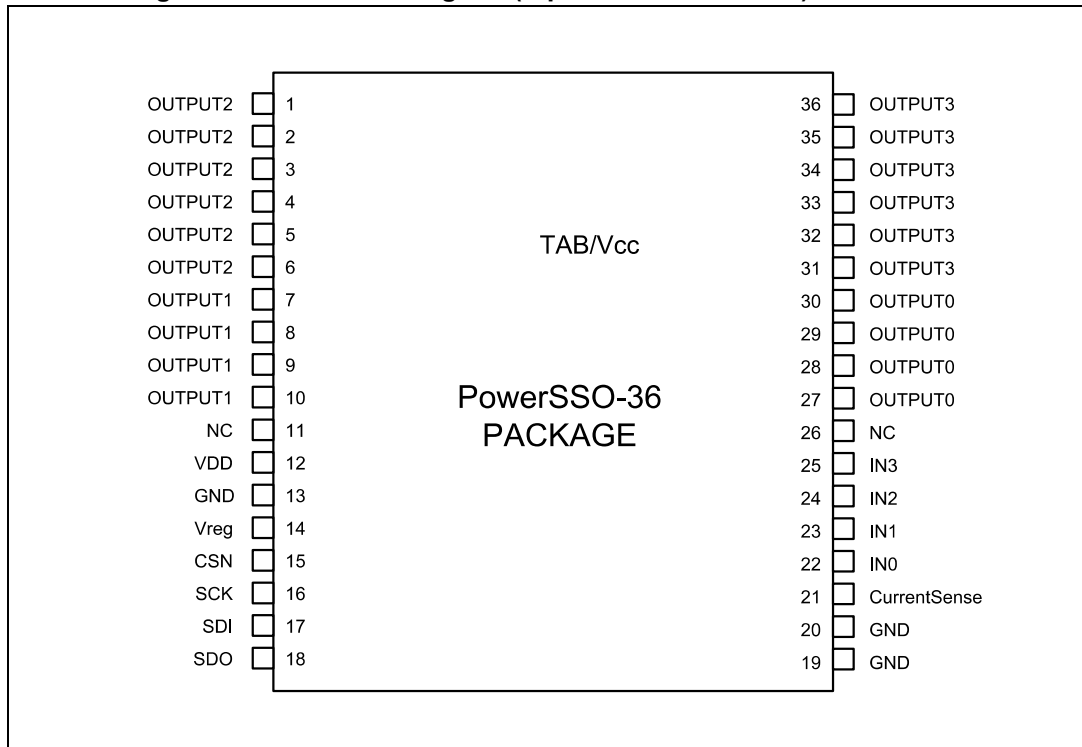


Figure 2. Connection diagram (top view—not to scale)



Note: Pins 31,32,33,34,35 and 36 (OUTPUT3) must be connected together.

Note: Pins 27,28,29 and 30 (OUTPUT0) must be connected together.

Note: Pins 7,8,9 and 10 (OUTPUT1) must be connected together.

Note: Pins 1,2,3,4,5 and 6 (OUTPUT2) must be connected together.

Table 1. Pin functionality description

| Pin number | Name | Function |
|-----------------|---------|--|
| — | Vcc | Battery connection. This is the backside TAB and is the direct connection to drain Power MOSFET switches. |
| 19, 20 | GND | Ground connection. This pin serves as the ground connection for the logic part of the device. |
| 13 | GND | Ground connection. This is a Kelvin ground connection for the logic part of the device and is used to connect an external EMC capacitor to the VREG pin. It must not be connected to application ground. |
| 27, 28,29, 30 | OUTPUT0 | Power OUTPUT 0. It is the direct connection to the source Power MOSFET switch No. 0. |
| 7, 8, 9, 10 | OUTPUT1 | Power OUTPUT 1. It is the direct connection to the source Power MOSFET switch No. 1. |
| 1, 2, 3, 4,5, 6 | OUTPUT2 | Power OUTPUT 2. It is the direct connection to the source Power MOSFET switch No. 2. |

Table 1. Pin functionality description (continued)

| Pin number | Name | Function |
|-------------------|------------------|---|
| 31,32,33,34,35,36 | OUTPUT3 | Power OUTPUT 3. It is the direct connection to the source Power MOSFET switch No. 3. |
| 15 | CSN | Chip select not (active low). It is the selection pin of the device. It is a CMOS compatible input. |
| 16 | SCK | Serial clock. It is a CMOS compatible input. |
| 17 | SDI | Serial data input. Transfers data to be written serially into the device on SCK rising edge. |
| 18 | SDO | Serial data output. Transfers data serially out of the device on SCK falling edge. |
| 14 | V _{REG} | Output of the 3 V regulated internal supply for the digital control. Connect a low ESR capacitor close to this pin. |
| 22 | IN0 | Direct Input pin for channel 0. Controls the OUTPUT 0 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register. |
| 23 | IN1 | Direct Input pin for channel 1. Controls the OUTPUT 1 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register. |
| 24 | IN2 | Direct Input pin for channel 2. Controls the OUTPUT 2 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register. |
| 25 | IN3 | Direct Input pin for channel 3. Controls the OUTPUT 3 state in limp home mode, is ORed to SPI control register in normal operating mode when corresponding bit is set in DIENCR (Direct Input ENable) control register. |
| 12 | V _{DD} | External 5 V or 3.0 V supply. Powers the SPI interface. |
| 21 | CurrentSense | Analog CurrentSense generator proportional to output current. CurrentSense can be programmed as bulb/LED mode for each channel. The pin can deliver the CurrentSense of OUTPUT 0, 1, 2 or 3. The value of resistance that is connected between the CurrentSense pin and device ground determines the reading level for the microcontroller. |
| 11, 26 | NC | Not connected |

2 Functional description

2.1 Device interfaces

- SPI: bi-directional interface, accessing RAM/ROM registers (CSN, CLK, SDI, SDO)
- INx: input pins for outputs control while device is in Fail Safe mode, Standby mode or Reset mode (usable also in Normal mode according to "Direct Input Enable Control Register" - DIENCR setting)
- CSense: current-sense output used for analogue monitoring (monitored signal selection via RAM register)
- V_{DD}: 5 V supply / 3 V option: V_{DD} can be shared with microcontroller for 3 V or 5 V. This gives the range of the SPI for 3 V to 5 V. The V_{REG} block is able to handle both the 3 V and 5 V.

2.2 Operating modes

The device can operate in seven different modes:

- Reset mode
- Fail Safe mode
- Normal mode
- Standby mode
- Sleep mode 1
- Sleep mode 2
- Battery undervoltage mode

The Reset mode, the Fail Safe mode and the Sleep mode 1 are combined into the Limp home mode. In this mode the chip is able to operate without the connection to the SPI. All transitions between the states in limp home mode are driven by V_{DD} and INx. The outputs are controlled by the direct inputs INx.

For an overview over the operating modes and the triggering conditions please refer to [Table 10: Operating modes](#).

2.2.1 Startup transition phase

This is not an operation mode but a transition step to Reset operation mode from the power-ON. In this phase, neither digital supply voltage V_{DD} nor V_{CC} are available ($V_{DD} < V_{DD_POR_ON}$ and $V_{CC} < V_{USD}$).

This phase has not to be confused with Undervoltage mode where also the power supply is not available ($V_{CC} < V_{USD}$) after an operation mode. The device leaves this phase to Reset mode as soon as $V_{CC} > V_{USD}$. In case ($V_{CC} < V_{USD}$) but ($V_{DD} > V_{DD_POR_ON}$) then the device leaves this phase to Fail-Safe-Mode.

2.2.2 Reset mode

The device is in Limp Home state.

Reset mode is entered after Startup but also each time the digital supply voltage V_{DD} falls below V_{DD_POR_OFF} ($V_{DD} < V_{DD_POR_OFF}$ and $V_{CC} > V_{USD}$).

The outputs are controlled by the direct inputs INx. At least one INx is in logic High.

The SPI is inactive (no read / write possible) and the diagnostics are not available. The registers have the Reset values.

The device leaves this mode only if $V_{DD} > V_{DD_POR_ON}$ or all INx go to low.

The reset bit inside the Global Status Byte is set to 0 (for more information refer to the Global Status Byte register description).

The diagnostics is not available, but the protections are fully functional. In case of overtemperature or power limitation, the outputs work in unlimited auto-restart.

The device enters Reset mode under three conditions:

- Automatically during startup
- If it is in any other mode and if V_{DD} falls below $V_{DD_POR_OFF}$
- If it is in Sleep mode 1 and if only one input INx is set to 1

Reset mode can be left with 2 conditions:

- If V_{DD} rises above $V_{DD_POR_ON}$, the device enters Fail Safe mode
- If all inputs INx are 0, the device enters Sleep mode 1.

2.2.3 Fail Safe mode

The device is in Limp Home state.

The digital supply voltage V_{DD} is available ($V_{DD} > V_{DD_POR_ON}$) and the SPI registers are active (SPI read/write).

The device enters Fail Safe mode under five conditions:

- If it is in Reset mode or in Sleep mode 1 and V_{DD} rises above $V_{DD_POR_ON}$, ($V_{DD} > V_{DD_POR_ON}$)
- If it is in Standby mode or in Sleep mode 2 and CSN is low for $t > t_{stdby_out}$
- If it is in Normal mode and bit EN is cleared
- If it is in Normal mode and $WDTB$ is not toggled within t_{WDTB} (watchdog timeout)
- If it is in Normal mode and the SPI sends a SW reset

In case of Fail Safe mode, there is no analogue diagnostics (CurrentSense is inactive, not available) but the digital diagnosis is available through SPI bus.

The outputs are controlled by the direct inputs INx regardless of SPI commands.

The registers are cleared to their reset value if Fail Safe is entered through a SW reset.

The reset bit is 1 if the last state was Reset mode or the last command was a SW reset and it is reset to 0 after the first valid SPI access (for more information refer [Section 4.3.1: Global Status byte description](#)).

The SPI diagnostics is available.

The protections are fully functional. In case of overtemperature or power limitation, the outputs work in unlimited auto-restart.

The device exits Fail Safe mode under three conditions:

- If the SPI sends the goto Normal mode sequence, the device enters Normal mode:
 - In a first communication set bit $UNLOCK = 1$
 - In the consecutive communication set bit $STBY = 0$ and bit $EN = 1$

This mechanism avoids entering the Normal mode unintentionally.

- If the SPI sends the goto standby mode sequence, the device enters Standby mode:
 - In a first communication set bit $UNLOCK = 1$
 - In the consecutive communication set bit $STBY = 1$ and bit $EN = 0$

This mechanism avoids entering the Standby mode unintentionally.

- If V_{DD} falls below V_{DD_POR_OFF}, the device enters Reset mode.

Transition to Fail-Safe-mode from Normal mode, using the SPI register

Only one frame is needed.

Table 2. Frame 1: write CTRL 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------|------------------|--------|--------|------------------|-------|-------|-------------------|
| Command | | | | | | | |
| OC1 | OC0 | | | Address | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x ⁽¹⁾ | x ⁽¹⁾ | GOSTBY | UNLOCK | x ⁽¹⁾ | x | x | EN ⁽¹⁾ |
| X ⁽²⁾ | | | | | | | |

1. To avoid an SPI Error Frame due to a stuck at Zero, one bit of data field has to be at '1'. Bit "EN" has to be at '0' to force the device in Fail safe mode.

2. X: do not care.

Transition to Fail-Safe-mode from Normal mode by SW-Reset

SPI Reset is occurring by using the "Read device information" command (applicable only on ROM area) at reserved ROM address 0x3F. This is equivalent of sending a 0xFF command.

Only one frame is needed.

Table 3. Frame 1: read (ROM) 0x3FH 0x--

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|-------|---------|-------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Data ⁽¹⁾ | | | | | | | |
| x | x | x | x | x | x | x | x |
| X ⁽²⁾ | | | | | | | |

1. The "X" data field cannot be all ones, otherwise a stuck to VDD is detected.

2. X: do not care.

2.2.4 Normal mode

In this mode, all device functions are available. The transition to this mode is only possible from a previous Fail-Safe mode.

Outputs can be driven by SPI commands or a combination of SPI command and direct inputs IN_x.

To maintain the device in normal mode, the watchdog toggle bit in register CONFIG has to be toggled within the watchdog timeout period t_{WDTB} (see [Table 58: Dynamic characteristics - Mode 1](#) or [Table 59: Dynamic characteristics - Mode 2](#)).

Diagnosis is available through SPI bus (digital) and through CurrentSense pin (analogue CurrentSense).

The protections are fully functional. The outputs can be set to latch-off or programmable time limited auto-restart. In auto-restart the outputs are switched on again automatically after an overtemperature or power limitation event, while in latch the relevant status register has to be cleared to switch them on again. In time limited auto-restart the behavior is like auto-restart but within limited programmed time frame (refer to [Section 6.2: Blanking window values](#)).

The device enters Normal mode under one condition:

- If it is in Fail Safe mode and the go to Normal mode sequence is sent through SPI: this mechanism avoids entering Normal mode unintentionally.
 - In a first communication set bit UNLOCK = 1
 - In the consecutive communication set bit STBY = 0 and bit EN = 1

The transition from Fail-Safe-mode to Normal mode is performed by two special SPI sequences

Table 4. Frame 1: write CTRL 0x10

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Table 5. Frame 2: write CTRL 0x01

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Normal mode can be left with five conditions:

- If V_{DD} falls below $V_{DD_POR_OFF}$, the device enters Reset mode.
- If the SPI sends the goto standby sequence, the device enters Standby mode: this mechanism avoids entering Standby mode unintentionally.
 - In a first communication set UNLOCK = 1
 - In the consecutive communication set STBY = 1 and EN = 0
- If the SPI clears the EN bit (EN = 0), the device enters Fail Safe mode.
- Watchdog time out: If WDTB is not toggled within the monitoring timeout period t_{WDTB} , the device enters Fail Safe mode.
- If the SPI sends a SW reset command (Command byte = 0xFFh), all registers are cleared and the device enters Fail Safe mode.

2.2.5 Standby mode

The device is in low consumption state of the digital part.

The device enters Standby mode under three conditions:

- If it is in Fail Safe mode and the SPI sends the goto standby sequence: this mechanism avoids entering Standby mode unintentionally.
 - In a first communication set UNLOCK = 1
 - In the consecutive communication set STBY = 1 and EN = 0
- If it is in Normal mode and the SPI sends the goto standby sequence: This mechanism avoids entering Standby mode unintentionally.
 - In a first communication set UNLOCK = 1
 - In the consecutive communication set STBY = 1 and EN = 0
- If it is in Sleep mode 2 and at least one input INx is set to one.

The outputs are controlled by the direct inputs INx only.

The current consumption from V_{DD} drops down to I_{DDstd} (see [Table 54: DC characteristics - Mode 1](#)).

The digital supply voltage V_{DD} is available ($V_{DD} > V_{DD_POR_ON}$) but SPI is inactive (no read/write is possible, the SPI registers are frozen to their last state before entering standby mode).

The Standby mode will stay under above condition if at least one INx in logic High. CSN is in inactive High state (independent of MCU).

The diagnostics is not available.

The protections are fully functional. The outputs are set to unlimited auto-restart mode. Standby mode can be left with three conditions:

- If V_{DD} falls below $V_{DD_POR_OFF}$, the device enters Reset mode.
- If CSN is low for $t > t_{stdby_out}$, the device wakes up. As the EN bit has been set to 0, the device enters Fail Safe mode and recovers full functionality with command of the outputs and diagnostics.
- If all direct inputs INx are 0, the device enters Sleep Mode 2 resulting in minimal supply current from V_{CC} and V_{DD} .

Transition from Fail-Safe-mode to Standby mode using SPI: two frames needed.

Table 6. Frame 1: write CTRL 0x10

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

Table 7. Frame 2: write CTRL 0x20

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Transition from Normal mode to Standby mode using SPI: two frames needed

Table 8. Frame 2: write CTRL 0x11

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

Table 9. Frame 2: write CTRL 0x20

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|--------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Data | | | | | | | |
| x | x | GOSTBY | UNLOCK | x | x | x | EN |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

2.2.6 Sleep mode 1

The device is in Limp Home state.

The device has very low consumption for both digital and power parts. Current consumption from Digital part is nearly zero and the current consumption on V_{CC} is below I_{STBY} (low supply current).

The device enters Sleep mode 1 under one condition:

- If from Reset mode, all direct inputs IN_x are going low.

The digital supply voltage V_{DD} is not available ($V_{DD} < V_{DD_POR_OFF}$) and SPI is inactive (the read and write functions are not possible and all registers are cleared and have the reset values).

The diagnostics is not available (neither Analogue nor digital diagnostics). The output stages are all off.

Protections are inactive.

Sleep-mode-1 can be left with two conditions:

- If V_{DD} rises above $V_{DD_POR_ON}$, the device enters Fail Safe mode.
- If at least one of the inputs IN_x is set to 1, the device enters Reset mode.

2.2.7 Sleep mode 2

The device is in very low consumption state for both digital and power parts. Current consumption from Digital part is below I_{DDstd} and the current consumption on V_{CC} is below I_{SOFF} (low supply current).

The digital supply voltage V_{DD} is available ($V_{DD} > V_{DD_POR_ON}$) but SPI is not active (the read and write functions are not possible and all registers are frozen).

CSN is in inactive High state (independent of MCU).

The diagnostics is not available (neither analogue nor digital diagnostics). The output stages are all off.

Protections are inactive.

The device enters Sleep-mode-2 under one condition:

- If from Standby mode, all direct inputs IN_x are going low.

Sleep mode 2 can be left with three conditions:

- If V_{DD} falls below $V_{DD_POR_ON}$, the device enters Reset mode.
- If CSN is low for $t > t_{stdby_out}$, the device enters Fail Safe mode.
- If at least one of the inputs IN_x is set to 1, the device enters Standby mode.

2.2.8 Battery undervoltage mode

This is not an operation mode but a transition step, where power supply voltage is ($V_{CC} < V_{USD}$).

If the battery supply voltage V_{CC} falls below the undervoltage shutdown threshold ($V_{CC} < V_{USD}$) the device enters Battery undervoltage mode.

The CurrentSense signal is not available.

The output stages are off regardless of SPI status or IN_x .

There are three cases and, depending on the operation mode, the following occurs:

1. From Normal mode and from Fail-safe mode:
In these modes the digital supply voltage V_{DD} is available ($V_{DD} > V_{DD_POR_ON}$). The SPI is active and read/write functions are possible. The SPI diagnostics is available. After entering to the Undervoltage mode, the information about the undervoltage is saved in a flag (VCCUV), the SPI

register contents are retained. The SPI-register reading is always possible. If V_{CC} rises above the threshold ($V_{USD} + V_{USDhyst}$) the device returns to the last mode and the flag is cleared (VCCUV). If during this state V_{DD} decreases to $V_{DD} < V_{DD_POR_OFF}$, the device is reset completely. The last operation mode information is lost, the device logic part is unpowered, therefore after increasing the supply voltage to ($V_{CC} > V_{USD} + V_{USDhyst}$) the operation mode will be Reset mode. If during this state, the INx is changed, the operation mode is not changed and the output state is changed accordingly after V_{CC} recovering.

2. From Standby and Sleep-mode-2 modes:

In these modes the digital supply voltage V_{DD} is available ($V_{DD} > V_{DD_POR_ON}$). The SPI is not active and the registers are frozen. The SPI diagnostics is not available. After entering to the Undervoltage mode, the information about the undervoltage is not saved in a flag (VCCUV).

If V_{CC} rises above the threshold ($V_{USD} + V_{USDhyst}$) the device returns to the last mode. If during this state (undervoltage mode) V_{DD} decreases to $V_{DD} < V_{DD_POR_OFF}$, the device is reset completely. The last operation mode information is lost, the device logic part is unpowered, therefore after increasing the supply voltage to ($V_{CC} > V_{USD} + V_{USDhyst}$) the operation mode will be Reset-mode.

If during this state (under voltage mode) the INx is changed, the operation mode is also changed. After V_{CC} recovering, this new operation mode is taken into account.

3. From Reset mode or Sleep-mode1:

In this modes the digital supply voltage V_{DD} is not available ($V_{DD} < V_{DD_POR_OFF}$) and SPI is not active. It is not possible to read/write via SPI, all SPI registers have the reset values. After entering to the Undervoltage mode, the information about the undervoltage is not saved in a flag (VCCUV).

If V_{CC} rises above the threshold $V_{USD} + V_{USDhyst}$, the device returns to the last mode. If during this state V_{DD} increases to $V_{DD} > V_{DD_POR_ON}$, the device is completely reset. After V_{CC} recovering ($V_{CC} > V_{USD} + V_{USDhyst}$), there will be a startup transition.

The undervoltage flag (VCCUV) is not saved in the following operation modes: Reset mode, Sleep mode 1, Sleep mode 2 and Standby mode.

Figure 3. Battery undervoltage shutdown diagram

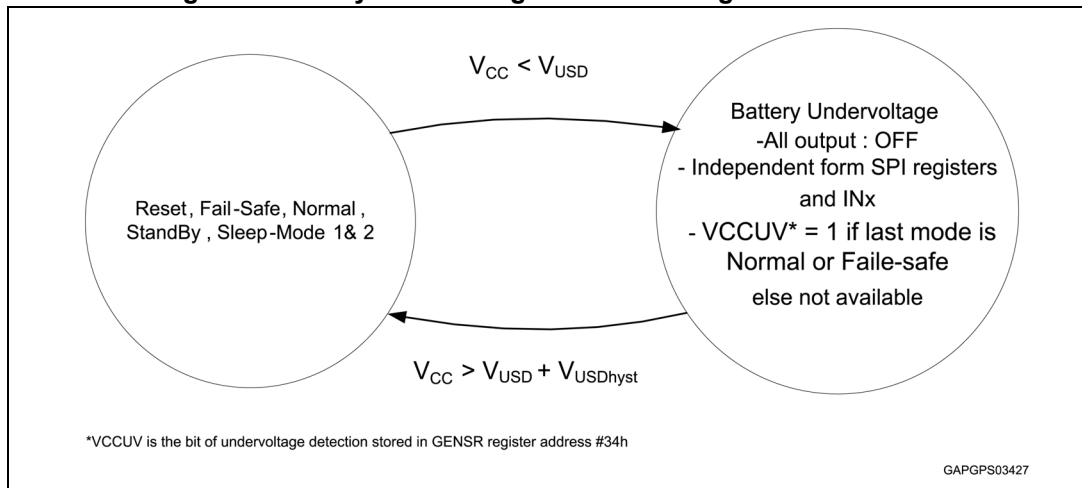
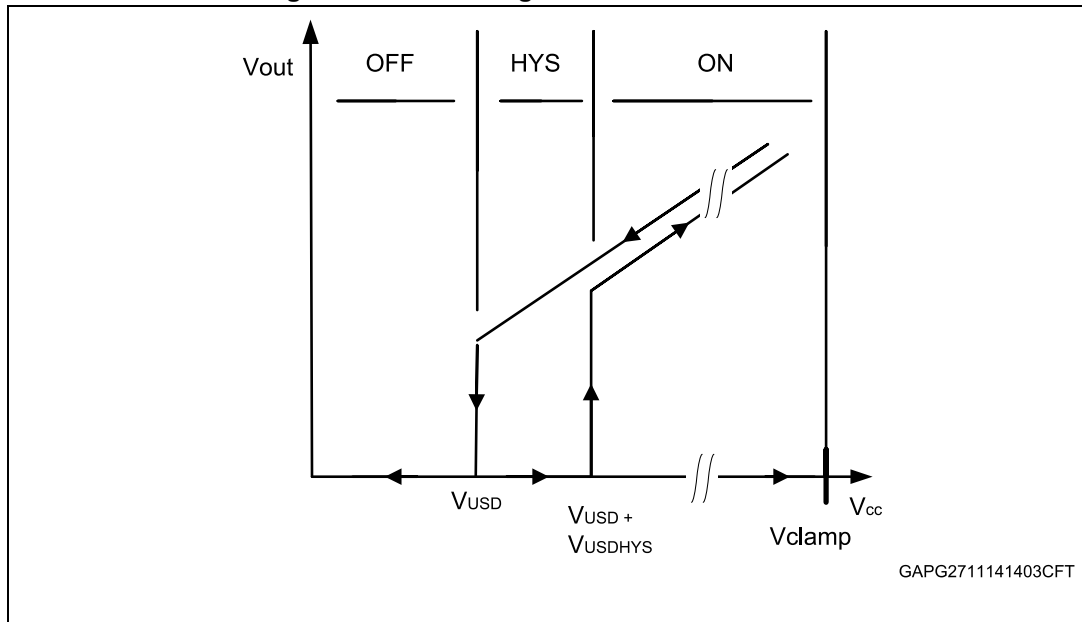


Figure 4. Undervoltage shutdown



2.2.9 Limp Home mode

The Reset mode, the Fail Safe mode and the Sleep mode 1 are combined into the Limp home mode. In this mode the chip is able to operate without the connection to the SPI. All transitions between the states in limp home mode are driven by V_{DD} and INx . The outputs are controlled by the direct inputs INx .

For a direct entry to the Limp Home mode during Normal operating mode, MCU uses the Watchdog Toggle Bit (WDTB) or dedicated SPI command. Changing the polarity of the WDTB within Watchdog Timeout (t_{WDTB}) keeps the device in Normal mode.

For an overview of the operating modes and the triggering conditions please refer to the table below.

Table 10. Operating modes

| Operating mode | Entering conditions | Leaving conditions | Characteristics |
|---|---|---|---|
| Startup transition (this is not an operating mode) | | <ul style="list-style-type: none"> - $V_{CC} > V_{USD}$: reset - ($V_{DD} > V_{DD_POR_ON}$) and ($V_{CC} < V_{USD}$): Fail Safe | <ul style="list-style-type: none"> - Outputs: OFF - SPI: inactive - Registers: reset values - Diagnostics: not available - Reset bit = X |
| Reset (Limp Home mode) | <ul style="list-style-type: none"> - Startup mode: $V_{CC} > V_{USD}$ - Sleep 1: - INx Low to High - Any other mode: $V_{DD} < V_{DD_POR_OFF}$ | <ul style="list-style-type: none"> - All INx low: sleep 1 - $V_{DD} > V_{DD_POR_ON}$: Fail Safe | <ul style="list-style-type: none"> - Outputs: according to INx - SPI: inactive - Registers: reset values - Diagnostics: not available - Reset bit = X |

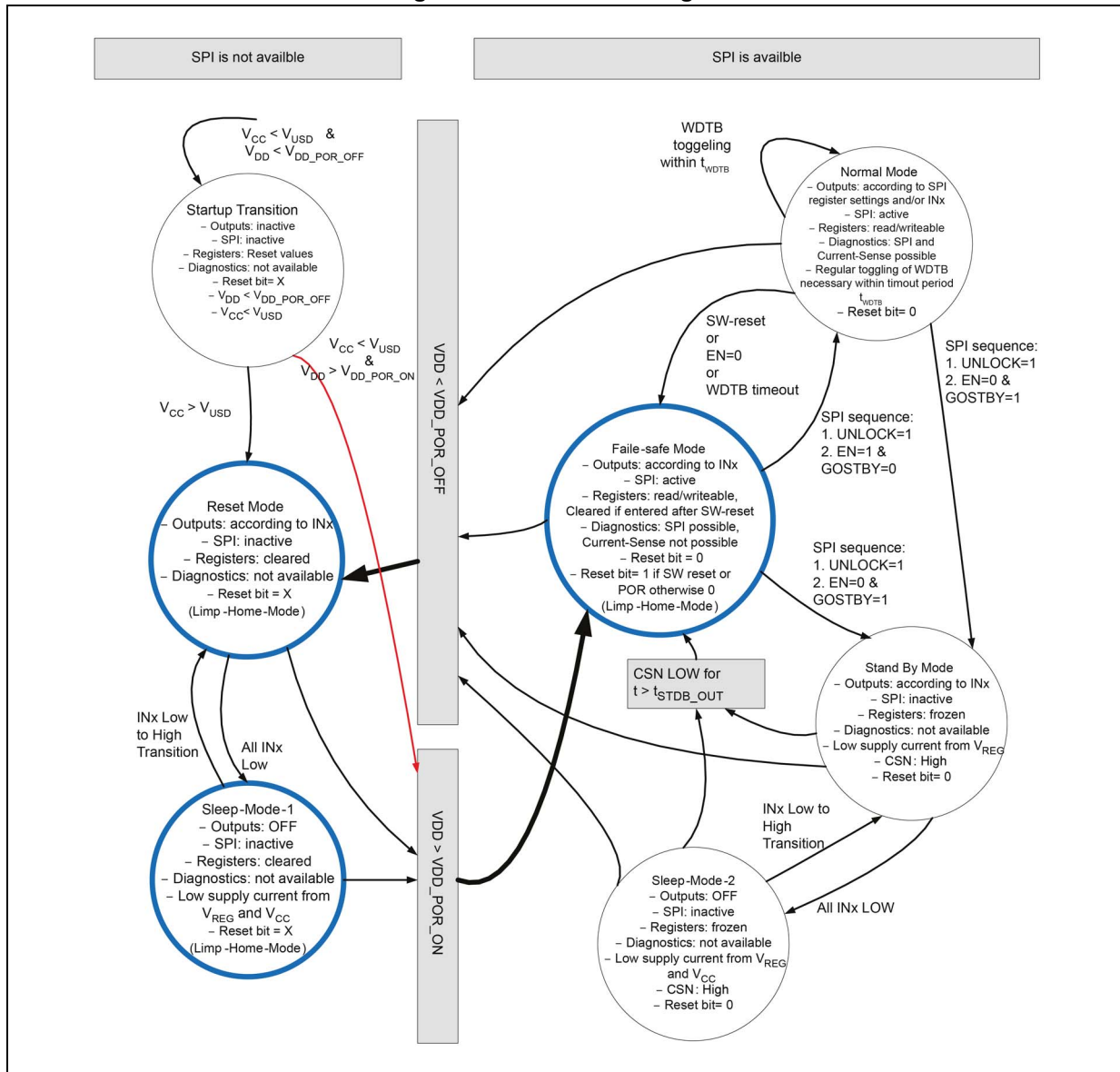
Table 10. Operating modes (continued)

| Operating mode | Entering conditions | Leaving conditions | Characteristics |
|-------------------------------|---|--|--|
| Sleep 1 (Limp Home mode) | Reset: all INx = 0 | <ul style="list-style-type: none"> - V_{DD} > V_{DD_POR_ON}: Fail Safe - INx low to high: reset | <ul style="list-style-type: none"> - Outputs: OFF - SPI: inactive - Registers: reset values - Diagnostics: not available - Low supply current from V_{DD} and V_{CC} - Reset bit = X |
| Fail Safe (Limp Home mode) | <ul style="list-style-type: none"> - Reset or sleep 1: V_{DD} > V_{DD_POR_ON} - Standby or sleep 2: CSN low for t > t_{stdby_out} - Normal: EN = 0 or WDTB toggling timeout or SW-reset | <ul style="list-style-type: none"> - V_{DD} < V_{DD_POR_OFF}: reset - SPI sequence - 1. UNLOCK = 1 - 2. STBY = 0 and EN = 1: normal - SPI sequence - 1. UNLOCK = 1 - 2. STBY = 1 and EN = 0: Standby | <ul style="list-style-type: none"> - Outputs: according to INx - SPI: active - Registers: read/write possible, cleared if entered after SW reset - Diagnostics: SPI possible, CurrentSense diagnostic is not possible - Reset bit = 1 if entered after SW reset or POR, else Reset bit = 0 |
| Normal | <ul style="list-style-type: none"> - Fail Safe: SPI sequence - 1. UNLOCK = 1 - 2. STBY = 0 and EN = 1 | <ul style="list-style-type: none"> - V_{DD} < V_{DD_POR_OFF}: reset - SPI sequence - 1. UNLOCK = 1 - 2. STBY = 1 and EN = 0: Standby - EN = 0 or WDTB time out or SW reset: Fail- Safe | <ul style="list-style-type: none"> - Outputs: according to SPI register settings and/or INx - SPI: active - Registers: read/write is possible - Diagnostics: SPI and CurrentSense diagnostic possible - Regular toggling of WDTB is necessary within timeout period t_{WDTB} - Reset bit = 0 |
| Standby | <ul style="list-style-type: none"> - Normal: SPI sequence - 1. UNLOCK = 1 - 2. STBY = 1 and EN = 0 - Fail Safe: SPI sequence - 1. UNLOCK = 1 - 2. STBY = 1 and EN = 0 - Sleep 2: INx low to high | <ul style="list-style-type: none"> - V_{DD} < V_{DD_POR_OFF}: Reset - CSN low for t > t_{stdby_out}: Fail-Safe - All INx low: sleep 2 | <ul style="list-style-type: none"> - Outputs: OFF - SPI: inactive - Registers: frozen - Diagnostics: not available - Low supply current from V_{DD} and V_{CC} - CSN: High - Reset bit = 0 |

Table 10. Operating modes (continued)

| Operating mode | Entering conditions | Leaving conditions | Characteristics |
|---|------------------------------|---|---|
| Sleep 2 | Standby: all INx = 0 | <ul style="list-style-type: none"> – $V_{DD} > V_{DD_POR_OFF}$: reset – CSN low for $t > t_{stdby_out}$: Fail-Safe – INx low to high: Standby | <ul style="list-style-type: none"> – Outputs: OFF – SPI: inactive – Registers: frozen – Diagnostics: not available – Low supply current from V_{DD} and V_{CC} – CSN: High – Reset bit = 0 |
| Battery undervoltage (this is not an operating mode) | Any mode: $V_{CC} < V_{USD}$ | $V_{CC} > V_{USD} + V_{USDhyst}$: back to last mode | <ul style="list-style-type: none"> – Outputs: OFF and independent from INx and SPI – SPI: as the last mode – Reset bit = 0 |

Figure 5. Device state diagram



3 Protections

3.1 Pre-warning

If the case-temperature rises above the case-thermal detection pre-warning threshold T_{CSD} , the bit T_{CASE} in the Global Status Byte is set. T_{CASE} is cleared automatically when the case- temperature drops below the case-temperature reset threshold T_{CR} .

3.2 Junction overtemperature (OT)

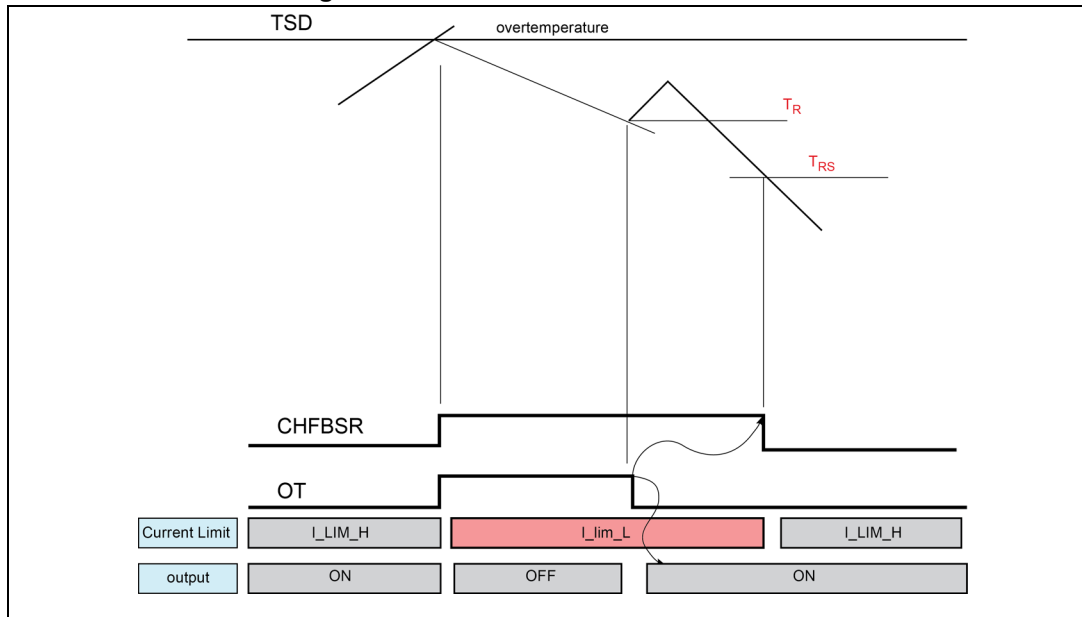
If the junction temperature of one channel rises above the shutdown temperature T_{TSD} , an overtemperature event (OT) is detected.

The channel is switched OFF and the corresponding bit in the Address 0x30h - Channel Feedback Status Register (CHFBSR) is set. Consequently, the thermal shutdown bit (bit 4) in the Global Status Byte and the Global Error Flag are set.

In Limp Home Mode each output channel works in unlimited auto-restart, whereas in Normal Mode it can be either set as latch-off or programmable time limited auto-restart operations in case of junction overtemperature event.

- In Auto-restart operation, the output is switched off as described and switches on again automatically when the junction temperature falls below the reset temperature T_R . The status bit is latched during OFF-state of the channel in order to allow asynchronous diagnostic and it is automatically cleared when the junction temperature falls below the thermal reset temperature of OT detection T_{RS} .
- In Latched OFF operation, the output remains switched OFF until the junction temperature falls below T_R and a write command to the addressed latched OFF channel is sent (CHLOFFTCRx). The action will clear the corresponding flag in CHLOFFSR and bit 2 in the Global Status Byte. Bit 2 only remains stuck at logic high if another fault condition is present at the same time.
- In time limited auto-restart, during the programmed time, it reacts as in auto-restart operation mode. After the programmed time expiration, the output remains switched OFF and acts as above described in latch-off mode.

Figure 6. Thermal shutdown



3.3 Power limitation (PL)

If the difference between junction temperature and case temperature ($\Delta T = T_j - T_c$) rises above the power limitation threshold ΔT_{PLIM} , a power limitation event is detected. The channel is switched OFF and the corresponding bit in the Address 0x30h - Channel Feedback Status Register (CHFBSR) is set. Consequently, the Power limitation bits (bit 4) in the Global Status Byte and the Global Error Flag are set.

In Limp Home Mode each output channel works in unlimited auto-restart, whereas in Normal Mode it can be either set as latch-off or programmable time limited auto-restart operations in case of power limitation event.

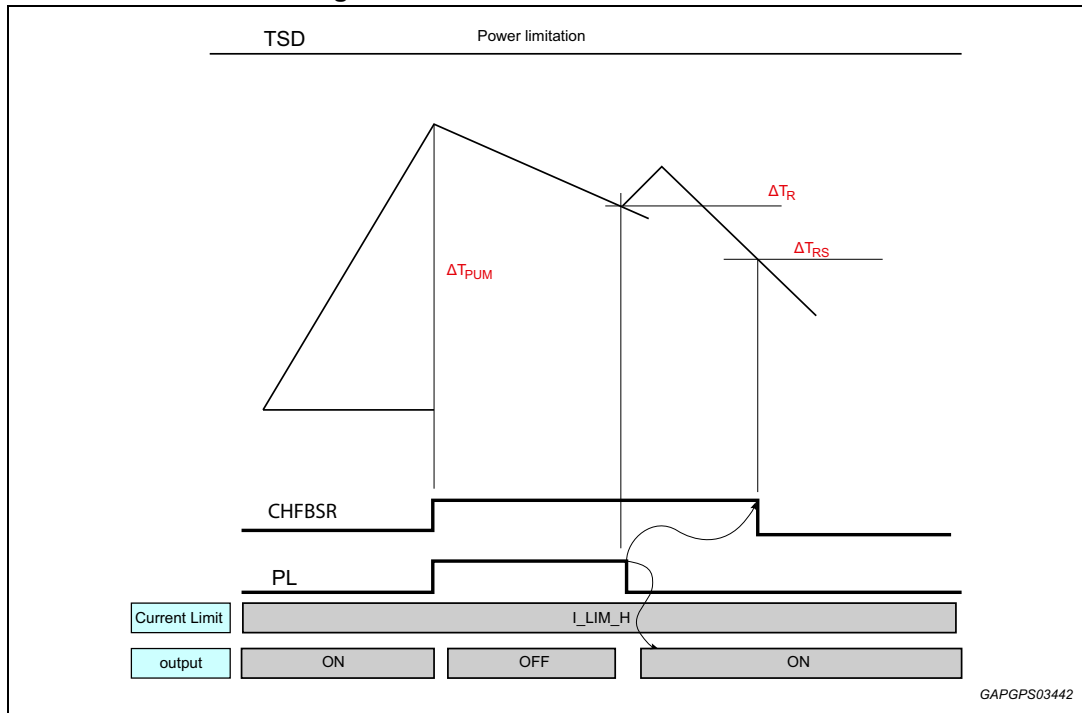
- In Auto-restart operation, the output is switched off as described and switches on again automatically when the difference of junction temperature and case temperature ($\Delta T = T_j - T_c$) decreases below ΔT_{PLIMR} .

In OFF-state of the channel, the status bit is latched in order to allow asynchronous diagnostic and is cleared during a Read and Clear command.

The payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

- In Latched OFF operation, the output remains switched OFF until the difference of junction temperature and case temperature ($\Delta T = T_j - T_c$) decreases below ΔT_{PLIMR} and a write command to the addressed latched OFF channel is sent (CHLOFFTCRx). The action will clear the corresponding flag in CHLOFFSR and bit 2 in the Global Status Byte. Bit 2 only remains stuck at logic high if another latch-off condition is present at the same time.
- In time limited auto-restart, during the programmed time, the device reacts as in auto-restart operation mode. After the programmed time expiration, the output remains switched OFF and acts as above described in latch-off mode.

Figure 7. Power limitation



4 SPI functional description

4.1 SPI communication

The SPI communication is based on a standard ST-SPI 16-bit interface, using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

4.1.1 Signal description

During all operations, V_{DD} must be held stable and within the specified valid range: $V_{DD\ min}$ to $V_{DD\ max}$.

Table 11. SPI signal description

| Name | Function |
|------------------------|---|
| Serial clock SCK | This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SDO) change after the falling edge of Serial Clock (SCK). |
| Serial data input SDI | This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of Serial Clock (SCK). |
| Serial data output SDO | This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (SCK). |
| Chip select CSN | <p>When this input signal is High, the device is deselected and Serial Data Output (SDO) is high impedance. Driving this input Low enables the communication. The communication must start on a Low level of Serial Clock (SCK). Data are accepted only if exactly 16 bits (or 8 bits Short Frame option) have been shifted in.</p> <p>Note: as per the ST_SPI standard, in case of failing communication:</p> <ul style="list-style-type: none"> – Stuck @HIGH: <p>If the device is in Normal Mode, a WDTB Timeout will force the device into Fail-safe mode. The Serial Data-Out (SDO) will stay in High impedance (High Z). Any valid communication arrived after this event will be accepted by the device.</p> – Stuck @LOW: <p>in this case and whatever the mode of the device, a CSN Timeout protection will be activated and force the device to release the SPI bus. Then the Serial Data-Out (SDO) will go into High impedance (High Z).</p> <p>A reset of the CSN Timeout (described as $t_{S\ HIGH}$ parameter in Table 58: Dynamic characteristics - Mode 1) is activated with a transition Low to High on CSN pin (or with a Power On Reset or Software reset). With this reset, the Serial Data-Out (SDO) will be released and any valid communication will be accepted by the device. Without this reset, next communication will not be taken into account by the device.</p> |

4.1.2 Connecting to the SPI bus

A schematic view of the architecture between the bus and devices can be seen in [Figure 9: Bus master and two devices in a normal configuration](#).

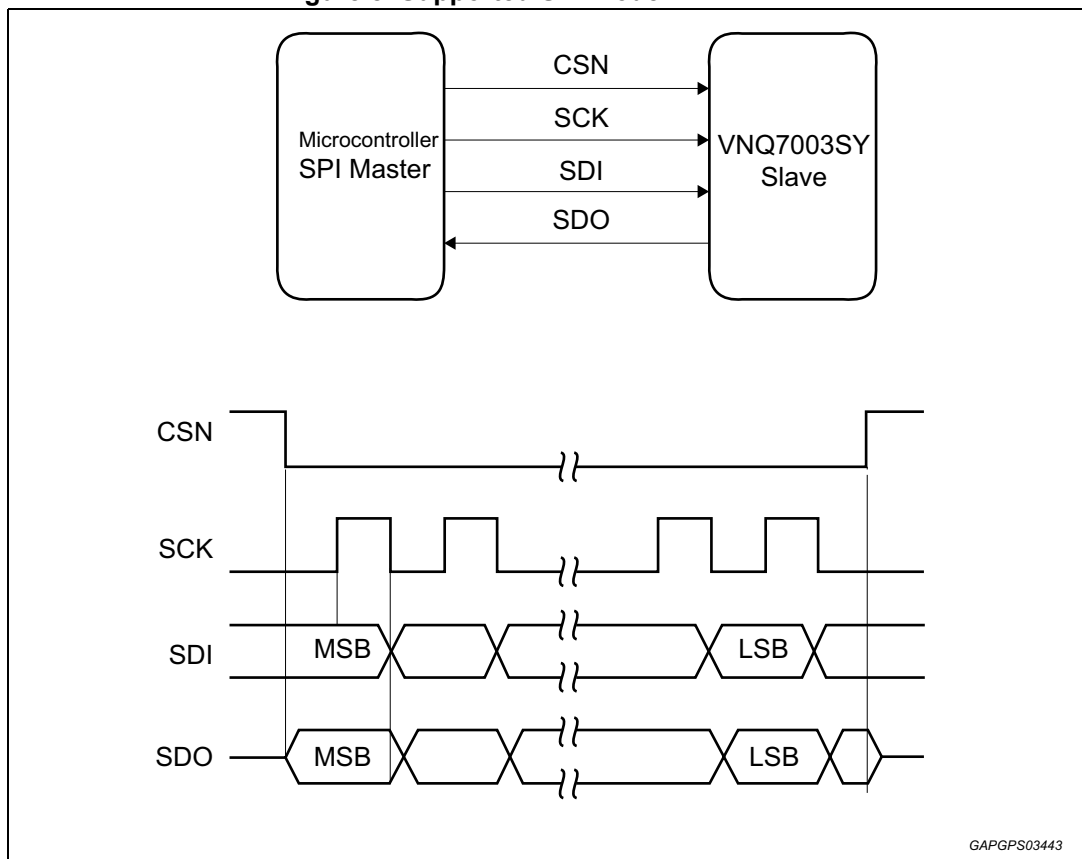
All input data bytes are shifted into the device, MSB first. The Serial Data Input (SDI) is sampled on the first rising edge of the Serial Clock (SCK) after Chip Select (CSN) goes low.

All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the Chip Select (CSN).

4.1.3 SPI mode

Supported SPI mode during a communication phase can be seen in the following figure:

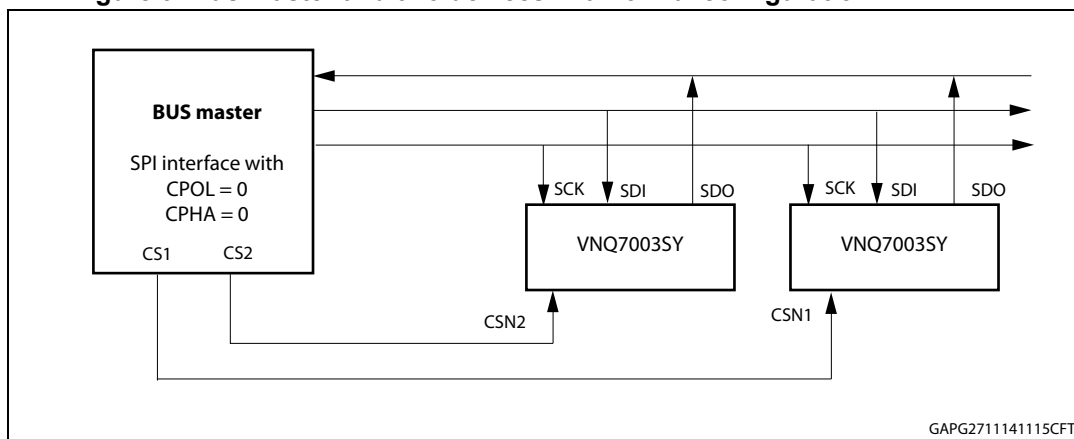
Figure 8. Supported SPI mode



This device can be driven by a micro controller with its SPI peripheral running in the following mode:

- CPOL = 0, CPHA = 0

Figure 9. Bus master and two devices in a normal configuration



4.2 SPI protocol

4.2.1 SDI format

SDI, Frame 16-bit

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6 bit address (A0:A5). The command byte is followed by an input data byte (D0:D7).

Table 12. Command byte

| MSB | | | | | | | LSB |
|-----|----|----|----|----|----|----|-----|
| OC1 | A5 | A4 | A3 | A2 | A1 | A0 | A0 |

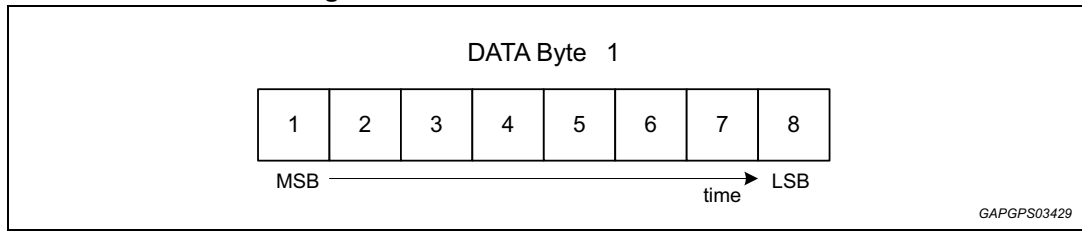
Table 13. Input data byte

| MSB | | | | | | | LSB |
|-----|----|----|----|----|----|----|-----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

SDI, Frame 8 bit

SPI Data-In Frame length 8 bits is defined for the device requiring fast write access to single 8 bit register, called SOCR address 0x07h. SDI Frame consists of Input Data Byte content only, no Operation Code + Address is transmitted.

Figure 10. SDI Frame 8 bits



4.2.2 SDO format

SDO, Frame 16-bit

SDO format during each communication frame starts with a specific byte called Global Status Byte (see [Section 4.3.1: Global Status byte description](#) for more details of bit0- bit7). This byte is followed by an output data byte (D0:D7).

Table 14. Global status byte

| | | | | | | | | |
|------------|------|------|------|------|------|------|------------|--|
| MSB | | | | | | | LSB | |
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |

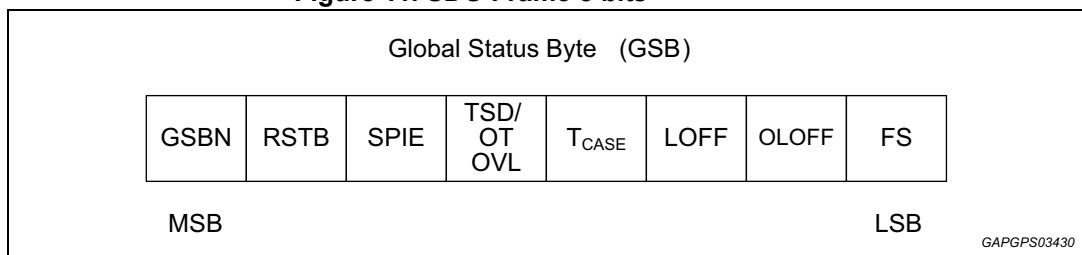
Table 15. Output data byte

| | | | | | | | | |
|------------|----|----|----|----|----|----|------------|--|
| MSB | | | | | | | LSB | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

SDO, Frame 8-bit

SDO Frame of 8 bits consists of GSB content only.

Figure 11. SDO Frame 8 bits



4.2.3 Operating code definition

The SPI interface features four different addressing modes which are listed in [Table 16: Operating codes](#).

Table 16. Operating codes

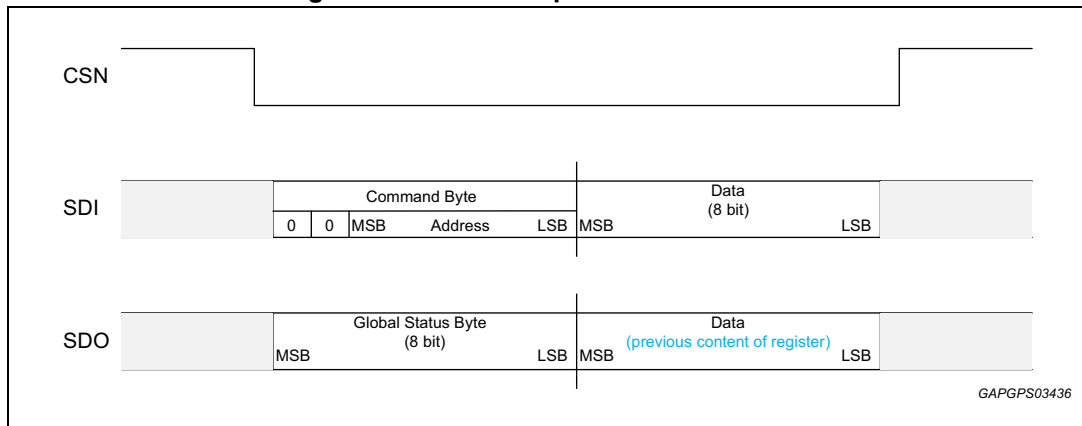
| OC1 | OC0 | Meaning |
|-----|-----|---------------------------------|
| 0 | 0 | Write operation |
| 0 | 1 | Read operation |
| 1 | 0 | Read and clear status operation |
| 1 | 1 | Read device information |

Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in [Table 20: RAM memory map](#)). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence outgoing data are shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the previous content of the addressed register.

Figure 12. SPI write operation



Read mode

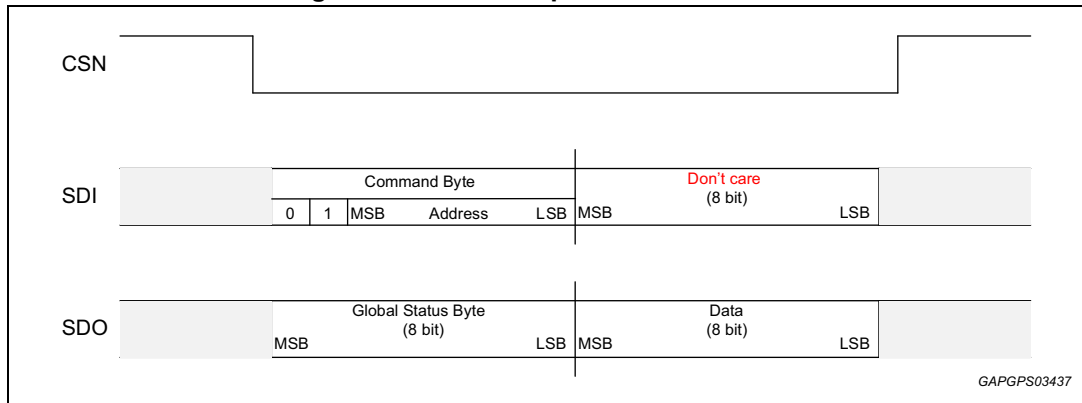
The read mode of the device allows to read and to check the state of any register. Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the content of the addressed register.

In case of a read mode on an unused address, the global status/error byte on the SDO pin is followed by 0x00h byte.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 13. SPI read operation



Read and clear status command

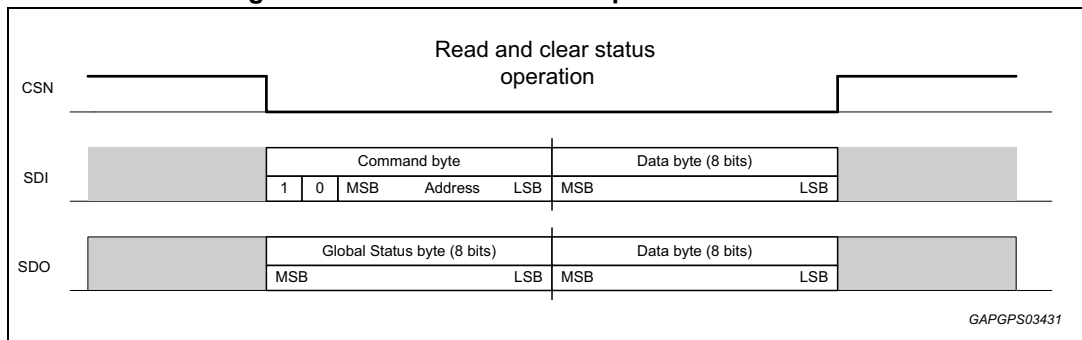
The read and clear status operation is used to clear the content of the addressed status register (see [Table 20: RAM memory map](#)). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 14. SPI read and clear operation



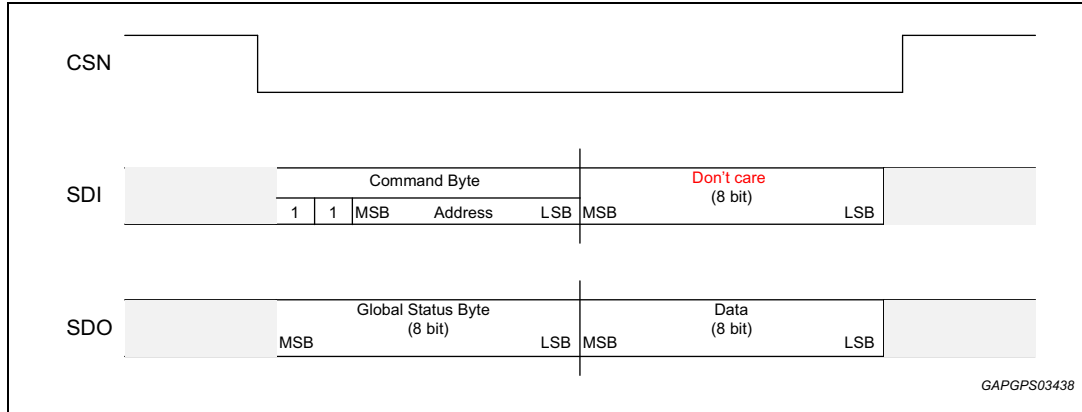
Read device information

Specific information can be read but not modified during this mode. Accessible data can be seen in [Table 21: ROM memory map](#).

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read while the data byte is "don't care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

Figure 15. SPI read device information



4.2.4 Special commands

0xFF — SW-Reset: set all control registers to default

An Opcode '11' (read device information) addressed at '111111' forces a Software Reset of the device.

An OpCode '11' at address '111111' with data field equal to '11111111' the SPI frame is recognized as a frame error and SPIE bit of GSB is set.

Table 17. 0xFF: SW_Reset

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|-------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

0xBF — clear all status registers (RAM access)

When an OpCode '10' (read and clear operation) at address b'111111 is performed.

Table 18. Clear all status registers (RAM access)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|---------|-------|-------|-------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | Address | | | | | |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Note: Reset Value = the value of the register after a power on.

Note: Default value = the default value of the register. Currently this is equivalent to the Reset value.

Note: Cleared register = explicitly read and clear of the register, if it is not write protected.

4.3 Register map

Device contains a set of RAM registers used for device configuration, the device status and ROM registers for device identification. Since ST-SPI is used, Global Status byte defines the device status, containing fault information.

4.3.1 Global Status byte description

The data shifted out on SDO during each communication starts with a specific byte called Global Status Byte. This one is used to inform the microcontroller about global faults which can happen at channel-side level (i.e. like thermal shutdown, OLOFF...) or on the SPI interface (like Watchdog monitoring timeout event, communication error,...). This specific register has the following format.

Table 19. Global status byte

| Bit | Name | Reset | Content |
|-----|---|-------|--|
| 7 | Global Status Bit Not | 0 | The GSBN is a logically NOR combination of Bit 0 to Bit 6. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low. |
| 6 | Reset bit | 1 | The RSTB indicates a device reset. In case this bit is set, all internal Control Registers are set to default and kept in that state until the bit is cleared. The Reset bit is automatically cleared by any valid SPI communication |
| 5 | SPI Error | 0 | The SPIE is a logical OR combination of errors related to a wrong SPI communication (SCK count and SDI stuck at errors). The SPIE is automatically cleared by a valid SPI communication. |
| 4 | Thermal shutdown (OT) or Power limitation (PL) or VDS | 0 | This bit is set in case of thermal shutdown, power limitation or in case of high VDS (VDS) at turn-off detected on any channel. The contribution of high VDS failure is maskable. |
| 3 | T _{CASE} | 0 | This bit is set if the frame temperature is greater than the threshold and can be used as a temperature pre-warning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (TCR). |
| 2 | Latch OFF (LOFF) | 0 | The Device Error bit is set when one or more channels are latched OFF |
| 1 | Open-load at off-state or output shorted to VCC | 0 | This bit is set in case of open-load off-state or output shorted to V _{CC} condition detected on any channel |
| 0 | FailSafe | 1 | The bit is set in case device operates in Fail Safe Mode |

Note: The FFh or 00h combinations for the Global Status Byte are not possible, exclusive combination exists between bit 7 and bit 0 - bit 6. Consequently a FFh or 00h combination for the Global Status Byte must be detected by the microcontroller as a failure (SDO stuck to GND or to VDD or loss of SCK).

4.3.2 RAM

RAM registers can be separated according to the frequency of usage

- init - register is read/ written during initialization phase (single shot action)
- continuous - read/ write/ read and clear registers often accessed, applying outputs control and diagnostic
- rare - read/ read and clear status of device registers accessed on demand (in case of failure)

Table 20. RAM memory map

| Address | Name | Access | Content | Access type | Reset value |
|-------------------|---------------|------------|------------------------------------|-------------|-------------|
| Control registers | | | | | |
| 00h | CTRL | Read/Write | Device enable, standby, protected | init | 0x00 |
| 01h | DIENCR | Read/Write | Direct Input Enable Control | init | 0x00 |
| 02h | OLOFFC R | Read/Write | Open-load OFF-state Control | init | 0x00 |
| 03h | CCR | Read/Write | Channel Control | init | 0x00 |
| 04h | FASTSW CR | Read/Write | Fast Switching Control Register | init | 0x00 |
| 05h | RESERVED | | | | |
| 06h | CSMUXC R | Read/Write | CurrentSense Multiplexer Control | continuous | 0x00 |
| 07h | SOCR | Read/Write | SPI Output Control | continuous | 0x00 |
| 08h | CHLOFF TCR0,1 | Read/Write | Channel Latch OFF Timer Control | init | 0x00 |
| 09h | CHLOFF TCR2,3 | Read/Write | Channel Latch OFF Timer Control | init | 0x00 |
| ... | area not used | | | | |
| Status registers | | | | | |
| 2Fh | DIENSR | Read only | Direct Input Status | rare | 0x00 |
| 30h | CHFBSR | Read/Clear | Channel Feedback Status Register | continuous | 0x00 |
| 31h | STKFLTR | Read/Clear | Open-load OFF-state/Stuck to Vcc | rare | 0x00 |
| 32h | CHLOFF SR | Read only | Channels latch-off status register | rare | 0x00 |
| 33h | VDSFSR | Read/Clear | VDS feedback | rare | 0x00 |

Table 20. RAM memory map (continued)

| Address | Name | Access | Content | Access type | Reset value |
|-----------------|----------|------------|-------------------------|-------------|-------------|
| 34h | GENSR | Read/Clear | Generic Status | rare | 0x00 |
| ... | | | not used area | | |
| other registers | | | | | |
| 3Eh | RESERVED | | | | |
| 3Fh | CONFIG | Read/Write | Configuration Register, | continuous | 0x00 |

Note: Any command (write, read or read and clear status) executed on a “not used”. RAM register, i.e. a not assigned address, does not have any effect: there is no change in the Global Status byte (no communication error, no error flag). The data written to this address (2nd byte of SDI frame) is ignored. The data read from this address (2nd byte of SDO frame) contains 00, independent of what has been written previously to this address.

Note: A write command on “don’t care” bits of an assigned RAM register address does not have any effect: There is no change on the Global Status byte. The data written to the “don’t care bits” is ignored. The content of the “don’t care bits” remains at “0” independent of the data written to these bits.

4.3.3 ROM

This memory is used for device identification.

Table 21. ROM memory map

| Address | Name | Description | Access | Content |
|---------|----------------|--|-----------|---------|
| 00h | Company code | Indicates the code of STM company | Read only | 00H |
| 01h | Device Family | indicates the product family | Read only | 01H |
| 02h | Product Code 1 | Indicates the first code of the product | Read only | 56H |
| 03h | Product Code 2 | Indicates the second code of the product | Read only | 48H |
| 04h | Product Code 3 | Indicates the third code of the product | Read only | 31H |
| ... | | not used area | | |
| 0Ah | Version | Silicon version | Read only | 03H |
| ... | not used area | | | |
| 10h | SPI Mode | Different Modes of the SPI (see chapter ‘SPI Modes’) | Read only | 18H |
| 11h | WD Type 1 | Indicates the type of WatchDog used in the | Read only | 46H |
| 12h | | not used area | | |

Table 21. ROM memory map (continued)

| Address | Name | Description | Access | Content |
|---------|-------------------|---|-----------|---------|
| 13h | WD bit position 1 | Indicates the address of the register containing the WD | Read only | 7FH |
| 14h | WD bit position 2 | Indicates the position of the WD toggle bit | Read only | C0H |
| ... | not used area | | | |
| 20h | SPI CPHA | Indicates the polarity and phase of the SPI interface | Read Only | 55H |
| 3Eh | GSB Options | Options of GSB byte (standard GSB definition) | Read Only | 00H |
| 3Fh | Advanced OP. Code | — | — | — |

4.3.4 SPI modes

By reading out the <SPI Mode> register general information of SPI usage of the Device Application Registers can be read.

Table 22. SPI Mode

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| BR | DL2 | DL1 | DL0 | SPI8 | 0 | S1 | S0 |

SPI Burst Read

Table 23. SPI Burst Read

| Bit 7 | Description |
|-------|-------------|
| 0 | BR disabled |
| 1 | BR enabled |

The Burst Read is not implemented in this product so this bit is disabled.

SPI Data Length

The SPI Data Length value indicates the length of the SCK count monitor which is running for all the accesses to the Device Application Registers. In case a communication frame with an SCK count is not equal to the reported one, the device will lead to a SPI Error and the data will be rejected.

The Frame Length is specified on 3 bits in SPI Mode register located in ROM part. The 16bit SPI communication is implemented in this product so these bits are '001'.

Table 24. SPI Data Length

| Bit 6 | Bit 5 | Bit 4 | Description |
|-------|-------|-------|-------------|
| DL2 | DL1 | DL0 | |
| 0 | 0 | 0 | Invalid |
| 0 | 0 | 1 | 16bit SPI |
| 0 | 1 | 0 | 24bit SPI |
| ... | | | ... |
| 1 | 1 | 1 | 64bit SPI |

SPI 8 bit Frame

The SPI 8 bit Frame bit indicates if an 8 bit Frame communication is available.

The intention of an 8 bit Frame enhancement is to provide fast write access to one 8 bit register, which is very often rewritten with new content.

SOCR register address is predefined as addressed register during 8 bit SPI Communications.

Table 25. SPI 8 bit Frame

| Bit 3 | Description |
|-------|----------------------------------|
| SPI8 | |
| 0 | 8 bit Frame option not available |
| 1 | 8 bit Frame option is available |

The SPI 8 bit Frame is implemented in this product so this bit is equal to '1'.

A short Frame with a Data Field equal to '00000000' is rejected and considered as a SPI Frame Error condition.

Data Consistency Check (Parity/CRC)

For some devices a Data Consistency Check is required. Therefore either a parity-check or for very sensitive systems a CRC may be implemented.

It is defined on 2 bits, in SPI Mode register located in ROM Part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO).

Table 26. SPI Data Consistency Check

| Bit 1 | Bit 0 | Description |
|-------|-------|-------------|
| S1 | S0 | |
| 0 | 0 | not used |
| 0 | 1 | Parity used |
| 1 | 0 | CRC used |
| 1 | 1 | Invalid |

In case either the Parity or the CRC check is implemented it is always located at the end of the communication.

As these two checks are not implemented in the product, the two bits are equal to '00'.

4.4 Output switching slopes control

Outputs switching slopes are set by configuration register FASTSWCR.

Address 0x04h - Fast Switching Configuration Register (FASTSWCR).

The FASTSWCR allows configuring each channel in fast switching mode.

The typical switching slopes are shown in the following table:

Table 27. Switching slopes

| FASTSWCR | Channel 0,1 (V/μs) | Channel 2, 3 (V/μs) |
|----------|--------------------|---------------------|
| 0 | 0.30 | 0.20 |
| 1 | 0.45 | 0.30 |

4.5 Output control

Depending on the actual device mode, outputs can be controlled by SPI register or Direct Input INx.

1. **SPI register SOCR** - in normal mode outputs can be turned ON/OFF, applying Bit[n] = 1/0

[n]: is the related channel, n = 0 for the channel 0, and n = 3 for channel 4

Example 1:

Turning ON channel 1 and 2 with turning OFF others (without taking in consideration the PWM or phase shifting)

Table 28. Write SOCR 0x06

| Bit7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|---------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | | | | Address | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Data | | | | | | | |
| x | x | x | x | SOCR3 | SOCR2 | SOCR1 | SOCR0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Example 2:

Turning ON channel 0 without changing other channels status

Dummy = Read SOCR

Dummy = [Dummy.OR.0x01] & 0x3F => Dummy = b00000111



Table 29. Write SOCR Dummy

| Bit7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|-------|-------|---------|-------|-------|
| Command | | | | | | | |
| OC1 | OC0 | | | | Address | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Data | | | | | | | |
| x | x | x | x | SOCR3 | SOCR2 | SOCR1 | SOCR0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

2. **Direct Input INx** - in Fail safe, Standby and Reset modes, turn ON/OFF the outputs by applying high, respectively low, logic levels to dedicated pin.

While in normal mode, output can use INx pin to control output if corresponding bit in DIENCR is at logic high level.

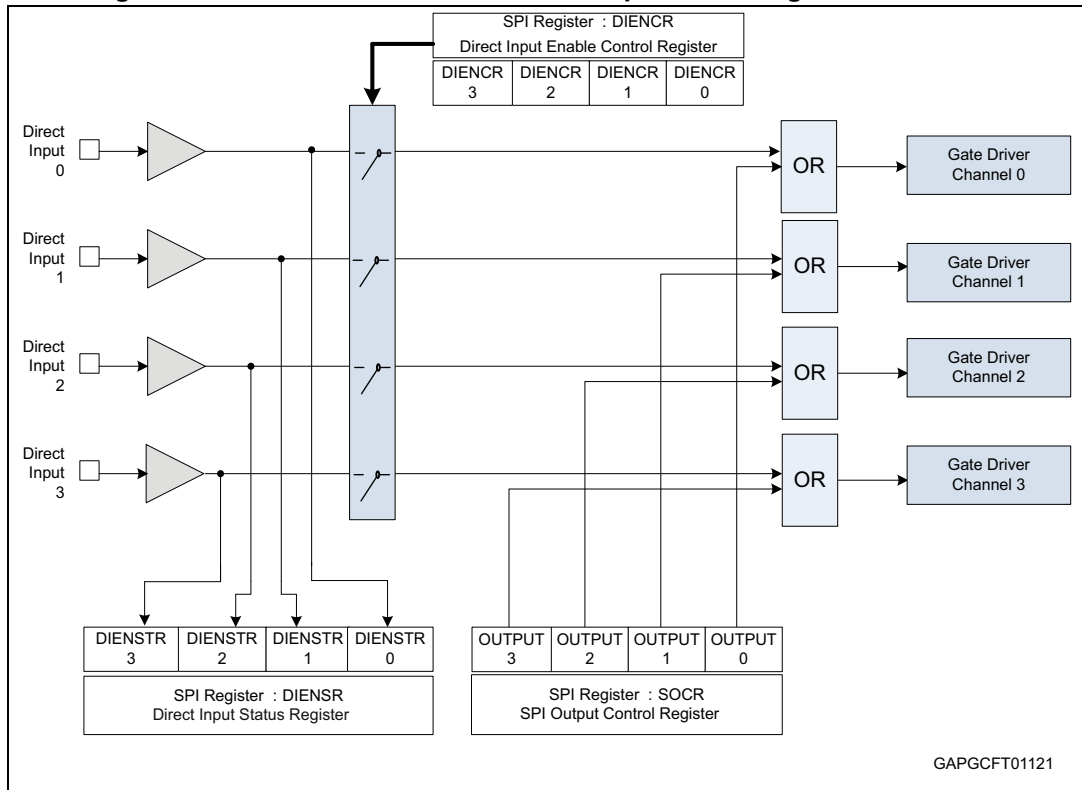
Then this truth table specifies output state:

Table 30. Truth table

| DIENCRx | SOCRx | INx | OUTPUTx state |
|---------|-------|-----|---------------|
| 1 | 1 | X | ON |
| 1 | 0 | L | OFF |
| 1 | 0 | H | ON |
| 0 | 1 | X | ON |
| 0 | 0 | X | OFF |

The output channels 0 and 1 can be configured to operate in BULB or LED mode using the Channel Control Register (CCR). If the relevant bit in CCR is 0, the output is configured in BULB mode, if it is set to 1, the output is configured in LED mode.

Figure 16. VNQ7004SY: 4-channel direct input block diagram



4.6 Control registers

4.6.1 Address 0x00h — Control Register (CTLR)

Table 31. CTLR — Control Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | — | |
| 6 | Reserved | — | — | |
| 5 | GOSTBY | R/W | 0 | Go to Standby mode 1: Enter Standby mode It is necessary to do 2 write accesses to enter standby: 1. Write UNLOCK = 1 2. Write GOSTBY = 1 and EN = 0 |
| 4 | UNLOCK | R/W | 0 | Unlock bit, has to be set before GOSTBY or EN can be set |
| 3 | Reserved | — | — | |

Table 31. CTLR — Control Register (continued)

| Bit | Name | Access | Reset | Content |
|-----|--------|--------|-------|---|
| 2 | CTDTH1 | R/W | 0 | Case Thermal Detection Threshold |
| 1 | CTDTH0 | R/W | 0 | These bits allow to configure the case thermal detection of the device. Three temperature thresholds are available by programming these two bits. CDTH1 CTDH0 Detection temp 0 0 120 °C 0 1 130 °C 1 X 140 °C |
| 0 | EN | R/W | 0 | Enter Normal mode 1: Normal mode 0: Fail Safe mode It is necessary to do 2 write accesses to enter Normal mode: 1. Write UNLOCK = 1 2. Write EN = 1 and GOSTBY = 0 |

4.6.2 Address 0x01h — Direct Input Enable Control Register (DIENCR)

Table 32. DIENCR — Direct Input Enable Control Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | — | Reserved |
| 6 | Reserved | — | — | |
| 5 | Reserved | — | — | |
| 4 | Reserved | — | — | |
| 3 | DIENCR3 | R/W | 0 | The DIENCR enables the control of the corresponding output channel by the direct input. 1: parallel input INx controls OUTPUTx 0: function disabled |
| 2 | DIENCR2 | R/W | 0 | |
| 1 | DIENCR1 | R/W | 0 | |
| 0 | DIENCR0 | R/W | 0 | |

Note: Please refer also to [Table 30: Truth table](#).

4.6.3 Address 0x02h — Open-load OFF-State Control Register (OLOFFCR)

Table 33. OLOFFCR — Open-load OFF-state control register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|--|
| 7 | Reserved | — | — | Reserved |
| 6 | Reserved | — | — | |
| 5 | Reserved | — | — | |
| 4 | Reserved | — | — | |
| 3 | OLOFFCR3 | R/W | 0 | The OLOFFCR enables an internal pull-up current generator to distinguish between the open-load OFF-state fault and the output shorted to V _{CC} fault. 1: Pull-up current generator enabled for OUTPUTX 0: Pull-up current generator disabled for OUTPUTX |
| 2 | OLOFFCR2 | R/W | 0 | |
| 1 | OLOFFCR1 | R/W | 0 | |
| 0 | CCRO | R/W | 0 | |

4.6.4 Address 0x03h — Channel Control Register (CCR)

Table 34. CCR — Channel control register

| Bit | Name | Access | Reset | Content |
|-----|---------|--------|-------|---|
| 7 | Reserve | — | — | Reserved |
| 6 | Reserve | — | — | |
| 5 | Reserve | — | — | |
| 4 | Reserve | — | — | |
| 3 | Reserve | — | — | |
| 2 | Reserve | — | — | |
| 1 | CCR1 | R/W | 0 | The CCR selects the BULB or LED mode for the corresponding output. 1: LED mode selected for OUTPUTX 0: BULB mode selected for OUTPUTX |
| 0 | CCR0 | R/W | 0 | |

4.6.5 Address 0x04h — Fast Switching Configuration Register (FASTSWCR)

Table 35. FASTSWCR — Fast Switching Configuration Register

| Bit | Name | Access | Reset | Content |
|-----|-----------|--------|-------|--|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | FASTSWCR3 | R/W | 0 | The FASTSWCR allows to configure each channel in fast switching mode 1: Fast Switch 0: Normal Switch |
| 2 | FASTSWCR2 | R/W | 0 | |
| 1 | FASTSWCR1 | R/W | 0 | |
| 0 | FASTSWCR0 | R/W | 0 | |

4.6.6 Address 0x06h — CurrentSense Multiplexer Control Register (CSMUXCR)

Table 36. CSMUXCR — CurrentSense Multiplexer Control Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | MUXEN | R/W | 0 | The MUXEN enables the CurrentSense output. Monitored channel is selected by MUXCH bits (0..2) |
| 2 | MUXCH | R/W | 0 | Mux channel selection: encoding. |
| 1 | | R/W | 0 | MUXCH = 0..3 - correspond to output channel monitor MUXCH = 4..7 - reserved |
| 0 | | R/W | 0 | b0 ~LSB, b3 ~MSB |

Table 37. Truth table for CurrentSense Mux Control

| b2 | b1 | b0 | CurrentSense enable |
|----|----|----|---------------------|
| 0 | 0 | 0 | CH0 |
| 0 | 0 | 1 | CH1 |
| 0 | 1 | 0 | CH2 |
| 0 | 1 | 1 | CH3 |

4.6.7 Address 0x07h — SPI Output Control Register (SOCR)

Table 38. SOCR — SPI Output Control Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | — | Reserved |
| 6 | Reserved | — | — | |
| 5 | Reserved | — | — | |
| 4 | Reserved | — | — | |
| 3 | SOCR3 | R/W | 0 | The SOCR register controls the output drivers in Normal Mode. One bit per channel and the dx corresponds to channel-x. 1: The corresponding output is enabled 0: The corresponding output is disabled |
| 2 | SOCR2 | R/W | 0 | |
| 1 | SOCR1 | R/W | 0 | |
| 0 | SOCR0 | R/W | 0 | |

Please refer also to [Table 30: Truth table](#).

4.6.8 Address 0x08h — Channel Latch OFF Timer Control Register (ch0, ch1) (CHLOFFTCR0,1)

In Normal Mode, the output behavior in case of power limitation or thermal shutdown is programmable, as latch-off, time limited auto-restart (*t_{blanking}*). The default mode is the latch-off mode.

In latched off-state the fault has to be cleared to re-enable the output channel after an overtemperature or power limitation event through a new value written through SPI command at CHLOFFTCRx register.

In fail-safe state, the device operates in unlimited auto-restart mode.

Example 3:

Table 39. Channel configuration

| Bit x3 | Bit x2 | Bit x1 | Bit x0 | | Blanking time window duration |
|--------|--------|--------|--------|-----|--|
| 0 | 0 | 0 | 0 | 0x0 | 0 ms (latch-off configuration - default) |
| 0 | 0 | 0 | 1 | 0x1 | 17 ms |
| 0 | 0 | 1 | 0 | 0x2 | 34 ms |
| 0 | 0 | 1 | 1 | 0x3 | 51 ms |
| | | | | | |
| 1 | 1 | 1 | 0 | 0xE | 238 ms |
| 1 | 1 | 1 | 1 | 0xF | 255 ms |

Table 40. CHLOFFTCR0,1 — Channel Latch OFF Timer Control Register (ch0, ch1)

| Bit | Name | Access | Reset | Content |
|-----|-------------|--------|-------|--|
| 7 | CHLOFFTCR13 | R/W | 0 | CHLOFFTCR1x It configures the blanking time duration in case of power limitation or overtemperature for the corresponding output. CHLOFFTCR10 - CHLOFFTCR13: for channel 1 |
| 6 | CHLOFFTCR12 | R/W | 0 | |
| 5 | CHLOFFTCR11 | R/W | 0 | |
| 4 | CHLOFFTCR10 | R/W | 0 | |
| 3 | CHLOFFTCR03 | R/W | 0 | CHLOFFTCR0x It configures the blanking time duration in case of the power limitation for the corresponding output. CHLOFFTCR00 - CHLOFFTCR03: for channel 0 |
| 2 | CHLOFFTCR02 | R/W | 0 | |
| 1 | CHLOFFTCR01 | R/W | 0 | |
| 0 | CHLOFFTCR00 | R/W | 0 | |

4.6.9 Address 0x09h — Channel Latch OFF Timer Control Register (ch2, ch3) (CHLOFFTCR2,3)

Table 41. CHLOFFTCR2,3 — Channel Latch OFF Timer Control Register (ch2, ch3)

| Bit | Name | Access | Reset | Content |
|-----|-------------|--------|-------|---|
| 7 | CHLOFFTCR33 | R/W | 0 | CHLOFFTCR3x It configures the blanking time duration in case of the power limitation for the corresponding output. CHLOFFTCR30 - CHLOFFTCR33: for channel 3 |
| 6 | CHLOFFTCR32 | R/W | 0 | |
| 5 | CHLOFFTCR31 | R/W | 0 | |
| 4 | CHLOFFTCR30 | R/W | 0 | |

Table 41. CHLOFFTCR2,3 — Channel Latch OFF Timer Control Register (ch2, ch3) (continued)

| Bit | Name | Access | Reset | Content |
|-----|-------------|--------|-------|--|
| 3 | CHLOFFTCR23 | R/W | 0 | CHLOFFTCR2x |
| 2 | CHLOFFTCR22 | R/W | 0 | It configures the blanking time duration in case of the power limitation for the corresponding output. CHLOFFTCR20 - CHLOFFTCR23: for channel 2 |
| 1 | CHLOFFTCR21 | R/W | 0 | |
| 0 | CHLOFFTCR20 | R/W | 0 | |

5 Diagnostic

Device is capable to provide digital diagnostic information through SPI interface and analogue diagnostic signal using CurrentSense signal.

5.1 Analogue diagnostic

The Analogue output signal provides:

- Mirror Current - output in current mode, proportional of the load current in normal operation, according to K-ratio
- No signal - output is in High Z (tri-state)

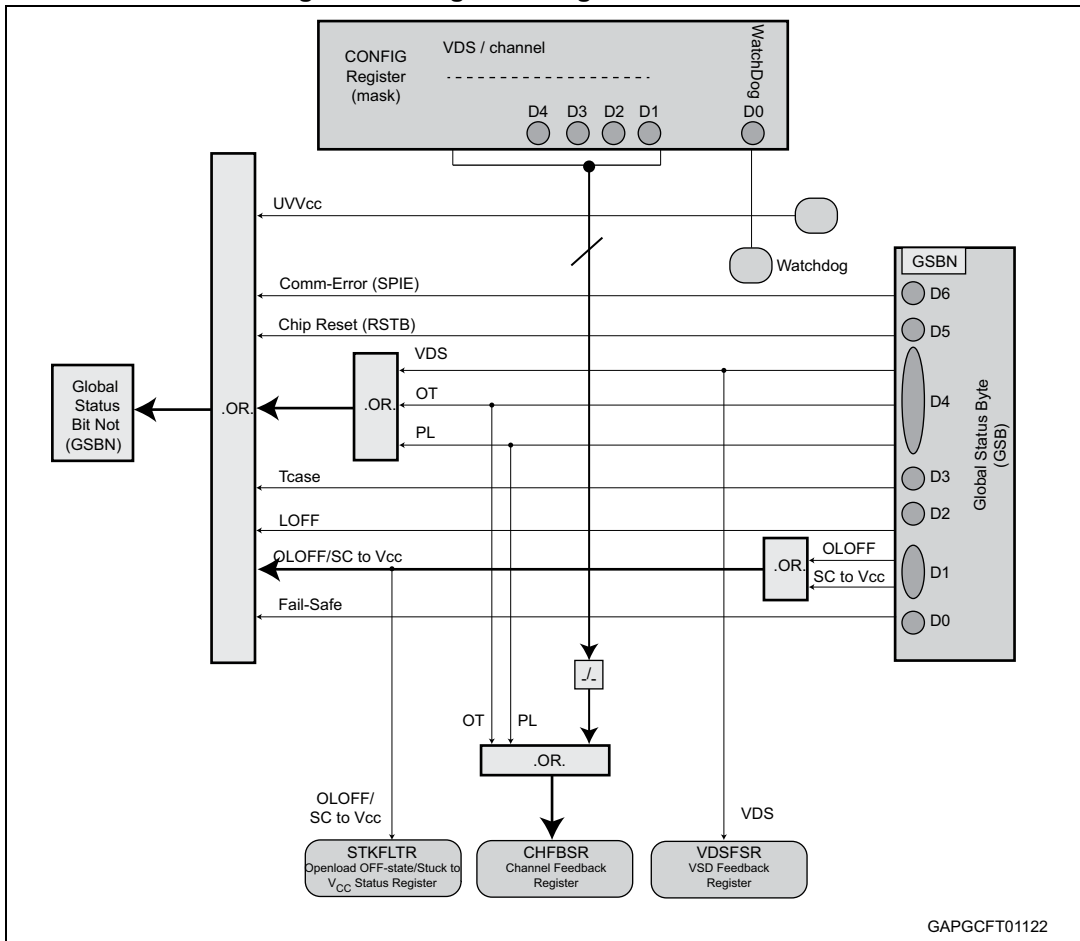
The CSMUXCR register is used to enable the CurrentSense feature of each channel to the CurrentSense pin.

Each channel integrates an analog CurrentSense function which can be connected to the CurrentSense pin by setting the MUXEN bit (bit 3) and by setting the corresponding channel in the MUX channel selection bits (bits 0, 1 and 2) in the address 0x06h - CurrentSense Multiplexer Control Register (CSMUXCR).

5.2 Digital diagnostic

Global status byte (GSB) provides preliminary status of device every SPI communication with device. It informs about device actual mode (normal/ fail-safe).

Figure 17. Diagnostic registers



By reading additional status registers, more detailed information is provided. Status information is stored in the status registers.

5.2.1 Status registers

Table 42. Status registers

| Address | Name | Access | Description |
|---------|----------|------------|--|
| 0x2F | DIENSR | Read | Direct Input Status register. This register is a real time one and reads back the Input state for each direct input. The register content is cleared if the battery voltage is not present. |
| 0x30 | CHFBSR | Read/Clear | Channel Feedback Status Register Each bit specifies channel fault state, providing a logical "OR" combination of VDS, PWLM, OT failure flags related to OUTPUTx. The contribution of VDS failure can be masked through CONFIG register settings. |
| 0x31 | STKFLTR | Read/Clear | Open-load OFF-state/ Stuck to V _{CC} Status Register Provides information about open load or stuck to V _{CC} , depending on the configuration of the OLOFFCR register. |
| 0x32 | CHLOFFSR | Read | Channels latch-off status register One bit per channel. In case a channel is latch-off, this flag is set and is readable by MCU In latched-off state the fault has to be cleared through a Write operation of dedicated CHLOFFTCRx register to re-enable the output channel after an overtemperature or power limitation event |
| 0x33 | VDSFSR | Read/Clear | VDS feedback status register Each bit specifies channel fault state in case of high voltage drop across PowerMos (VDS) |
| 0x34 | GENSR | Read/Clear | Generic Status register Bit 7: Undervoltage warning flag Bit 6: Reset warning bit. This bit is set in case of Reset event (HW Reset or SW Reset). Bit 5: SPI Error warning bit. Bit 6 & Bit 5 have to be cleared through a Read & Clear command. Bit 7 is a real time bit. |

Note: Regarding **CHLOFFSR** register, **Time limited auto-restart** and for further information about the Configurable blanking time, please refer to the related chapter.

5.3 Over load (VDS high voltage, Over Load (OVL))

During low duty cycle PWM operation on a shorted load, ON-time may be too short to allow power limitation or overtemperature detection. CurrentSense output is disabled. This would make detection of over load condition impossible. To overcome this, always when an output channel is turned OFF, the voltage drop on the PowerMOS (V_{DS}) is measured. If V_{DS} (voltage across PowerMOS output stage) exceeds the threshold defined by the parameter

V_{DS_OVL} , an over load condition is detected. The corresponding bit in the over load status register VDSFSR (address 0x33h) is set.

The same information is saved in the Channel Feedback Status Register (CHFBSR), if it is not masked in the CONFIG register.

Consequently, the bit 4 in the Global Status Byte and the Global Error Flag are set, if it is not masked in the CONFIG register.

The VDSFSR is a warning and the channel can be switched on again even if the VDSFSRx bit is set. The VDSFSRx bit remains unchanged until a read and clear command on VDSFSR is sent by the SPI or until the output is turned off the next time, when V_{DS} is evaluated again.

In case of low duty cycle PWM operation (i.e. 3% typical at 200 Hz in Bulb mode), V_{DS} might be greater than a threshold defined by the parameter V_{DS_OVL} even if the output is not in over load state so that a false warning is issued.

Please refer to the [Section 4.3.1: Global Status byte description](#), [Section 5.7: Address 0x30h — Channel Feedback Status Register \(CHFBSR\)](#) and [Section 5.10: Address 0x33h — VDS Feedback Status Register \(VDSFSR\)](#).

5.4 Open-load ON-state detection

The open-load ON-state is performed by reading the CurrentSense.

5.5 Open-load OFF-state detection

If the output voltage V_{OUT} in OFF-state of the output is greater than the open-load detection threshold voltage V_{OL} , an open-load OFF-state / Stuck to V_{CC} event is detected. The corresponding bit in the Open-load OFF-state / Stuck to V_{CC} status register STKFLTR (address 0x31h) is set. Consequently, the OLOFF bit (bit 1) in the Global Status Register and the Global Status Bit Not are set. To avoid false detection, the diagnosis starts after turn-off of a channel with an additional delay t_{DOLOFF} .

To distinguish between an open-load OFF-state event and a short to V_{CC} condition, an internal pull-up current generator can be enabled for each channel by setting the corresponding bit in the open-load OFF-state control register (OLOFFCR, address 0x02h).

The activated pull-up current generators are active in Normal Mode, in Fail Safe Mode and in Standby Mode. In Sleep Mode 2, the current generators are switched off. The register contents, however, are saved also in Sleep Mode 2, consequently the current generators are reactivated after a return to Standby or a wakeup to Fail Safe Mode. A hardware reset ($V_{DD} < V_{DD_POR_OFF}$) or a software reset (Command byte = FFh) clears all register contents and hence the current generators are switched off.

Figure 18. Open-load OFF-state detection

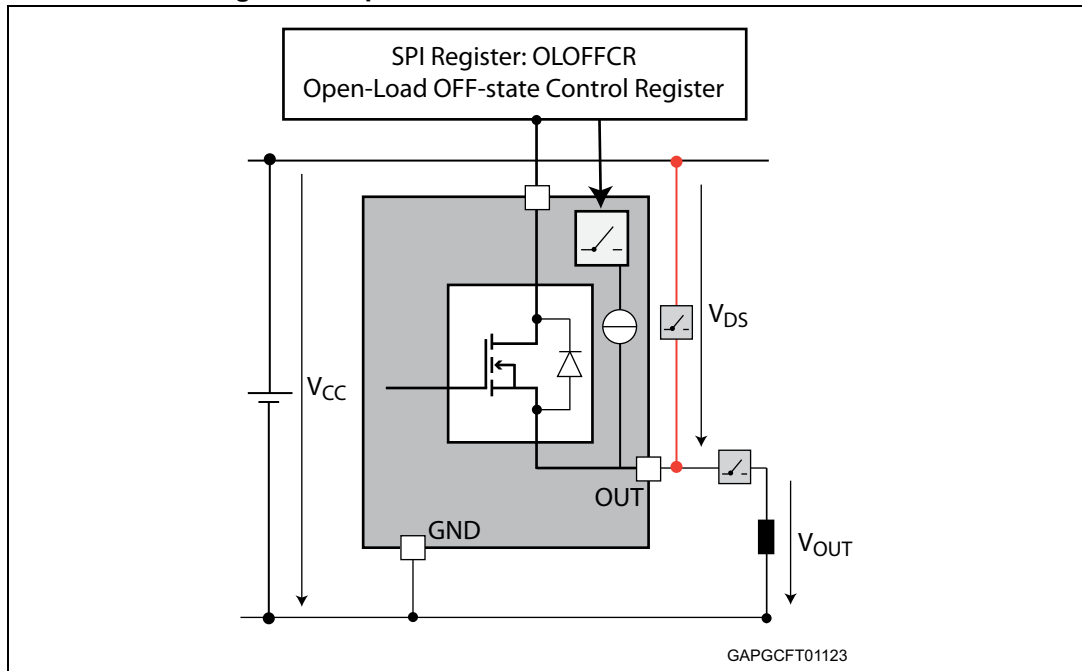


Table 43. STKFLTR state

| | With internal pull-up generator | Without internal pull-up generator |
|-------------------------------|---------------------------------|------------------------------------|
| Case 1: load connected | "0" / no fault | "0" / no fault |
| Case 2: no load | "1" / fault | "0" / no fault |
| Case 3: output shorted to Vcc | "1" / fault | "1" / fault |

5.6 Address 0x2Fh — DIENSR: Direct Input Status register

Table 44. DIENSR — Direct Input Status register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|--|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | DIENSTR3 | R | 0 | The DIENSTRx registers read back the status of the Direct Inputs. 1: The corresponding input is HIGH 0: The corresponding input is LOW DIENSTR0 is the direct input status of the channel 0 |
| 2 | DIENSTR2 | R | 0 | |
| 1 | DIENSTR1 | R | 0 | |
| 0 | DIENSTR0 | R | 0 | |

5.7 Address 0x30h — Channel Feedback Status Register (CHFBSR)

Table 45. CHFBSR — Channel Feedback Status Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | CHFBSR3 | R/C | 0 | The CHFBSRx provides a logical "OR" combination of VDS, PL, OT failure flags related to OUTPUTx. |
| 2 | CHFBSR2 | R/C | 0 | The contributions of VDS failure flags are maskable through CONFIG register settings. |
| 1 | CHFBSR1 | R/C | 0 | |
| 0 | CHFBSR0 | R/C | 0 | CHFBSRx = 1: Channel OUTPUTx on failure CHFBSRx = 0: Channel OUTPUTx no failure The bits are refreshed continuously in ON-state and latched in OFF-state. The bits are not set in case of latch-off configuration and if contribution of VDS failure flags is masked. In order to clear the bit in OFF-state, it is necessary to send a Read-Clear command |

5.8 Address 0x31h — Open-load OFF-State / Stuck to VCC Status Register (OLOFFCR)

Table 46. STKFLTR — Open-load OFF-State / Stuck to VCC Status Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | OLOFFSR3 | R/C | 0 | The OLOFFCR bit is set in OFF-state after turn-off delay, the t_{DOFF} is elapsed if $V_{OUT} > V_{OL}$. It gives an information about open load or a stuck to Vcc which depends on the configuration of the OLOFFCR register (for details refer to the functional description). The bit is continuously refreshed in OFF-state and it is latched during ON-state. In order to clear the bit in ON-state it is necessary to send a Read and Clear command. |
| 2 | OLOFFSR2 | R/C | 0 | |
| 1 | OLOFFSR1 | R/C | 0 | |
| 0 | OLOFFSR0 | R/C | 0 | 1: Open-load in OFF-state or stuck to Vcc condition occurred for OUTPUTX 0: No fault detected |

5.9 Address 0x32h — Channels latch-off status register (CHLOFFSR)

Table 47. CHLOFFSR — Channels latch-off status register

| Bit | Name | Access | Reset | Content |
|-----|-----------|--------|-------|--|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | CHLOFFSR3 | R | 0 | Latch OFF flag register. One bit per channel. – In case of latch-OFF of a channel because of power-limitation or overtemperature, this flag is set and readable by MCU – In latch-off state the fault has to be cleared through a Write operation of dedicated CHLOFFTCRx register to re-enable the output channel after an overtemperature or power limitation event. A SW reset event clears the content of the register |
| 2 | CHLOFFSR2 | R | 0 | |
| 1 | CHLOFFSR1 | R | 0 | |
| 0 | CHLOFFSR0 | R | 0 | |

5.10 Address 0x33h — VDS Feedback Status Register (VDSFSR)

Table 48. VDSFSR — VDS Feedback Status Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | |
| 5 | Reserved | — | 0 | |
| 4 | Reserved | — | 0 | |
| 3 | VDSFSR3 | R/C | 0 | VDS Feedback status. One bit per channel. – The VDSFSRx bit is set if, at the instant when the channel is commanded off or is latched-off, the $V_{CC} - V_{OUT}$ voltage drop exceeds V_{DS_OVL} threshold. The bit is latched until the next turn OFF. In order to clear the bit it is necessary to send a read and clear command. The VDSFSRx bit is set to: 1: High VDS detected on OUTPUTx 0: no fault detected Note: As the status register is not updated while CSN is low, it is possible that the update of the VDSFSR is delayed until the next time it is commanded off, if the PowerMOS is turned off during an SPI- frame. |
| 2 | VDSFSR2 | R/C | 0 | |
| 1 | VDSFSR1 | R/C | 0 | |
| 0 | VDSFSR0 | R/C | 0 | |

5.11 Address 0x34h — Generic Status Register (GENSR)

Table 49. GENSR — Generic Status Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | VCCUV | R | 0 | VCC undervoltage detection, Active High: this bit is related to the VCC undervoltage detection and is real time, means that it is set when $V_{CC} < V_{USD}$ and it is automatically reset as soon as $V_{CC} > V_{USD} + V_{USDHYST}$. This bit sets the Global Error Flag of the GSB. |
| 6 | RST | R/C | 0 | Active High: this bit is high in case of chip reset (hardware reset due to a loss of VREG supply or software reset). This bit is set until a Read and Clear Command is performed. |
| 5 | SPIE | R/C | 0 | Active High: this bit is set at end of Communication in case of wrong number of clock cycles during a communication frame or invalid bus condition or SDI stuck at High or Low conditions. This bit is set until a Read and Clear is performed. |
| 4 | Reserved | — | 0 | |
| 3 | Reserved | — | 0 | |
| 2 | Reserved | — | 0 | |
| 1 | Reserved | — | 0 | |
| 0 | Reserved | — | 0 | |

5.12 Address 0x3Fh — Configuration Register (CONFIG)

Table 50. CONFIG — Configuration Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|---|
| 7 | Reserved | — | 0 | Reserved |
| 6 | Reserved | — | 0 | Reserved |
| 5 | Reserved | — | 0 | Reserved |
| 4 | VDSMASK3 | R/W | 0 | Masks the contribution of the VDS status bit in the channel feedback status register and Global Status Byte For channel 3 1: VDS bit is masked 0: VDS bit not masked |
| 3 | VDSMASK2 | R/W | 0 | Masks the contribution of the VDS status bit in the channel feedback status register and Global Status Byte For channel 2 1: VDS bit is masked 0: VDS bit not masked |
| 2 | VDSMASK1 | R/W | 0 | Masks the contribution of the VDS status bit in the channel feedback status register and Global Status Byte For channel 1 1: VDS bit is masked 0: VDS bit not masked |

Table 50. CONFIG — Configuration Register

| Bit | Name | Access | Reset | Content |
|-----|----------|--------|-------|--|
| 1 | VDSMASK0 | R/W | 0 | Masks the contribution of the VDS status bit in the channel feedback status register and Global Status Byte For channel 0 1: VDS bit is masked 0: VDS bit not masked |
| 0 | WDTB | R/W | 0 | Changing the polarity of the Watchdog Toggle Bit (WDTB) within Watchdog Timeout (WDTO linked to t_{WDTB} parameter, see Table 58: Dynamic characteristics - Mode 1) keeps the device in NORMAL operating mode |

Figure 19. Diagnostic flowchart based on GSB

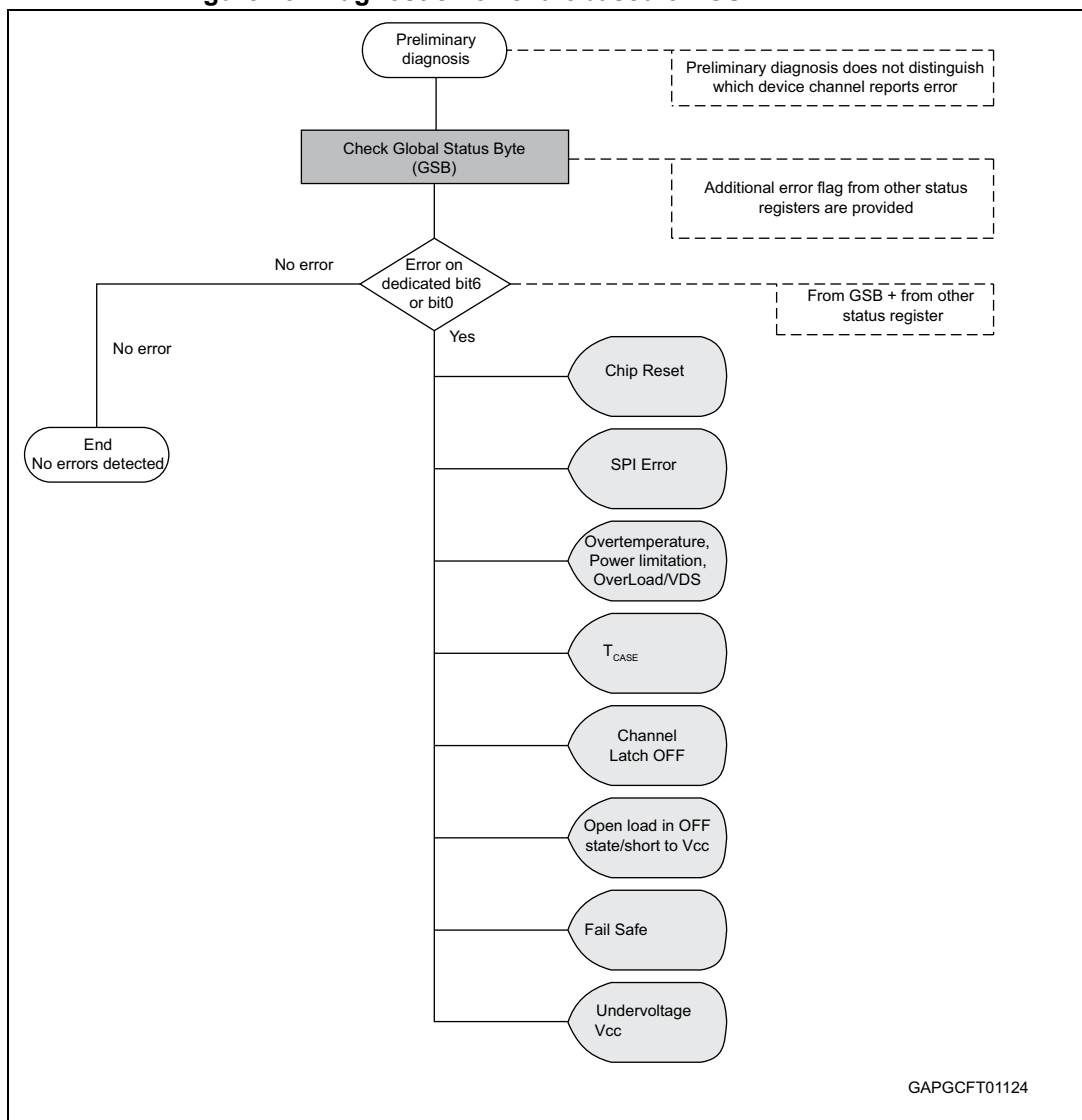


Figure 20. Diagnostic flowchart for open-load off-state respectively stuck to VCC failure

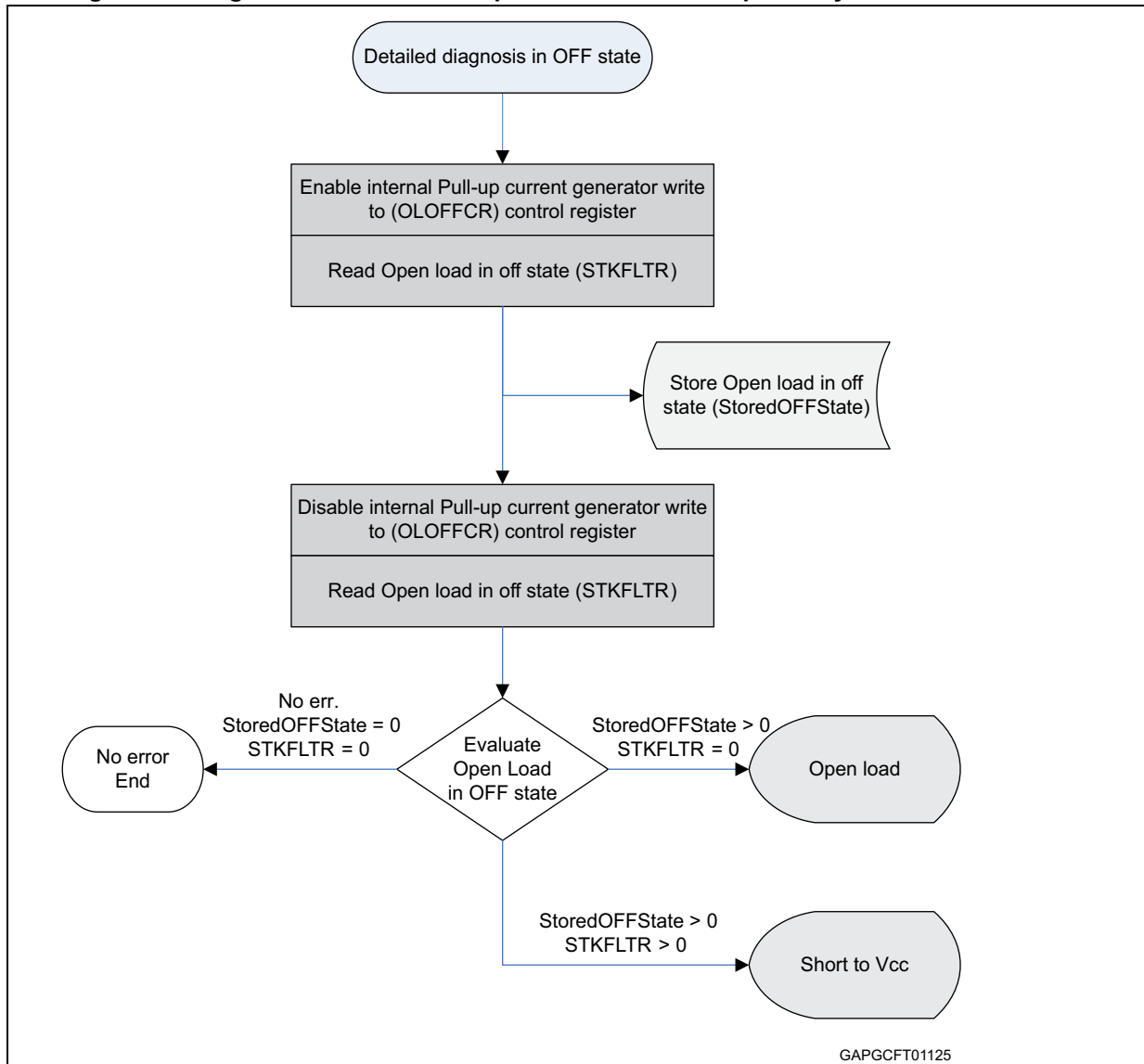
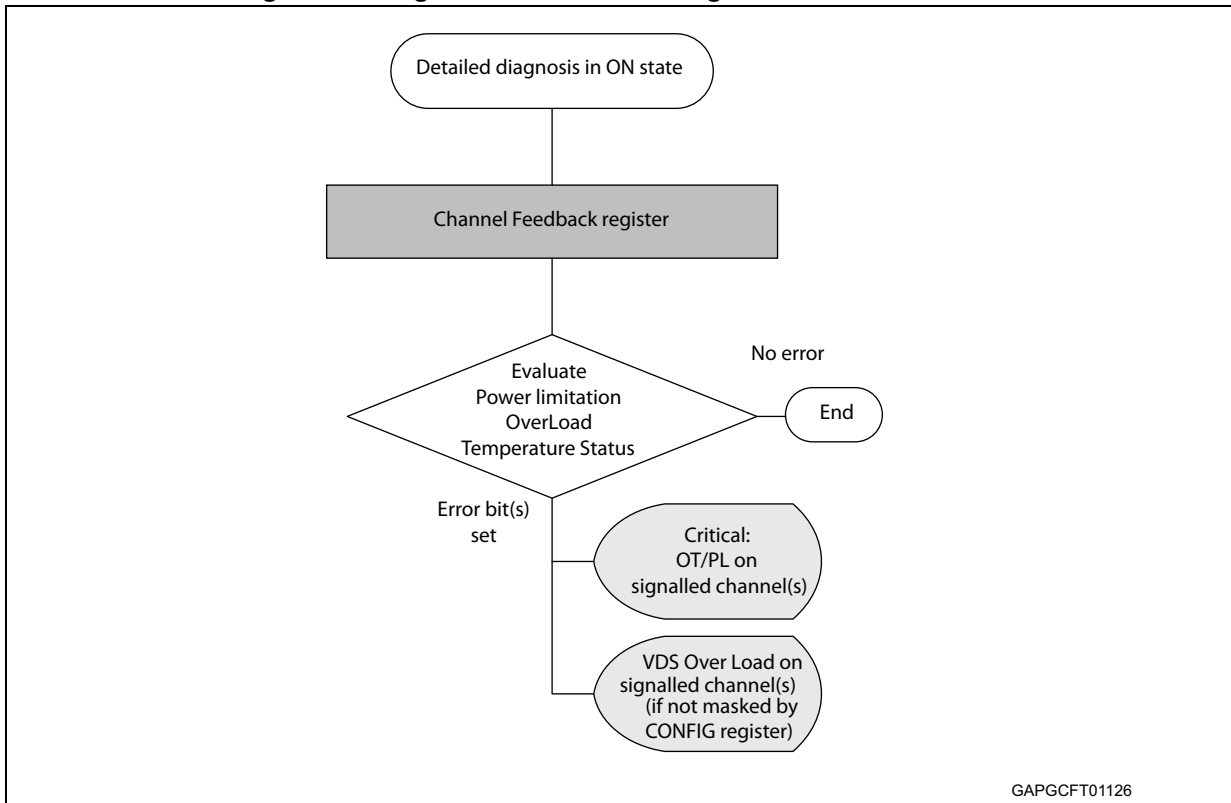


Figure 21. Diagnostic flowchart for digital overload detection



GAPGCF01126

6 Programmable blanking window

Dedicated registers for each channel (CHLOFFTCR0,1 and CHLOFFTCR2,3) provide a variable and programmable blanking window in case of power limitation or overtemperature event. During this period, the corresponding channel is in auto-restart mode and the channel is allowed to stay in power-limitation and/or overtemperature state before latching off, once blanking time is expired, if the cause of the power limitation or overtemperature event is still present. In this case the channel latches off and the related flag in the latch-off error register (CHLOFFSR) is set. Latch-off flag is also reported in the Global Status Byte (see [Section 4.3.1: Global Status byte description](#)).

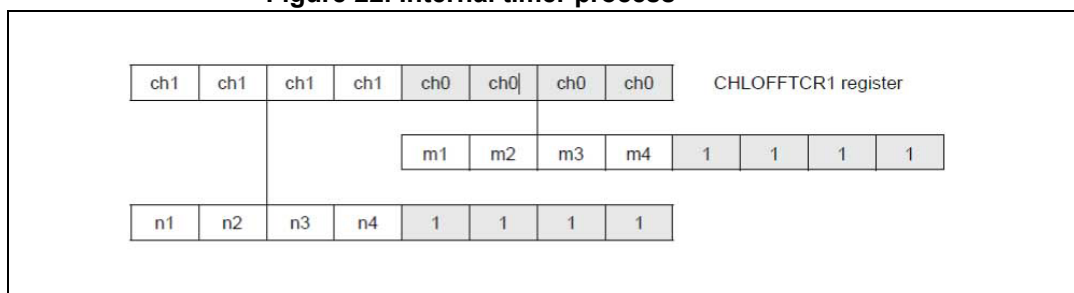
If during the blanking time the cause of power limitation and/or overtemperature event disappears, the timer stops then the rest of the blanking time will be available for another power limitation and/or overtemperature event. Therefore it is up to MCU to reset the timer by refreshing the programmed value in the dedicated register (CHLOFFTCR0,1 or CHLOFFTCR2,3).

MCU can keep the device in auto-restart forever artificially, by refreshing the programmed blanking time.

6.1 Timer

The 4 bit value per channel written in CHLOFFTCRx register is translated internally into an 8 bit value. The four MSB of this 8 bit value correspond to the content of CHLOFFTCRx register, while the four LSB are filled with 0xF. The 8 bit value refers to an analogue timer value.

Figure 22. Internal timer process



The granularity of the 8-bit counter is tSTEP. At each power limitation or overtemperature event, the 8-bit counter is decreased by the number of steps equal to the duration of power limitation or overtemperature event. If power limitation or overtemperature phase lasts for less than tSTEP the counter is decreased by one step.

After each downcount of the 8-bit register, the 4 MSB bits will be transferred to the 4 bits of corresponding CHLOFFTCRx register in order to refresh this register to the new value of the timer. The microcontroller can read only the 4 MSB bits content of the register. In consequence, the microcontroller can detect a change of every 16 steps of downcounting.

Downcounting is stopped and the content of the 8-bit counter is frozen, when the channel is commanded off through Direct Input or SOCR register or when the channel goes into Fail Safe mode.

6.2 Blanking window values

Typical values of the configurable blanking window are shown in [Table 51: Time values written by MCU and their real value in timer register](#).

Table 51. Time values written by MCU and their real value in timer register

| Bit 7 or bit 3 | Bit 6 or bit 2 | Bit 5 or bit 1 | Bit 4 or bit 0 | 0xm | 0xmF | Typical value of blanking time |
|----------------|----------------|----------------|----------------|-----|------|--------------------------------|
| 0 | 0 | 0 | 0 | 0x0 | 0xF | Latch-OFF (ZERO) |
| 0 | 0 | 0 | 1 | 0x1 | 0x1F | 17 ms |
| 0 | 0 | 1 | 0 | 0x2 | 0x2F | 34 ms |
| 0 | 0 | 1 | 1 | 0x3 | 0x3F | 51 ms |
| | | | | 0x4 | 0x4F | 68 ms |
| | | | | ... | ... | ... |
| 1 | 1 | 1 | 0 | 0xE | 0xEF | 238 ms |
| 1 | 1 | 1 | 1 | 0xF | 0xFF | 255 ms |

A peculiarity exists for the value 0x0. It configures the channel in Latch-OFF mode without blanking time. Consequently the channel will latch-off upon the first occurrence of power limitation or overtemperature event.

6.3 Limp Home mode

In Limp Home mode, the device is in unlimited auto-restart operation. The blanking time window has no effect on the duration of the auto-restart.

6.4 Registers

For more details refer to the SPI register and Diagnostics.

- Address 08h - Channel Latch OFF Timer Control Register (CHLOFFTCR0,1)
- Address 09h - Channel Latch OFF Timer Control Register (CHLOFFTCR2,3)

8 bit registers (Latch-OFF timer: R/W) are used for channel behavior configuration and the timer value setting. For each channel 4 bits are used.

The value is written by MCU from 0x0 to 0xF.

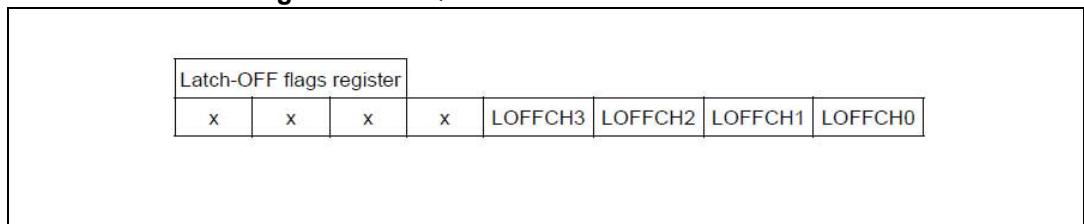
Latch-Off timer register access

- **Write command** – store new value, read-back (during write command) old value equal to the TIMER down-counting.
 - Any write command will clear the Flag in the Latch-OFF-Flag register and reset the timer.
 - This function will be used by MCU to clear the flag in the Latch-OFF-Flag register, which is READ only register.
- **Read command** – reads currently down-counted TIMER value. If channel was latched because of timer expired, channel is kept latched after read command.
- Address 32h - Channels latch-off status register – CHLOFFSR

Each channel has one flag. Unused channels or not existent one is reserved bit. In case of latch-OFF of a channel, this flag will be set and readable by MCU.

Example 2:

Figure 23. VNQ7004SY CHLOFFSR

**Latch-OFF Flag register access**

- **Write command** – not allowed (status register)
- **Read command** – reads current status of channels; this has no impact on latched / un-latched channels.
- **Clear command** – not allowed. To clear this register, a write operation in the corresponding bit of CHLOFFTCR is required.

7 Electrical specifications

7.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 52: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 52. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------------|---|-----------------------|------|
| V _{REG} | DC SPI supply stabilization | 3.6 | V |
| -V _{REG} | Reverse DC SPI supply stabilization | -0.3 | V |
| V _{CCJS} | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| V _{CC} | DC supply voltage | 38 | V |
| -V _{CC} | Reverse DC supply voltage (without external components) | -0.3 | V |
| I _{OUT0,1,2,3} | Maximum DC output current | Internally limited | A |
| -I _{OUT0,1} | Reverse DC output current | 9 | A |
| -I _{OUT2,3} | | 20 | A |
| I _{SENSE} | DC CurrentSense input current | +10/-1 | mA |
| E _{MAX0,1} | Maximum switching energy (single pulse) T _{DEMAG} = 0.1 ms; T _{jstart} = 150°C | 12.5 | mJ |
| E _{MAX2,3} | Maximum switching energy (single pulse) T _{DEMAG} = 0.1 ms; T _{jstart} = 150°C | 39.6 | mJ |
| V _{SDO} | DC SPI pin voltage | V _{DD} + 0.3 | V |
| -V _{SDO} | Reverse DC SPI pin voltage | -0.3 | V |
| I _{SDI,CSN,SCK} | DC SPI pin current | +10/-1 | mA |
| V _{DD} | DC Digital Control supply | 7 | V |
| -V _{DD} | Reverse DC Digital Control supply | -0.3 | V |
| I _{DIN0,1} | DC direct input current | +1/-1 | mA |
| I _{DIN2,3} | | +1/-1 | mA |
| ESD | Electrostatic discharge (ANSI-ESDA-JEDEC-JS-001-2014) | 2000 | V |
| | – IN0,1,2,3 | 2000 | |
| | – VDD | 2000 | |
| | – VREG | 2000 | |
| | – CSN, SDI, SCK | 2000 | |
| | – SDO | 2000 | |
| | – CurrentSense | 4000 | |
| | – OUT0,1,2,3 | 4000 | |

Table 52. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------|--------------------------------|------------|------|
| T _j | Junction operating temperature | -40 to 150 | °C |
| T _{STG} | Storage temperature | -55 to 150 | °C |
| I _{LAT} | Latch up current | ±20 | mA |

7.2 Thermal data

Table 53. Thermal data

| Symbol | Parameter | Typ. value | Unit |
|------------------------|---|-------------------------------|------|
| R _{thj-board} | Thermal resistance junction-board (JEDEC JESD 51-8) | 3.8 | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient | See Figure 31 | |

7.3 SPI electrical characteristics

Mode 1: 4.5 V < V_{DD} < 5.5 V, V_{DD} and V_{REG} independent; -40 °C < T_j < 150 °C, unless otherwise specified.

Mode 2: 2.7 V < V_{DD} < 3.3 V, V_{DD} and V_{REG} short circuited; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 54. DC characteristics - Mode 1

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------|--|---|--------------------|------|--------------------|------|
| V_{DD} pin | | | | | | |
| V _{DD_POR_ON} | Power-on reset threshold. Device leaves the Reset mode. Supply of digital part is reset. | V _{DD} increasing; V _{CC} > V _{USD} | | 2.3 | 2.8 | V |
| V _{DD_POR_OFF} | Power-on shutdown threshold. Device enters Reset mode. Supply of digital part in shutdown. | V _{DD} decreasing; V _{CC} > V _{USD} | 1.4 | 2.0 | | V |
| V _{POR_HYST} | Power-on reset hysteresis | | | 0.5 | | V |
| I _{DD} | Digital part supply current in normal mode (@ V _{DD} = 5 V) | V _{DD} = 5 V; SPI active without frame communication | | 0.6 | 1.0 | mA |
| I _{DDstd} | Digital part supply current in standby state (@ V _{DD} = 5 V) | V _{DD} = 5 V; T _j = 125 °C, I _{Nx} = 0 V | | 5 | 20 | µA |
| SDI, SCK pins | | | | | | |
| I _{IL} | Low level Input current | V _{SDI,SCK} = 0.3 V _{DD} | 1 | | | µA |
| I _{IH} | High level Input current | V _{SDI,SCK} = 0.7 V _{DD} | | | 10 | µA |
| V _{IL} | Input low voltage | | | | 0.3V _{DD} | V |
| V _{IH} | Input high voltage | | 0.7V _{DD} | | | V |

Table 54. DC characteristics - Mode 1 (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--------------------------|--|--------------------|------|--------------------|------|
| V _{I_HYST} | Input hysteresis voltage | | | 1.0 | | V |
| V _{SDI_CL} | SDI clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |
| V _{SCK_CL} | SCK clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |
| SDO pin | | | | | | |
| V _{OL} | Output low voltage | I _{SDO} = -5 mA; CSN low; fault condition; no SCK | | | 0.2V _{DD} | V |
| V _{OH} | Output high voltage | I _{SDO} = 5 mA; CSN low; no fault condition; no SCK | 0.8V _{DD} | | | V |
| I _{LO} | Output leakage current | V _{SDO} = 0 V or 5 V, CSN high; -40 °C < T _j < 85 °C | -5 | | 5 | µA |
| CSN pin | | | | | | |
| I _{IL_CSN} | Low level Input current | V _{CSN} = 0.3 V _{DD} | -10 | | | µA |
| I _{IH_CSN} | High level Input current | V _{CSN} = 0.7 V _{DD} | | | -1 | µA |
| V _{IL_CSN} | Output low voltage | | | | 0.3V _{DD} | V |
| V _{IH_CSN} | Output high voltage | | 0.7V _{DD} | | | V |
| V _{HYST_CSN} | Input hysteresis voltage | | | 1.0 | | V |
| V _{CL_CSN} | CSN clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |
| V _{SCK_CL} | SCK clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |

Table 55. DC characteristics - Mode 2

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------|--|--|------|------|------|------|
| V_{DD} pin | | | | | | |
| V _{DD_POR_ON} | Power-on reset threshold. Device leaves the Reset mode. Supply of digital part is reset. | V _{DD} increasing; V _{CC} > V _{USD} | | 2.3 | 2.8 | V |
| V _{DD_POR_OFF} | Power-on shutdown threshold. Device enters Reset mode. Supply of digital part in shutdown. | V _{DD} decreasing; V _{CC} > V _{USD} | 1.4 | 2.0 | | V |
| V _{POR_HYST} | Power-on reset hysteresis | | | 0.3 | | V |

Table 55. DC characteristics - Mode 2 (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--|---|--------------------|------|--------------------|------|
| I _{DD} | Digital part supply current in normal mode (@ V _{DD} = 3 V) | V _{DD} = 3 V; SPI active without frame communication | | 0.3 | 0.5 | mA |
| I _{DDstd} | Digital part supply current in standby state (@ V _{DD} = 3 V) | V _{DD} = 3 V; T _j = 125 °C, I _{Nx} = 0 V | | 2 | 10 | μA |
| SDI, SCK pins | | | | | | |
| I _{IL} | Low level Input current | V _{SDI,SCK} = 0.3 V _{DD} | 1 | | | μA |
| I _{IH} | High level Input current | V _{SDI,SCK} = 0.7 V _{DD} | | | 10 | μA |
| V _{IL} | Input low voltage | | | | 0.3V _{DD} | V |
| V _{IH} | Input high voltage | | 0.7V _{DD} | | | V |
| V _{L_HYST} | Input hysteresis voltage | | | 0.8 | | V |
| V _{SDI_CL} | SDI clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |
| V _{SCK_CL} | SCK clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |
| SDO pin | | | | | | |
| V _{OL} | Output low voltage | I _{SDO} = -5 mA; CSN low; fault condition; no SCK | | | 0.2V _{DD} | V |
| V _{OH} | Output high voltage | I _{SDO} = 5 mA; CSN low; no fault condition; no SCK | 0.8V _{DD} | | | V |
| I _{LO} | Output leakage current | V _{SDO} = 0 V or V _{DD} , CSN high; -40 °C < T _j < 85 °C | -5 | | 5 | μA |
| CSN pin | | | | | | |
| I _{IL_CSN} | Low level Input current | V _{CSN} = 0.3 V _{DD} | -10 | | | μA |
| I _{IH_CSN} | High level Input current | V _{CSN} = 0.7 V _{DD} | | | -1 | μA |
| V _{IL_CSN} | Output low voltage | | | | 0.3V _{DD} | V |
| V _{IH_CSN} | Output high voltage | | 0.7V _{DD} | | | V |
| V _{HYST_CSN} | Input hysteresis voltage | | | 0.8 | | V |
| V _{CL_CSN} | CSN clamping voltage | I _{IN} = 1 mA | 5.8 | | 7.3 | V |
| | | I _{IN} = -1 mA | | -0.6 | | V |

Table 56. AC characteristics (SDI, SCK, CSN, SDO pins) - Mode 1

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------|-------------------------------|------|------|------|------|
| C _{OUT} | Output capacitance (SDO) | V _{OUT} = 0 V to 5 V | — | — | 10 | pF |
| C _{IN} | Input capacitance (SDI) | V _{IN} = 0 V to 5 V | — | — | 10 | pF |
| | Input capacitance (other pins) | V _{IN} = 0 V to 5 V | — | — | 10 | pF |

Table 57. AC characteristics (SDI, SCK, CSN, SDO pins) - Mode 2

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------|-------------------------------|------|------|------|------|
| C _{OUT} | Output capacitance (SDO) | V _{OUT} = 0 V to 3 V | — | — | 10 | pF |
| C _{IN} | Input capacitance (SDI) | V _{IN} = 0 V to 3 V | — | — | 10 | pF |
| | Input capacitance (other pins) | V _{IN} = 0 V to 3 V | — | — | 10 | pF |

Table 58. Dynamic characteristics - Mode 1

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|---|-------------------------|------|------|------|------|
| f _c | Clock frequency | Duty cycle = 50% | | | 4 | MHz |
| t _{WHCH} | CSN timeout: time to release SDO bus | | 30 | | 70 | ms |
| t _{WDTB} | Watchdog toggle bit timeout | | 30 | | 70 | ms |
| t _{SLCH} | CSN low setup time | | 120 | | | ns |
| t _{SHCH} | CSN high setup time | | 1200 | | | ns |
| t _{DVCH} | Data in setup time | | 20 | | | ns |
| t _{CHDX} | Data in hold time | | 30 | | | ns |
| t _{CH} | Clock high time | | 115 | | | ns |
| t _{CL} | Clock low time | | 115 | | | ns |
| t _{CLQV} | Clock low to output valid | C _{OUT} = 1 nF | | 150 | | ns |
| t _{QLQH} | Output rise time | C _{OUT} = 1 nF | | 110 | | ns |
| t _{QHQL} | Output fall time | C _{OUT} = 1 nF | | 110 | | ns |
| t _{WU} | Rising edge of V _{DD} to first allowed communication | | 3 | | 23 | μs |
| t _{stdby_out} | Minimum time during which CSN must be toggled low to go out of STDBY mode | | 30 | 80 | 150 | μs |
| t _{SCLK} | SCK setup time before CSN rising | | 150 | | | ns |
| t _{CSNQV} | CSN low to output valid | | | 50 | 100 | ns |
| t _{CSNQT} | CSN high to output tristate | | | 50 | 100 | ns |

Table 59. Dynamic characteristics - Mode 2

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------|---|-------------------------|------|------|------|------|
| f _c | Clock frequency | Duty cycle = 50% | | | 4 | MHz |
| t _{WHCH} | CSN timeout: time to release SDO bus | | 30 | | 70 | ms |
| t _{WDTB} | Watchdog toggle bit timeout | | 30 | | 70 | ms |
| t _{SLCH} | CSN low setup time | | 120 | | | ns |
| t _{SHCH} | CSN high setup time | | 1200 | | | ns |
| t _{DVCH} | Data in setup time | | 20 | | | ns |
| t _{CHDX} | Data in hold time | | 30 | | | ns |
| t _{CH} | Clock high time | | 115 | | | ns |
| t _{CL} | Clock low time | | 115 | | | ns |
| t _{CLQV} | Clock low to output valid | C _{OUT} = 1 nF | | 150 | | ns |
| t _{QLQH} | Output rise time | C _{OUT} = 1 nF | | 110 | | ns |
| t _{QHQL} | Output fall time | C _{OUT} = 1 nF | | 110 | | ns |
| t _{WU} | Rising edge of V _{DD} to first allowed communication | | 3 | | 23 | μs |
| t _{stdby_out} | Minimum time during which CSN must be toggled low to go out of STDBY mode | | 30 | 80 | 150 | μs |
| t _{SCLK} | SCK setup time before CSN rising | | 150 | | | ns |
| t _{CSNQV} | CSN low to output valid | | | 50 | 100 | ns |
| t _{CSNQT} | CSN high to output tristate | | | 50 | 100 | ns |

Figure 24. SPI dynamic characteristics

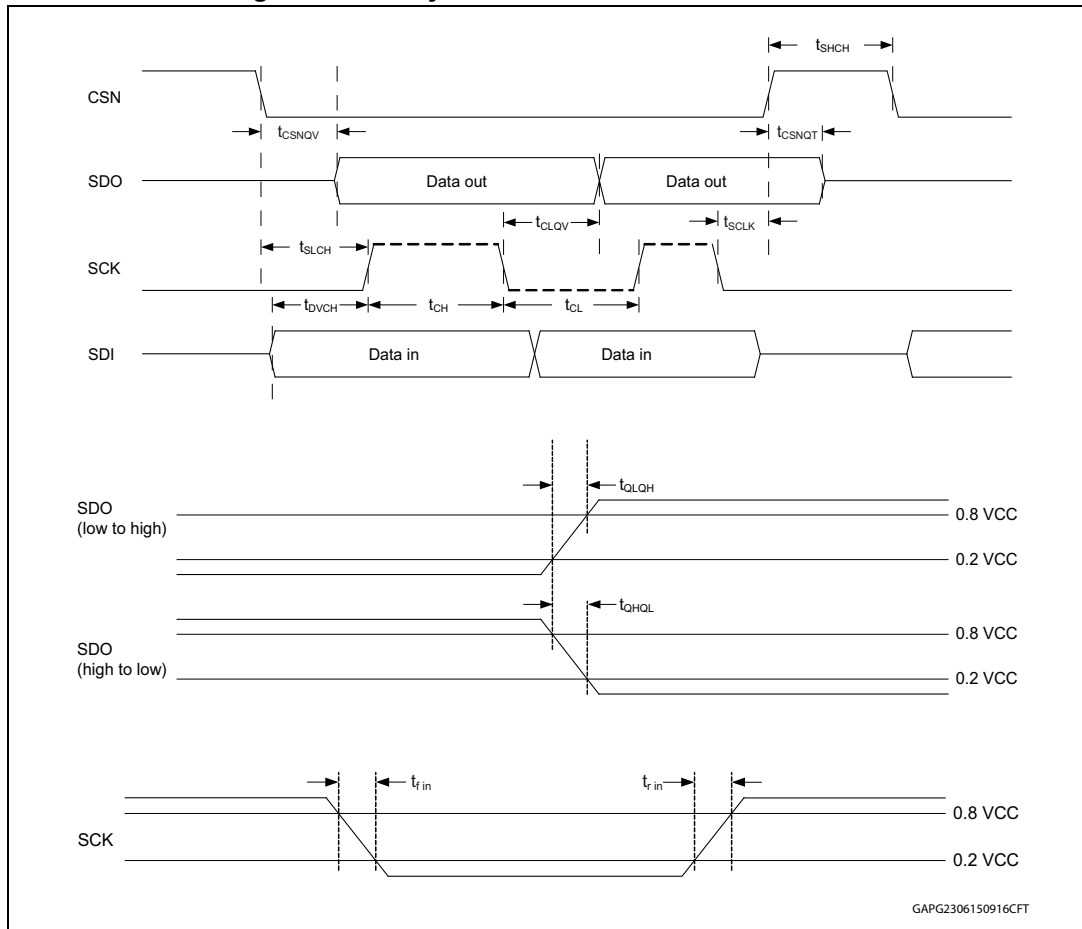


Table 60. VREG pin - Mode 1

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------------------|--|------|------|------|----------|
| V_{REG} | Supply voltage in normal mode | $V_{DD} = 5\text{ V}$; normal mode | 2.5 | 3 | 3.5 | V |
| | Supply voltage in standby mode | $V_{DD} = 5\text{ V}$; standby mode | 2.5 | 3 | 3.5 | V |
| Z_{REG} | Output impedance | $V_{DD} = 5\text{ V}$; $I_{REG} = 5\text{ mA}$ | | 50 | | Ω |
| I_{REG_Max} | Maximum output current | $V_{REG} = 90\% * V_{REG(typ)}$; $V_{DD} = 5\text{ V}$ | | 7 | | mA |

7.4 Electrical characteristics

7 V < V_{CC} < 28 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 61. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|--|--|------|------|------|------|
| V _{CC} | Operating supply voltage | | 4 | 13 | 28 | V |
| V _{USD} | Undervoltage shutdown | | | 3 | 4 | V |
| V _{USDhyst} | Undervoltage shutdown hysteresis | | | 0.25 | | V |
| V _{clamp} | V _{CC} clamp voltage | I _{CC} = 20 mA; I _{OUT0,1,2,3} = 0 A | 38 | 46 | 52 | V |
| I _{stby} | Supply current in sleep mode at V _{CC} = 13 V; T _j = 25 °C | Sleep mode1; V _{CC} = 13 V; T _j = 25 °C; V _{DD} = 0 V | | 0.1 | 2 | μA |
| | | Sleep mode2; V _{CC} = 13 V; T _j = 25 °C; V _{DD} = 5 V | | 5 | 10 | μA |
| I _{s(on)} | Supply current in ON-state | ON-state (all channels ON); V _{CC} = 13 V; V _{DD} = 5 V; I _{OUT} = 0 A | | 8.5 | 14 | mA |
| I _{L(off)} | OFF state output current at V _{CC} = 13 V, T _j = 25 °C | V _{DD} = 0 V; V _{CC} = 13 V; T _j = 25 °C; V _{in} = V _{out} = 0 V | 0 | 0.1 | 0.5 | μA |
| | OFF-state output current at V _{CC} = 13 V, T _j = 125 °C | V _{DD} = 0 V; V _{CC} = 13 V; T _j = 125 °C; V _{in} = V _{out} = 0 V | 0 | | 3 | μA |
| V _{F0,1} | Output V _{CC} diode voltage at T _j = 150 °C | V _{CC} = 13 V; I _{OUT} = 3 A; T _j = 150 °C | | | 0.7 | V |
| V _{F2,3} | | V _{CC} = 13 V; I _{OUT} = 6 A; T _j = 150 °C | | | 0.7 | V |

Table 62. Logic inputs (IN0,1,2,3 pins)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|--------------------------|-------------------------|------|------|------|------|
| V _{IL0,1,2,3} | Input low level voltage | | | | 0.9 | V |
| I _{IL0,1,2,3} | Low level input current | V _{IN} = 0.9 V | 1 | | | μA |
| V _{IH0,1,2,3} | Input high level voltage | | 2.1 | | | V |
| I _{IH0,1,2,3} | High level input current | V _{IN} = 2.1 V | | | 10 | μA |
| V _{I(hyst)0,1,2,3} | Input hysteresis voltage | | 0.2 | | | V |
| V _{ICL2,3} | Input clamp voltage | I _{IN} = 1 mA | 5.5 | | 7.5 | V |
| | | I _{IN} = -1 mA | | -0.7 | | V |
| V _{ICL0,1} | Input clamp voltage | I _{IN} = 1 mA | 5.5 | | 8.2 | V |
| | | I _{IN} = -1 mA | | -0.7 | | V |

Table 63. Protection

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|-------------------------|-------------------------|-------------------------|------|
| DT _{PLIM} ⁽¹⁾ | Junction-case temperature difference triggering power limitation protection | V _{CC} = 13 V | | 60 | | °C |
| DT _{PLIMR} | Junction-case temperature difference resetting power limitation protection | V _{CC} = 13 V | | 35 | | °C |
| T _{TSD} | Shutdown temperature | V _{CC} = 13 V | 150 | 175 | 200 | °C |
| T _R | Reset temperature | V _{CC} = 13 V, latched off mode disabled | T _{RS} + 1 | T _{RS} + 5 | | °C |
| T _{RS} | Thermal reset of CHFBSR fault detection | V _{CC} = 13 V, latched off mode disabled | 135 | | | °C |
| T _{HYST} | Thermal hysteresis (T _{TSD} - T _R) | V _{CC} = 13 V, latched off mode disabled | | 10 | | °C |
| T _{CSD} ⁽²⁾ | Case thermal detection pre-warning | V _{CC} = 13 V (see Table 31: CTLR — Control Register) | T _{CSD} nom-15 | T _{CSD} nom | T _{CSD} nom+15 | °C |
| T _{CR} ⁽²⁾ | Case thermal detection reset | V _{CC} = 13 V | | T _{CSD} nom-15 | | °C |
| V _{DS_OVL} | V _{DS} overload detection threshold | | V _{CC} - 1.5 | V _{CC} - 1.0 | V _{CC} - 0.5 | V |
| t _{Blanking} | Programmable blanking time | | -20 | | 20 | % |
| t _{ON_MIN} | Minimum turn-on time per channel to avoid false V _{DS} error flag at V _{CC} = 13 V | Bulb mode, ch0 and ch1 | | | 220 | µs |
| | | LED mode, ch0 and ch1 | | | 150 | µs |
| | | Bulb mode, ch2 and ch3 | | | 220 | µs |

1. $Z_{thj-case} \times P = \Delta T_{PLIM}$, $Z_{th-case}$ is the thermal impedance, P is the Power.
2. Guarantee by Design and Characterization.

Table 64. Open-load detection (7V < V_{CC} < 18 V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------|--|--|-----------------------|-----------------------|-----------------------|------|
| V _{OL} | Open-load OFF-state voltage detection threshold | CHx off | V _{CC} - 1.5 | V _{CC} - 1.0 | V _{CC} - 0.5 | V |
| I _{PU} | Pull-up current generator for open-load at OFF-state detection | Pull-up current generator active, V _{out} = V _{CC} - 1.0 V | -1.4 | -0.75 | -0.4 | mA |
| t _{DOLOFF} | Delay time after turn off to allow open-load OFF-state detection | | 0.25 | 0.75 | 1.25 | ms |

7.4.1 BULB mode

Table 65. BULB - power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|---------------------|---|------|------|------|------|
| RON_ch0,1 | ON-state resistance | I _{OUT} = 3 A; T _j = 25 °C | — | 35 | | mΩ |
| | | I _{OUT} = 3 A; T _j = 150 °C | — | | 70 | mΩ |
| | | I _{OUT} = 3 A; V _{CC} = 4 V; T _j = 25 °C | — | | 52.5 | mΩ |
| RON_ch2,3 | ON-state resistance | I _{OUT} = 6 A; T _j = 25 °C | — | 9 | | mΩ |
| | | I _{OUT} = 6 A; T _j = 150 °C | — | | 18 | mΩ |
| | | I _{OUT} = 6 A; V _{CC} = 4 V; T _j = 25 °C | — | | 13.5 | mΩ |

Table 66. BULB - switching (V_{CC} = 13 V; Normal switch mode)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|--|------|------|------------------|------|
| t _{don} ⁽¹⁾ | Turn-on delay time Ch _{0,1} | From 50% CSN to 20% V _{OUT} , R _L = 4.3 Ω | 25 | 70 | 115 | μs |
| | Turn-on delay time Ch _{2,3} | From 50% CSN to 20% V _{OUT} , R _L = 2.2 Ω | 50 | 100 | 150 | μs |
| t _{doff} ⁽¹⁾ | Turn-off delay time Ch _{0,1} | From 50% CSN to 80% V _{OUT} , R _L = 4.3 Ω | 30 | 45 | 60 | μs |
| | Turn-off delay time Ch _{2,3} | From 50% CSN to 80% V _{OUT} , R _L = 2.2 Ω | 40 | 60 | 80 | μs |
| t _{skew} ⁽¹⁾ | Turn-off turn-on time Ch _{0,1} | From 50% CSN to 50% V _{OUT} , R _L = 4.3 Ω | -60 | | 40 | μs |
| | Turn-off turn-on time Ch _{2,3} | From 50% CSN to 50% V _{OUT} , R _L = 2.2 Ω | -85 | | 15 | μs |
| (dV _{OUT} /dt) _{on} ⁽¹⁾ | Turn-on voltage slope Ch _{0,1} | V _{OUT} = 2.6 V to 10.4 V; R _L = 4.3 Ω | 0.05 | 0.3 | 0.7 | V/μs |
| | Turn-on voltage slope Ch _{2,3} | V _{OUT} = 2.6 V to 10.4 V; R _L = 2.2 Ω; normal switch mode | 0.05 | 0.2 | 0.7 | V/μs |
| (dV _{OUT} /dt) _{off} ⁽¹⁾ | Turn-off voltage slope Ch _{0,1} | V _{OUT} = 10.4 V to 2.6 V; R _L = 4.3 Ω; normal switch mode | 0.05 | 0.3 | 0.7 | V/μs |
| | Turn-off voltage slope Ch _{2,3} | from V _{OUT} = 10.4 V to 2.6 V; R _L = 2.2 Ω; normal switch mode | 0.05 | 0.2 | 0.7 | V/μs |
| W _{ON} | Switching losses energy at turn-on Ch _{0,1} | R _L = 4.3 Ω | | 0.3 | 1 ⁽²⁾ | |
| | Switching losses energy at turn-on Ch _{2,3} | R _L = 2.2 Ω | | 0.9 | 2 ⁽²⁾ | |
| W _{OFF} | Switching losses energy at turn-off Ch _{0,1} | R _L = 4.3 Ω | | 0.3 | 1 ⁽²⁾ | |
| | Switching losses energy at turn-off Ch _{2,3} | R _L = 2.2 Ω | | 0.9 | 2 ⁽²⁾ | |

1. See [Figure 26: Switching characteristics](#).

2. Parameter guaranteed by design and characterization; not subject to production test.

Table 67. BULB - switching (VCC = 13 V; Fast switch mode)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|---|--|------|------|------------------|------|
| $t_{don}^{(1)}$ | Turn-on delay time Ch _{0,1} | From 50% CSN to 20% V _{OUT} , R _L = 4.3 Ω | 25 | 70 | 115 | μs |
| | Turn-on delay time Ch _{2,3} | From 50% CSN to 20% | 50 | 100 | 150 | μs |
| $t_{doff}^{(1)}$ | Turn-off delay time Ch _{0,1} | From 50% CSN to 80% V _{OUT} , R _L = 4.3 Ω | 20 | 30 | 40 | μs |
| | Turn-off delay time Ch _{2,3} | From 50% CSN to 80% | 30 | 45 | 60 | μs |
| $t_{skew}^{(1)}$ | Turn-off turn-on time Ch _{0,1} | From 50% CSN to 50% V _{OUT} , R _L = 4.3 Ω | -75 | | 25 | μs |
| | Turn-off turn-on time Ch _{2,3} | From 50% CSN to 50% | -110 | | -10 | μs |
| $(dV_{OUT}/dt)_{on}^{(1)}$ | Turn-on voltage slope Ch _{0,1} | V _{OUT} = 2.6 V to 10.4 V; R _L = 4.3 Ω | 0.05 | 0.4 | 0.9 | V/μs |
| | Turn-on voltage slope Ch _{2,3} | V _{OUT} = 2.6 V to 10.4 V; | 0.05 | 0.3 | 0.7 | V/μs |
| $(dV_{OUT}/dt)_{off}^{(1)}$ | Turn-off voltage slope Ch _{0,1} | V _{OUT} = 10.4 V to 2.6 V; R _L = 4.3 Ω | 0.05 | 0.4 | 0.9 | V/μs |
| | Turn-off voltage slope Ch _{2,3} | from V _{OUT} = 10.4 V to | 0.05 | 0.35 | 0.7 | V/μs |
| W _{ON} | Switching losses energy at turn-on Ch _{0,1} | R _L = 4.3 Ω | | 0.2 | 1 ⁽²⁾ | mJ |
| | Switching losses energy at turn-on Ch _{2,3} | R _L = 2.2 Ω | | 0.8 | 2 ⁽²⁾ | mJ |
| W _{OFF} | Switching losses energy at turn-off Ch _{0,1} | R _L = 4.3 Ω | | 0.2 | 1 ⁽²⁾ | mJ |
| | Switching losses energy at turn-off Ch _{2,3} | R _L = 2.2 Ω | | 0.6 | 2 ⁽²⁾ | mJ |

1. See [Figure 26: Switching characteristics](#).
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 68. BULB - protection and diagnostic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--|--|------|------|------|------|
| I _{limH_ch0,1} | Short circuit current at V _{CC} = 13 V | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN0,1} = 5 V | 25 | 35 | 50 | A |
| | Short circuit current at 5 V < V _{CC} < 18 V ⁽¹⁾ | V _{IN0,1} = 5 V | | | 50 | A |
| I _{limL_ch0,1} | Short circuit current during thermal cycling | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN0,1} = 5 V, T _R < T _j < T _{TSD} | | 11.5 | | A |

Table 68. BULB - protection and diagnostic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--|--|---------------------|---------------------|---------------------|------|
| I _{limH_ch2,3} | Short circuit current at V _{CC} = 13 V | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN2,3} = 5 V | 55 | 80 | 110 | A |
| | Short circuit current at 5 V < V _{CC} < 18 V ⁽¹⁾ | V _{IN2,3} = 5 V | | | 110 | A |
| I _{limL_ch2,3} | Short circuit current during thermal cycling | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN2,3} = 5 V, T _R < T _J < T _{TSD} | | 26.5 | | A |
| V _{DEMAG} | Turn-off output voltage clamp; 25 °C < T _j < 150 °C | I _{OUT} = 2 A; V _{IN0,1,2,3} = 0 V; L = 6 mH | V _{CC} -40 | V _{CC} -44 | V _{CC} -48 | V |

1. Parameter guaranteed by design and characterization; not subjected to production test.

Table 69. BULB - CurrentSense (7 V < V_{CC} < 18 V, channel 0,1; T_j = -40 °C to 150 °C)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------------|--|---|------|------|------|------|
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.4 A; V _{SENSE} = 0.5 V | -30% | 3700 | 30% | |
| dK ₁ /K ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 0.4 A; V _{SENSE} = 0.5 V | -20 | | 20 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 2 A; V _{SENSE} = 4 V | -15% | 3700 | 15% | |
| dK ₂ /K ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 2 A; V _{SENSE} = 4 V | -10 | | 10 | % |
| K ₃ | I _{OUT} /I _{SENSE} | I _{OUT} = 6 A; V _{SENSE} = 4 V | -10% | 3700 | 10% | |
| dK ₃ /K ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 6 A; V _{SENSE} = 4 V | -8 | | 8 | % |
| I _{SENSE0} | Analog sense current | CurrentSense disabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A All channels are OFF | 0 | | 1 | μA |
| | | Current Sense Enabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A; V _{INx} = 5 V; others Channels ON in Bulb Mode at their load nominal current e.g. Ch0: V _{IN0} = 5 V; V _{IN1,2,3} = 5 V; I _{OUT0} = 0 A; I _{OUT1} = 2 A; I _{OUT2,3} = 6 A | 0 | | 15 | μA |
| | | CurrentSense disabled; V _{INx} = 5 V -1 V < V _{SENSE} < 5 V ⁽²⁾ | -0.5 | | 0.5 | μA |
| t _{DSENSE1H} ⁽³⁾ | Delay response time from rising edge of CSN pin (turn-on of the channel) | Normal switch mode; V _{SENSE} < 4 V, R _{SENSE} = 2 kΩ; I _{SENSE} = 90% of I _{SENSEmax} (see Figure 25: CurrentSense delay characteristics) | | 150 | 400 | μs |

Table 69. BULB - CurrentSense (7 V < VCC < 18 V, channel 0,1; Tj = -40 °C to 150 °C) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|---|---|------|------|------|---------------|
| $t_{\text{DSENSE1L}}^{(3)}$ | Delay response time from rising edge of CSN pin (turn-off of the channel) | Normal switch mode; $V_{\text{SENSE}} < 4 \text{ V}$, $R_{\text{SENSE}} = 2 \text{ k}\Omega$; $I_{\text{SENSE}} = 10 \% \text{ of } I_{\text{SENSEmax}}$ (see Figure 25: CurrentSense delay characteristics) | | 50 | 250 | μs |
| $t_{\text{DSENSE2H}}^{(3)}$ | Delay response time from CurrentSense MUX enable | Bit3 of CSMUXCR register (MUXEN) from 0 to 1; $R_{\text{SENSE}} = 2 \text{ k}\Omega$; $R_{\text{L}} = 4.3 \Omega$ | | 20 | 40 | μs |
| $t_{\text{DSENSE2L}}^{(3)}$ | Delay response time from CurrentSense MUX disable | Bit3 of CSMUXCR register (MUXEN) from 1 to 0; $R_{\text{sense}} = 2 \text{ k}\Omega$; $R_{\text{L}} = 4.3 \Omega$ | | 5 | 20 | μs |
| $t_{\text{D}_{\text{XtoY}}}$ | CurrentSense transition delay from ChX to ChY | | | | 100 | μs |
| $V_{\text{SENSE_CL}}$ | CurrentSense clamp voltage | $I_{\text{SENSE}} = 1 \text{ mA}$ | 8 | 9 | 10 | V |
| | | $I_{\text{SENSE}} = -1 \text{ mA}$ | -10 | -9 | -8 | V |
| $V_{\text{SENSE_SAT}}$ | CurrentSense saturation voltage | $V_{\text{CC}} = 7 \text{ V}$; $R_{\text{SENSE}} = 2.7 \text{ k}\Omega$; $V_{\text{IN0,1}} = 5 \text{ V}$; $I_{\text{OUT0,1}} = 12 \text{ A}$; $T_{\text{j}} = -40^\circ\text{C}$ | 4.8 | | | V |
| $I_{\text{SENSE_SAT}}^{(2)}$ | CurrentSense saturation current | $V_{\text{CC}} = 7 \text{ V}$; $V_{\text{SENSE}} = 4 \text{ V}$; $V_{\text{IN0,1}} = 5 \text{ V}$; $T_{\text{j}} = 150^\circ\text{C}$ | 4 | | | mA |
| $I_{\text{OUT_SAT_B}}^{(2)}$ | Output saturation current in BULB mode | $V_{\text{CC}} = 7 \text{ V}$; $V_{\text{SENSE}} = 4 \text{ V}$; $V_{\text{IN0,1}} = 5 \text{ V}$; $T_{\text{j}} = 150^\circ\text{C}$ | 15 | | | A |

1. All values refer to $V_{\text{CC}} = 13 \text{ V}$; $T_{\text{j}} = 25^\circ\text{C}$, unless otherwise specified.
2. Parameter guaranteed by design and characterization; not subjected to production test.
3. Transition delays are measured up to $\pm 10\%$ of final conditions.

Table 70. BULB - CurrentSense (7 V < VCC < 18 V, channel 2,3; Tj = -40 °C to 150 °C)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|-----------------------------------|--|------|-------|------|------|
| K_1 | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 450 \text{ mA}$; $V_{\text{SENSE}} = 0.5 \text{ V}$ | -50% | 10100 | 50% | |
| $dK_1/K_1^{(1) (2)}$ | CurrentSense ratio drift | $I_{\text{OUT}} = 450 \text{ mA}$; $V_{\text{SENSE}} = 0.5 \text{ V}$ | -30 | | 30 | % |
| K_2 | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 6 \text{ A}$; $V_{\text{SENSE}} = 4 \text{ V}$ | -11% | 10100 | 11% | |
| $dK_2/K_2^{(1) (2)}$ | CurrentSense ratio drift | $I_{\text{OUT}} = 6 \text{ A}$; $V_{\text{SENSE}} = 4 \text{ V}$ | -9 | | 9 | % |
| K_3 | $I_{\text{OUT}}/I_{\text{SENSE}}$ | $I_{\text{OUT}} = 18 \text{ A}$; $V_{\text{SENSE}} = 4 \text{ V}$ | -10% | 10100 | 10% | |
| $dK_3/K_3^{(1) (2)}$ | CurrentSense ratio drift | $I_{\text{OUT}} = 18 \text{ A}$; $V_{\text{SENSE}} = 4 \text{ V}$ | -8 | | 8 | % |

Table 70. BULB - CurrentSense (7 V < VCC < 18 V, channel 2,3; Tj = -40 °C to 150 °C) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|---|---|------|------|------|------|
| ISENSE0 | Analog sense current | CurrentSense disabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A; All channels are OFF | 0 | | 1 | μA |
| | | Current Sense Enabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A; V _{INx} = 5 V; other channels ON in Bulb Mode at their load nominal current e.g. Ch2: V _{IN2} = 5 V; V _{IN0,1,3} = 5 V; I _{OUT2} = 0 A; I _{OUT0,1} = 2 A; I _{OUT3} = 6 A | 0 | | 15 | μA |
| | | CurrentSense disabled; V _{INx} = 5 V; -1 V < V _{SENSE} < 5 V ⁽²⁾ | -0.5 | | 0.5 | μA |
| t _{DSENSE1H} ⁽³⁾ | Delay response time from rising edge of CSN pin (turn-on of the channel) | Normal switch mode; V _{SENSE} < 4 V, R _{SENSE} = 2 kΩ; I _{SENSE} = 90 % of I _{SENSEmax} (see Figure 25: CurrentSense delay characteristics) | | 250 | 400 | μs |
| t _{DSENSE1L} ⁽³⁾ | Delay response time from rising edge of CSN pin (turn-off of the channel) | Normal switch mode; V _{SENSE} < 4 V, R _{SENSE} = 2 kΩ;; I _{SENSE} = 10 % of I _{SENSEmax} (see Figure 25: CurrentSense delay characteristics) | | 50 | 250 | μs |
| t _{DSENSE2} ⁽³⁾ | Delay response time from CurrentSense MUX enable | Bit3 of CSMUXCR register (MUXEN) from 0 to 1; R _{SENSE} = 2 kΩ; R _L = 2.2 Ω | | 20 | 100 | μs |
| t _{DSENSE2L} ⁽³⁾ | Delay response time from CurrentSense MUX disable | Bit3 of CSMUXCR register (MUXEN) from 1 to 0; R _{SENSE} = 2 kΩ; R _L = 2.2 Ω | | 5 | 20 | μs |
| t _{D_XtoY} | CurrentSense transition delay from ChX to ChY | | | | 100 | μs |
| V _{SENSE_CL} | CurrentSense clamp voltage | I _{SENSE} = 1 mA | 8 | 9 | 10 | V |
| | | I _{SENSE} = -1 mA | -10 | -9 | -8 | V |
| V _{SENSE_SAT} | CurrentSense saturation voltage | V _{CC} = 7 V; R _{SENSE} = 2.7 kΩ; V _{IN2,3} = 5 V; I _{OUT2,3} = 36 A; T _j = -40°C | 4.8 | | | V |
| I _{SENSE_SAT} ⁽²⁾ | CurrentSense saturation current | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN2,3} = 5 V; T _j = 150°C | 4 | | | mA |
| I _{OUT_SAT_BULB} ⁽²⁾ | Output saturation current in BULB mode | V _{CC} = 7 V; V _{SENSE} = 4 V; V _{IN2,3} = 5 V; T _j = 150°C | 42 | | | A |

1. All values refer to VCC = 13 V; Tj = 25°C, unless otherwise specified.
2. Parameter guaranteed by design and characterization; not subjected to production test.
3. Transition delays are measured up to ±10% of final conditions.

7.4.2 LED mode (Channel 0, 1)

7 V < V_{CC} < 18 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 71. LED - power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---------------------|---|------|------|-------|------|
| R _{ON} Ch0,1 | ON-state resistance | I _{OUT} = 1.3 A; T _j = 25 °C | — | 85 | | mΩ |
| | | I _{OUT} = 1.3 A; T _j = 150 °C | — | | 170 | mΩ |
| | | I _{OUT} = 1.3 A; V _{CC} = 4 V; T _j = 25 °C | — | | 127.5 | mΩ |

Table 72. LED - switching (V_{CC} = 13 V; Normal switch mode)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|-------------------------------------|---|------|------|------------------|------|
| t _{don} ⁽¹⁾ | Turn-on delay time | From 50% CSN to 20% V _{OUT} R _L = 13 Ω | 20 | 60 | 100 | μs |
| t _{doff} ⁽¹⁾ | Turn-off delay time | From 50% CSN to 80% V _{OUT} R _L = 13 Ω | 25 | 40 | 55 | μs |
| t _{skew} ⁽¹⁾ | Turn-off, turn-on time | From 50% CSN to 50% V _{OUT} , R _L = 13 Ω | -60 | | 40 | μs |
| (dV _{OUT} /dt) ⁽¹⁾ | Turn-on voltage slope | V _{OUT} = 2.6 V to 10.4 V R _L = 13 Ω | 0.05 | 0.2 | 0.7 | V/μs |
| (dV _{OUT} /dt) _{off} ⁽¹⁾ | Turn-off voltage slope | From V _{OUT} = 10.4 V to 2.6 V R _L = 13 Ω | 0.05 | 0.3 | 0.7 | V/μs |
| W _{ON} | Switching losses energy at turn-on | R _L = 13 Ω | | 0.1 | 1 ⁽²⁾ | mJ |
| W _{OFF} | Switching losses energy at turn-off | R _L = 13 Ω | | 0.1 | 1 ⁽²⁾ | mJ |

1. See [Figure 26: Switching characteristics](#).
2. Parameter guaranteed by design and characterization; not subjected to production test.

Table 73. LED - switching (V_{CC} = 13 V; Fast switch mode)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|-------------------------------------|--|------|------|------------------|------|
| t _{don} ⁽¹⁾ | Turn-on delay time | From 50% CSN to 20% V _{OUT} R _L = 13 Ω | 20 | 60 | 100 | μs |
| t _{doff} ⁽¹⁾ | Turn-off delay time | From 50% CSN to 80% V _{OUT} R _L = 13 Ω | 15 | 25 | 35 | μs |
| t _{skew} ⁽¹⁾ | Turn-off, turn-on time | From 50% CSN to 50% V _{OUT} R _L = 13 Ω | -70 | | 30 | μs |
| (dV _{OUT} /dt) _{on} ⁽¹⁾ | Turn-on voltage slope | V _{OUT} = 2.6 V to 10.4 V R _L = 13 Ω | 0.05 | 0.6 | 1 | V/μs |
| (dV _{OUT} /dt) _{off} ⁽¹⁾ | Turn-off voltage slope | From V _{OUT} = 10.4 V to 2.6 V R _L = 13 Ω | 0.05 | 0.6 | 1 | V/μs |
| W _{ON} | Switching losses energy at turn-on | R _L = 13 Ω | | 0.06 | 1 ⁽²⁾ | mJ |
| W _{OFF} | Switching losses energy at turn-off | R _L = 13 Ω | | 0.06 | 1 ⁽²⁾ | mJ |

1. See [Figure 26: Switching characteristics](#).
2. Parameter guaranteed by design and characterization; not subjected to production test.

Table 74. LED - protection and diagnosis

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|-------------------------|---|---|------|------|-----|------|
| I _{limH_ch0,1} | Short circuit current at V _{CC} = 13 V | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN0,1} = 5 V | 7 | 12 | 18 | A |
| | Short circuit current at 5V < V _{CC} < 18 V ⁽¹⁾ | V _{IN0,1} = 5 V | | | 18 | A |
| I _{limL_ch0,1} | Short circuit current during thermal cycling | V _{CC} = 13 V, V _{DD} = 0 V, V _{IN0,1} = 5 V, T _R < T _J < T _{TSD} | | 4 | | A |

1. Parameter guaranteed by design and characterization; not subjected to production test.

Table 75. LED - CurrentSense (7 V < V_{CC} < 18 V; T_J = -40 °C to 150 °C)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|---|--|------|------|------|------|
| K ₀ | I _{OUT} /I _{SENSE} | I _{OUT} = 10 mA; V _{SENSE} = 0.5 V = 0.5V 0.5 V | -60% | 1400 | 60% | |
| dK ₀ /K ₀ ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 10 mA; V _{SENSE} = 0.5 V | -50 | | 50 | % |
| K ₁ | I _{OUT} /I _{SENSE} | I _{OUT} = 50 mA; V _{SENSE} = 0.5 V | -50% | 1400 | 50% | |
| dK ₁ /K ₁ ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 50 mA; V _{SENSE} = 0.5 V | -30 | | 30 | % |
| K ₂ | I _{OUT} /I _{SENSE} | I _{OUT} = 0.3 A V _{SENSE} = 4 V | -20% | 1400 | 20% | |
| dK ₂ /K ₂ ^{(1) (2)} | CurrentSense ratio drift | I _{OUT} = 0.3 A; V _{SENSE} = 4 V | -13 | | 13 | % |
| I _{SENSE0} | Analog sense current | Current Sense disabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A; All channels are OFF | 0 | | 1 | μA |
| | | Current Sense Enabled; V _{SENSE} = 0 V; I _{OUTx} = 0 A; V _{INx} = 5 V; other channels ON in Bulb Mode at their load nominal current e.g. Ch0: V _{IN0} = 5 V; V _{IN1,2,3} = 5 V; I _{OUT0} = 0 A; I _{OUT1} = 2 A; I _{OUT2,3} = 6 A | 0 | | 10 | μA |
| | | CurrentSense disabled; V _{INx} = 5 V ⁽²⁾ ; -1 V < V _{SENSE} < 5 V ⁽²⁾ | -0.5 | | 0.5 | μA |
| t _{DSSENSE1H} ⁽³⁾ | Delay response time from rising edge of CSN pin (turn-on of the channel) | V _{SENSE} < 4 V, R _{SENSE} = 2 kΩ; I _{SENSE} = 90 % of I _{SENSEmax} (see Figure 25: CurrentSense delay characteristics) | | 150 | 250 | μs |
| t _{DSSENSE1L} ⁽³⁾ | Delay response time from rising edge of CSN pin (turn-off of the channel) | V _{SENSE} < 4 V, R _{SENSE} = 2 kΩ; I _{SENSE} = 10 % of I _{SENSEmax} (see Figure 25: CurrentSense delay characteristics) | | 50 | 120 | μs |

Table 75. LED - CurrentSense (7 V < VCC < 18 V; Tj = -40 °C to 150 °C) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------|---|---|------|------|------|---------------|
| $t_{DSENSE2H}^{(3)}$ | Delay response time from CurrentSense MUX enable | Bit3 of CSMUXCR register (MUXEN) from 0 to 1; $R_{SENSE} = 2\text{ k}\Omega$; $R_L = 13\ \Omega$ | | 20 | 100 | μs |
| $t_{DSENSE2L}^{(3)}$ | Delay response time from CurrentSense MUX disable | Bit3 of CSMUXCR register (MUXEN) from 1 to 0; $R_{SENSE} = 2\text{ k}\Omega$; $R_L = 13\ \Omega$ | | 5 | 20 | μs |
| t_{d_XtoY} | CurrentSense transition delay from ChX to ChY | | | | 100 | μs |
| V_{SENSE_CL} | CurrentSense clamp voltage | $I_{SENSE} = 1\text{ mA}$ | 8 | 9 | 10 | V |
| | | $I_{SENSE} = -1\text{ mA}$ | -10 | -9 | -8 | V |
| V_{SENSE_SAT} | CurrentSense saturation voltage | $V_{CC} = 7\text{ V}$; $R_{SENSE} = 2.7\text{ k}\Omega$; $V_{IN0,1} = 5\text{ V}$; $I_{OUT0,1} = 4\text{ A}$; $T_j = -40^\circ\text{C}$ | 4.8 | | | V |
| $I_{SENSE_SAT}^{(2)}$ | CurrentSense saturation current | $V_{CC} = 7\text{ V}$; $V_{SENSE} = 4\text{ V}$; $V_{IN0,1} = 5\text{ V}$; $T_j = 150^\circ\text{C}$ | 4 | | | mA |
| $I_{OUT_SAT_LED}^{(2)}$ | Output saturation current in LED mode | $V_{CC} = 7\text{ V}$; $V_{SENSE} = 4\text{ V}$; $V_{IN0,1} = 5\text{ V}$; $T_j = 150^\circ\text{C}$ | 6 | | | A |

1. All values refer to $V_{CC} = 13\text{ V}$; $T_j = 25^\circ\text{C}$, unless otherwise specified.
2. Parameter guaranteed by design and characterization; not subjected to production test.
3. Transition delays are measured up to $\pm 10\%$ of final conditions.

Figure 25. CurrentSense delay characteristics

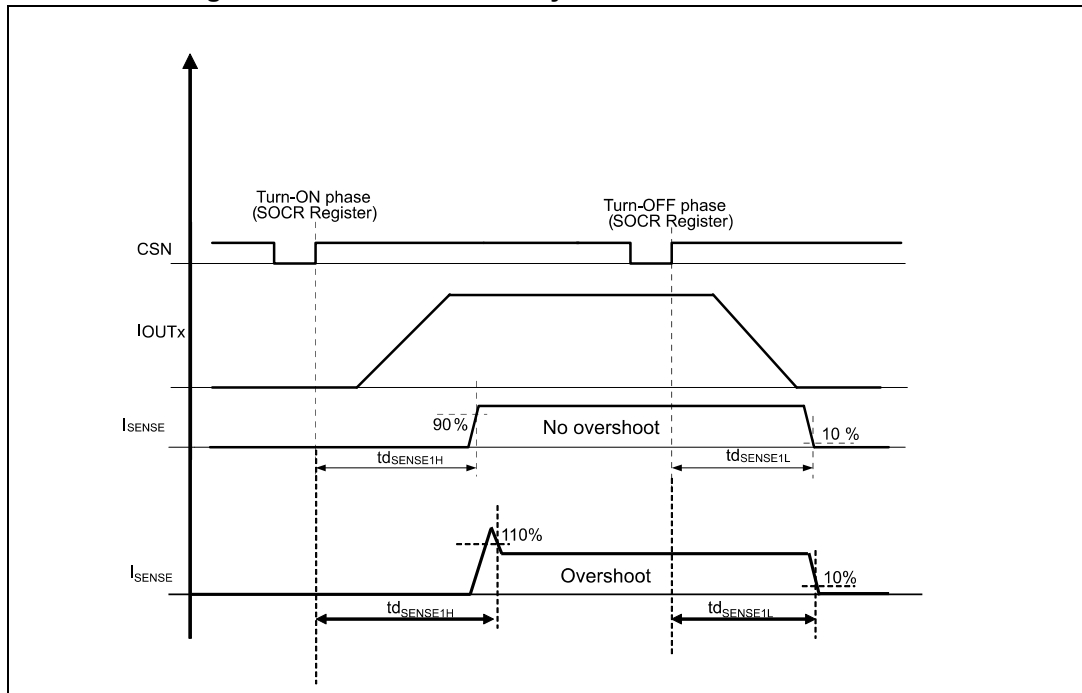
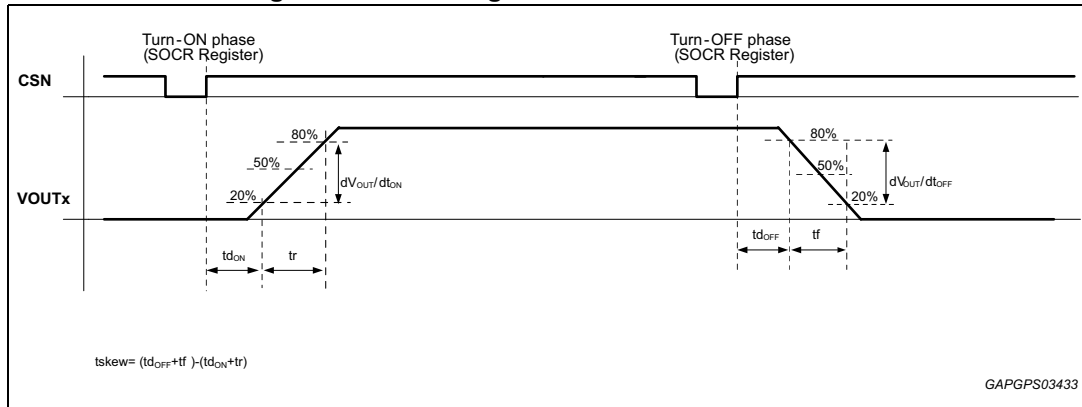


Figure 26. Switching characteristics



8 ISO Pulse

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011(E) and ISO 16750-2:2010.

The related function performances status classification is shown in the [Table 76: ISO 7637-2 - electrical transient conduction along supply line](#).

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, with external components as shown in [Figure 27: M0-7 SPI Standard connection SPI only](#) and [Figure 28: M0-7 SPI standard, full connection](#).

“Status II” is defined in ISO 7637-1 Function Performed Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 76. ISO 7637-2 - electrical transient conduction along supply line

| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal Impedance |
|--|--|-------------------|---------------------------------------|-------------------------------------|--------|---|
| | Level | US ⁽¹⁾ | | | | |
| 1 ⁽²⁾ | III | -112 V | 500 pulses | 0.5 s | 5 s | 2 ms, 10 Ω |
| 2a ⁽³⁾ | IV | +112 V | 500 pulses | 0.2 s | 5 s | 50 μs, 2 Ω |
| 3a ⁽²⁾ | IV | -220 V | 1 h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 3b | IV | +150 V | 1 h | 90 ms | 100 ms | 0.1 μs, 50 Ω |
| 4 ⁽⁴⁾ | IV | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| Load dump according to ISO 16750-2:2010 | | | | | | |
| Test B ⁽³⁾ | | 40 V | 5 pulse | 1 min | | 400 ms, 2 Ω |

1. Us is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), Chapter 5.6.
2. Device goes in reset state and must be reinitialized.
3. With 38V external suppressor referred to ground (-40 °C < T_j < 150 °C).
4. Test pulse in ISO 7637-2:2004(E).

9 Application schematics

Figure 27. M0-7 SPI Standard connection SPI only

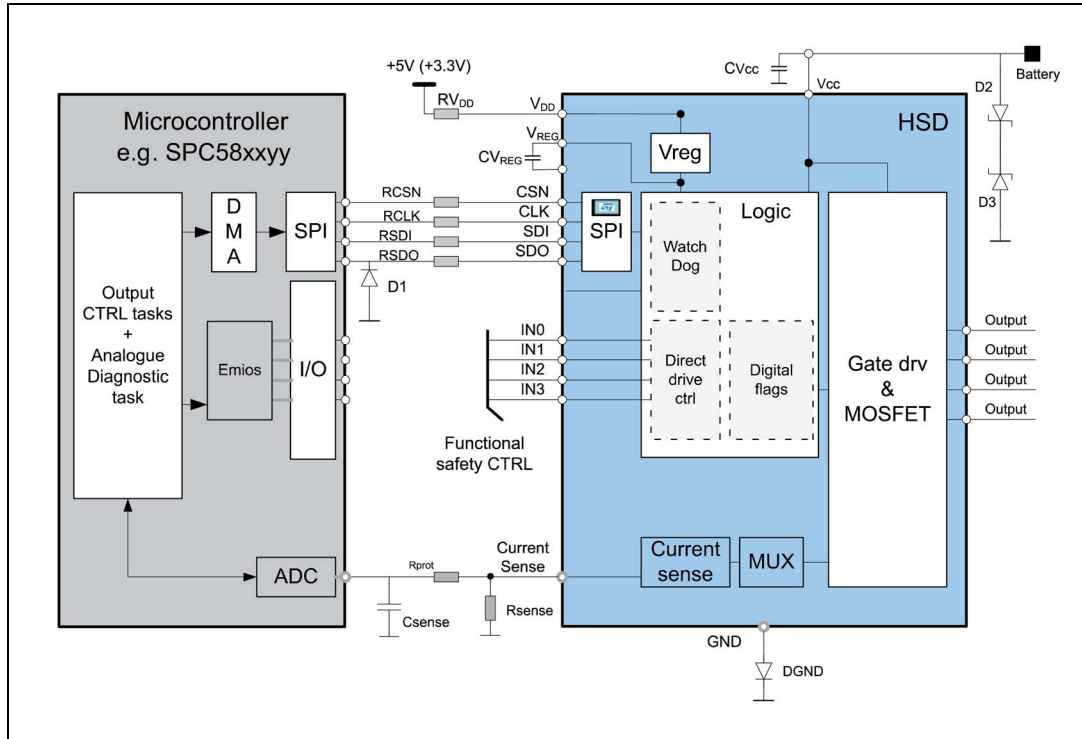


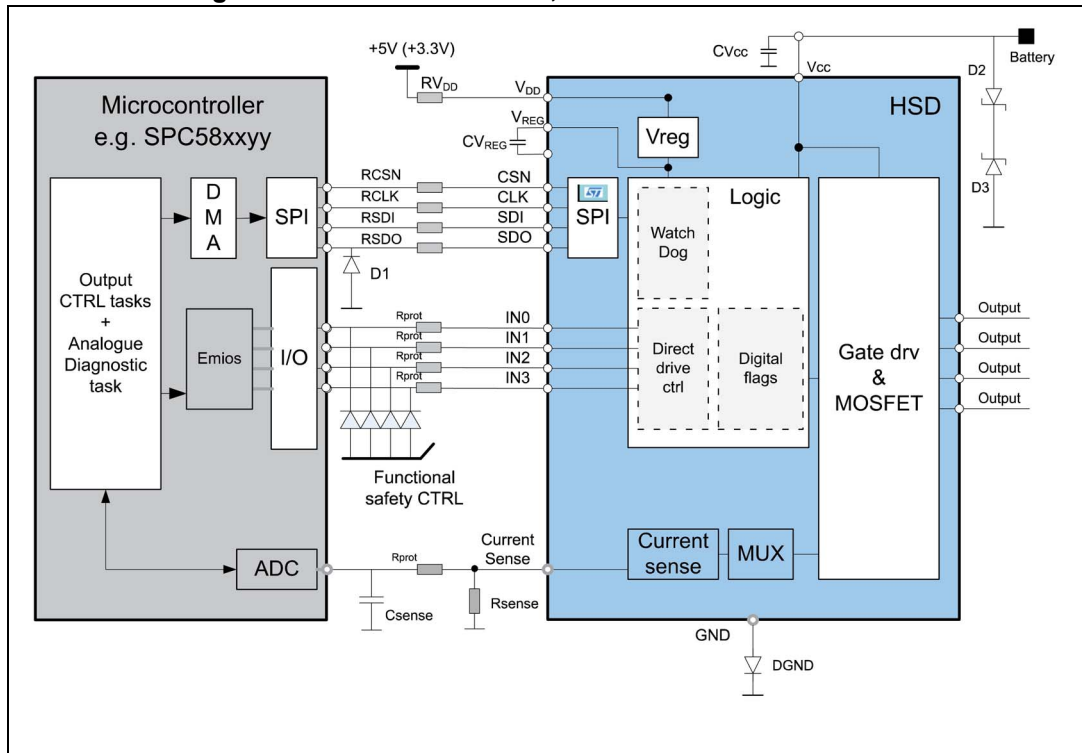
Table 77. Component values

| Reference | Value | comment |
|--------------------|-------------------------|--|
| RV _{DD} | 330 Ω | Device logic protection |
| CV _{REG} | 100 nF | Optional for EMI reduction- Low ESR, mount close to IC |
| CV _{CC} | 100 nF | Battery voltage spikes filtering mounted close to IC |
| RCSN | 2.7 kΩ | Microcontroller protection during overvoltage and reverse polarity |
| RCLK | 2.7 kΩ | Microcontroller protection during overvoltage and reverse polarity |
| RSDI | 2.7 kΩ | Microcontroller protection during overvoltage and reverse polarity |
| RSDO | 220 Ω | Microcontroller protection during overvoltage and reverse polarity |
| D1 | Schottky (i.e. BAT54-Y) | Microcontroller protection during overvoltage and reverse polarity |
| R _{PROT} | 15K Ω | Microcontroller protection during: overvoltage, reverse polarity and loss of GND |
| R _{SENSE} | 1K Ω | Sensing resistor |

Table 77. Component values (continued)

| Reference | Value | comment |
|-----------|--|--|
| Csense | 470 pF | Microcontroller ADC spikes filter |
| D2 | Suppressor 20 V | Negative transient protection. |
| D3 | Suppressor 36 V | Overvoltage protection. |
| DGND | BAS21 for $V_{DD} = 5V$ Schottky (i.e., BAT54-Y) for $V_{DD} = 3.3V$ | Reverse polarity protection. Usage of schottky or standard diode dependent on V_{DD} |

Figure 28. M0-7 SPI standard, full connection



10 Package and PCB thermal data

10.1 PowerSSO-36 thermal data

Figure 29. PowerSSO-36 PC board

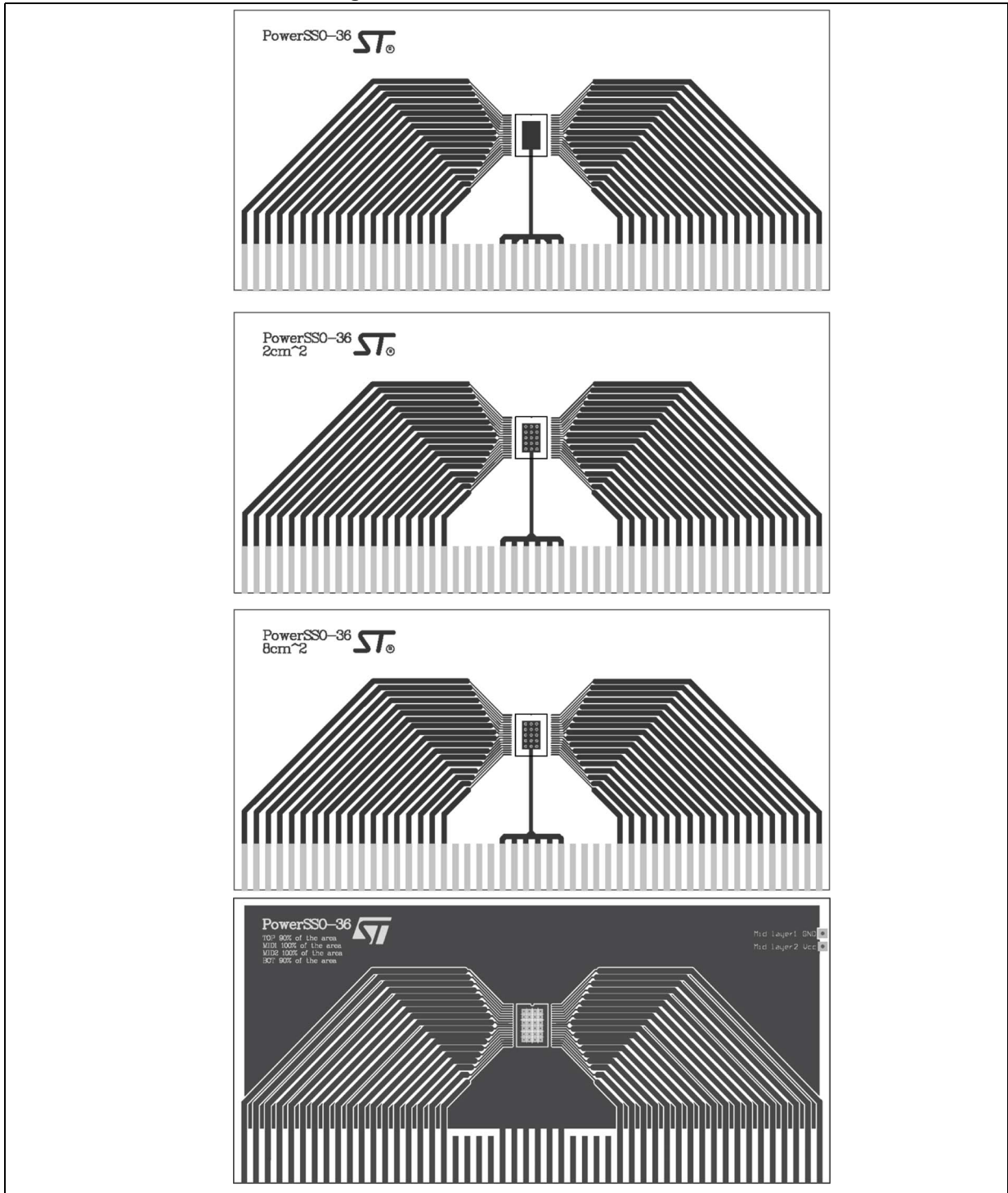


Table 78. PCB properties

| Dimension | Value |
|---|---|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 129 mm x 60 mm |
| Board Material | FR4 |
| Copper thickness (top and bottom layers) | 0.070 mm |
| Copper thickness (inner layers) | 0.035 mm |
| Thermal vias separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Copper thickness on vias | 0.025 mm |
| Footprint dimension (top layer) | 4.1 mm x 6.5 mm |
| Heatsink copper area dimension (bottom layer) | Footprint, 2 cm ² or 8 cm ² |

Figure 30. Rthj-amb vs PCB copper area in open box free air conditions

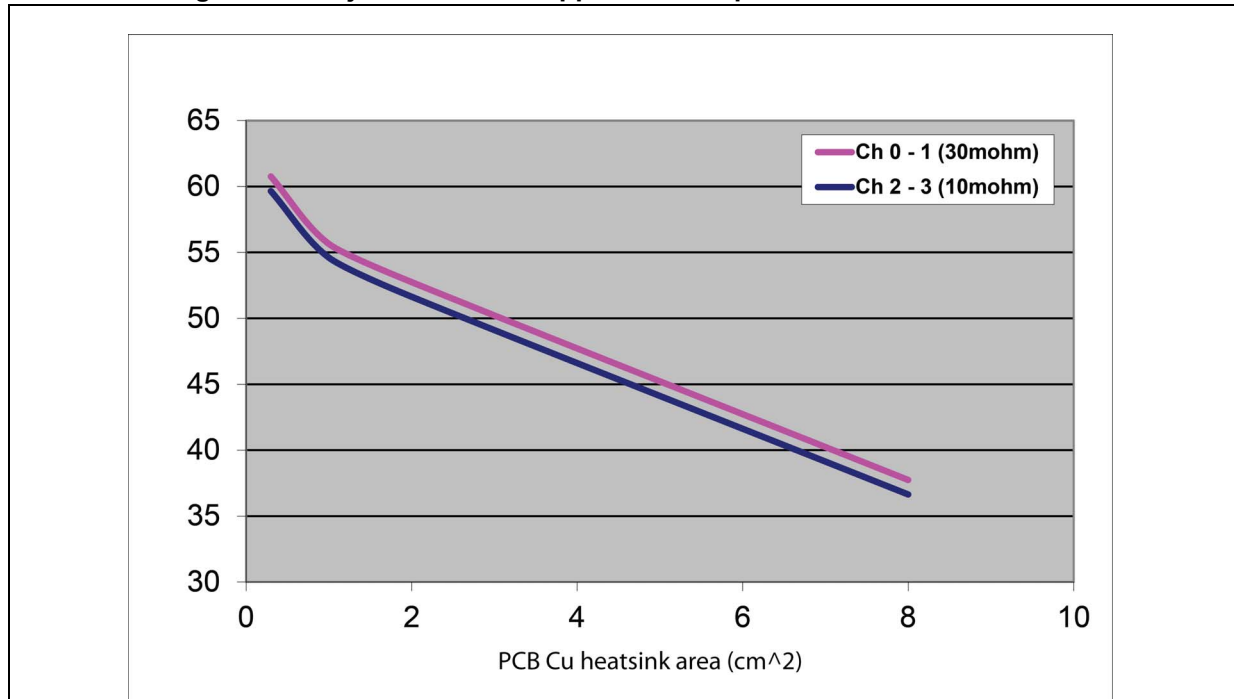
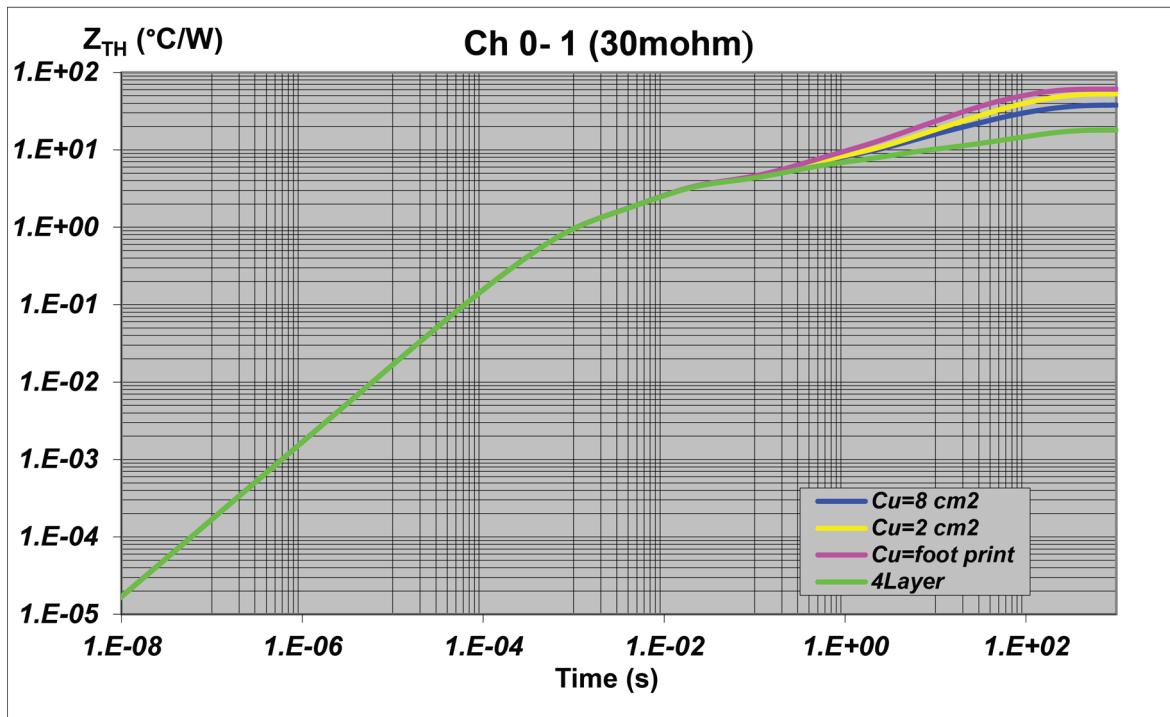
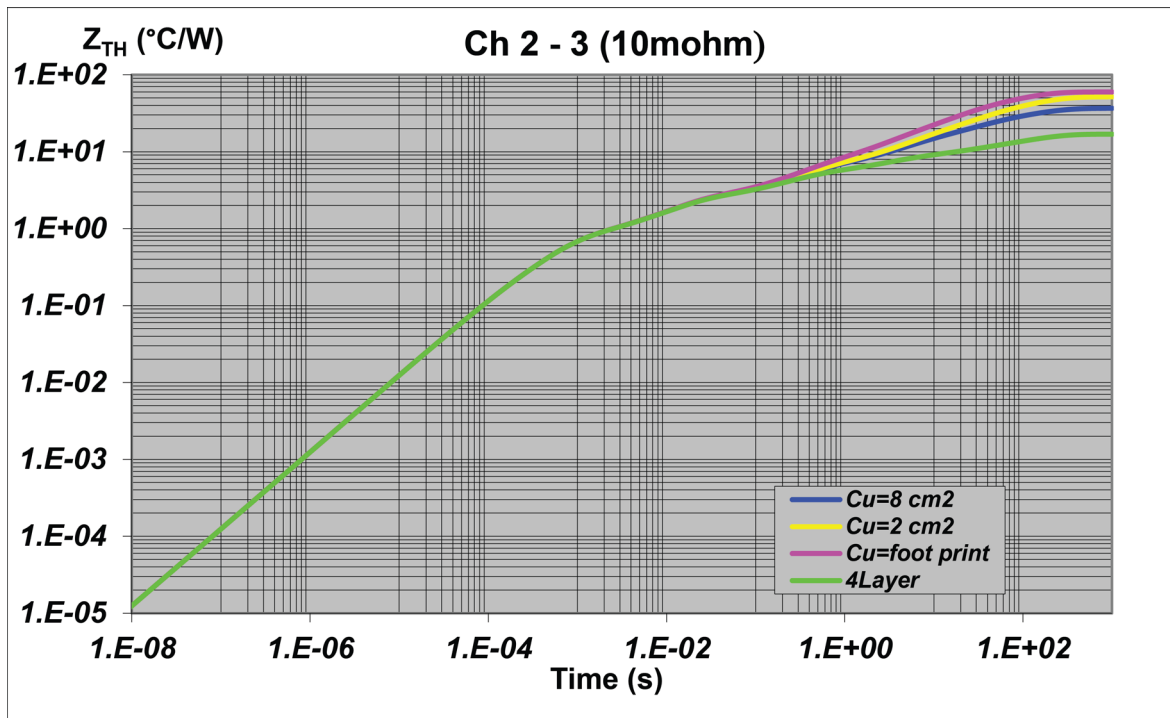


Figure 31. PowerSSO-36 thermal impedance junction ambient single pulse

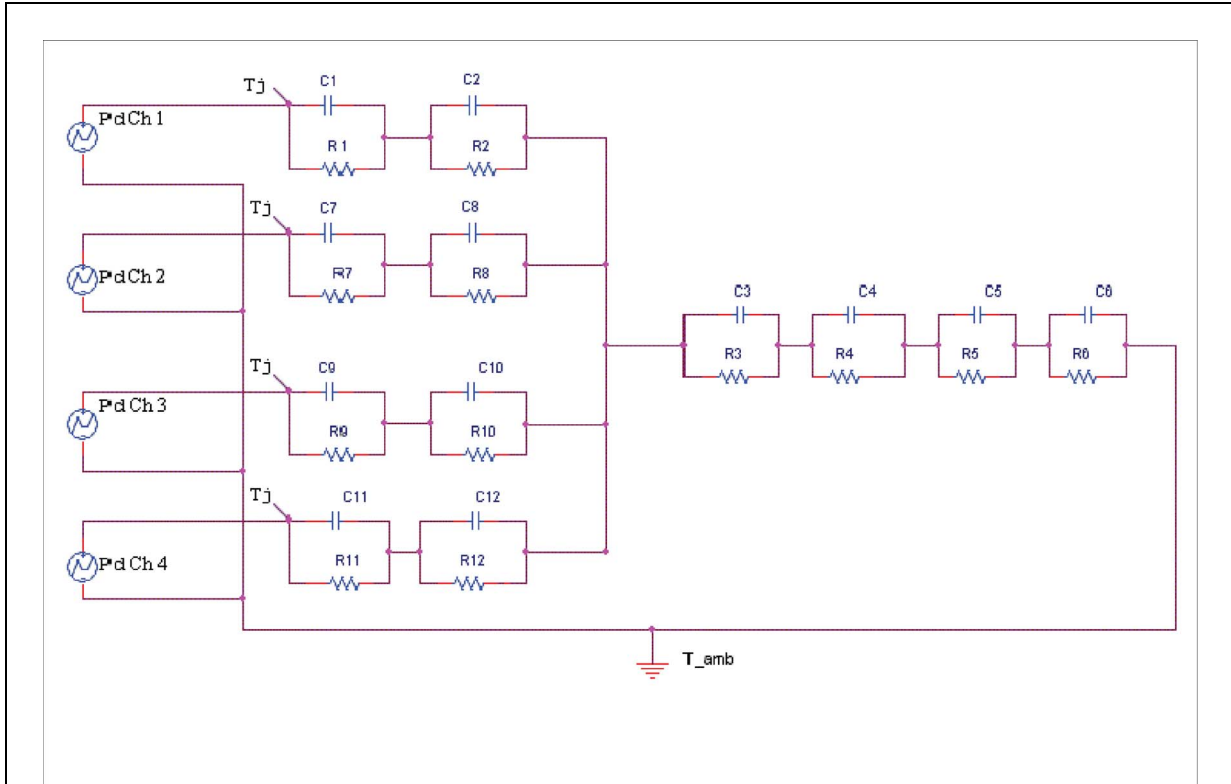


Equation 1

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp} (1 - \delta)$$

where $\delta = t_p/T$

Figure 32. Thermal fitting model for PowerSSO-36



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 79. Thermal parameters

| Area/island (cm ²) | FP | 2 | 8 | 4L |
|--------------------------------|-----|-----|-----|-----|
| R1 = R7 (°C/W) | 0.9 | | | |
| R2 = R8 (°C/W) | 2.5 | | | |
| R3 (°C/W) | 3.4 | 3.4 | 3.4 | 2.6 |
| R4 (°C/W) | 6 | 6 | 6 | 3 |
| R5 (°C/W) | 18 | 14 | 10 | 2 |
| R6 (°C/W) | 30 | 26 | 15 | 7 |
| R7 (°C/W) | 0.9 | | | |
| R8 (°C/W) | 2.5 | | | |
| R9 (°C/W) | 0.7 | | | |
| R10 (°C/W) | 1.6 | | | |

Table 79. Thermal parameters (continued)

| Area/island (cm ²) | FP | 2 | 8 | 4L |
|--------------------------------|--------|-----|-----|----|
| R11 (°C/W) | 0.7 | | | |
| R12 (°C/W) | 1.6 | | | |
| C1 (W·s/°C) | 0.0007 | | | |
| C2 (W·s/°C) | 0.004 | | | |
| C3 (W·s/°C) | 0.1 | | | |
| C4 (W·s/°C) | 0.5 | 0.8 | 0.8 | 1 |
| C5 (W·s/°C) | 1 | 2 | 3 | 10 |
| C6 (W·s/°C) | 3 | 5 | 9 | 18 |
| C7 (W·s/°C) | 0.0007 | | | |
| C8 (W·s/°C) | 0.004 | | | |
| C9 (W·s/°C) | 0.0009 | | | |
| C10 (W·s/°C) | 0.008 | | | |
| C11 (W·s/°C) | 0.0009 | | | |
| C12 (W·s/°C) | 0.008 | | | |

11 Maximum demagnetization energy (VCC = 16 V)

Figure 33. Maximum turn off current versus inductance - Channel 0,1

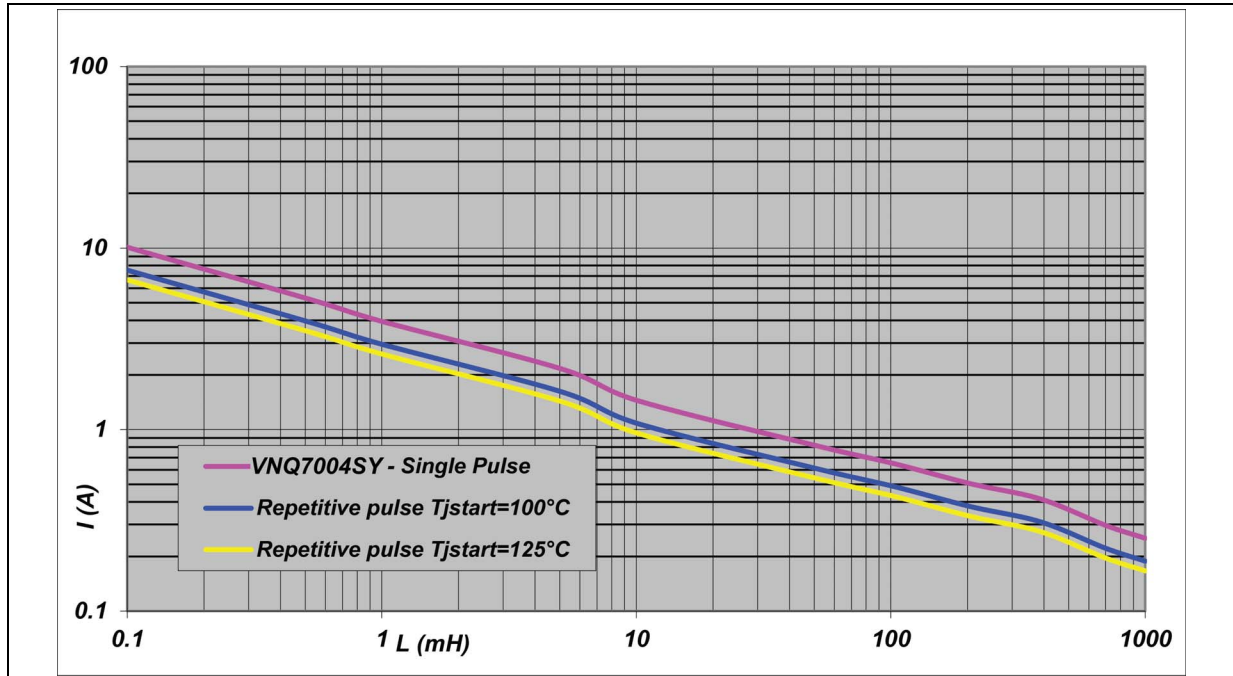
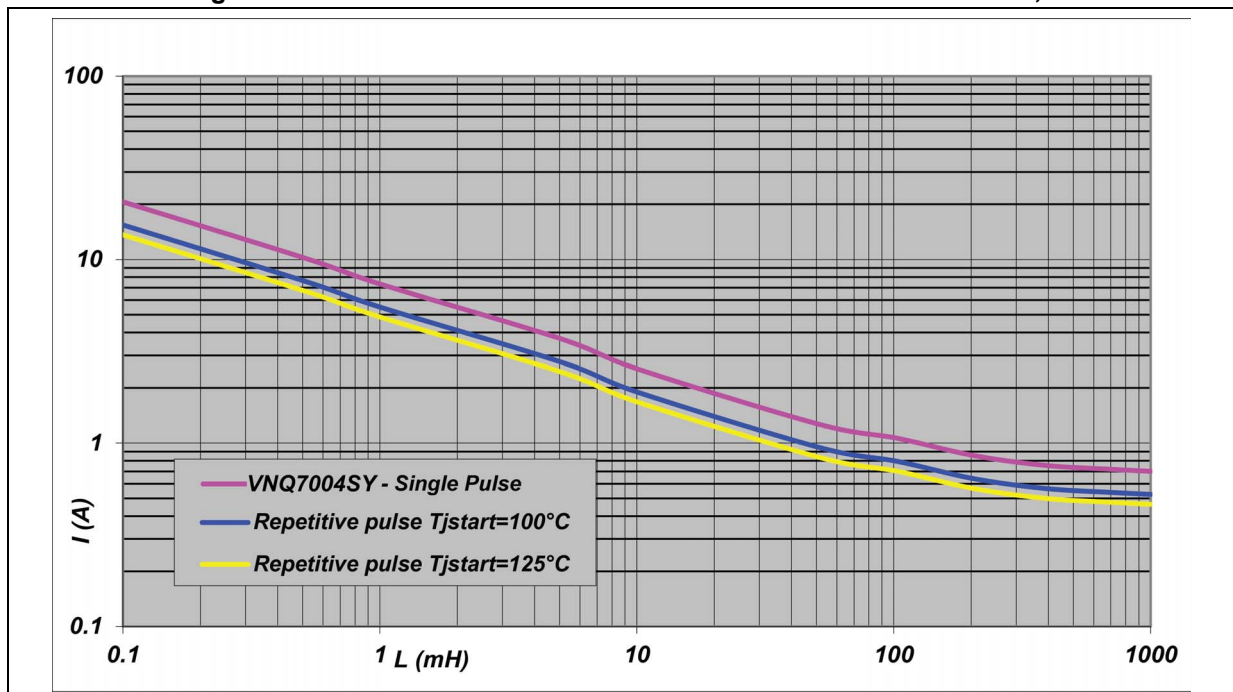


Figure 34. Maximum turn off current versus inductance - Channel 2,3



Note: Values are generated with $R_L = 0 \Omega$.
 In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

12 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

12.1 PowerSSO-36 package information

Figure 35. PowerSSO-36 package outline

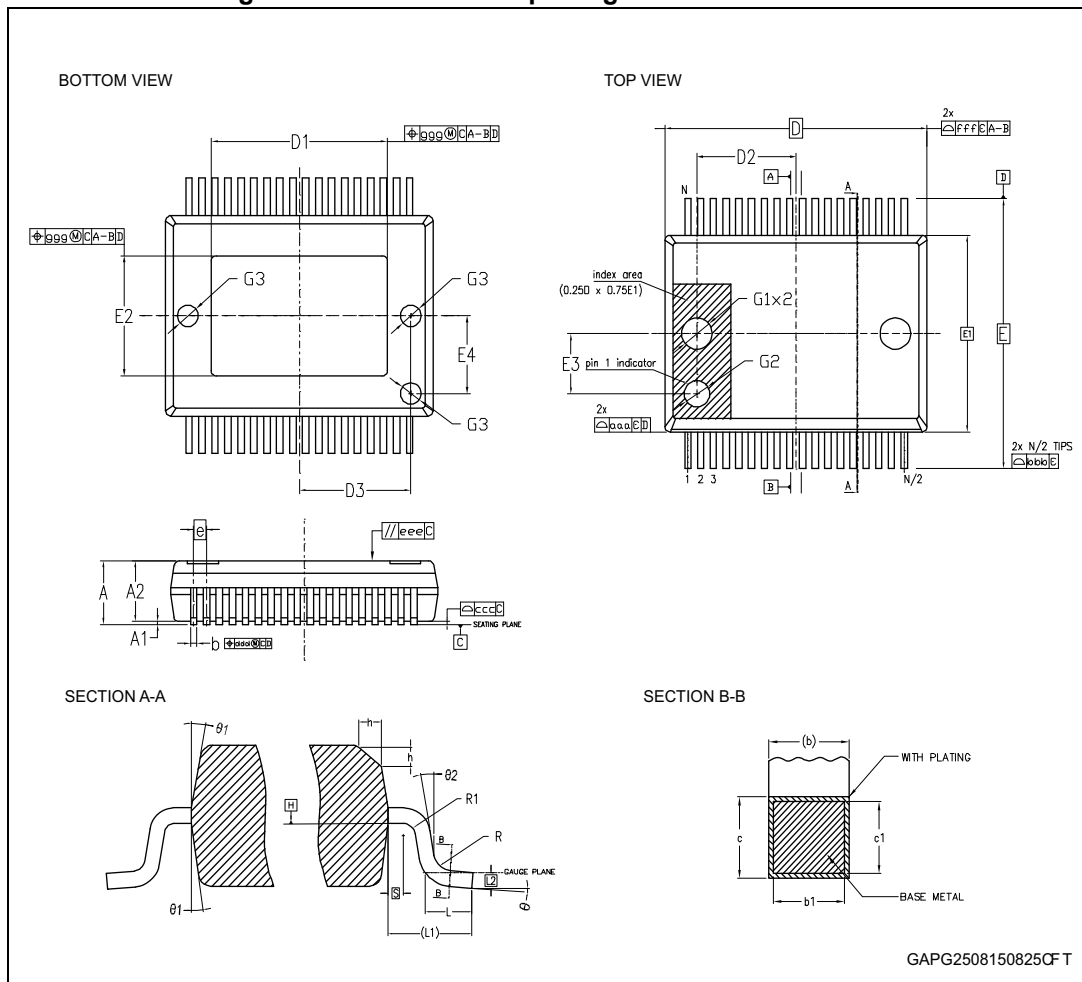


Table 80. PowerSSO-36 mechanical data

| Ref. | Dimensions | | |
|--------------------------------|-------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| Θ | 0° | | 8° |
| Θ1 | 5° | | 10° |
| Θ2 | 0° | | |
| A | 2.15 | | 2.45 |
| A1 | 0.00 | | 0.10 |
| A2 | 2.15 | | 2.35 |
| b | 0.18 | | 0.32 |
| b1 | 0.13 | 0.25 | 0.30 |
| c | 0.23 | | 0.32 |
| c1 | 0.20 | 0.20 | 0.30 |
| D | 10.30 BSC | | |
| D1 | 6.90 | | 7.50 |
| D2 | | 3.65 | |
| D3 | | 4.30 | |
| e | 0.50 BSC | | |
| E | 10.30 BSC | | |
| E1 | 7.50 BSC | | |
| E2 | 4.30 | | 5.20 |
| E3 | | 2.30 | |
| E4 | | 2.90 | |
| G1 | | 1.20 | |
| G2 | | 1.00 | |
| G3 | | 0.80 | |
| h | 0.30 | | 0.40 |
| L | 0.55 | 0.70 | 0.85 |
| L1 | 1.40 REF | | |
| L2 | 0.25 BSC | | |
| N | 36 | | |
| R | 0.30 | | |
| R1 | 0.20 | | |
| S | 0.25 | | |
| Tolerance of form and position | | | |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.20 | | |

Table 80. PowerSSO-36 mechanical data (continued)

| Ref. | Dimensions | | |
|------|-------------|------|------|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| eee | | 0.10 | |
| fff | | 0.20 | |
| ggg | | 0.15 | |

12.2 PowerSSO-36 packing information

Figure 36. PowerSSO-36 reel 13"

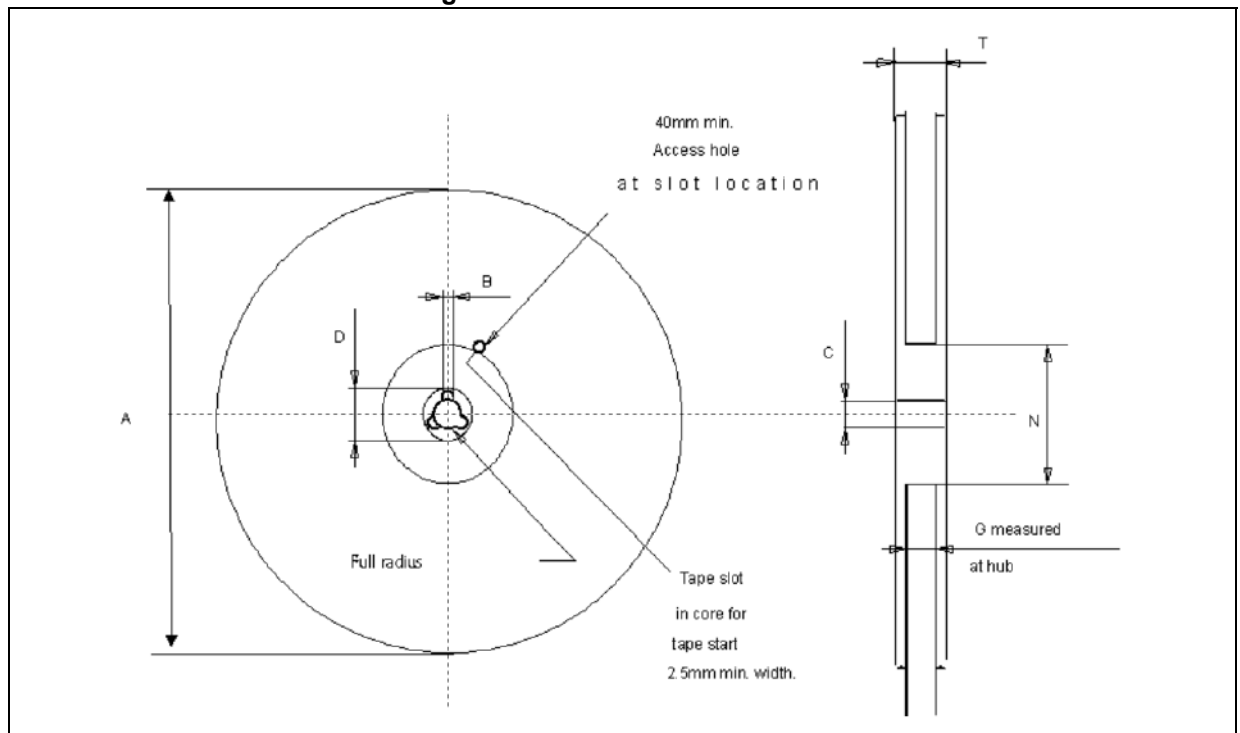


Table 81. Reel dimensions

| Description | Value ⁽¹⁾ |
|-----------------|----------------------|
| Base quantity | 1000 |
| Bulk quantity | 1000 |
| A (max) | 330 |
| B (min) | 1.5 |
| C (± 0.2) | 13 |
| F | 20.2 |
| G (+2 / -0) | 24.4 |
| N (min) | 100 |
| T (max) | 30.4 |

1. All dimensions are in mm.

Figure 37. PowerSSO-36 carrier tape

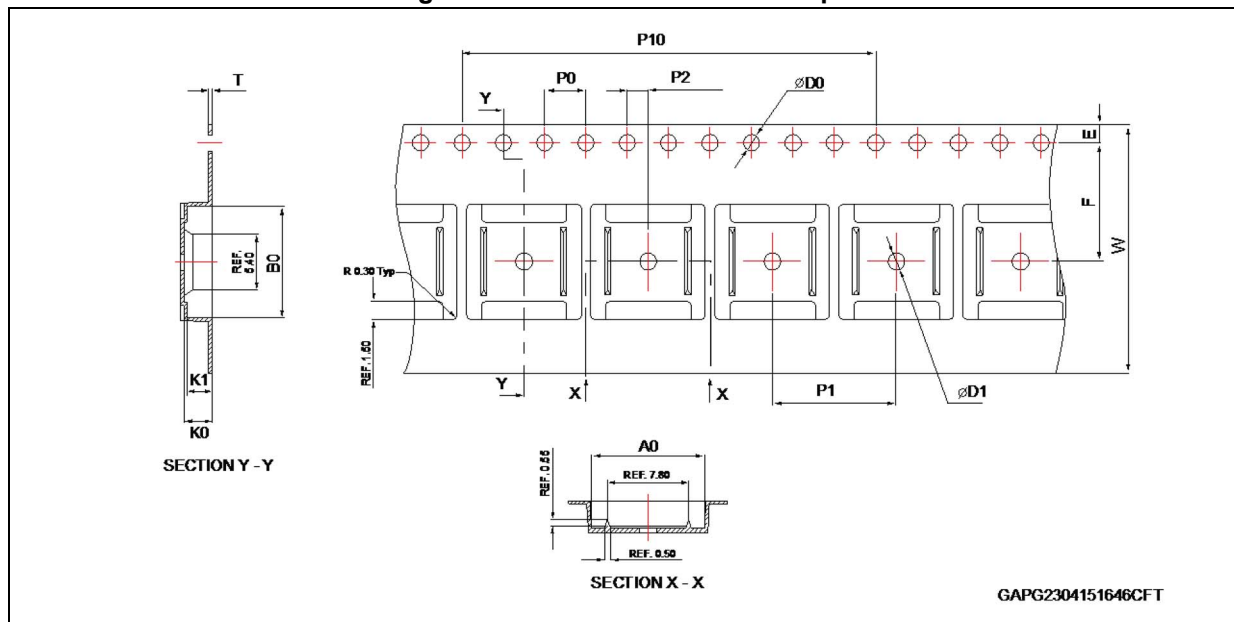


Table 82. PowerSSO-36 carrier tape dimensions

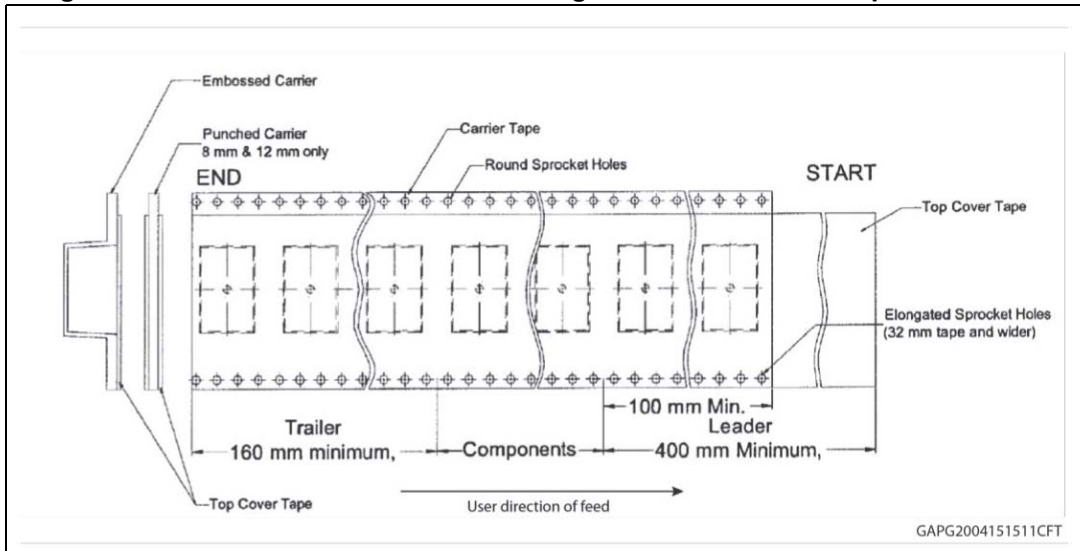
| Description | Value ⁽¹⁾ |
|----------------|----------------------|
| A ₀ | 10.90 \pm 0.10 |
| B ₀ | 10.80 \pm 0.10 |
| K ₀ | 2.75 \pm 0.10 |
| K ₁ | 2.45 \pm 0.10 |
| D ₀ | 1.50 (+0.10 / -0) |
| D ₁ | 1.60 \pm 0.10 |

Table 82. PowerSSO-36 carrier tape dimensions (continued)

| Description | Value ⁽¹⁾ |
|-----------------|----------------------|
| P ₀ | 4.00 ± 0.10 |
| P ₁ | 12.00 ± 0.10 |
| P ₂ | 2.00 ± 0.10 |
| P ₁₀ | 40.00 ± 0.20 |
| E | 1.75 ± 0.10 |
| F | 11.50 ± 0.10 |
| W | 24.00 ± 0.30 |
| T | 0.30 ± 0.05 |

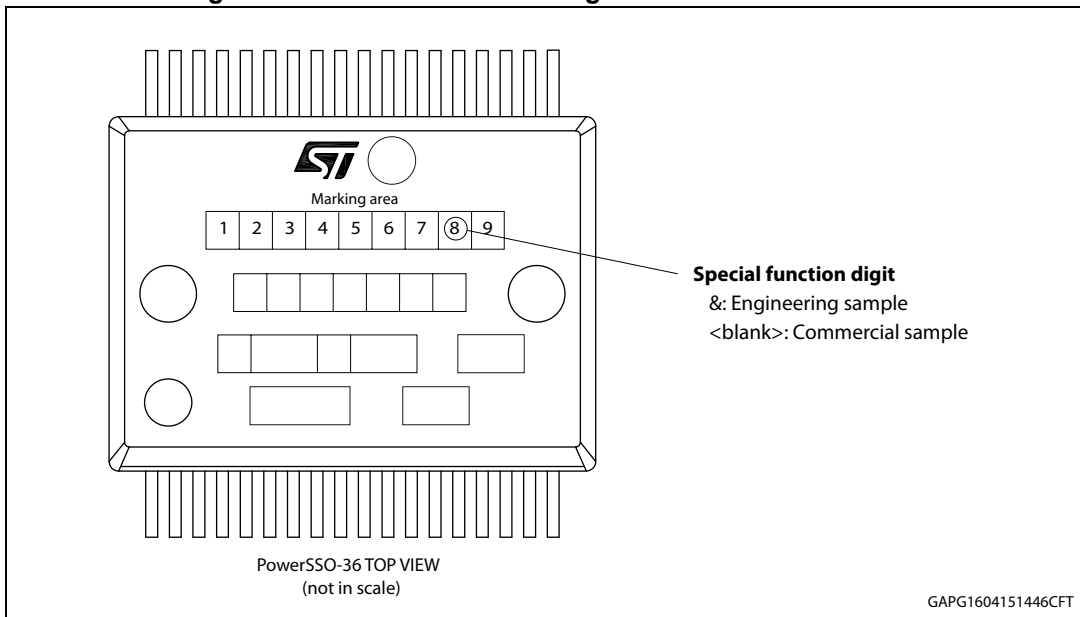
1. All dimensions are in mm

Figure 38. PowerSSO-36 schematic drawing of leader and trailer tape



12.3 PowerSSO-36 marking information

Figure 39. PowerSSO-36 marking information



Note: *Engineering Samples: Parts marked as “&” are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity. Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.*

13 Order codes

Table 83. Device summary

| Package | Order codes | |
|-------------|-------------|---------------|
| | Tube | Tape and reel |
| PowerSSO-36 | VNQ7004SY | VNQ7004SYTR |

14 Revision history

Table 84. Document revision history

| Date | Revision | Description of changes |
|-------------|----------|--|
| 23-Jan-2018 | 1 | Initial release. |
| 04-Apr-2018 | 2 | <p>In Table 67: BULB - switching (VCC = 13 V; Fast switch mode):</p> <ul style="list-style-type: none"> – updated parameter description of “t_{skew}” symbol from “Turn-off turn-on time” in “Turn-off turn-on time Ch2,3” – updated parameter description of “$(dV_{OUT}/dt)_{on}$” symbol from “Turn-on voltage slope” in “Turn-on voltage slope Ch2,3” – updated parameter description of “$(dV_{OUT}/dt)_{off}$” symbol from “Turn-off voltage slope” in “Turn-off voltage slope Ch2,3” – updated parameter description of “W_{ON}” symbol from “Switching losses energy” in “Switching losses energy at turn-on Ch2,3” – updated parameter description of “W_{OFF}” symbol from “Switching losses energy” in “Switching losses energy at turn-off Ch2,3” <p>Updated title of Table 72: LED - switching (VCC = 13 V; Normal switch mode)</p> |

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