ATBTLC1000 QFN SoC

Ultra Low Power BLE 4.1 SoC

DATASHEET

Description

The Atmel® ATBTLC1000 is an ultra-low power Bluetooth® SMART (BLE 4.1) System on a Chip with Integrated MCU, Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It can be used as a Bluetooth Low Energy link controller or data pump with external host MCU or as a standalone applications processor with embedded BLE connectivity and external memory.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

Features

- Complies with Bluetooth V4.1, ETSI EN 300 328 and EN 300 440 Class 2, FCC CFR47 Part 15 and ARIB STD-T66
- 2.4GHz transceiver and modem
  - -95dBm/-93dBm programmable receiver sensitivity
  - -20 to +3.5dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
  - Single wire Debug (SWD) interface
  - Four-channel DMA controller
  - Brownout detector and Power On Reset
  - Watch Dog Timer
- Memory
  - 128kB embedded RAM (96kB available for application)
  - 128kB embedded ROM
- Hardware Security Accelerators
  - AES-128
  - SHA-256
- Peripherals
  - 12 digital and one wakeup GPIOs with 96kΩ internal pull-up resistors, two Mixed Signal GPIO
  - 2x SPI Master/Slave
  - 2x I^2C Master/Slave and 1x I^2C Slave
  - 2x UART
  - 1x SPI Flash
  - Three-axis quadrature decoder
  - 4x Pulse Width Modulation (PWM), three General Purpose Timers, and one Wakeup Timer

  - 2-channel 11-bit ADC
- Clock
  - Integrated 26MHz RC oscillator
  - 26MHz crystal oscillator
  - Integrated 2MHz sleep RC oscillator
  - 32.768kHz RTC crystal oscillator
- Ultra Low power
  - 1.1µA sleep current (8KB RAM retention and RTC running)
  - 3.0mA peak TX current (0dBm, 3.6V)
  - 3.0mA peak RX current (3.6V, -93dBm sensitivity)
  - 9.7µA average advertisement current (three channels, 1s interval)
- Integrated Power management
  - 1.8 to 4.3V battery voltage range
- Fully integrated Buck DC/DC converter
- Bluetooth SIG Certification
  - QD ID Controller (see declaration D028678)
  - QD ID Host (see declaration D028679)

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1 Ordering Information

Ordering code	Package	Description
ATBTLC1000A-MU-T	4x4mm QFN 32	ATBTLC1000 Tape & Reel
ATBTLC1000A-MU-Y	4x4mm QFN 32	ATBTCL1000 Tray

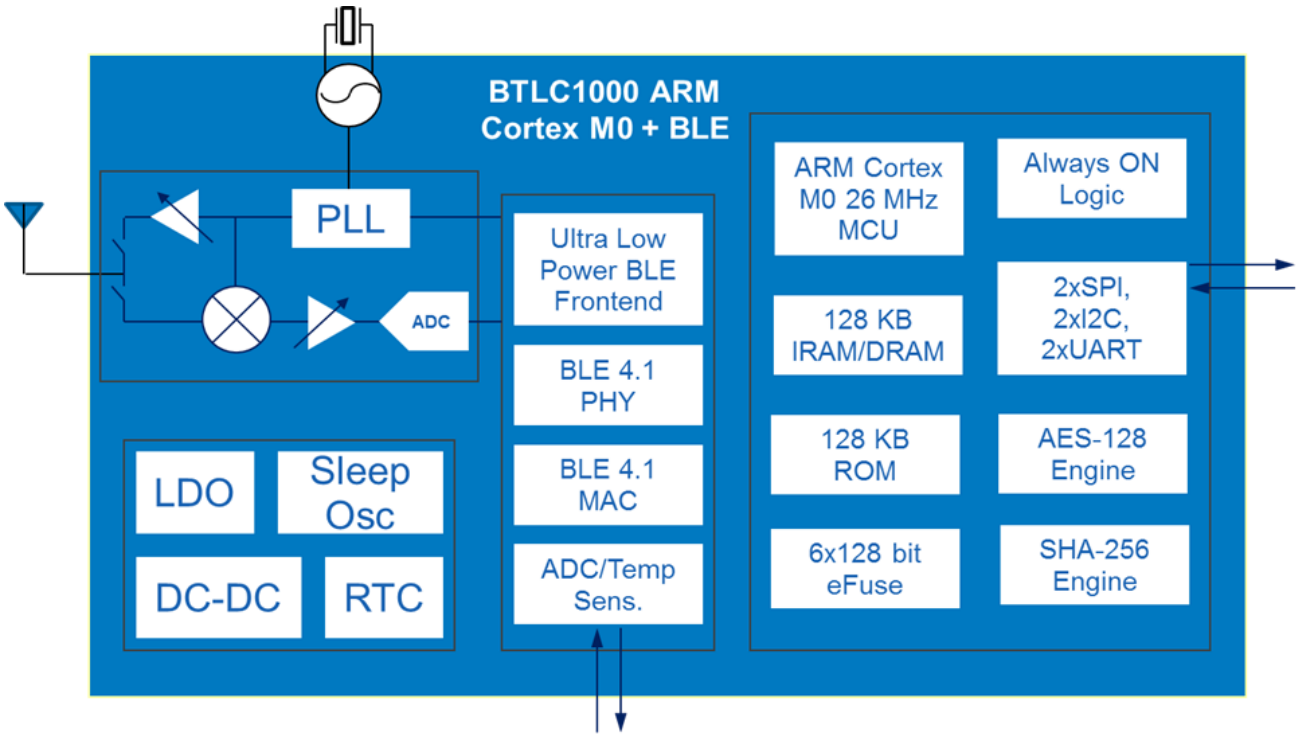
2 Package Information

Table 2-1. ATBTLC1000 4x4 QFN 32 Package Information

Parameter	Value	Units	Tolerance
Package Size	4x4	mm	±0.1mm
QFN Pad Count	32		
Total Thickness	0.85	mm	+0.15/-0.05mm
QFN Pad Pitch	0.4		
Pad Width	0.2		
Exposed Pad size	2.7 x 2.7		

3 Block Diagram

Figure 3-1. ATBTLC1000 Block Diagram



4 Pinout Information

ATBTLC1000 is offered in an exposed pad 32-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. In Figure 4-1 the QFN package pin assignment is shown. The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – digital I/O power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The ATBTLC1000 pins are described in Table 4-1.

Figure 4-1. ATBTLC1000 Pin Assignment

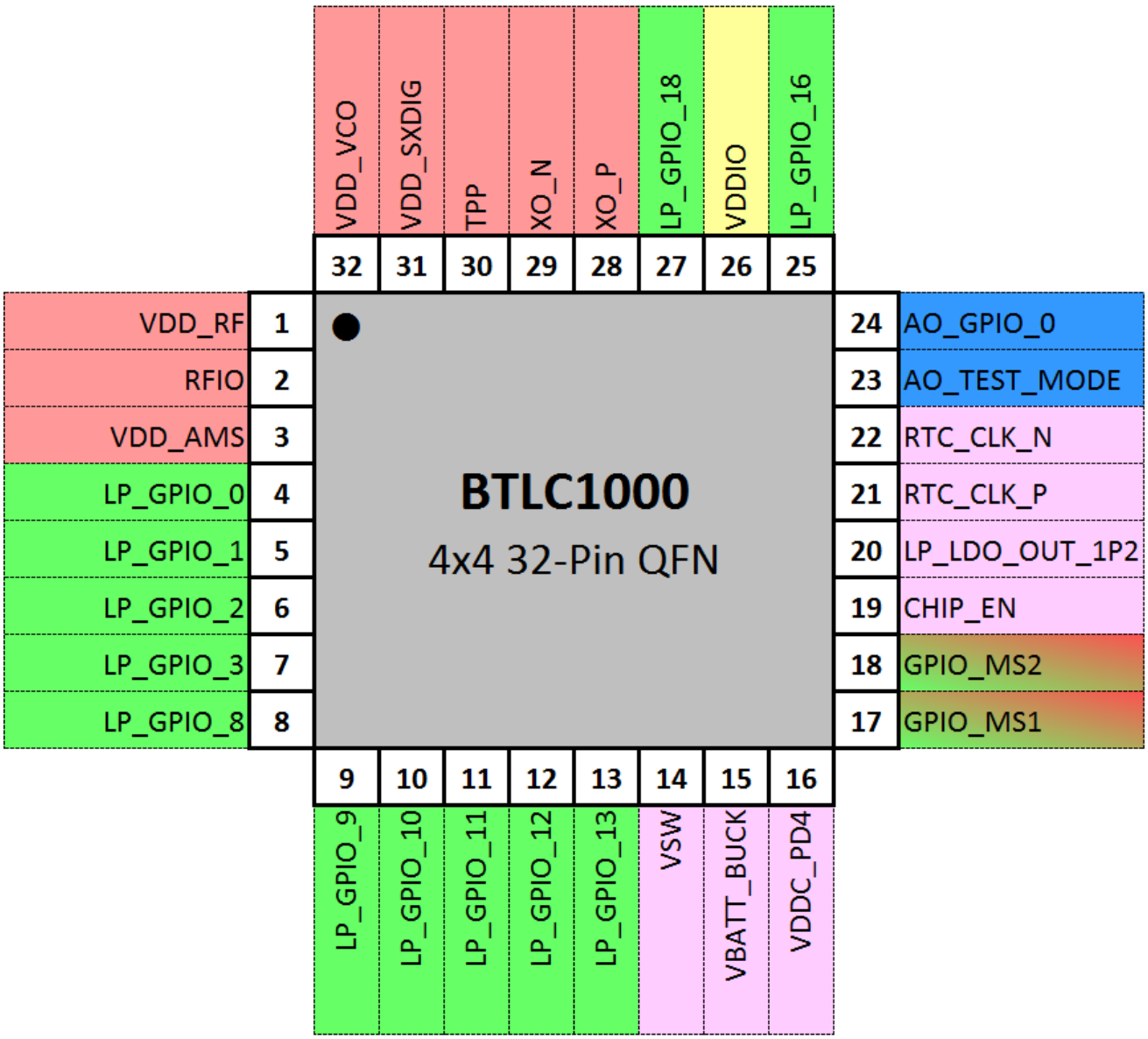


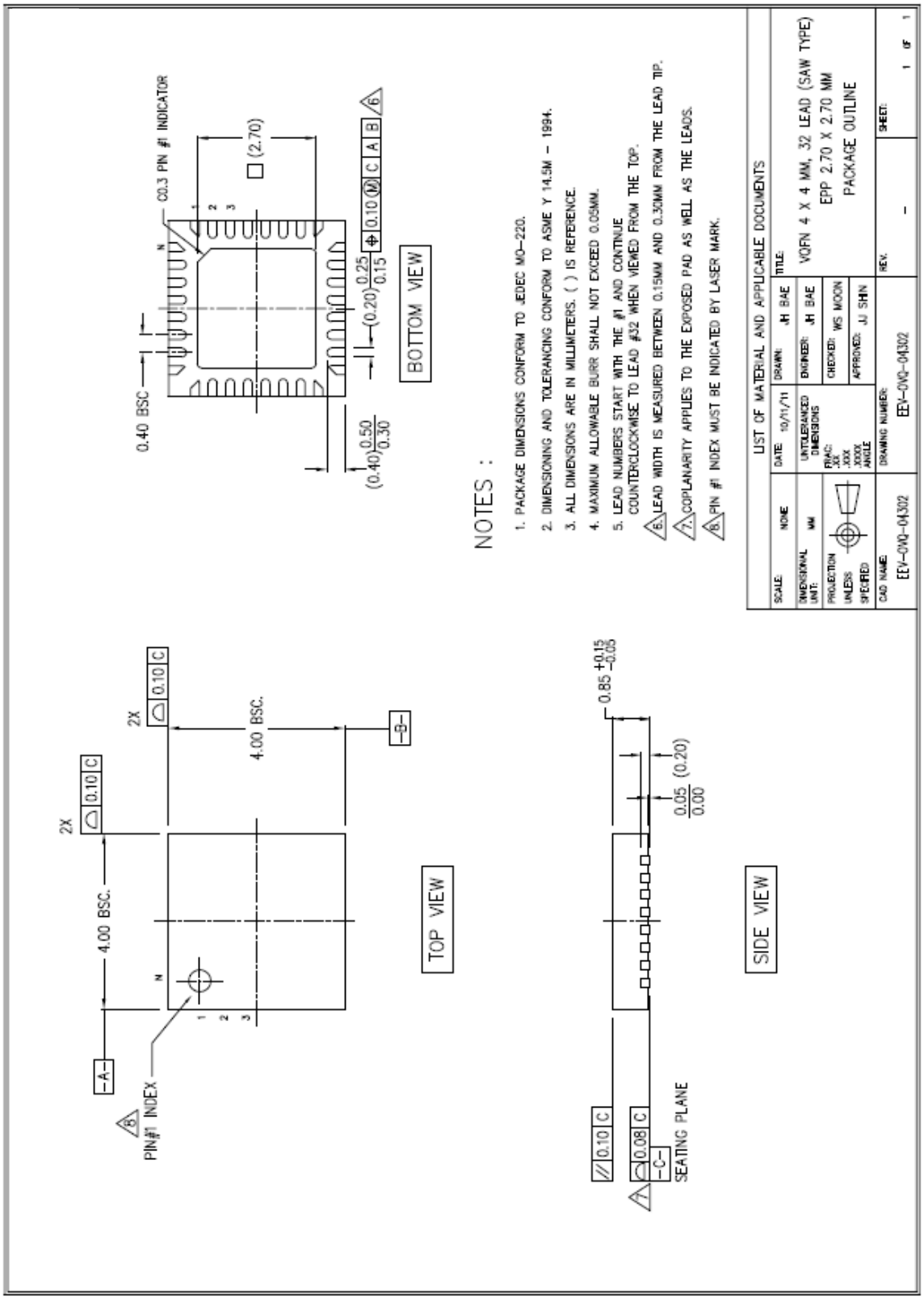
Table 4-1. ATBTLC1000 Pin Description

Pin #	Pin name	Pin type	Description / Default function
1	VDD_RF	Analog/RF	RF Supply 1.2V
2	RFIO	Analog/RF	RX input and TX output
3	VDD_AMS	Analog/RF	AMS Supply 1.2V
4	LP_GPIO_0	Digital I/O	SWD Clock
5	LP_GPIO_1	Digital I/O	SWD I/O
6	LP_GPIO_2	Digital I/O	UART RXD
7	LP_GPIO_3	Digital I/O	UART TXD
8	LP_GPIO_8	Digital I/O	UART_CTS
9	LP_GPIO_9	Digital I/O	UART_RTS
10	LP_GPIO_10	Digital I/O	SPI SCK/SPI FLASH SCK
11	LP_GPIO_11	Digital I/O	SPI MOSI/SPI FLASH TXD
12	LP_GPIO_12	Digital I/O	SPI SSN/SPI FLASH SSN
13	LP_GPIO_13	Digital I/O	SPI MISO/SPI FLASH RXD
14	VSW	PMU	DC/DC Converter Switching Node
15	VBATT_BUCK	PMU	DC/DC Converter Supply and General Battery Connection
16	VDDC_PD4	PMU	DC/DC Converter 1.2V output and feedback node
17	GPIO_MS1	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
18	GPIO_MS2	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
19	CHIP_EN	PMU	Master Enable for chip
20	LP_LDO_OUT_1P2	PMU	Low Power LDO output (connect to 1µF decoupling cap)
21	RTC_CLK_P	PMU	RTC terminal + / 32.768kHz XTAL +
22	RTC_CLK_N	PMU	RTC terminal – / 32.768kHz XTAL -
23	AO_TEST_MODE	Digital Input	Test Mode Selection (SCAN ATE)/GND for normal operation
24	AO_GPIO_0	Digital I/O	Always-on External Wakeup
25	LP_GPIO_16	Digital I/O	GPIO
26	VDDIO	Digital I/O Power	I/O Supply, can be less than or equal to VBATT_BUCK
27	LP_GPIO_18	Digital I/O	GPIO
28	XO_P	Analog/RF	XO Crystal +
29	XO_N	Analog/RF	XO Crystal -
30	TPP	Analog/RF	Test MUX + output
31	VDD_SXDIG	Analog/RF	Synthesizer Digital Supply 1.2V
32	VDD_VCO	Analog/RF	Synthesizer VCO Supply 1.2V
Paddle	Paddle Pad	Power	Ground connection, must be tied to system board ground

5 Package Drawing

The ATBTLC1000 QFN package is RoHS/green compliant.

Figure 5-1. ATBTLC1000 4x4 QFN 32 Package Outline Drawing

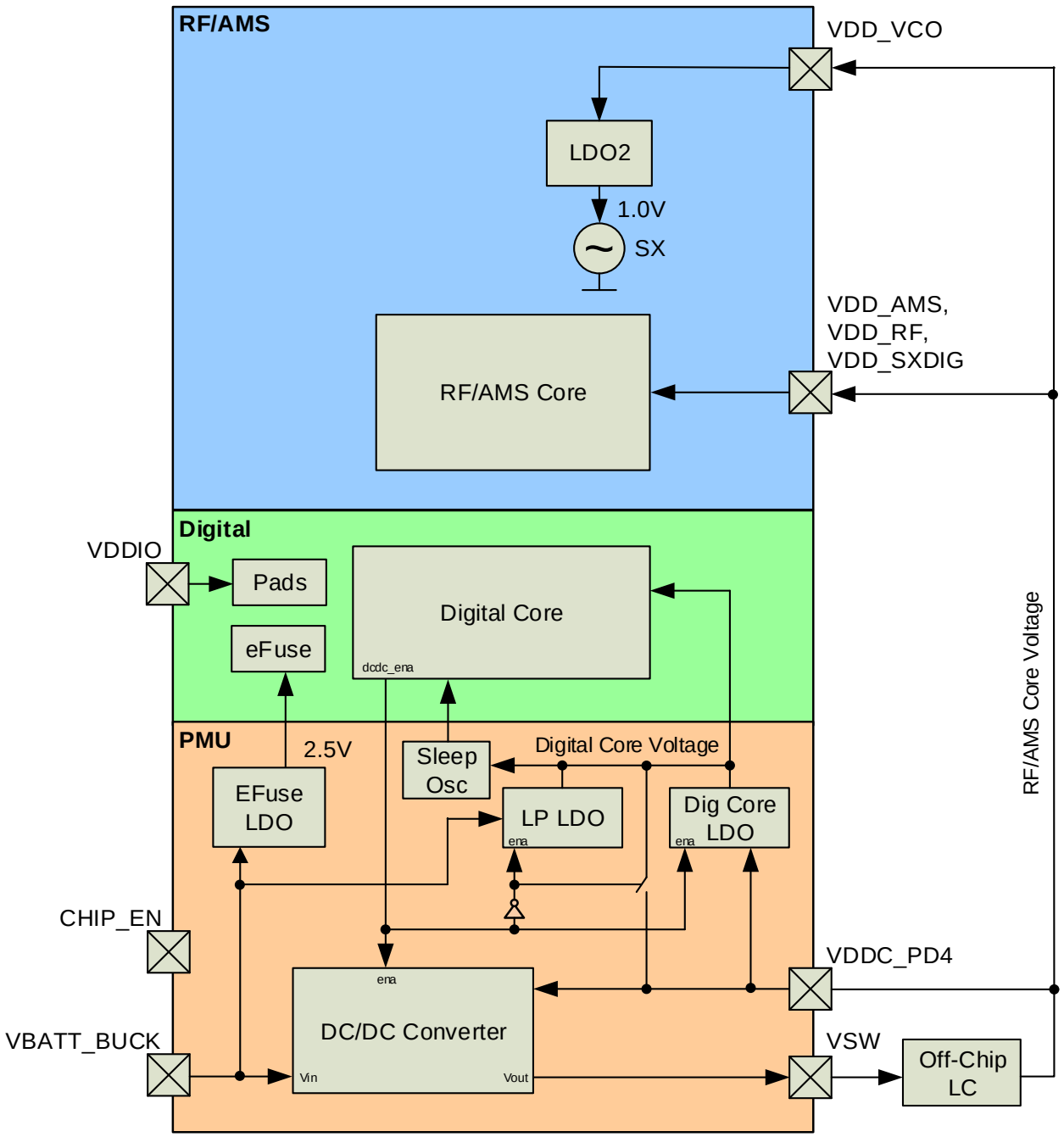


6 Power Management

6.1 Power Architecture

ATBTLC1000 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The integrated power management block includes a DC/DC buck converter and separate Low Drop Out (LDO) regulators for different power domains. The DC/DC buck converter converts battery voltage to a lower internal voltage for the different circuit blocks and does this with high efficiency. The DC/DC requires three external components for proper operation (two inductors, L, 4.7µH and 9.1nH, and one capacitor, C, 4.7µF).

Figure 6-1. ATBTLC1000 Power Architecture



6.2 DC/DC Converter

The DC/DC Converter is intended to supply current to the BLE digital core and the RF transceiver core. The DC/DC consists of a power switch, 26MHz RC oscillator, controller, external inductor, and external capacitor. The DCDC is utilizing pulse skipping discontinuous mode as its control scheme. The DC/DC specifications are shown in the following tables and figures.

Table 6-1. DC/DC Converter Specifications (performance is guaranteed for (L) 4.7µH and (C) 4.7µF)

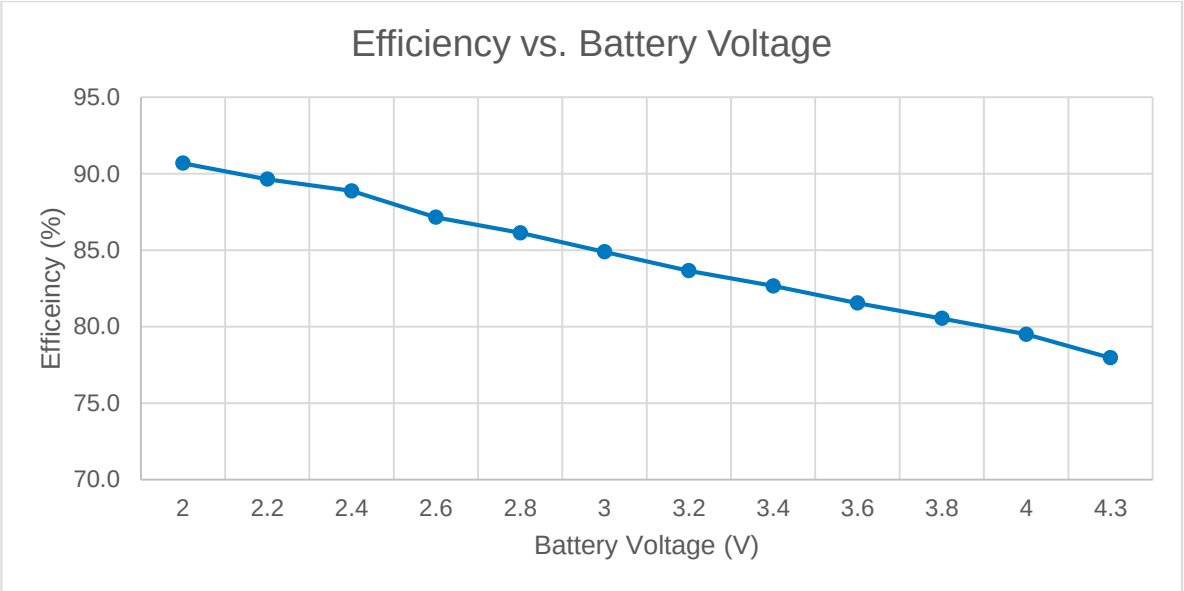
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output current capability	I_{REG}	0	10	30	mA	Dependent on external component values and DC/DC settings with acceptable efficiency
External capacitor range	C_{EXT}	2	4.7	20	µF	External capacitance range
External inductor range	L_{EXT}	2	4.7	10	µH	External inductance range
Battery voltage	V_{BAT}	1.8	3	4.3	V	Functionality and stability given
Output voltage range	V_{REG}	1.05	1.2	1.47		25mV step size
Current consumption	I_{DD}		125		µA	DC/DC quiescent current
Startup time	$t_{startup}$	20		600	µs	Dependent on external component values and DC/DC settings
Voltage ripple	ΔV_{REG}	5	10	30	mV	Dependent on external component values and DC/DC settings
Efficiency	η		85		%	Measured at 3V VBATT, at load of 10mA
Overshoot at startup	V_{OS}		0		mV	No overshoot, no output pre-charge
Line Regulation	ΔV_{REG}		10			From 1.8 to 4.3V
Load regulation	ΔV_{REG}		5			From 0 to 10mA

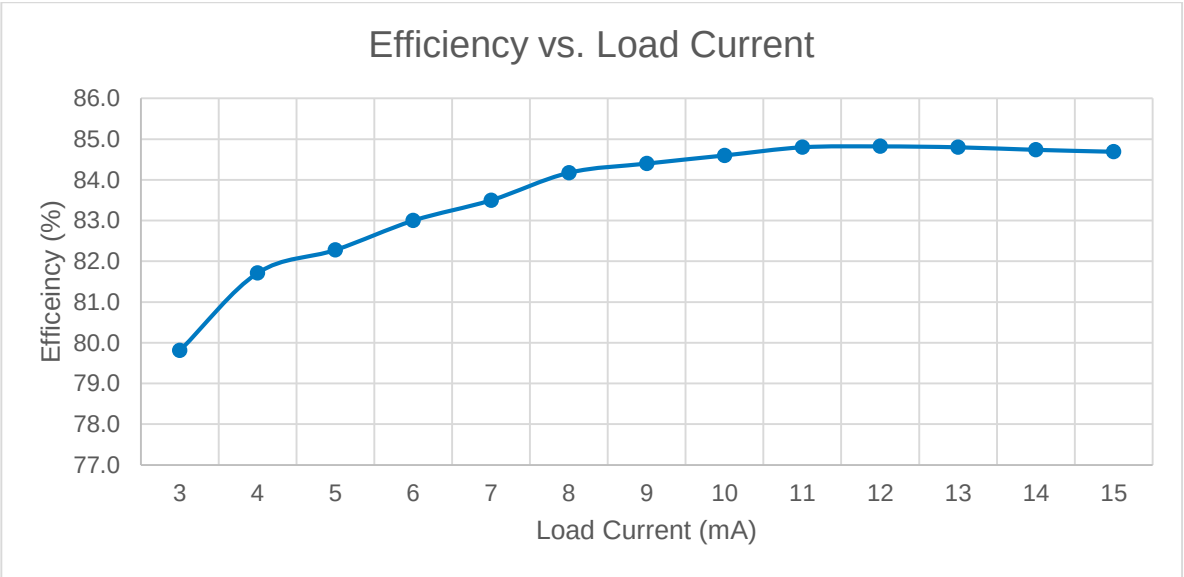
Figure 6-2. DC/DC Converter Allowable Onboard Inductor and Capacitor Values (VBATT = 3V)

Inductor [µH]	Efficiency [%]	Vripple [mV]			RX Sensitivity (1) [dBm]
		C=2.2µF	C=4.7µF	C=10µF	
2.2	83	N/A	<5	<5	~1.5dB degrade
4.7	85	9	5	<5	~0.7dB degrade

Note: 1. Degradation relative to design powered by external LDO and DC/DC disabled.

Figure 6-3. DC/DC Converter Efficiency





6.3 Power Consumption

6.3.1 Description of Device States

ATBTLC1000 has multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered on if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal (Application may or may not be active)
- BLE_On_Receive – Device is actively receiving a BLE signal (Application may or may not be active)
- MCU_Only – Device has ARM processor powered on and BLE subsystem powered down
- Ultra_Low_Power – BLE is powered down and Application is powered down (with or without RAM retention)
- Power_Down – Device core supply off

6.3.2 Controlling the Device States

The following pins are used to switch between the main device states:

- CHIP_EN – used to enable PMU
- VDDIO – I/O supply voltage from external supply

In Power_Down state, VDDIO is on and CHIP_EN is low (at GND level). To switch between Power_Down state and MCU_Only state CHIP_EN has to change between low and high (VDDIO voltage level). Once the device is MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage.

When no power is supplied to the device (the DC/DC Converter output and VDDIO are both off and at ground potential), a voltage cannot be applied to the ATBTLC1000 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

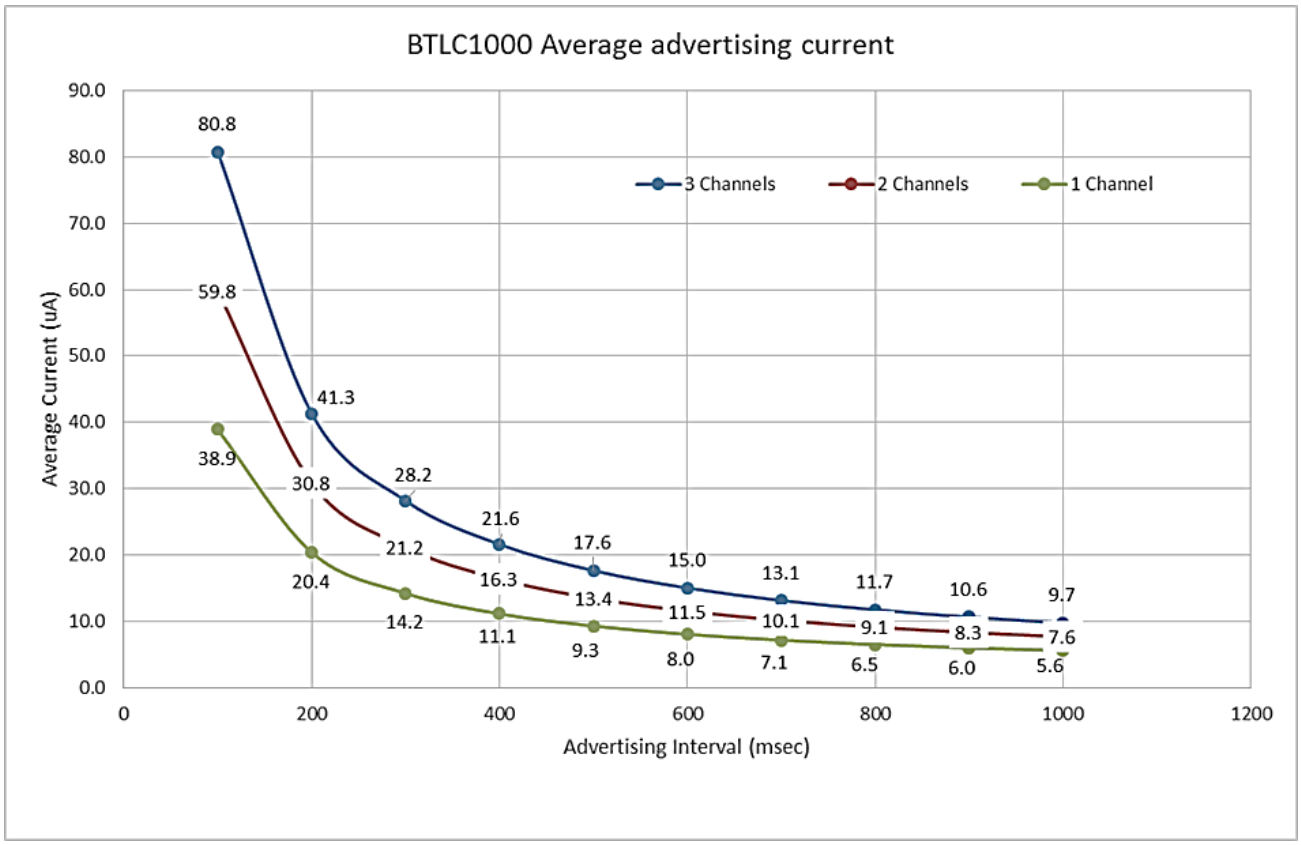
6.3.3 Current Consumption in Various Device States

Table 6-2. Device State Current Consumption with VBAT = 3.6V

Device State	CHIP_EN	VDDIO	I_{VBAT} (typical) (note 3)	I_{VDDIO} (typical) (note 3)	Remark
Power_Down	Off	On	<50nA	<50nA	
Ultra_Low_Power Standby	On	On	900nA	50nA	
Ultra_Low_Power with 8KB retention, BLE timer, no RTC (1)	On	On	1.1µA	0.2µA	
Ultra_Low_Power with 8KB retention, BLE timer, with RTC (2)	On	On	1.25µA	0.1uA	
MCU_Only, idle (waiting for interrupt)	On	On	.85mA	0.2µA	
BLE_On_Receive@-96dBm	On	On	4.2mA	0.2µA	
BLE_On_Transmit, 0dBm output power	On	On	3.0mA	0.2µA	
BLE_On_Transmit, 3.5dBm output power	On	On	4.0mA	0.2µA	

Notes:
1. Sleep clock derived from internal 32kHz RC oscillator.
2. Sleep clock derived from external 32.768kHz crystal specified for CL=7pF, using the default on-chip capacitance only, without using external capacitance.
3. Expected values for production silicon.

Figure 6-4. ATBTLC1000 Average Advertising Current(1)



Note: 1. The Average advertising current is measured at VBAT = 3.6V, TX POUT=0dBm.

6.4 Power Sequence

6.5 Power-up Sequence

The power-up sequence for ATBTLC1000 is shown in Figure 6-5. The timing parameters are provided in Table 6-3.

Figure 6-5. ATBTLC1000 Power-up Sequence

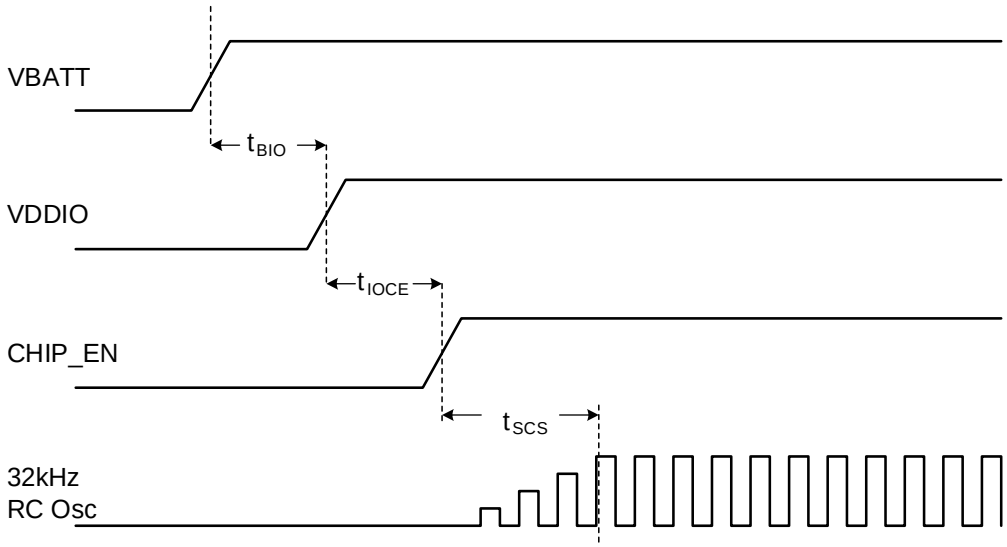


Table 6-3. ATBTLC1000 Power-up Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together
t_{IOCE}	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_{SCS}	10		µs	CHIP_EN rise to 31.25kHz (2MHz/64) oscillator stabilizing	

6.6 Power-down Sequence

Figure 6-6. ATBTLC1000 Power-down Sequence

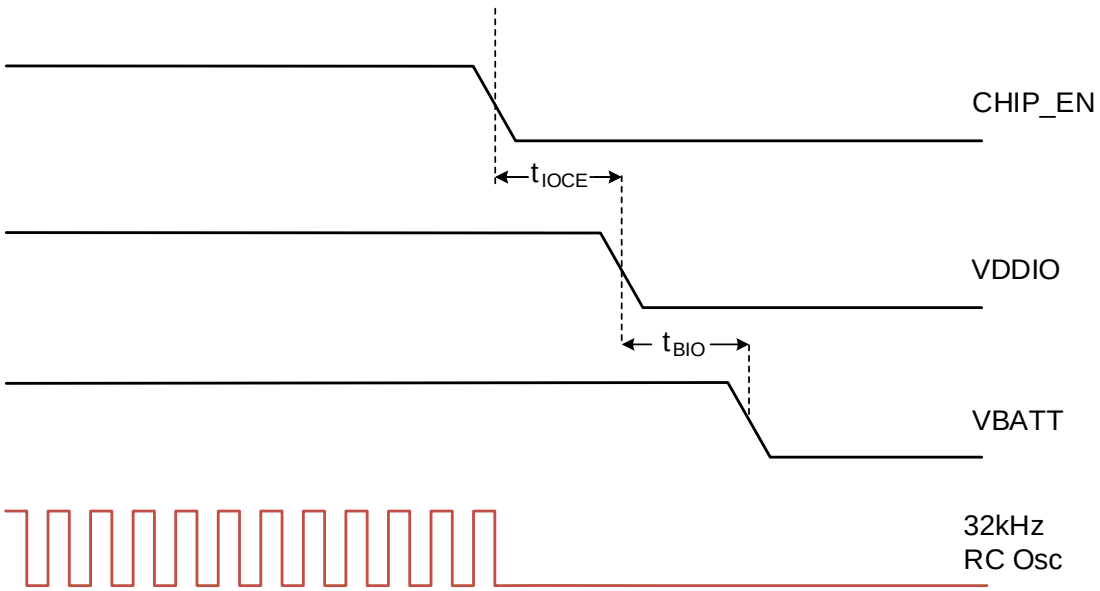


Table 6-4. ATBTLC1000 Power-down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_{IOCE}	0		ms	CHIP_EN fall to VDDIO fall	CHIP_EN must fall before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_{BIO}	0			VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or be tied together

6.7 Power On Reset (POR) and Brown Out Detector (BOD)

The ATBTLC1000 has a POR circuit for proper system power bring up and a brownout detector to reset the system's operation when a drop in battery voltage is detected.

- POR is a power on reset circuit that outputs a HI logic value when the VBATT_BUCK is below a voltage threshold. The POR output becomes a LO logic value when the VBATT_BUCK is above a voltage threshold.

- BOD is a brownout detector that outputs a HI logic value when the VBATT_BUCK voltage falls below a pre-defined voltage threshold. When the VBATT_BUCK voltage level is restored above a voltage threshold, the BOD output becomes a LO logic value.
- The counter creates a pulse that holds the chip in reset for 256*(64*T_2MHz) ~ 8.2ms

Figure 6-7 and Figure 6-8 illustrate the system block diagram and timing.

Table 6-5 shows the BOD thresholds.

Figure 6-7. ATBTLC1000 POR and BOD Block Diagram

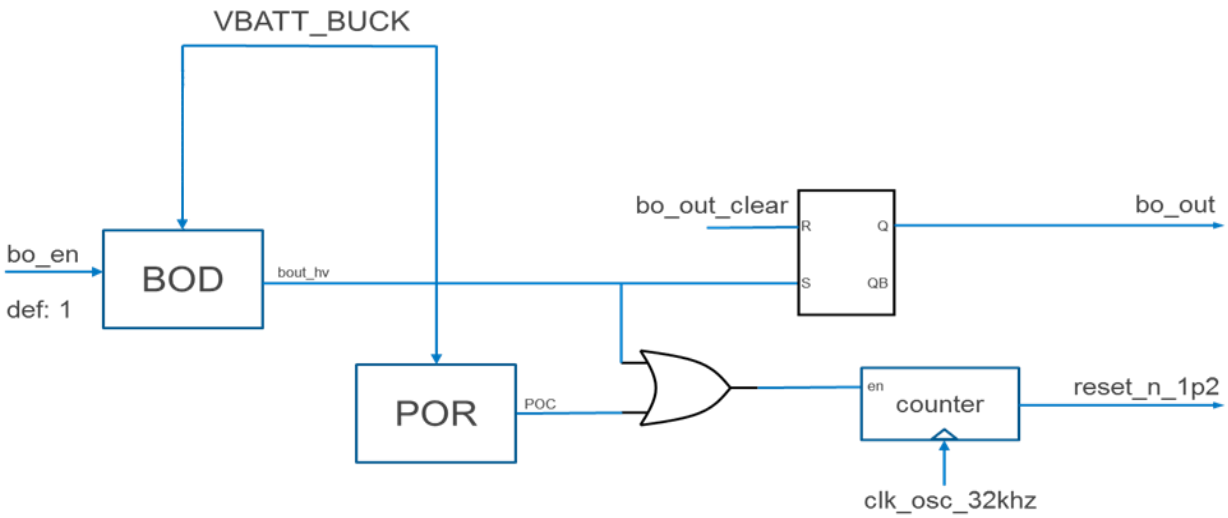


Figure 6-8. ATBTLC1000 POR and BOD Timing Sequence

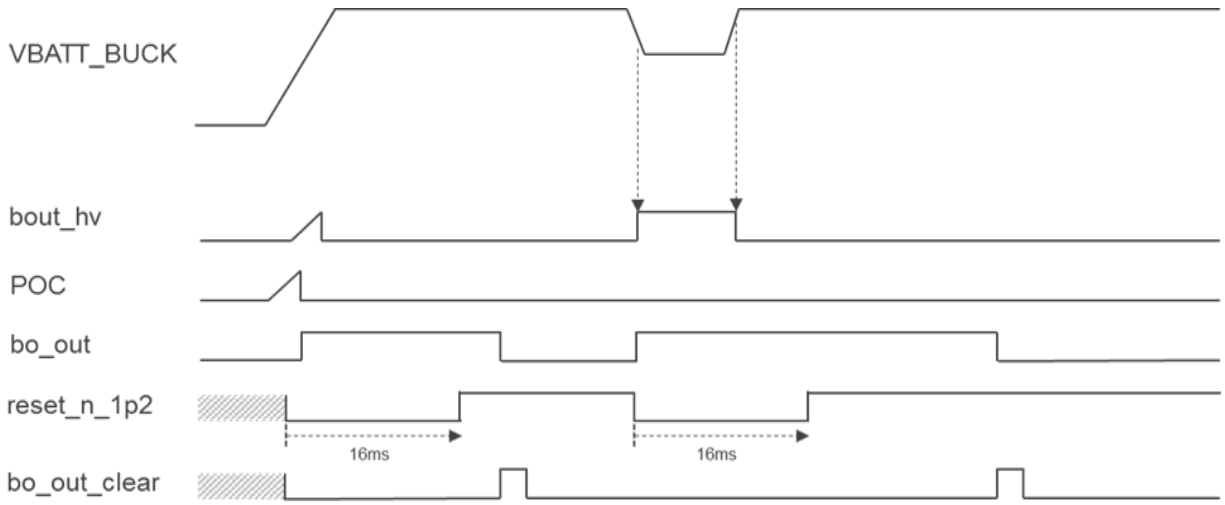


Table 6-5. ATBTLC1000 BOD Thresholds

Parameter	Min.	Typ.	Max.	Comment
BOD threshold	1.73V	1.80V	1.92V	
BOD threshold temperature coefficient		-1.09mV/C		
BOD current consumption		300nA		
t_{POR}		8.2ms		

7 Clocking

7.1 Overview

Figure 7-1. ATBTLC1000 Clock Architecture

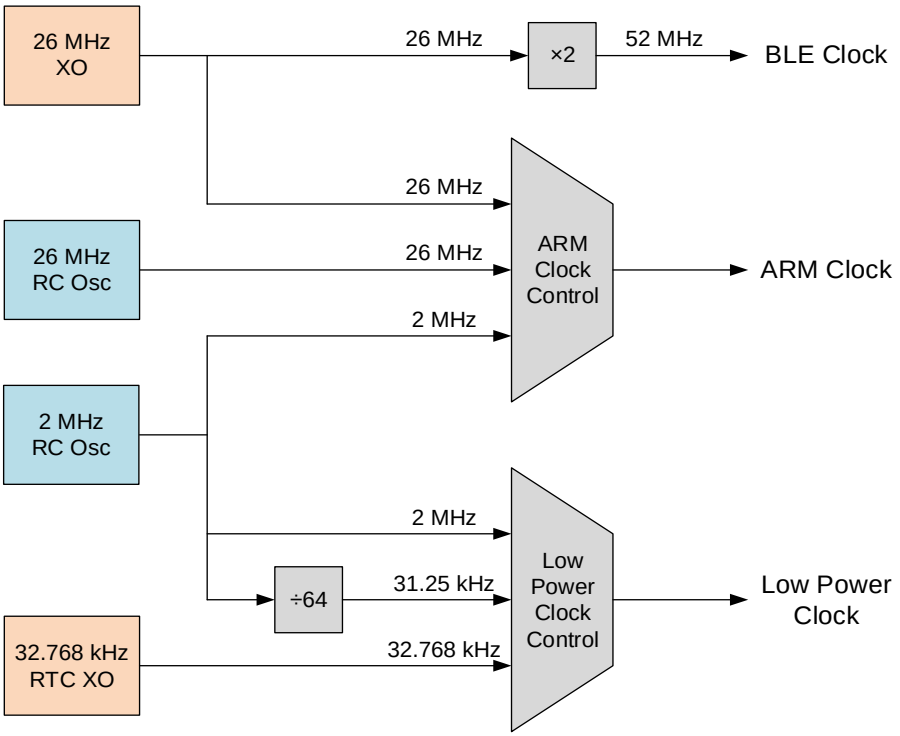


Figure 7-1 provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I²C); the nominal MCU clock speed is 26MHz. The Low Power Clock is used to drive all the low-power applications like BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26MHz Crystal Oscillator (XO) must be used for the BLE operations or in the event, a very accurate clock is required for the ARM subsystem operations.

The 26MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±40% over process, voltage, and temperature.

The 2MHz integrated RC Oscillator can be used as the Low Power Clock for applications that require fast wakeup of the ARM or for generating a ~31.25kHz clock for slower wakeup but lowest power in sleep mode. This 2MHz oscillator can also be used as the ARM Clock for low-power applications where the MCU needs to remain ON but run at a reduced clock speed. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The 32.768kHz RTC Crystal Oscillator (RTC XO) is recommended to be used for BLE operations (although optional) as it will reduce power consumption by providing the best timing for wakeup precision, allowing circuits to be in low-power sleep mode for as long as possible until they need to wake up and connect during the BLE connection event. The ~31.25kHz clock derived from the 2MHz integrated RC Oscillator can be used instead of RTC XO but it has low accuracy over process, voltage, and temperature variations (up to ±40%). Therefore, using the integrated RC Oscillator is NOT guaranteed to meet the ±500ppm BLE specification on sleep timing.

7.2 26MHz Crystal Oscillator (XO)

Table 7-1. ATBTLC1000 26MHz Crystal Oscillator Parameters

Parameter	Min.	Typ.	Max.	Units
Crystal Resonant Frequency	N/A	26	N/A	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability - Initial Offset (1)	-50		50	ppm
Stability - Temperature and Aging	-40		40	ppm

Note: 1. Initial offset must be calibrated to maintain ±25ppm in all operating conditions. This calibration is performed during final production testing and calibration offset values are stored in eFuse. More details are provided in the calibration application note.

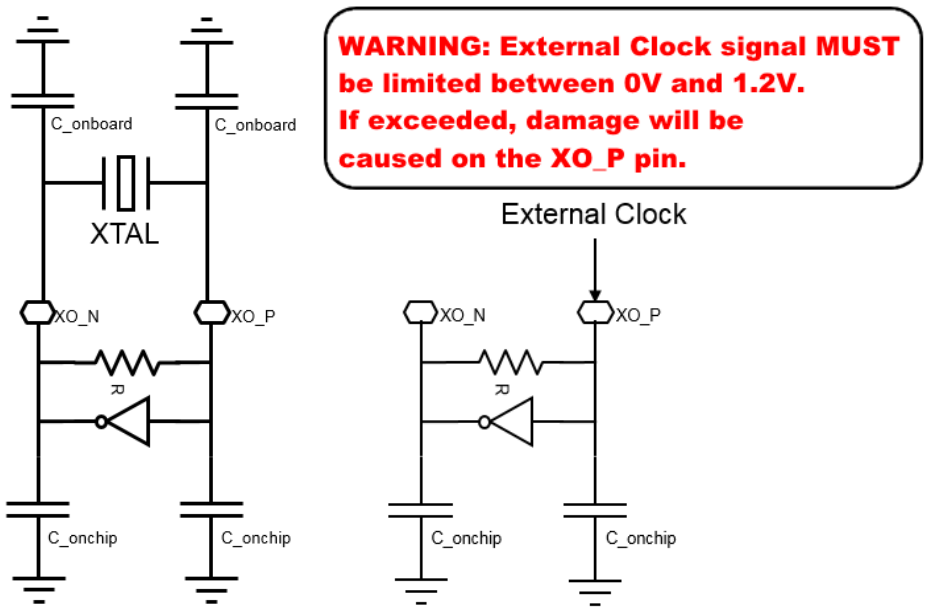
The block diagram in Figure 7-2 (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal.

The XO has up to 10pF internal capacitance on each terminal XO_P and XO_N (programmable in steps of 1.25pF). To bypass the crystal oscillator, an external Signal capable of driving 10pF can be applied to the XO_P terminal as shown in Figure 7-2 (b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.
When bypassing XO_P from an external clock, XO_N is required to be floating.

It is recommended that only crystals specified for CL=8pF be used in customer designs since this affects the sleep/wake up timing of the device. CL other than 8pF may require upgraded firmware and device re-characterization.

Figure 7-2. ATBTLC1000 Connections to XO



(a) Crystal oscillator is used (b) Crystal oscillator is bypassed

Table 7-2. ATBTLC1000 26MHz XTAL Cl_onchip Programming

Register	Cl_onchip	[pF]
rx_xo_regs[7,6,15] = 000	1.00	
rx_xo_regs[7,6,15] = 001	2.25	
rx_xo_regs[7,6,15] = 010	3.50	
rx_xo_regs[7,6,15] = 011	4.75	
rx_xo_regs[7,6,15] = 100	6.00	
rx_xo_regs[7,6,15] = 101	7.25	
rx_xo_regs[7,6,15] = 110	8.50	
rx_xo_regs[7,6,15]= 111	9.75	
If rx_reg7[1] = 1 add 5pF to above value		

Table 7-3 specifies the electrical and performance requirements for the external clock.

Table 7-3. ATBTLC1000 XO Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	26	26	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.75	1.2	V_{pp}	
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.3 32.768kHz RTC Crystal Oscillator (RTC XO)

7.3.1 General Information

ATBTLC1000 has a 32.768kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power sleep mode for as long as possible until they need to wake up for the next connection timed event.

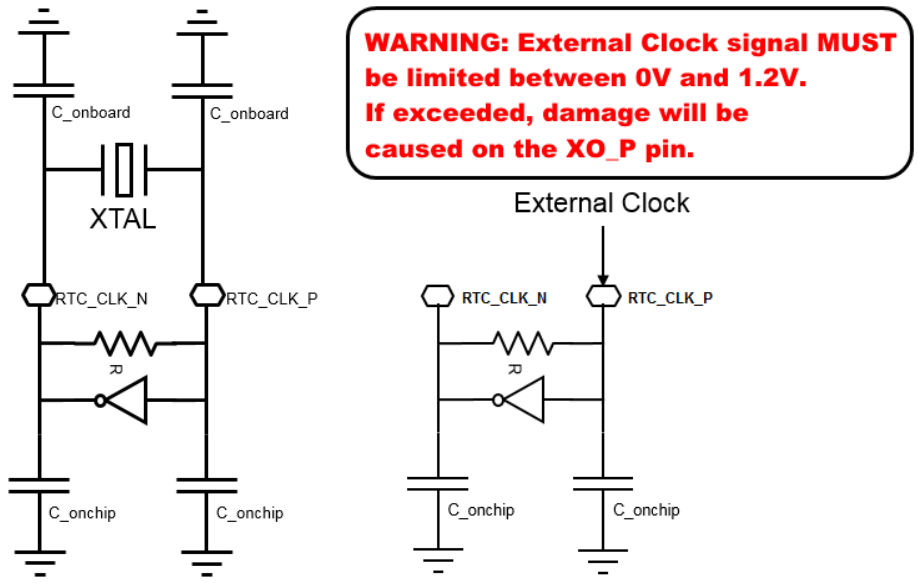
The block diagram in Figure 7-3(a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15pF on each terminal, RTC_CLK_P and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~1pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal as shown in Figure 7-3 (b).

The need for external bypass capacitors depends on the chosen crystal characteristics. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.

When bypassing RTC_CLK_P from an external clock, RTC_CLK_N is required to be floating.

Figure 7-3. ATBTLC1000 Connections to RTC XO



(a) Crystal oscillator is used (b) Crystal oscillator is bypassed

Table 7-4. 32.768kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	Cl_onchip	[pF]
0000	0.0	
0001	1.0	
0010	2.0	
0011	3.0	
0100	4.0	
0101	5.0	
0110	6.0	
0111	7.0	
1000	8.0	
1001	9.0	
1010	10.0	
1011	11.0	
1100	12.0	
1101	13.0	
1110	14.0	
1111	15.0	

7.3.2 RTC XO Design and Interface Specification

The RTC consists of two main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to maintain a phase shift of 360°C with the motional arm and keep total negative resistance to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with supply voltage of 1.2V.

Table 7-5. RTC XO Interface

Pin Name	Function	Register Default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20MΩ Feedback resistance 1 = 30MΩ Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700fF: 0000=700fF 1111=11.2pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt cap of 1.2pF 1000= for crystal with shunt cap >3pF	0X4000F404<19:16>="1000"
VDD_XO	1.2V	

7.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp. = 25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at supply voltage of 1.2V and temp. = 25°C.

Figure 7-4. RTC Drawn Current vs. Tuning Caps at 25°C

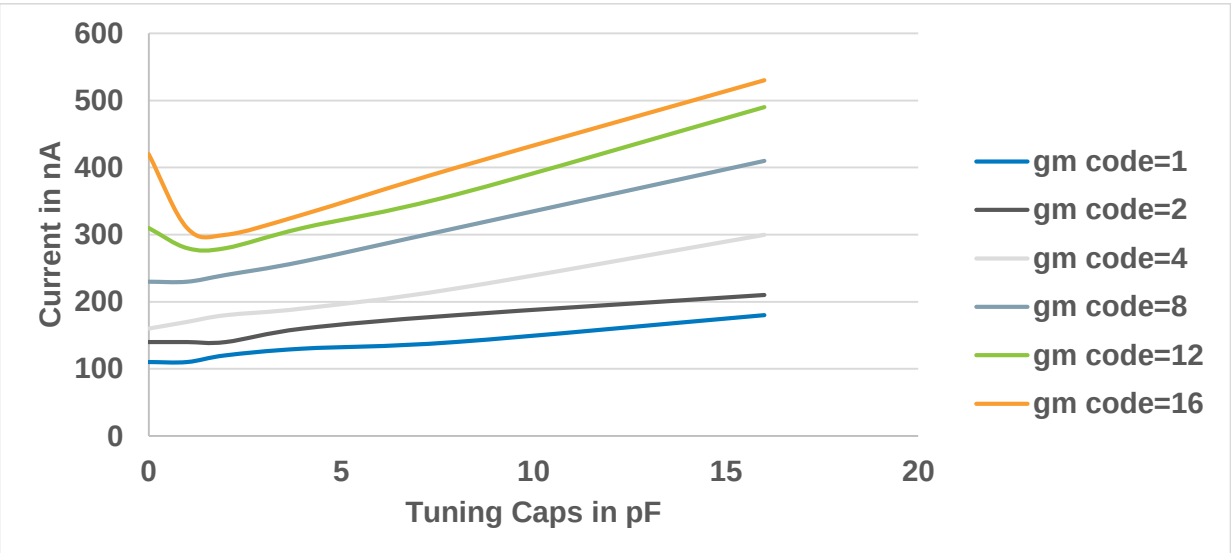
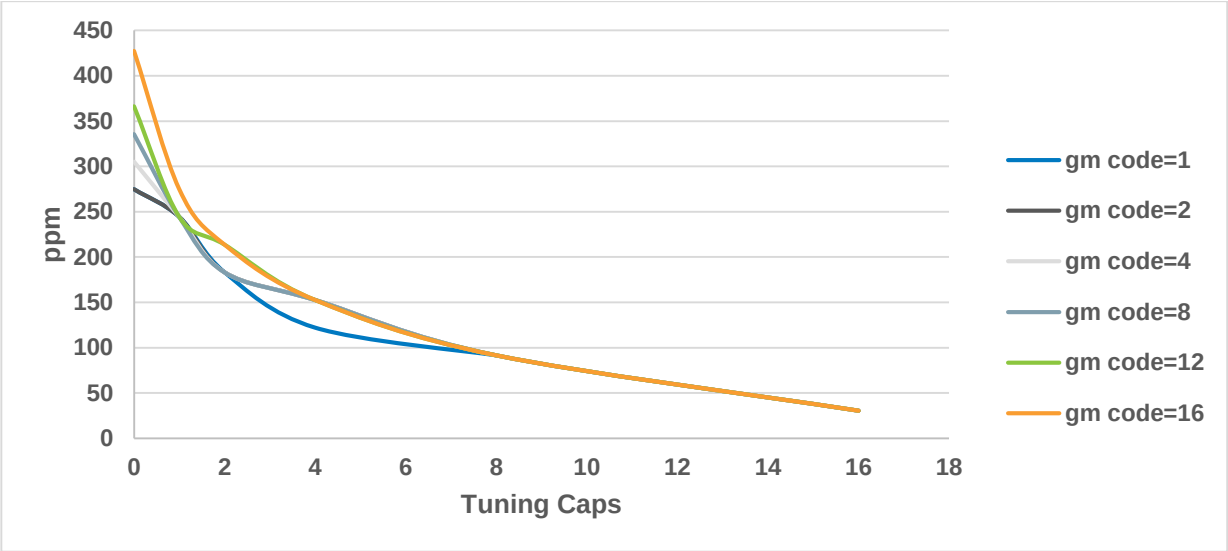


Figure 7-5. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



7.3.4 RTC Characterization with Supply Variation and Temp. = 25°C

Figure 7-6. RTC Drawn Current vs. Supply Variation

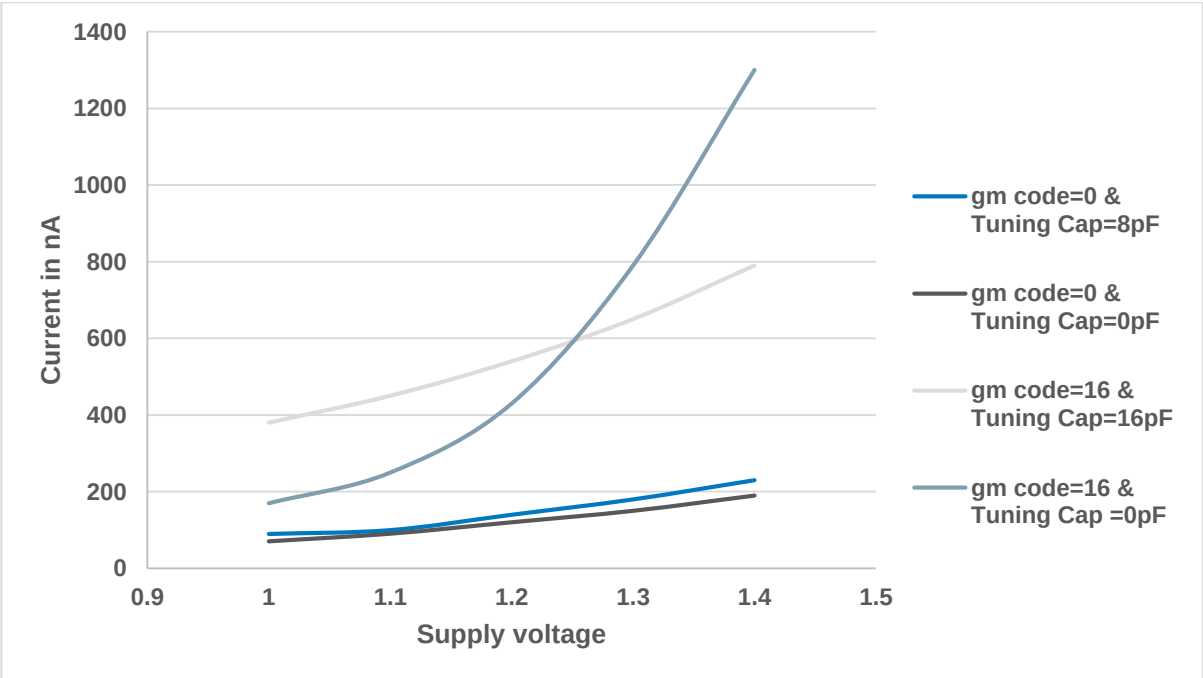
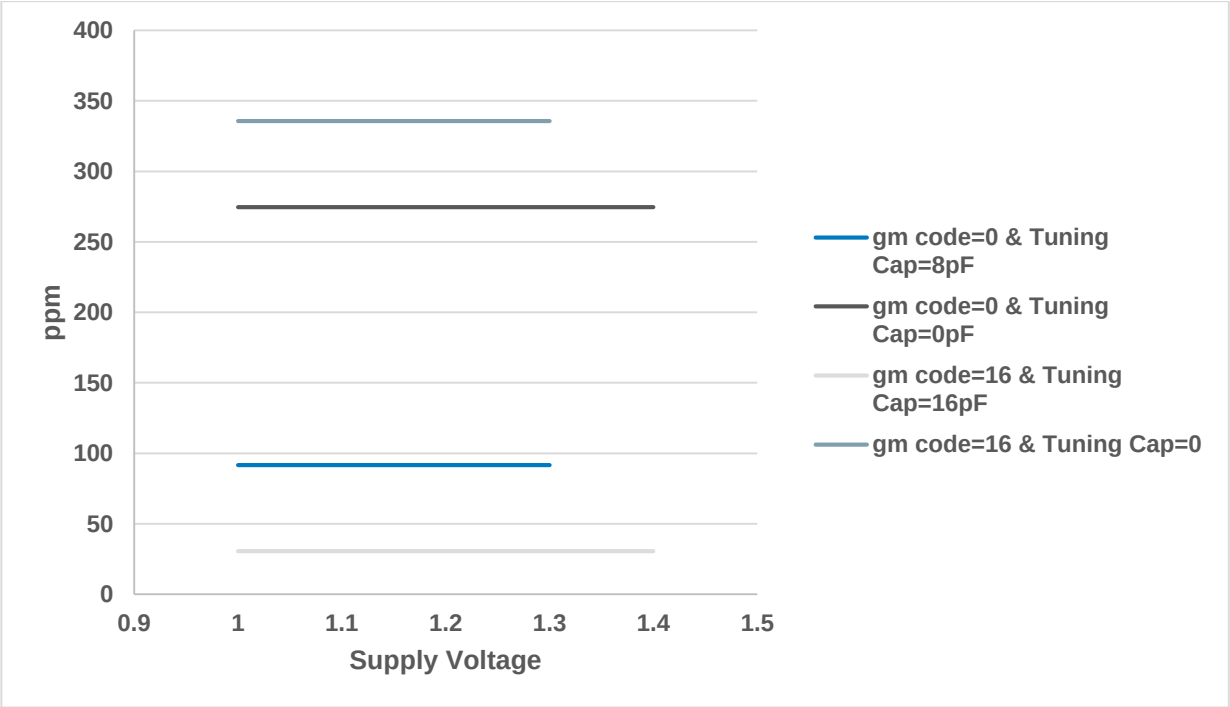


Figure 7-7. RTC Frequency Deviation vs. Supply Voltage



7.4 2MHz and 26MHz Integrated RC Oscillators

The 2MHz integrated RC Oscillator circuit without calibration has a frequency variation of 50% over process, temperature, and voltage variation. The ~31.25kHz clock is derived from the 2MHz clock by dividing by 64 and provides for lowest sleep power mode with a real-time clock running. As described above, calibration over process, temperature, and voltage is required to maintain the accuracy of this clock.

Figure 7-8. 32kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

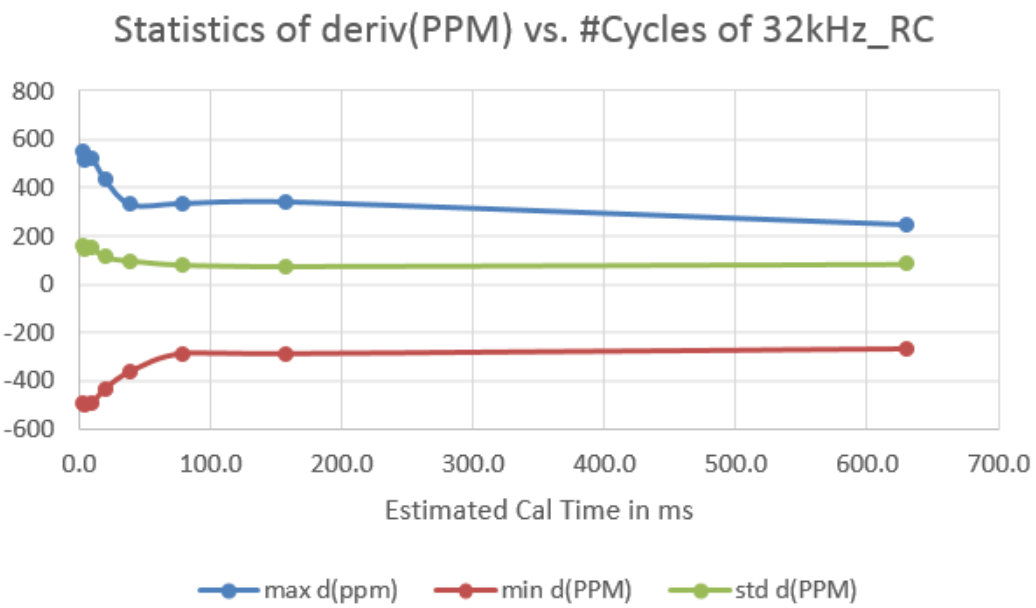
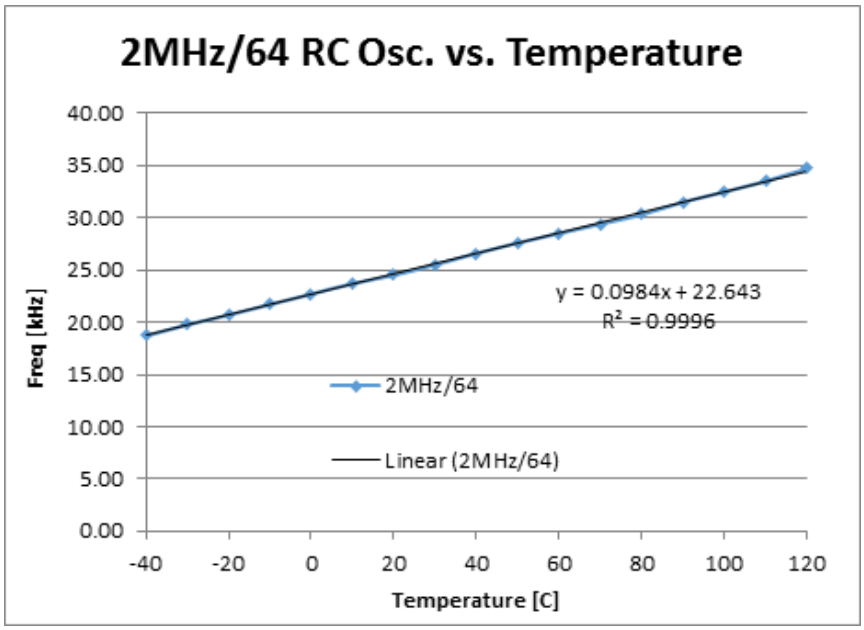


Figure 7-9. 32kHz RC Oscillator Frequency Variation over Temperature



The 26MHz integrated RC Oscillator circuit has a frequency variation of 50% over process, temperature, and voltage variation.

8 CPU and Memory Subsystem

8.1 ARM Subsystem

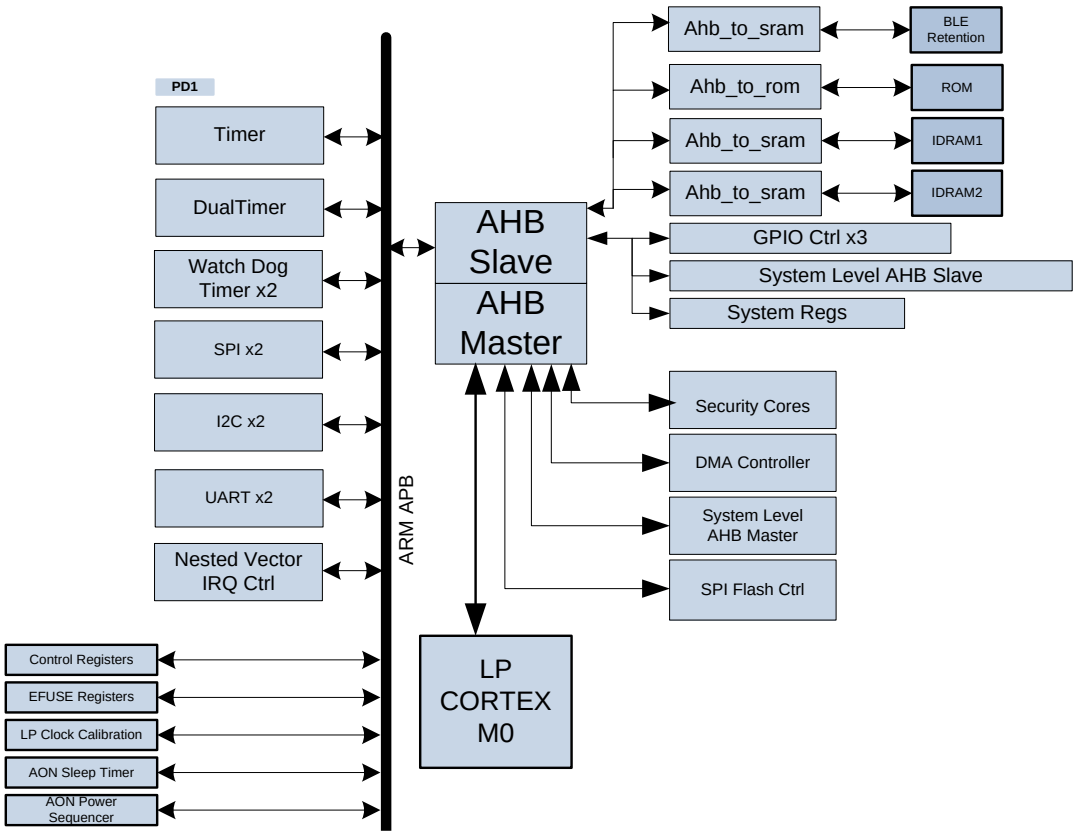
ATBTLC1000 has an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

The Cortex-M0 Microcontroller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC-like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution, with four hardware breakpoint and two watch point options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

Figure 8-1. ATBTLC1000 ARM Cortex-M0 Subsystem



8.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic, high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

8.1.2 Module Descriptions

8.1.2.1 Timer

The 32-bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation, and time tracking.

8.1.2.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in a Free-running, Periodic, or One-shot mode.

8.1.2.3 Watchdog

The two watchdog blocks allow the CPU to be interrupted if it has not interacted with the watchdog timer before it expires. In addition, this interrupt will be an output of the core so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This will allow the CPU to get back to a known state in the event a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

8.1.2.4 Wake up Timer

This timer is a 32-bit count-down timer that operates on the 32kHz sleep clock. It can be used as a general purpose timer for the ARM or as a wakeup source for the chip. It has the ability to be a onetime programmable timer, as it will generate an interrupt/wakeup on expiration and stop operation. It also has the ability to be programmed in an auto reload fashion where it will generate an interrupt/wakeup and then proceed to start another count down sequence.

8.1.2.5 SPI Controller

See Section 10.3.

8.1.2.6 I^2C Controller

See Section 10.2.

8.1.2.7 SPI-Flash Controller

The AHB SPI-Flash Controller is used to access an external SPI Flash device to access various instruction/data code needed for storing application code, code patches, and OTA images. Supports several SPI modes including 0, 1, 2, and 3. See Section 10.4.

8.1.2.8 UART

See Section 10.5.

8.1.2.9 DMA Controller

Direct Memory Access (DMA) allows certain hardware subsystems to access main system memory independently of the Cortex-M0 Processor.

The DMA features and benefits are:

- Supports any address alignment
- Supports any buffer size alignment
- Peripheral flow control, including peripheral block transfer
- The following modes are supported:
  - Peripheral to peripheral transfer
  - Memory to memory
  - Memory to peripheral
  - Peripheral to memory
  - Register to memory

- Interrupts for both TX done and RX done in memory and peripheral mode
- Scheduled transfers
- Endianness byte swapping
- Watchdog timer
- 4-channel operation
- 32-bit Data width
- AHB MUX (on read and write buses)
- Command lists support
- Usage of tokens

8.1.2.10 Nested Vector Interrupt Controller

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little-endian. Any attempt to read or write a half-word or byte individually is unpredictable.

The NVIC allows the CPU to be able to individually enable, disable each interrupt source, and hold each interrupt until it has been serviced and cleared by the CPU.

Table 8-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

For a description of each register, see the Cortex-M0 documentation from ARM.

8.1.2.11 GPIO Controller

The AHB GPIO is a general-purpose I/O interface unit allowing the CPU to independently control all input or output signals on ATBTLC1000. These can be used for a wide variety of functions pertaining to the application.

The AHB GPIO provides a 16-bit I/O interface with the following features:

- Programmable interrupt generation capability
- Programmable masking support
- Thread safe operation by providing separate set and clear addresses for control registers
- Inputs are sampled using a double flip-flop to avoid meta-stability issues

8.2 Memory Subsystem

The Cortex-M0 core uses a 128KB instruction/boot ROM along with a 128KB shared instruction and data RAM.

8.2.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data used by the ARM. The size of IDRAM1 and IDRAM2 is 128KB that can be used for BLE subsystem as well as for the user application. IDRAM1 contains three 32KB and IDRAM2 contains two 16KB memories that are accessible to the ARM and used for instruction/data storage.

8.2.2 ROM

The ROM is used to store the boot code and BLE firmware, stack and selected user profiles. ROM contains the 128KB memory that is accessible to the ARM.

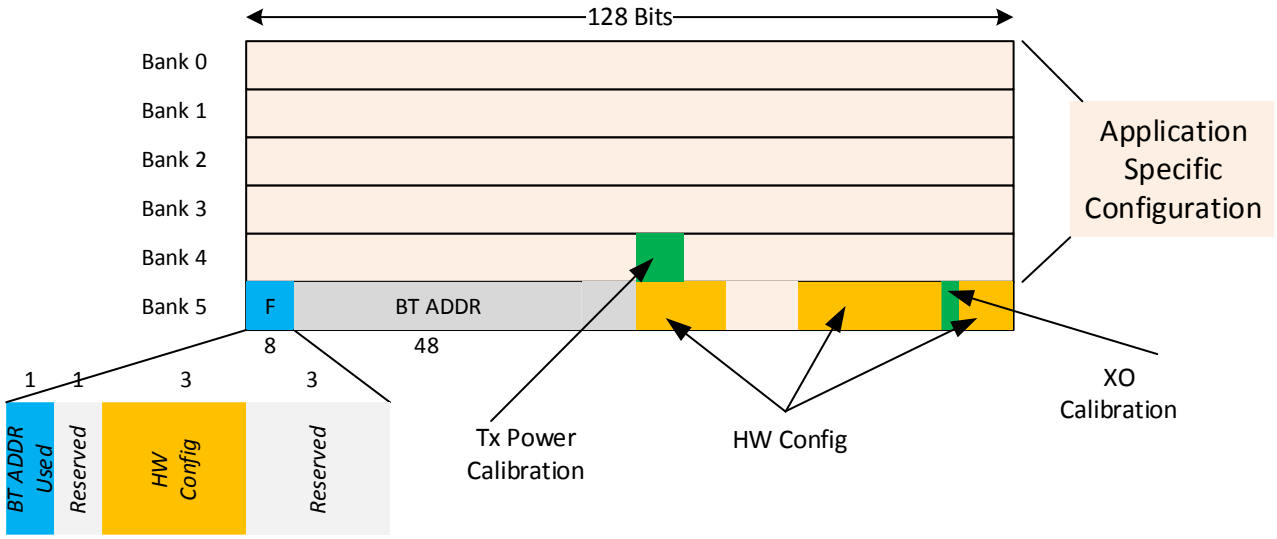
8.2.3 BLE Retention Memory

The BLE functionality requires 8KB (or more depending on the application) state, instruction, and data to be retained in memory when the processor either goes into Sleep Mode or Power Off Mode. The RAM is separated into specific power domains to allow tradeoff in power consumption with retention memory size.

8.3 Non-Volatile Memory

ATBTLC1000 has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable memory can be used to store customer-specific parameters, such as BLE address, XO calibration information, TX power, and crystal frequency offset, as well as other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bitmap of the first bank is shown in Figure 8-2. The purpose of the first 80 bits in bank 0 is fixed, and the remaining bits are general-purpose software dependent bits, or reserved for future use. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating BLE address (this can be done by invalidating the last programmed bank and programming a new bank). Refer to ATBTLC1000 Programming Guide for the eFuse programming instructions.

Figure 8-2. ATBTLC1000 eFuse Bit Map



9 Bluetooth Low Energy (BLE) Subsystem

The BLE subsystem implements all the critical real-time functions required for full compliance with Specification of the Bluetooth System, v4.1, Bluetooth SIG.

It consists of a Bluetooth 4.1 baseband controller (core), radio transceiver and the Atmel Bluetooth Smart Stack, the BLE Software Platform.

9.1 BLE Core

The baseband controller consists of modem and Medium Access Controller (MAC) and it encodes and decodes HCI packets, constructs baseband data packages, schedules frames, and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control.

The core performs Link Control Layer management supporting the main BLE states, including advertising and connection.

9.1.1 Features

- Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation, connect up to eight slaves
- Frequency Hopping
- Advertising/Data/Control packet types
- Encryption (AES-128, SHA-256)
- Bit stream processing (CRC, whitening)
- Operating clock 52MHz

9.2 BLE Radio

The radio consists of a fully integrated transceiver, including Low Noise Amplifier, Receive (RX) down converter, and analog baseband processing as well as Phase Locked Loop (PLL), Transmit (TX) Power Amplifier, and Transmit/Receive switch. At the RF front end, no external RF components on the PCB are required other than the antenna and a matching component.

The RX sensitivity and TX output power of the radio together with the 4.1 PHY core provide a 100dB RF link budget for superior range and link reliability.

9.2.1 Receiver Performance

Table 9-1. ATBTLC1000 BLE Receiver Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Sensitivity with external 1.2V		-96		dBm
Sensitivity with on-chip DC/DC		-95		
Maximum receive signal level		+5		
CCI		12.5		dB
ACI (N±1)		0		
N+2 Blocker (Image)		-22		
N-2 Blocker		-38		
N+3 Blocker (Adj. Image)		-35		

Parameter	Minimum	Typical	Maximum	Unit
N-3 Blocker		-43		
N±4 or greater		-45		dB
Intermod (N+3, N+6)		-32		
OOB (2GHz<f<2.399GHz)	-15			dBm
OOB (f<2GHz or f>2.5GHz)	-10			
RX peak current draw		4.00 (1)		mA

Note: 1. At -93dBm sensitivity setting. Add 0.2mA at 3.6V for best sensitivity setting.

All measurements performed at 3.6V VBATT and 25°C, with tests following the Bluetooth V4.1 standard tests.

There are two gain settings for Sensitivity, high gain (-95dBm) and low gain (-93dBm). Low gain has lower current consumption.

9.2.2 Transmitter Performance

The transmitter has fine step power control with P_{out} variable in <3dB steps below 0dBm and in <0.5dB steps above 0dBm.

Table 9-2. ATBTLC1000 BLE Transmitter Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Output power range	-20	0	3.5	
Maximum output power		3.5		
In-band Spurious (N±2)		-45		
In-band Spurious (N±3)		-50		
2nd harmonic P_{out}	-41			dBm
3rd harmonic P_{out}	-41			
4th harmonic P_{out}	-41			
5th harmonic P_{out}	-41			
Frequency deviation		±250		kHz
TX peak current draw		3.0 (1)		mA

Note: 1. At 0dBm TX output power.

All measurements performed at 3.6V VBATT and 25°C, with tests following the Bluetooth V4.1 standard tests.

9.3 Atmel Bluetooth SmartConnect Stack

The ATBTLC1000 has a completely integrated Bluetooth Low Energy stack on chip, fully qualified, mature, and Bluetooth V4.1 compliant.

Customer applications interface with the BLE protocol stack through the Atmel BLE API, which supports direct access to the GAP, SMP, ATT, GATT client / server, and L2CAP service layer protocols in the embedded firmware.

The stack includes numerous BLE profiles for applications like:

- Smart Energy
- Consumer Wellness

- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Automotive

Together with the Atmel Studio Software Development environment, additional customer profiles can be easily developed.

The Atmel Bluetooth SmartConnect software development kit is based on Keil and IAR™ compiler tools and contains numerous application code examples for embedded and hosted modes.

In addition to the protocol stack, drivers for each peripheral hardware block are provided.

10 External Interfaces

10.1 Overview

ATBTLC1000 external interfaces include: 2xSPI Master/Slave (SPI0 and SPI1), 2xI²C Master/Slave (I²C0 and I²C1), 1xI²C Slave-only (I²C2), 2xUART (UART1 and UART2), 1xSPI Flash, 1xSWD, and General Purpose Input/Output (GPIO) pins. For specific programming instructions, refer to the ATBTLC1000 Programming Guide.

Table 10-1 illustrates the different peripheral functions that are software selectable for each pin. This allows for maximum flexibility of mapping desired interfaces on GPIO pins. MUX1 option allows for any MEGAMUX option from Table 10-2 to be assigned to a GPIO.

Table 10-1. ATBTLC1000 Pin-MUX Matrix of External Interfaces

Pin Name	Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_0	4	Up	GPIO 0	MEGAMUX 0	SWD CLK					TEST OUT 0
LP_GPIO_1	5	Up	GPIO 1	MEGAMUX 1	SWD I/O					TEST OUT 1
LP_GPIO_2	6	Up	GPIO 2	MEGAMUX 2	UART1 RXD		SPI1 SCK	SPI0 SCK	SPI FLASH SCK	TEST OUT 2
LP_GPIO_3	7	Up	GPIO 3	MEGAMUX 3	UART1 TXD		SPI1 MOSI	SPI0 MOSI	SPI FLASH TXD	TEST OUT 3
LP_GPIO_8	8	Up	GPIO 8	MEGAMUX 8	I²C0 SDA	I²C2 SDA		SPI0 SSN	SPI FLASH SSN	TEST OUT 8
LP_GPIO_9	9	Up	GPIO 9	MEGAMUX 9	I²C0 SCL	I²C2 SCL		SPI0 MISO	SPI FLASH RXD	TEST OUT 9
LP_GPIO_10	10	Up	GPIO 10	MEGAMUX 10	SPI0 SCK				SPI FLASH SCK	TEST OUT 10
LP_GPIO_11	11	Up	GPIO 11	MEGAMUX 11	SPI0 MOSI				SPI FLASH TXD	TEST OUT 11
LP_GPIO_12	12	Up	GPIO 12	MEGAMUX 12	SPI0 SSN				SPI FLASH SSN	TEST OUT 12
LP_GPIO_13	13	Up	GPIO 13	MEGAMUX 13	SPI0 MISO				SPI FLASH RXD	TEST OUT 13
LP_GPIO_16	25	Up	GPIO 16	MEGAMUX 16	SPI FLASH SCK		SPI1 SSN	SPI0 SCK	SPI FLASH SSN	TEST OUT 16
LP_GPIO_18	27	Up	GPIO 18	MEGAMUX 18	SPI FLASH SSN	I²C2 SCL	SPI1 MISO	SPI0 SSN	SPI FLASH RXD	TEST OUT 18
AO_GPIO_0	24	Up	GPIO 31	WAKEUP	RTC CLK IN	32KHZ CLK OUT				
GPIO_MS1	17	Up	GPIO 47							
GPIO_MS2	18	Up	GPIO 46							

Table 10-2 shows the various software selectable MEGAMUX options that correspond to specific peripheral functionality. Several MEGAMUX options provide an interface to manage Wi-Fi® BLE coexistence.

Table 10-2. ATBTLC1000 Software Selectable MEGAMUX Options

MUX_Sel	Function	Notes
0	UART1 RXD	
1	UART1 TXD	
2	UART1 CTS	
3	UART1 RTS	
4	UART2 RXD	
5	UART2 TXD	
6	UART2 CTS	
7	UART2 RTS	
8	I²C0 SDA	
9	I²C0 SCL	

MUX_Sel	Function	Notes
10	I²C1 SDA	
11	I²C1 SCL	
12	PWM 1	
13	PWM 2	
14	PWM 3	
15	PWM 4	
16	LP CLOCK OUT	32kHz clock output (RC Osc. or RTC XO)
17	WLAN TX ACTIVE	Coexistence: Wi-Fi is currently transmitting
18	WLAN RX ACTIVE	Coexistence: Wi-Fi is currently receiving
19	BLE TX ACTIVE	Coexistence: BLE is currently transmitting
20	BLE RX ACTIVE	Coexistence: BLE is currently receiving
21	BLE IN PROCESS	Coexistence Signal
22	BLE MBSY	Coexistence Signal
23	BLE SYNC	Coexistence Signal
24	BLE RXNTX	Coexistence Signal
25	BLE PTI 0	Coexistence: BLE Priority
26	BLE PTI 1	Coexistence: BLE Priority
27	BLE PTI 2	Coexistence: BLE Priority
28	BLE PTI 3	Coexistence: BLE Priority
29	QUAD DEC X IN A	
30	QUAD DEC X IN B	
31	QUAD DEC Y IN A	
32	QUAD DEC Y IN B	
33	QUAD DEC Z IN A	
34	QUAD DEC Z IN B	

An example of peripheral assignment using these MEGAMUX options is as follows:

- I²C0 pin-MUXed on LP_GPIO_8 and LP_GPIO_9 via MUX1 and MEGAMUX=8 and 9 (Table 10-2)
- I²C1 pin-MUXed on LP_GPIO_0 and LP_GPIO_1 via MUX1 and MEGAMUX=10 and 11 (Table 10-2)
- PWM pin-MUXed on LP_GPIO_16 via MUX1 and MEGAMUX=12 (Table 10-2)

Another example is to illustrate the available options for pin LP_GPIO_3, depending on the pin-MUX option selected:

- MUX0: the pin will function as bit 3 of the GPIO bus and is controlled by the GPIO controller in the ARM subsystem
- MUX1: any option from the MEGAMUX table can be selected, for example it can be a quad_dec, pwm, or any of the other functions listed in the MEGAMUX table
- MUX2: the pin will function as UART1 TXD; this can be also achieved with the MUX1 option via MEGAMUX, but the MUX2 option allows a shortcut for the recommended pinout

- MUX3: this option is not used and thus defaults to the GPIO option (same as MUX0)
- MUX4: the pin will function as SPI1 MOSI (this option is not available through MEGAMUX)
- MUX5: the pin will function as SPI0 MOSI (this option is not available through MEGAMUX)
- MUX6: the pin will function as SPI FLASH SCK (this option is not available through MEGAMUX)
- MUX7: the pin will function as bit 3 of the test output bus, giving access to various debug signals

10.2 I²C Master/Slave Interface

10.2.1 Description

ATBTLC1000 provides I²C Interface that can be configured as Slave or Master. I²C Interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). ATBTLC1000 I²C supports I²C bus Version 2.1 - 2000 and can operate in the following speed modes:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Ver2.1”.

10.2.2 I²C Interface Timing

The I²C Interface timing (common to Slave and Master) is provided in Figure 10-1. The timing parameters for Slave and Master modes are specified in Table 10-3 and Table 10-4 respectively.

Figure 10-1. ATBTLC1000 I²C Slave Timing Diagram

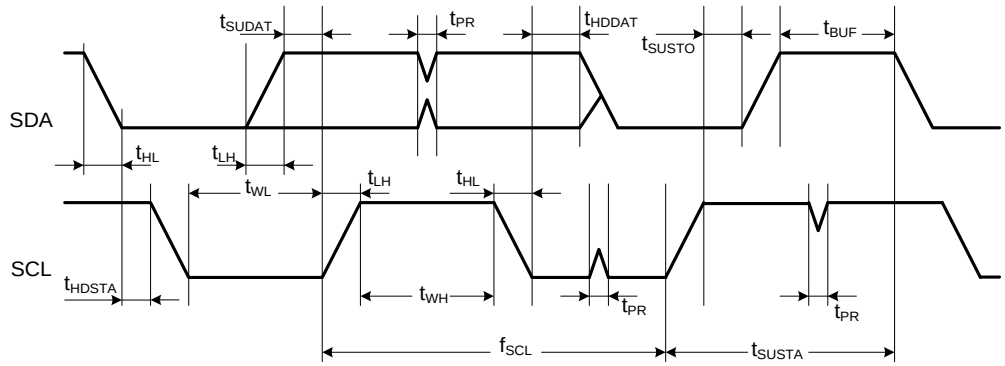


Table 10-3. ATBTLC1000 I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components

Parameter	Symbol	Min.	Max.	Units	Remarks
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

Table 10-4. ATBTLC1000 I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

10.3 SPI Master/Slave Interface

10.3.1 Description

ATBTLC1000 provides a Serial Peripheral Interface (SPI) that can be configured as Master or Slave. The SPI Interface pins are mapped as shown in Table 10-5. The SPI Interface is a full-duplex slave-synchronous serial interface. When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line. The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions, refer to ATBTLC1000 Programming Guide.

Table 10-5. ATBTLC1000 SPI Interface Pin Mapping

Pin Name	SPI Function
SSN	Active Low Slave Select
SCK	Serial Clock
MOSI	Master Out Slave In (Data)
MISO	Master In Slave Out (Data)

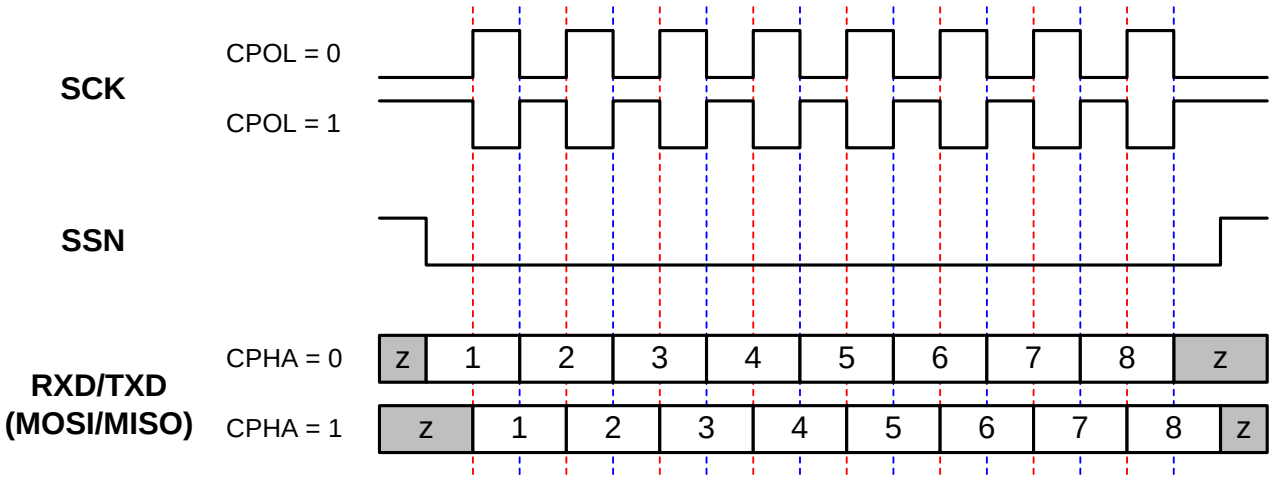
10.3.2 SPI Interface Modes

The SPI Interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 10-6 and Figure 10-2. The red lines in Figure 10-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 10-6. ATBTLC1000 SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 10-2. ATBTLC1000 SPI Clock Polarity and Clock Phase Timing



10.3.3 SPI Slave Timing

The SPI Slave timing is provided in Figure 10-3 and Table 10-7.

Figure 10-3. ATBTLC1000 SPI Slave Timing Diagram

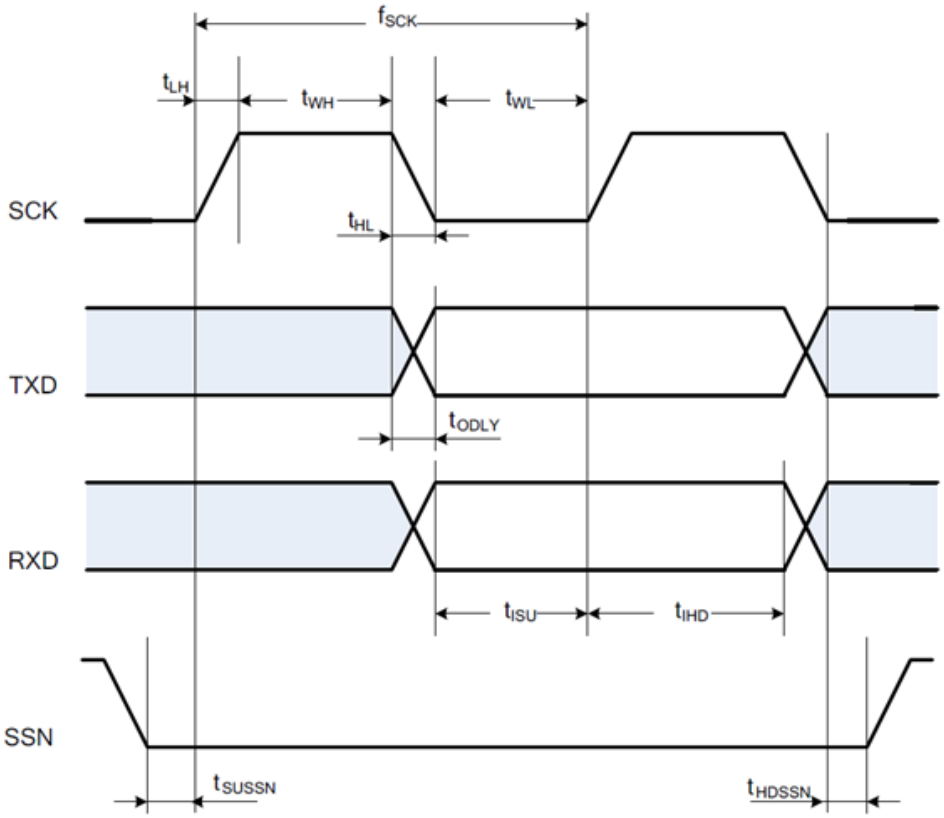


Table 10-7. ATBTLC1000 SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency	f_{SCK}		2	MHz
Clock Low Pulse Width	t_{WL}	240		ns
Clock High Pulse Width	t_{WH}	240		
Clock Rise Time	t_{LH}		10	
Clock Fall Time	t_{HL}		10	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	20	
Slave Select Setup Time	t_{SUSSN}	5		
Slave Select Hold Time	t_{HDSSN}	5		

10.3.4 SPI Master Timing

The SPI Master Timing is provided in Figure 10-4 and Table 10-8.

Figure 10-4. ATBTLC1000 SPI Master Timing Diagram

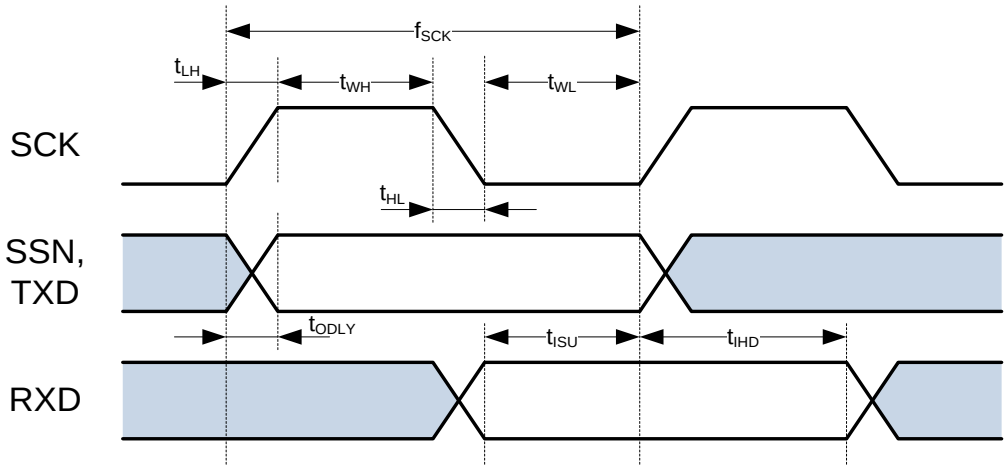


Table 10-8. ATBTLC1000 SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency	f_{SCK}		4	MHz
Clock Low Pulse Width	t_{WL}	120		ns
Clock High Pulse Width	t_{WH}	120		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	5	

10.4 SPI Flash Master Interface

10.4.1 Description

ATBTLC1000 provides an SPI Master interface for accessing external Flash memory. The TXD pin is the same as the Master Output, Slave Input (MOSI), and the RXD pin is the same as the Master Input, Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase shown in Table 10-6. External SPI Flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates an SPI master access to the Flash. Refer to the ATBTLC1000 Programming Guide for more specific instructions.

10.4.2 SPI Master Timing

The SPI Master Timing is provided in Figure 10-5 and Table 10-9.

Figure 10-5. ATBTLC1000 SPI Master Timing Diagram

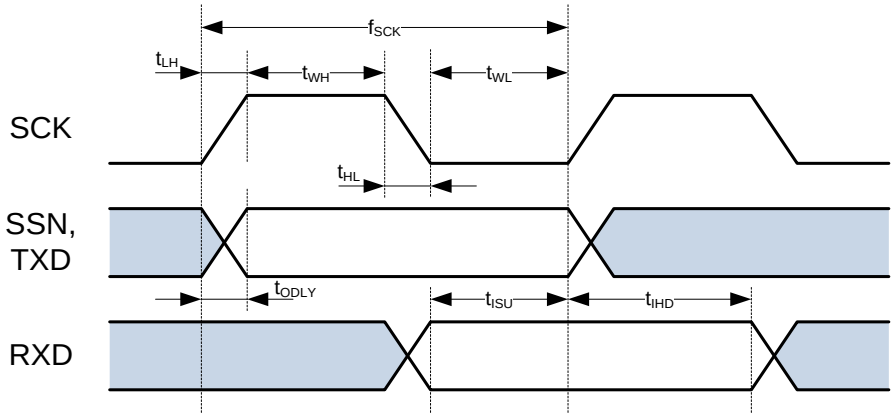


Table 10-9. ATBTLC1000 SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency	f_{SCK}		13	MHz
Clock Low Pulse Width	t_{WL}	33		ns
Clock High Pulse Width	t_{WH}	33		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	5	

10.5 UART Interface

ATBTLC1000 provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem has two UART interfaces: a 4-pin interface for control and data transfer. The UART interfaces are compatible with the RS-232 standard, where ATBTLC1000 operates as Data Terminal Equipment (DTE). The 4-pin UART has two pins for data (TX and RX) and two pins for flow control/handshaking: Request To Send (RTS) and Clear To Send (CTS**). The RTS and CTS are used for hardware flow control; they MUST be connected to the host MCU UART and enabled for the UART interface to be functional.** The pins associated with each the UART interfaces can be enabled on several alternative pins by programming their corresponding pin-MUX control registers (see Table 10-1 and Table 10-2 for available options).

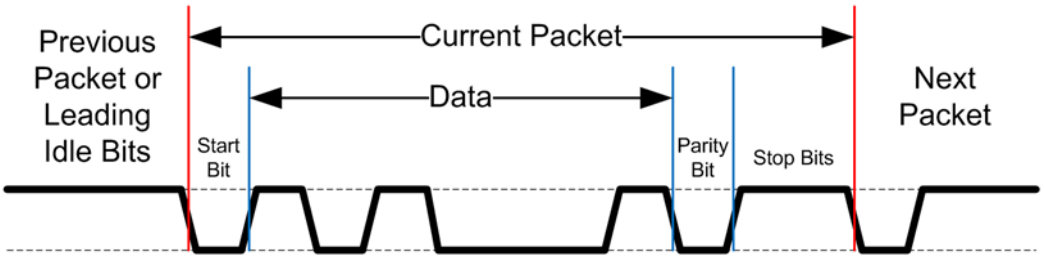
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 26MHz, 13MHz, 6.5MHz, and 3.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 26MHz/8.0 = 3.25MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 10-6. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Refer to the ATBTLC1000 Programming Guide for more specific instructions.

Figure 10-6. Example of UART RX or TX Packet



10.6 GPIOs

15 General Purpose Input/Output (GPIO) pins total, labeled LP_GPIO, GPIO_MS, and AO_GPIO, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output. The host or internal processor can program the output values.

LP_GPIO are digital interface pins, GPIO_MS are mixed signal/analog interface pins and AO_GPIO is an always-on digital interface pin that can detect interrupt signals while in deep sleep mode for wake-up purposes.

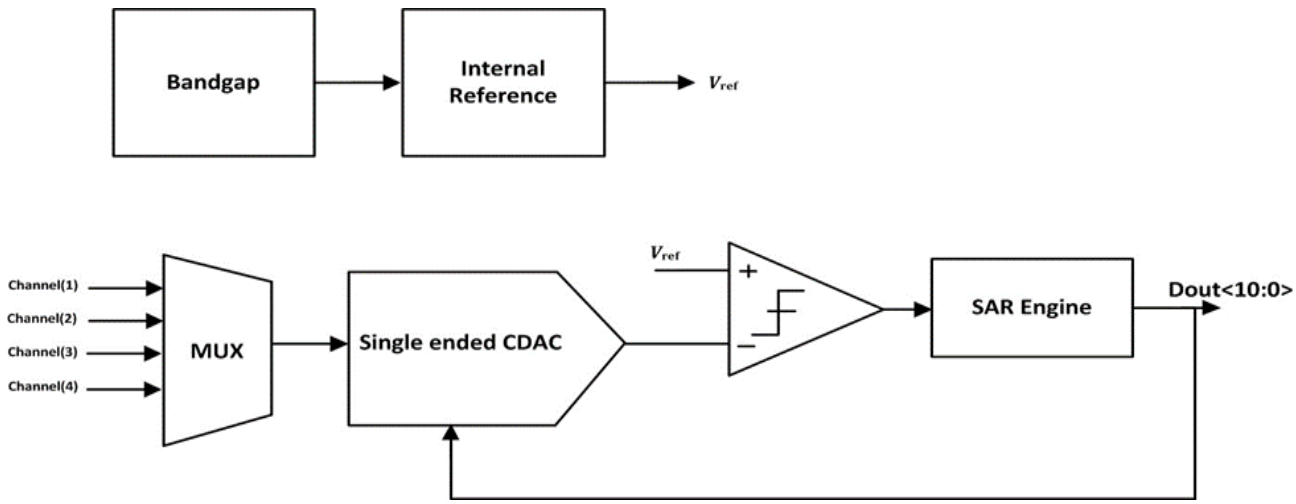
The LP_GPIO have interrupt capability, but only when in active/standby mode. In sleep mode they are turned off to save power consumption.

10.7 Analog to Digital Converter (ADC)

10.7.1 Overview

The ATBTLC1000 has an integrated Successive Approximation Register (SAR) ADC with 11-bit resolution and variable conversion speed up 1MS/s. The key building blocks are the capacitive DAC, comparator, and synchronous SAR engine as shown in Figure 10-7.

Figure 10-7. ATBTLC1000 SAR ADC Block Diagram



The ADC reference voltage can be either generated internally or set externally via one of the two available Mixed Signal GPIO pins on the ATBTLC1000.

There are two modes of operation:

A. High resolution (11-bit): Set the reference voltage to half the supply voltage or below. In this condition the input signal dynamic range is equal to twice the reference voltage (ENOB=10bit).

B. Medium Resolution (10-bit) : Set the reference voltage to any value below supply voltage (up to supply voltage - 300mV) and in this condition the input dynamic range is from zero to reference voltage (ENOB = 9bit).

Four input channels are time multiplexed to the input of the SAR ADC. However, on the ATBTLC1000, only two channel inputs are accessible from the outside, through pins 17 and 18 (Mixed Signal GPIO pins).

In power saving mode, the internal reference voltage is completely off and the reference voltage is set externally.

The ADC characteristics are summarized in Table 10-10.

Table 10-10. SAR ADC Characteristics

Conversion rate	1ks → 1MS
Selectable Resolution	10 → 11bit
Power consumption	13.5µA (at 100KS/s) (1)

Note: 1. With external reference.

10.7.2 Timing

The ADC timing is shown in Figure 10-8. The input signal is sampled twice, in the first sampling cycle the input range is defined either to be above reference voltage or below it and in the second sampling instant the ADC start its normal operation.

The ADC takes two sampling instants and N-1 conversion cycle (N=ADC resolution) and one cycle to sample the data out. Therefore, for 11-bit resolution it takes 13 clock cycles to do one Sample conversion.

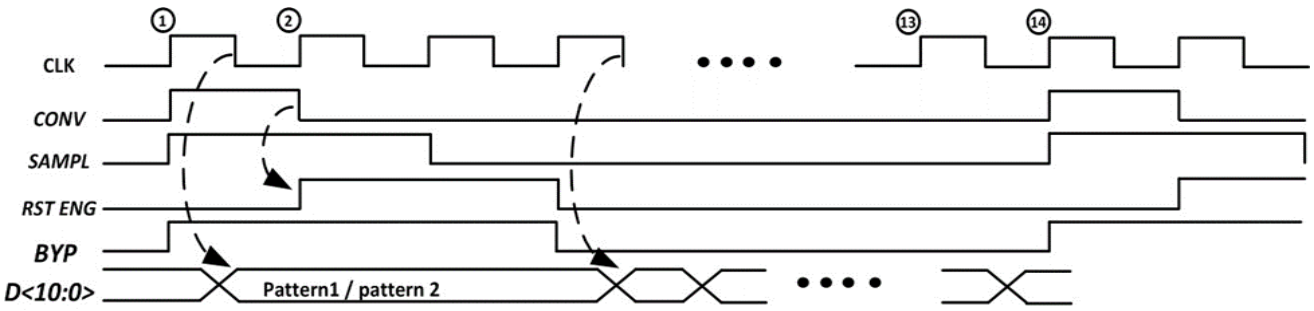
The Input clock equals N+2 the sampling clock frequency (N is the ADC resolution).

CONV signal : Gives indication about end of conversion.

SAMPL : The input signal is sampled when this signal is high.

RST ENG : When High SAR Engine is in reset mode (SAR engine output is set to mid-scale).

Figure 10-8. SAR ADC Timing



10.7.3 Performance

Table 10-11. Static Performance of SAR ADC

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0		VBAT	V
Resolution			11		bits
Sample rate			100	1000	KSPS
Input offset	Internal VREF	-10		+10	mV
Gain error	Internal VREF	-4		+4	%
DNL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-0.75		+1.75	LSB
INL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-2		+2.5	LSB
THD	1kHz sine input at 100KSPS		73		dB
SINAD	1kHz sine input at 100KSPS		62.5		dB
SFDR	1kHz sine input at 100KSPS		73.7		dB
Conversion time			13		cycles
Current consumption	Using external VREF, at 100KSPS		13.5		µA
	Using internal VREF, at 100KSPS		25.0		µA
	Using external VREF, at 1MSPS		94		µA
	Using internal VREF, at 1MSPS		150		µA
	Using internal VREF, during VBAT monitoring		100		µA
	Using internal VREF, during temperature monitoring		50		µA
Internal reference voltage	Mean value using VBAT=2.5V		1.026 (1)		V
	Standard deviation across parts		10.5		mV
VBAT Sensor Accuracy	Without calibration	-55		+55	mV
	With offset and gain calibration	-17		+17	mV
Temperature Sensor Accuracy	Without calibration	-9		+9	ºC
	With offset calibration	-4		+4	ºC

Note: 1. Effective VREF is 2xInternal Reference Voltage.

$T_c = 25^0C \;\; V_{BAT} = 3.0\,V, unless\ otherwise\ noted.$

Figure 10-9. INL of SAR ADC

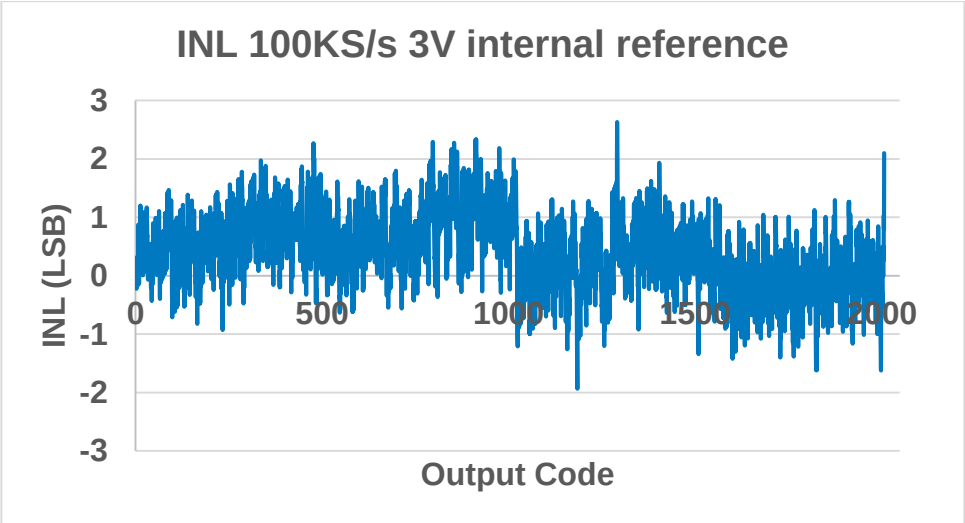


Figure 10-10. DNL of SAR ADC

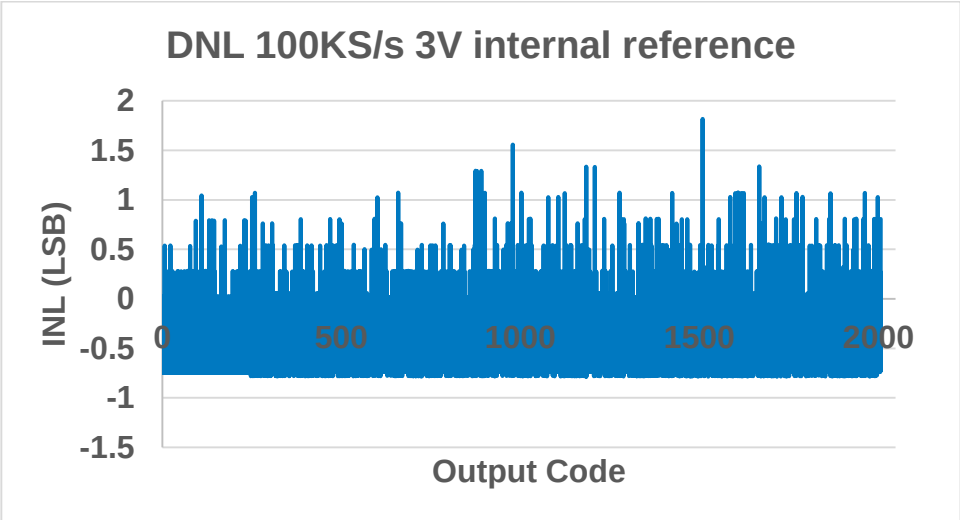
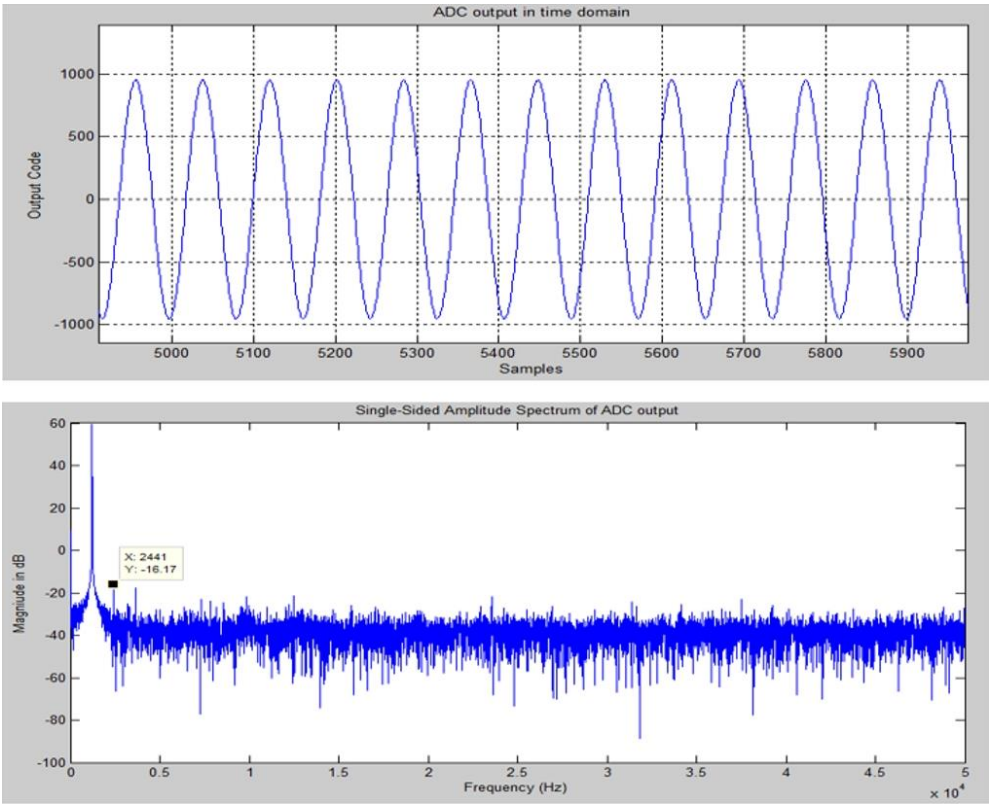
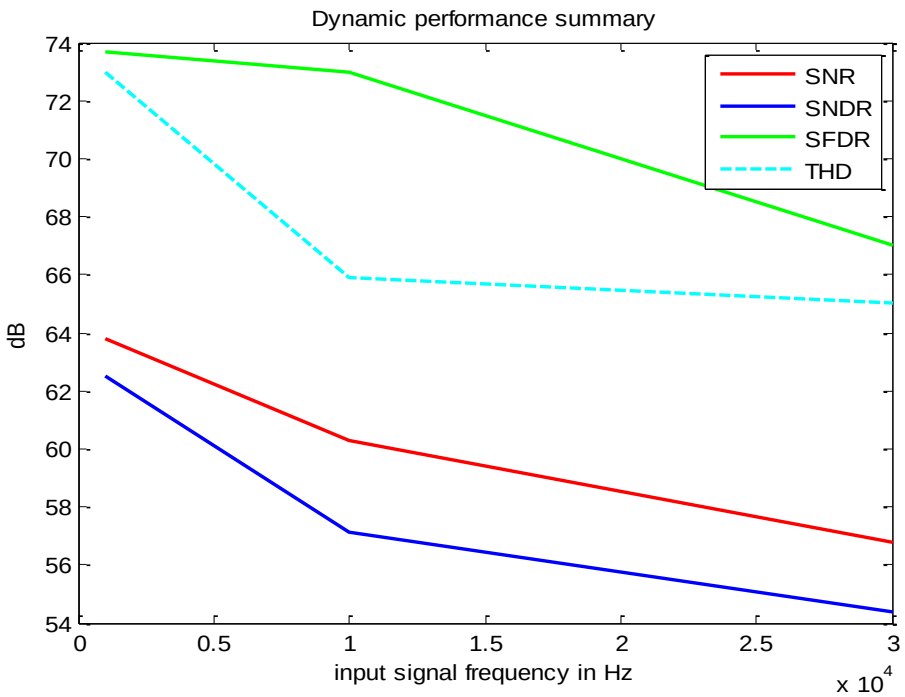


Figure 10-11. Sensor ADC Dynamic Measurement with Sinusoidal Input



Notes:
1. 25ºC, 3.6V VBAT, and 100kS/s
   Input signal: 1kHz sine wave, 3Vp-p amplitude
2. SNDR = 62.5dB
   SFDR = 73.7dB
   THD = 73.0dB

Figure 10-12. Sensor ADC Dynamic Performance Summary at 100KSPS



10.8 Software Programmable Timer and Pulse Width Modulator

ATBTLC1000 contains four individually configurable pulse width modulator (PWM) blocks to provide external control voltages. The base frequency of the PWM block (fPWM_base) is derived from the XO clock (26MHz) or the RC oscillator followed by a programmable divider.

The frequency of each PWM pulse (fPWM) is programmable in steps according to the following relationship:

$$f_{PWM} = \frac{f_{PWM_base}}{64 * 2^i} \qquad i = 0,1,2,\dots,8$$

The duty cycle of each PWM signal is configurable with 10-bit resolution (minimum duty cycle is 1/1024 and maximum is 1023/1024).

$f_{PWM_{base}}$ can be selected to have different values according to Table 10-12. Minimum and maximum frequencies supported for each clock selection are listed in the table as well.

Table 10-12. f_{PWM} Range for Different f_{PWM} Base Frequencies

$f_{PWM_{base}}$	f_{PWM} max.	f_{PWM} min.
26MHz	406.25kHz	6.347kHz
13MHz	203.125kHz	3.173kHz
6.5MHz	101.562kHz	1.586kHz
3.25MHz	50.781kHz	793.25Hz

10.9 Clock Output

ATBTLC1000 has an ability to output a clock. The clock can be output to any GPIO pin via the test MUX. Note that this feature requires that the ARM and BLE power domains stay on. If BLE is not used, the clocks to the BLE core are gated off, resulting in small leakage. The following two methods can be used to output a clock.

10.9.1 Variable Frequency Clock Output Using Fractional Divider

ATBTLC1000 can output the variable frequency ADC clock using a fractional divider of the 26MHz oscillator. This clock needs to be enabled using bit 10 of the lpmcu_clock_enables_1 register. The clock frequency can be controlled by the divider ratio using the sens_adc_clk_ctrl register (12-bits integer part, 8-bit fractional part).The division ratio can vary from 2 to 4096 delivering output frequency between 6.35kHz to 13MHz. This is a digital divider with pulse swallowing implementation so the clock edges may not be at exact intervals for the fractional ratios. However, it is exact for integer division ratios.

10.9.2 Fixed Frequency Clock Output

ATBTLC1000 can output the following fixed-frequency clocks:

- 52MHz derived from XO
- 26MHz derived from XO
- 2MHz derived from the 2MHz RC Osc.
- 31.25kHz derived from the 2MHz RC Osc.
- 32.768kHz derived from the RTC XO
- 26MHz derived from 26MHz RC Osc.
- 6.5MHz derived from XO
- 3.25MHz derived from 26MHz RC Osc.

For clocks 26MHz and above ensure that external pad load on the board is minimized to get a clean waveform.

10.10 Three-axis Quadrature Decoder

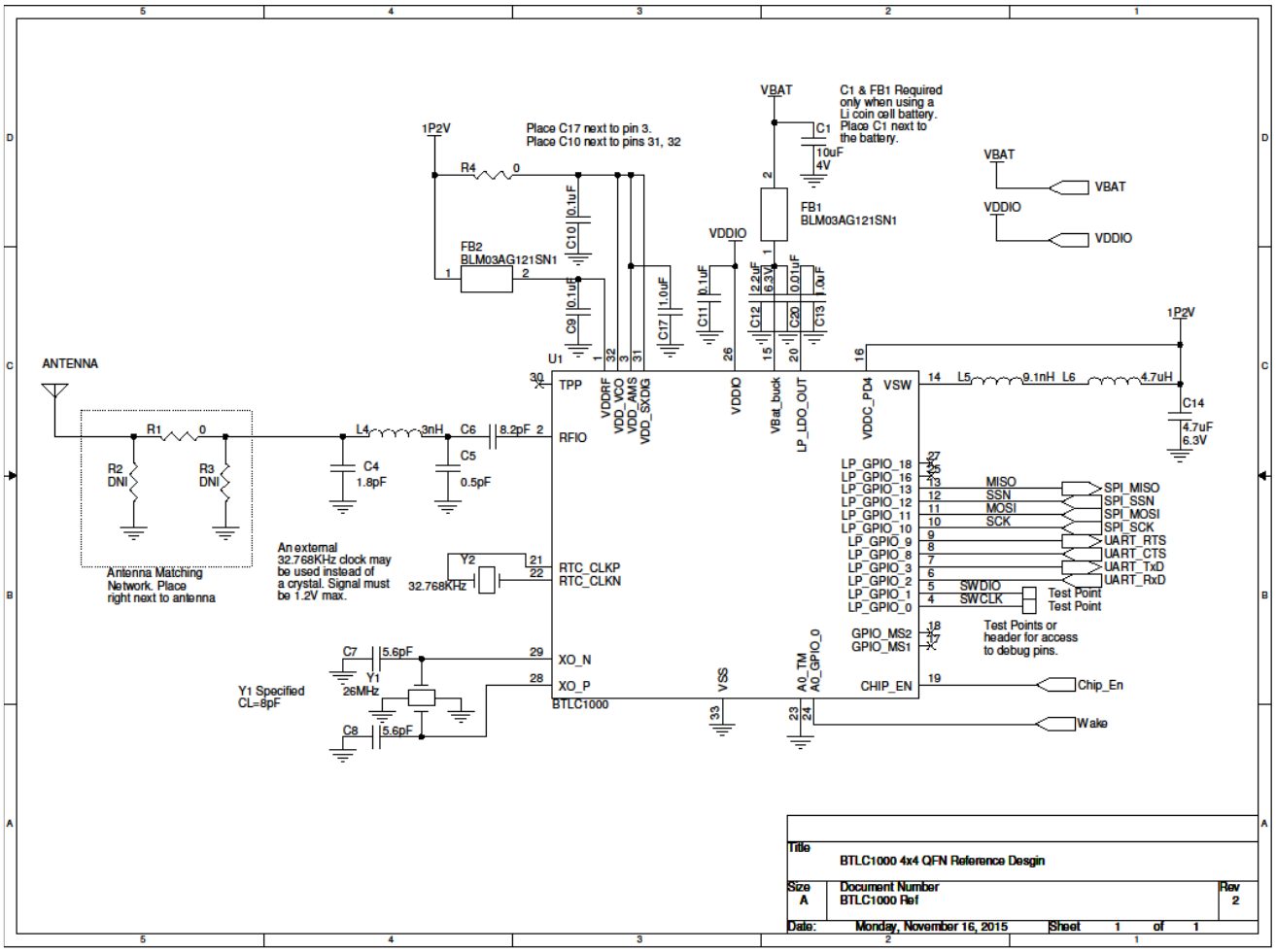
ATBTLC1000 has a three-axis Quadrature decoder (X, Y, and Z) that can determine the direction and speed of movement on three axes, requiring in total six GPIO pins to interface with the sensors. The sensors are expected to provide pulse trains as inputs to the quadrature decoder.

Each axis channel input will have two pulses with ±90 degrees phase shift depending on the direction of movement. The decoder counts the edges of the two waveforms to determine the speed and uses the phase relationship between the two inputs to determine the direction of motion.

The decoder is configured to interrupt ARM based on independent thresholds for each direction. Each quadrature clock counter (X, Y, and Z) is an unsigned 16-bit counter and the system clock uses a programmable sampling clock ranging from 26MHz, 13, 6.5, to 3.25MHz.

If wakeup is desired from threshold detection on an axis input, the always-on GPIO needs to be used (only one GPIO on ATBTLC1000).

11 Reference Design



12 Bill of Material (BOM)

BTLC1000 4x4 QFN W/FLASH Reference Design Revised: Monday, November 16, 2015

BTLC1000 Ref Revision: 2

Bill Of Materials November 16,2015 17:00:16

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	ANTENNA		Antenna, 2.4-2.5GHz, 50ohm, -40 - +85C			
2	1	C1	10uF	CAP,CER,10uF,20%,X5R,0402,4V,-55-85C	TDK	C1005X5R0G106M	0402
3	1	C4	1.8pF	CAP,CER,1.8pF,+/-0.1pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E1R8C	0201
4	1	C5	0.5pF	CAP,CER,0.5pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1ER50BA0	0201
5	1	C6	8.2pF	CAP,CER,8.2pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E8R2DDC1	0201
6	2	C7,C8	5.6pF	CAP,CER,5.6pF,+/-0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E5R6D030BA	0201
7	2	C9,C10	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-85C	Murata	GRM033R60J104KE19D	0201
8	1	C11	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	0201
9	1	C12	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K	0402
10	1	C13	1.0uF	CAP,CER,1.0uF,20%,X5R,0201,6.3V,-55-85C	TDK	C0603X5R0J105M030BC	0201
11	1	C14	4.7uF	CAP,CER,4.7uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J475K050BC	0402
12	1	C17	1.0uF	CAP,CER,1.0uF,20%,X6S,0201,4V,-55-85C	Murata	GRM033C80G105MEA2D	0201
13	1	C20	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-125C	Murata	GRM033R61A103KA01D	0201
14	2	FB1,FB2	BLM03AG121SN1	FERRITE,120 OHM @100MHz,200mA,0201,-55-125C	Murata	BLM03AG121SN1	0201
15	1	L4	3nH	Inductor,3nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N0C-T	0201
16	1	L5	9.1nH	INDUCTOR,Multilayer,9.1nH,5%,300mA,0.32 ohmsQ=8@100MHz,-55C-125C,0402	Murata	LQG15HS9N1J02D	0402
17	1	L6	4.7uH	INDUCTOR,unshielded,4.7uH,20%,120mA Saturation,0.5ohms,SRF=80MHz,0603,-55-125C	TDK	MLZ1608M4R7WT000	0603
18	2	R1,R4	0	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
19	2	R2,R3	DNI	RESISTOR,Thick Film,0 ohm,0201	Panasonic	ERJ-1GN0R00C	0201
20	2	TP1,TP2	non-component	Test Point,Surface Mount,0.040"sq w/0.25"hole		40X40_SM_TEST_POINT	0.04"SQx0.025"H
21	1	U1	BTLC1000	IC, BLE, 32QFN	Atmel	BTLC1000	32QFN
22	1	Y1	26MHz	CRYSTAL,26MHz,CL=8pF,20ppm temp.,-40-85C,ESR=80,2.5x2mm	Taitien	A0183-X-001-3	2.5mmx2.0mm
23	1	Y2	32.768KHz	Crystal, 32.768KHz,+/-20ppm,-40-+85C,CL=7pF, 2 lead, SM	ECS	ECS-.327-7-34B-TR	

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Table 13-1. ATBTLC1000 Absolute Maximum Ratings

Symbol	Characteristics	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	5.0	V
VBATT	Battery Supply Voltage	-0.3	5.0	
V_{IN} (1)	Digital Input Voltage	-0.3	VDDIO	
V_{AIN} (2)	Analog Input Voltage	-0.3	1.5	
V_{ESDHBM} (3)	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
T_A	Storage Temperature	-65	150	°C

Notes:
1. V_{IN} corresponds to all the digital pins
2. V_{AIN} corresponds to all the analog pins
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins include all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

13.2 Recommended Operating Conditions

Table 13-2. ATBTLC1000 Recommended Operating Conditions

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	I/O Supply Voltage Low Range	1.62	1.80	2.00	V
$VDDIO_M$	I/O Supply Voltage Mid-Range	2.00	2.50	3.00	
$VDDIO_H$	I/O Supply Voltage High Range	3.00	3.30	4.30	
VBATT	Battery Supply Voltage (1)	1.8	3.6	4.3	
	Operating Temperature	-40		85	°C

Note:
1. VBATT must not be less than VDDIO.
2. When powering up the device, VBATT must be greater or equal to 1.9V to ensure BOD does not trigger. BOD threshold is typically 1.8V and the device will be held in reset if VBATT is near this threshold on startup. After startup, BOD can be disabled and the device can operated down to 1.8V.

13.3 DC Characteristics

Table 13-3 provides the DC characteristics for the ATBTLC1000 digital pads.

Table 13-3. ATBTLC1000 DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
VDDIOL	Input Low Voltage VIL	-0.30		0.60	V
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
VDDIOM	Input Low Voltage VIL	-0.30		0.63	
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			
VDDIOH	Input Low Voltage VIL	-0.30		0.65	
	Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
	Output Low Voltage VOL			0.45	
	Output High Voltage VOH	VDDIO-0.50			
All	Output Loading			20	pF
	Digital Input Load			6	
VDDIOL	Pad drive strength (regular pads (1))	1.7	2.5		mA
VDDIOM	Pad drive strength (regular pads)	3.4	6.6		
VDDIOH	Pad drive strength (regular pads)	10.5	14		
VDDIOL	Pad drive strength (high-drive pads (1))	3.4	5.0		
VDDIOM	Pad drive strength (high-drive pads)	6.8	13.2		
VDDIOH	Pad drive strength (high-drive pads)	21	28		

Note: 1. The following are high-drive pads: GPIO_8, GPIO_9; all other pads are regular.

14 ERRATA

Issue: The measured current for the cases listed in Figure 6-3 will be higher than what is reported in the figure.

This is because the Power number values in the SDK4.0 release have not been fully optimized to their final values.

A small sample measurement has been performed on 10 samples and they show the following results:

Measurement condition:

- 1-sec adverting interval
- 37 byte advertising payload
- Connectable beacon
- Advertising on three channels (37, 38, 39)
- Vbatt and VDDIO are set to 3.3V

SAM L21 has a measurement floor of 80nA, which was compensated in the reported numbers (this number varies from board to board and needs to be compensated).

The Average advertising current: 11.3µA

The Average sleep current between beacons: 1.17µA

The average current for the 10 boards was (including 80nA floor):

Sample #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
Average Current (µA)	11.55	11.45	11.45	11.7	11.4	11.25	10.95	11.2	11.6	11.4

Work around: Will be resolved in a SDK update.

15 Document Revision History

Doc Rev.	Date	Comments
42409C	01/2016	1. Updated numbers in feature list. 2. Added UART flow control to LP_GPIO Pins in Table 4-1. 3. Removed 1µH Row and updated cap and ripple values in Figure 6-2. 4. Updated BLE on Transmit/BLE on Receive values in Table 6-2. 5. Updated text in describing BOD handling in Section 6.7. 6. Removed BGR block from diagram in Figure 6-7. 7. Added Table 6-5 for Brownout Thresholds and POR time in Table 6-5. 8. Updated oscillator variations in Sections 7.1, 7.4, and Figure 7-9. 9. Removed Supply Pins row in Table 7-5. 10. Updated Table 9-2 TX peak current values in Table 9-2. 11. Updated Reference Design. In Section 11. 12. Updated BOM. In Section 12. 13. Added note 2, in Table 13-2. 14. Removed reference Table 12-3 in title in Table 13-3. 15. Revised Sensitivity values in the Features, Section 7.1, and 7.4. 16 Added text to Section 7.1 regarding BLE sleep and connections. 17. Updated Figure 7-2 and Figure 7-3. 18. Revised Table 6-2 for consistency. 19. Added Errata area.
42409B	09/2015	1. Updated current numbers in the feature list. 2. Updated current numbers and added comments in Table 6-2. 3. Updated advertising current chart in Figure 6-4. 4. Updated capacitance value in Section 7.2. 5. Updated voltage value in Table 7-3. 6. Updated capacitance value and text in Section 7.3.1. 7. Added 32kHz RC Oscillator performance charts in Section 7.4. 8. Updated Receiver performance numbers and comments in Table 9-1. 9. Updated Transmitter performance numbers and comments in Table 9-2. 10. Updated ADC power consumption and added comment in Table 10-10. 11. Replaced the whole ADC performance Table 10-11. 12. Replaced ADC performance charts: Figure 10-9 and Figure 10-10. 13. Added new ADC performance charts: Figure 10-11 and Figure 10-12. 14. BTLC1000 corrected to ATBTLC1000.
42409A	09/2015	Initial document release



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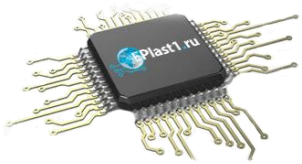
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