

98 dB, 96 kHz, Multi-Bit Audio A/D Converter

Features

- ◆ Advanced Multi-Bit $\Delta\Sigma$ Architecture
- ◆ 24-bit Conversion
- ◆ Supports Audio Sample Rates Up to 108 kHz
- ◆ 98 dB Dynamic Range at 5 V
- ◆ -92 dB THD+N at 5 V
- ◆ Low-Latency Digital Filter
- ◆ High-Pass Filter to Remove DC Offsets
- ◆ Single +3.3 V or +5 V Power Supply
- ◆ Power Consumption < 40 mW at 3.3 V
- ◆ Master or Slave Operation
- ◆ Slave Mode Speed Auto-Detect
- ◆ Master Mode Default Settings
- ◆ 256x or 384x MCLK/LRCK Ratio
- ◆ CS5343 Supports I²S Audio Format
- ◆ CS5344 Supports Left-Justified Audio Format

General Description

The CS5343/4 is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form at sample rates up to 108 kHz per channel.

The CS5343/4 uses a 3rd-order, multi-bit Delta-Sigma modulator followed by a digital filter, which removes the need for an external anti-alias filter.

The CS5343/4 also features a high-impedance sampling network which eliminates costly external components such as op-amps.

The CS5343/4 is available in a 10-pin TSSOP package for both Commercial (-40° to +85° C) and Automotive grades (-40° to +105° C). The CDB5343 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please refer to the “[Ordering Information](#)” on [page 19](#) for complete details.

The CS5343/4 is ideal for audio systems requiring wide dynamic range, negligible distortion and low noise, such as set-top boxes, DVD-karaoke players, DVD recorders, A/V receivers, and automotive applications.



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1. PIN DESCRIPTIONS



| Pin Name | Pin # | Pin Description |
|--------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDOUT | 1 | Serial Audio Data Output (Output) - Output for two's complement serial audio data. Also selects Master or Slave Mode; See Section 4.1 on page 12 for details. |
| SCLK | 2 | Serial Clock (Input/Output) - Serial clock for the serial audio interface. |
| LRCK | 3 | Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line. |
| MCLK | 4 | Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters. |
| FILT+ | 5 | Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits. |
| AINL AINR | 6 8 | Analog Input (Input) - The full-scale analog input level is specified in the Analog Characteristics specification table. |
| VQ | 7 | Quiescent Voltage (Output) - Filter connection for the internal quiescent reference voltage. |
| GND | 9 | Ground (Input) - Ground reference. Must be connected to analog ground. |
| VA | 10 | Power (Input) - Positive power supply for the digital and analog sections. |

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V, all voltages with respect to GND.

| Parameter | Symbol | Min | Typ | Max | Unit | |
|-------------------------------|-------------------|----------|-----|------|------|----|
| Power Supplies | VA | 3.1 | 3.3 | 3.5 | V | |
| | | 4.75 | 5.0 | 5.25 | V | |
| Ambient Operating Temperature | Commercial (-CZZ) | T_{AC} | -40 | - | 85 | °C |
| | Automotive (-DZZ) | T_{AD} | -40 | - | 105 | °C |

ABSOLUTE MAXIMUM RATINGS

GND = 0 V, all voltages with respect to GND. (Note 1)

| Parameter | Symbol | Min | Max | Unit |
|-----------------------------------------------|-----------|------|--------|------|
| DC Power Supplies | VA | -0.3 | +6.0 | V |
| Input Current (Note 2) | I_{in} | -10 | +10 | mA |
| Input Voltage (Note 3) | V_{IN} | -0.7 | VA+0.7 | V |
| Ambient Operating Temperature (Power Applied) | T_A | -50 | +115 | °C |
| Storage Temperature | T_{stg} | -65 | +150 | °C |

Notes:

1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
2. Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG CHARACTERISTICS - COMMERCIAL GRADE (-CZZ)

Test conditions (unless otherwise specified): $T_A = 25^\circ\text{C}$; Input test signal is a 997 Hz sine wave through recommended inputs as seen in [Figure 6 on page 14](#); source impedance less than or equal to 2.5 k Ω ; valid with FILT+ and VQ components as shown in [Figure 3 on page 11](#); measurement bandwidth is 10 Hz to 20 kHz; $F_s = 48\text{ kHz}$ or 96 kHz.

| Dynamic Performance for Commercial Grade | | | VA = 3.3 V | | | VA = 5.0 V | | | |
|-------------------------------------------------|----------------|-------|----------------------------------|-----------|----------|-------------------|-----|-----|-----------------------|
| | Symbol | | Min | Typ | Max | Min | Typ | Max | Unit |
| Dynamic Range | A-weighted | | 91 | 94 | - | 95 | 98 | - | dB |
| | unweighted | | 88 | 91 | - | 92 | 95 | - | dB |
| Total Harmonic Distortion + Noise | (Note 4) | | | | | | | | |
| | -1 dB | THD+N | - | -89 | -86 | - | -92 | -89 | dB |
| | -20 dB | | - | -71 | - | - | -75 | - | dB |
| | -60 dB | | - | -31 | - | - | -35 | - | dB |
| Dynamic Performance for Commercial Grade | | | VA = 3.3 V and VA = 5.0 V | | | | | | |
| | | | Min | Typ | Max | | | | Unit |
| Interchannel Isolation | | | - | 90 | - | | | | dB |
| DC Accuracy | | | | | | | | | |
| Interchannel Gain Mismatch | | | - | - | 0.1 | | | | dB |
| Gain Error | | | -3 | - | +3 | | | | % |
| Gain Drift | | | - | ± 100 | - | | | | ppm/ $^\circ\text{C}$ |
| Analog Input Characteristics | | | | | | | | | |
| Full-scale Input Voltage | VA = 3.3 V nom | | 0.560*VA | 0.568*VA | 0.575*VA | | | | Vpp |
| Full-scale Input Voltage | VA = 5 V nom | | 0.552*VA | 0.559*VA | 0.567*VA | | | | Vpp |
| Input Impedance | | | - | 7.5 | - | | | | M Ω |

Notes:

4. Referred to the typical full-scale input voltage

ANALOG CHARACTERISTICS - AUTOMOTIVE GRADE (-DZZ)

Test conditions (unless otherwise specified): $T_A = -40^\circ\text{C}$ to 85°C ; Input test signal is a 997 Hz sine wave through recommended inputs as seen in Figure 6 on page 14; source impedance less than or equal to 2.5 k Ω ; valid with FILT+ and VQ components as shown in Figure 3 on page 11; measurement bandwidth is 10 Hz to 20 kHz; $F_s = 48\text{ kHz}$ or 96 kHz .

| Dynamic Performance for Automotive Grade | | | VA = 3.1 to 3.5 V | | | VA = 4.75 to 5.25 V | | | |
|-------------------------------------------------|-----------------------|-------|------------------------------------------------------|-----------|----------|----------------------------|-----|-----|-----------------------|
| | Symbol | | Min | Typ | Max | Min | Typ | Max | Unit |
| Dynamic Range | A-weighted | | 86 | 94 | - | 90 | 98 | - | dB |
| | unweighted | | 83 | 91 | - | 87 | 95 | - | dB |
| Total Harmonic Distortion + Noise | (Note 5) | | | | | | | | |
| | -1 dB | THD+N | - | -88 | -76 | - | -91 | -84 | dB |
| | -20 dB | | - | -71 | - | - | -75 | - | dB |
| | -60 dB | | - | -31 | - | - | -35 | - | dB |
| Dynamic Performance for Automotive Grade | | | VA = 3.1 V to 3.5 V and VA = 4.75 V to 5.25 V | | | | | | |
| | | | Min | Typ | Max | | | | Unit |
| Interchannel Isolation | | | - | 90 | - | | | | dB |
| DC Accuracy | | | | | | | | | |
| Interchannel Gain Mismatch | | | - | - | - | 0.1 | | | dB |
| Gain Error | | | -3 | - | - | +3 | | | % |
| Gain Drift | | | - | ± 100 | - | - | | | ppm/ $^\circ\text{C}$ |
| Analog Input Characteristics | | | | | | | | | |
| Full-scale Input Voltage | VA = 3.1 V to 3.5 V | | 0.523*VA | 0.567*VA | 0.612*VA | | | | Vpp |
| Full-scale Input Voltage | VA = 4.75 V to 5.25 V | | 0.543*VA | 0.560*VA | 0.573*VA | | | | Vpp |
| Input Impedance | | | - | 7.5 | - | | | | M Ω |

Notes:

5. Referred to the typical full-scale input voltage

DIGITAL FILTER CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------------------|-------------------|--------|-------|-------|------|
| All Speed Modes | | | | | |
| Passband (-0.1 dB) | | 0 | - | 0.489 | Fs |
| Passband Ripple | | -0.031 | - | 0.031 | dB |
| Stopband | | 0.560 | - | - | Fs |
| Stopband Attenuation | | 60 | - | - | dB |
| Total Group Delay (Fs = Output Sample Rate) | t_{gd} | - | 12/Fs | - | s |
| High-Pass Filter Characteristics | | | | | |
| Frequency Response | -3.0 dB | - | 1 | - | Hz |
| | -0.13 dB (Note 6) | | 20 | - | Hz |
| Phase Deviation | @ 20 Hz (Note 6) | - | 10 | - | Deg |
| Passband Ripple | | - | - | 0 | dB |

Notes:

6. Response shown is for Fs equal to 48 kHz. Filter characteristics scale with Fs.

DC ELECTRICAL CHARACTERISTICS

GND = 0 V, all voltages with respect to 0 V. MCLK=12.288 MHz; Master Mode.

| Parameter | Symbol | VA = 3.3 V | | | VA = 5.0 V | | | Unit |
|-------------------------------------------------|--------|------------|---------|-----|------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Power Supply Current (Normal Operation) | I_A | - | 11 | 15 | - | 12 | 17 | mA |
| Power Supply Current (Power-Down Mode) (Note 7) | I_A | - | 10 | - | - | 40 | - | uA |
| Power Consumption (Normal Operation) | - | - | 36 | 50 | - | 60 | 85 | mW |
| Power Consumption (Power-Down Mode) (Note 7) | - | - | <1 | - | - | <1 | - | mW |
| Parameter | Symbol | Min | Typ | Max | | | | Unit |
| Power Supply Rejection Ratio (1 kHz) (Note 8) | PSRR | - | 65 | - | | | | dB |
| V _Q Nominal Voltage | | - | 0.44xVA | - | | | | V |
| Output Impedance | | - | 25 | - | | | | kΩ |
| Filt+ Nominal Voltage | | - | VA | - | | | | V |
| Output Impedance | | - | 220 | - | | | | kΩ |
| Maximum allowable DC current source/sink | | - | 2.5 | - | | | | uA |

Notes:

7. Device enters power-down mode when MCLK is held static.
8. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Units |
|-------------------------------------------------------------|----------|-----|-----|-----|---------|
| High-Level Input Voltage (% of VA) | V_{IH} | 60 | - | - | % |
| Low-Level Input Voltage (% of VA) | V_{IL} | - | - | 30 | % |
| High-Level Output Voltage at $I_o = 500 \mu A$ (% of VA) | V_{OH} | 70 | - | - | % |
| Low-Level Output Voltage at $I_o = 500 \mu A$ (% of VA) | V_{OL} | - | - | 15 | % |
| Input Leakage Current | I_{in} | -10 | - | 10 | μA |

SYSTEM CLOCKING AND SERIAL AUDIO INTERFACE

 Logic "0" = GND = 0 V; Logic "1" = VA, C_L = 20 pF.

| Parameter | | Symbol | Min | Typ | Max | Unit |
|--------------------------------|---------------------------|--------------------|--------------------------|-----|-----|------|
| Master Mode | | | | | | |
| MCLK Period | (Double-Speed, 384x Mode) | t _{clkw} | 24 | - | 30 | ns |
| | (Double-Speed, 192x Mode) | | 48 | - | 60 | ns |
| | (Double-Speed, 256x Mode) | | 36 | - | 45 | ns |
| | (Double-Speed, 128x Mode) | | 72 | - | 90 | ns |
| | (Single-Speed, 768x Mode) | | 24 | - | 30 | ns |
| | (Single-Speed, 384x Mode) | | 48 | - | 60 | ns |
| | (Single-Speed, 384x Mode) | | 108 | - | 651 | ns |
| | (Single-Speed, 512x Mode) | | 36 | - | 45 | ns |
| | (Single-Speed, 256x Mode) | | 72 | - | 90 | ns |
| | (Single-Speed, 256x Mode) | | 162 | - | 977 | ns |
| MCLK Duty Cycle | | | 40 | 50 | 60 | % |
| Output Sample Rate | (Single-Speed) | Fs | 4 | - | 24 | kHz |
| | (Single-Speed) | | 43 | - | 54 | kHz |
| | (Double-Speed) | | 86 | - | 108 | kHz |
| LRCK Duty Cycle | | | - | 50 | - | % |
| SCLK Duty Cycle | | | - | 50 | - | % |
| SDOUT valid before SCLK rising | | t _{stp} | 10 | - | - | ns |
| SDOUT valid after SCLK rising | | t _{hld} | 40 | - | - | ns |
| SCLK falling to LRCK edge | | t _{slrd} | -20 | - | 20 | ns |
| Slave Mode | | | | | | |
| MCLK Period | (Double-Speed, 384x Mode) | t _{clkw} | 24 | - | 30 | ns |
| | (Double-Speed, 192x Mode) | | 48 | - | 60 | ns |
| | (Double-Speed, 256x Mode) | | 36 | - | 45 | ns |
| | (Double-Speed, 128x Mode) | | 72 | - | 90 | ns |
| | (Single-Speed, 768x Mode) | | 24 | - | 325 | ns |
| | (Single-Speed, 384x Mode) | | 48 | - | 651 | ns |
| | (Single-Speed, 512x Mode) | | 36 | - | 488 | ns |
| | (Single-Speed, 256x Mode) | | 72 | - | 976 | ns |
| MCLK Duty Cycle | | | 40 | 50 | 60 | % |
| Input Sample Rate | (Single-Speed) | Fs | 4 | - | 54 | kHz |
| | (Double-Speed) | | 86 | - | 108 | kHz |
| LRCK Duty Cycle | | | 40 | 50 | 60 | % |
| SCLK Period | | t _{sclkw} | $\frac{1}{64 \times Fs}$ | - | - | ns |
| SCLK Duty Cycle | | | 45 | 50 | 55 | % |
| SDOUT valid before SCLK rising | | t _{stp} | 10 | - | - | ns |
| SDOUT valid after SCLK rising | | t _{hld} | 40 | - | - | ns |
| SCLK falling to LRCK edge | | t _{slrd} | -20 | - | 20 | ns |



Figure 1. CS5343 I²S Serial Audio Interface



Figure 2. CS5344 Left-Justified Serial Audio Interface

3. TYPICAL CONNECTION DIAGRAM



Figure 3. Typical Connection Diagram

4. APPLICATIONS

4.1 Operation as Clock Master or Slave

The CS5343/4 supports operation as either a clock master or slave. As a clock master, the left/right and serial clocks are synchronously generated on-chip and output on the LRCK and SCLK pins, respectively. As a clock slave, the LRCK and SCLK pins are always inputs and require external generation of the left/right and serial clocks. The selection of clock master or slave is made via a 10 k Ω pull-up resistor from SDOUT to VA for Master Mode selection or via a 10 k Ω pull-down resistor from SDOUT to GND for Slave Mode selection, as shown in [Table 1](#).

| Mode | Selection |
|-------------|----------------------------------------------------|
| Master Mode | 10 k Ω pull-up resistor from SDOUT to VA |
| Slave Mode | 10 k Ω pull-down resistor from SDOUT to GND |

Table 1. Master/Slave Mode Selection

4.1.1 Slave Mode Operation

A unique feature of the CS5343/4 is the automatic selection of either Single- or Double-Speed Mode when acting as a clock slave. The auto-mode selection feature supports all standard audio sample rates from 4 to 108 kHz. Please refer to [Table 2](#) for supported sample rate ranges in Slave Mode.

| Speed Mode | MCLK/LRCK Ratio | SCLK/LRCK Ratio | Input Sample Rate Range (kHz) |
|-------------------|-----------------|-----------------|-------------------------------|
| Single-Speed Mode | 256x | 64 | 4 - 54 |
| | 512x | 64 | 4 - 54 |
| | 384x | 48, 64 | 4 - 54 |
| | 768x | 48, 64 | 4 - 54 |
| Double-Speed Mode | 128x | 64 | 86 - 108 |
| | 256x | 64 | 86 - 108 |
| | 192x | 48, 64 | 86 - 108 |
| | 384x | 48, 64 | 86 - 108 |

Table 2. Speed Modes and the Associated Sample Rates (Fs) in Slave Mode

4.1.2 Master Mode Operation

As clock Master, the CS5343/4 generates LRCK and SCLK synchronously on-chip. Table 3 shows the available sample rates and associated clock ratios in Master Mode.

| Speed Mode | MCLK/LRCK Ratio | SCLK/LRCK Ratio | Input Sample Rate Range (kHz) |
|-------------------|-----------------|-----------------|-------------------------------|
| Single-Speed Mode | 256x | 64 | 4 - 24, 43 - 54 |
| | 512x | 64 | 43 - 54 |
| | 384x | 64 | 4 - 24, 43 - 54 |
| | 768x | 64 | 43 - 54 |
| Double-Speed Mode | 128x | 64 | 86 - 108 |
| | 256x | 64 | 86 - 108 |
| | 192x | 64 | 86 - 108 |
| | 384x | 64 | 86 - 108 |

Table 3. Speed Modes and the Associated Sample Rates (Fs) in Master Mode

4.1.2.1 Master Mode Speed Selection

During power-up in Master Mode, the LRCK and SCLK pins are inputs to configure speed mode and the output clock ratio. The LRCK pin is pulled low internally to select Single-Speed Mode by default, but Double-Speed Mode is accessed with a 10 kΩ pull-up resistor from LRCK to VA as shown in Table 4. Similarly, the SCLK pin is internally pulled-low by default to select a 256x/512x MCLK/LRCK ratio, but a MCLK/LRCK ratio of 348x/768x is accessed with a 10 kΩ pull-up resistor from SCLK to VA as shown in Table 4. Following the power-up routine, the LRCK and SCLK pins become clock outputs.

| Pin | Resistor Option | Clock Configuration |
|------|------------------------------------|------------------------------------|
| LRCK | Internal Pull-Down to GND (100 kΩ) | Single-Speed Mode (default) |
| | External Pull-Up to VA (10 kΩ) | Double-Speed Mode |
| SCLK | Internal Pull-Down to GND (100 kΩ) | 128x/256x/512x MCLK/LRCK (default) |
| | External Pull-Up to VA (10 kΩ) | 192x/384x/768x MCLK/LRCK |

Table 4. Speed Mode Selection in Master Mode

4.1.3 Master Clock

The CS5343/4 requires a Master clock (MCLK) which runs the internal sampling circuits and digital filters. There is an internal automatic MCLK divider which is activated based on the input frequency of MCLK. This divider selection allows the high and low MCLK speeds in a given speed mode (i.e. 256x and 512x in SSM). Table 4 lists some common audio output sample rates and the required MCLK frequency.

| Master and Slave Mode | | | | | |
|-----------------------|------------|-----------|---------|------------|---------|
| Sample Rate (kHz) | Speed Mode | MCLK(MHz) | | MCLK (MHz) | |
| | | 256x | 512x | 384x | 768x |
| 32 (*Slave Mode Only) | SSM | *8.192 | *16.384 | *12.288 | *24.576 |
| 44.1 | SSM | 11.289 | 22.579 | 16.934 | 33.868 |
| 48 | SSM | 12.288 | 24.576 | 18.432 | 36.864 |
| Sample Rate (kHz) | Speed Mode | MCLK(MHz) | | MCLK (MHz) | |
| | | 128x | 256x | 192x | 384x |
| 88.2 | DSM | 11.289 | 22.579 | 16.934 | 33.868 |
| 96 | DSM | 12.288 | 24.576 | 18.432 | 36.864 |

Table 5. Common MCLK Frequencies in Master and Slave Modes

4.2 Serial Audio Interface

The CS5343 output is serial data in I²S audio format and the CS5344 output is serial data in Left-Justified audio format. Figures 4 and 5 show the I²S and Left-Justified data relative to SCLK and LRCK. Additionally, Figures 1 and 2 display more information on the required timing for the serial audio interface format. For an overview of serial audio interface formats, please refer to Cirrus Application Note AN282.



Figure 4. CS5343 I²S Serial Audio Interface



Figure 5. CS5344 Left-Justified Serial Audio Interface

4.3 Digital Interface

VA supplies power to both the analog and digital sections of the ADC, and also powers the serial port. Consequently, the digital interface logic level must equal VA to within the limits specified under “[Digital Characteristics](#)” on page 8.

4.4 Analog Connections

The analog modulator samples the input signal at half of the internal master clock rate, or 6.144 MHz when MCLK = 12.288 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency ($n \times 6.144$ MHz), where $n=0,1,2,\dots$. Refer to Figure 6 which shows the recommended topology of the analog input network. The external shunt capacitor and internal input impedance form a single-pole RC filter to provide the appropriate filtering of noise at the modulator sampling frequency. Additionally, the 180 pF capacitor acts as a charge source for the internal sampling circuits. Capacitors of NPO or other high-quality dielectric will produce the best results while capacitors with a large voltage coefficient (such as general-purpose ceramics) can degrade signal linearity.



Figure 6. CS5343/4 Analog Input Network

4.4.1 Component Values

Three parameters determine the values of resistors R1 and R2 as shown in [Figure 6](#): source impedance, attenuation, and input impedance. [Table 6](#) shows the design equation used to determine these values.

- **Source Impedance:** Source impedance is defined as the impedance as seen from the ADC looking back into the signal network. The ADC achieves optimal THD+N performance with a source impedance less than or equal to 2.5 kΩ.
- **Attenuation:** The required attenuation factor depends on the magnitude of the input signal. The full-scale input voltage is specified under “[Analog Characteristics - Commercial Grade \(-CZZ\)](#)” on [page 5](#). The user should select values for R1 and R2 such that the magnitude of the incoming signal multiplied by the attenuation factor is less than or equal to the full-scale input voltage of the device.
- **Input Impedance:** Input impedance is the impedance from the signal source to the ADC analog input pins, including the ADC. Because the ADC’s input impedance (see the “[Analog Characteristics - Commercial Grade \(-CZZ\)](#)” table on [page 5](#)) is several orders of magnitude larger than the resistor values typically used for the input attenuator, its contribution can be neglected when calculating the input impedance. [Table 6](#) shows the input parameters and the associated design equations for the input attenuator.

| | |
|--------------------|----------------------------------|
| Source Impedance | $\frac{(R1 \times R2)}{R1 + R2}$ |
| Attenuation Factor | $\frac{(R2)}{(R1 + R2)}$ |
| Input Impedance | $(R1 + R2)$ |

Table 6. Analog Input Design Parameters

[Figure 7](#) illustrates an example configuration using two 4.99 kΩ resistors in place of R1 and R2. Based on the discussion above, this circuit provides an optimal interface for both the ADC and the signal source. First, consumer equipment frequently requires an input impedance of 10 kΩ, which the 4.99 kΩ resistors provide. Second, this circuit will attenuate a typical line level voltage, 2 V_{rms}, to the full-scale input of the ADC, 1 V_{rms} when V_A = 5 V. Finally, at 2.5 kΩ, the source impedance optimizes analog performance of the ADC.



Figure 7. CS5343/4 Example Analog Input Network

4.5 Grounding and Power Supply Decoupling

As with any high-resolution converter, designing with the CS5343/4 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 3](#) shows the recommended power arrangements, with V_A connected to a clean supply. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 μF, must be positioned to minimize the electrical path from FILT+ to GND. The CDB5343 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

4.6 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK, SCLK, and LRCK signals must be the same for all of the CS5343 and CS5344 devices in the system.

5. FILTER PLOTS - ALL SPEED MODES



Figure 8. Stopband Rejection



Figure 9. Transition Band



Figure 10. Transition Band (Detail)



Figure 11. Passband Ripple

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

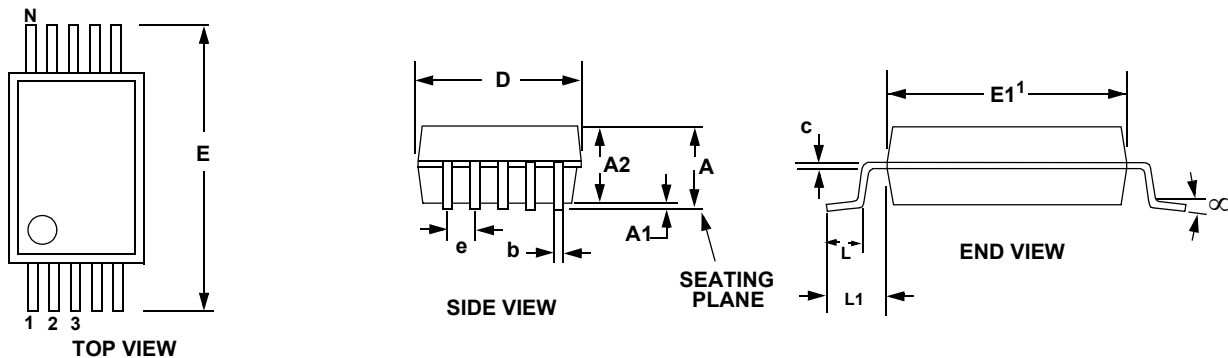
The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

7. PACKAGE DIMENSIONS

10LD TSSOP (3 mm BODY) PACKAGE DRAWING (Note 1)



| DIM | INCHES | | | MILLIMETERS | | | NOTE |
|-------|--------|------------|--------|-------------|----------|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| A | -- | -- | 0.0433 | -- | -- | 1.10 | |
| A1 | 0 | -- | 0.0059 | 0 | -- | 0.15 | |
| A2 | 0.0295 | -- | 0.0374 | 0.75 | -- | 0.95 | |
| b | 0.0059 | -- | 0.0118 | 0.15 | -- | 0.30 | 4, 5 |
| c | 0.0031 | -- | 0.0091 | 0.08 | -- | 0.23 | |
| D | -- | 0.1181 BSC | -- | -- | 3.00 BSC | -- | 2 |
| E | -- | 0.1929 BSC | -- | -- | 4.90 BSC | -- | |
| E1 | -- | 0.1181 BSC | -- | -- | 3.00 BSC | -- | 3 |
| e | -- | 0.0197 BSC | -- | -- | 0.50 BSC | -- | |
| L | 0.0157 | 0.0236 | 0.0315 | 0.40 | 0.60 | 0.80 | |
| L1 | -- | 0.0374 REF | -- | -- | 0.95 REF | -- | |
| μ | 0° | -- | 8° | 0° | -- | 8° | |

Controlling Dimension is Millimeters

Notes:

1. Reference document: JEDEC MO-187
2. D does not include mold flash or protrusions, which is 0.15 mm max. per side.
3. E1 does not include inter-lead flash or protrusions, which is 0.15 mm max per side.
4. Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.
5. Exceptions to JEDEC dimension.

THERMAL CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------------|----------------------------------|-----|-----|-----|------|
| Allowable Junction Temperature | T_J | - | - | 135 | °C |
| Junction to Ambient Thermal Impedance | (4-layer PCB) θ_{JA-4} | - | 100 | - | °C/W |
| | (2-layer PCB) θ_{JA-2} | - | 170 | - | °C/W |

8. ORDERING INFORMATION

| Product | Description | Package | Pb-Free | Grade | Temp Range | Container | Order # |
|---------|---------------------------------------------------------------------|----------|---------|------------|-----------------|-------------|-------------|
| CS5343 | 98 dB, Multi-Bit Audio A/D Converter, I ² S Audio Format | 10-TSSOP | Yes | Commercial | -40° to +85° C | Rail | CS5343-CZZ |
| | | | | | | Tape & Reel | CS5343-CZZR |
| CS5343 | 98 dB, Multi-Bit Audio A/D Converter, I ² S Audio Format | 10-TSSOP | Yes | Automotive | -40° to +105° C | Rail | CS5343-DZZ |
| | | | | | | Tape & Reel | CS5343-DZZR |
| CS5344 | 98 dB, Multi-Bit Audio A/D Converter, Left-Justified Audio Format | 10-TSSOP | Yes | Commercial | -40° to +85° C | Rail | CS5344-CZZ |
| | | | | | | Tape & Reel | CS5344-CZZR |
| CS5344 | 98 dB, Multi-Bit Audio A/D Converter, Left-Justified Audio Format | 10-TSSOP | Yes | Automotive | -40° to +105° C | Rail | CS5344-DZZ |
| | | | | | | Tape & Reel | CS5344-DZZR |
| CDB5343 | CS5343 Evaluation Board | - | No | - | - | - | CDB5343 |

9. REVISION HISTORY

| Release | Changes |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F1 | Updated “Recommended Operating Conditions” on page 4 Updated specifications and limits for “Analog Characteristics - Commercial Grade (-CZZ)” on page 5 Updated specifications and limits for “Analog Characteristics - Automotive Grade (-DZZ)” on page 6 Corrected “Power Supply Current (Normal Operation)” on page 7 Increased specification for Slave-Mode “SDOUT valid after SCLK rising” on page 9 Corrected Section 4.1.2.1 on page 13 Updated Section 4.1.3 on page 13 |
| F2 | Removed Fs < 43 kHz from master mode operation: -Updated master mode timing specifications in the “System Clocking and Serial Audio Interface” on page 9 -Updated Input Sample Rate Range in Table 3 on page 13 -Added note for “slave mode only” for Fs = 32 kHz in Table 5 on page 13 . |
| F3 | Updated Passband Ripple, Stopband Attenuation and Total Group Delay specs in “Digital Filter Characteristics” on page 7 . |
| F4 | Corrected a typographical error in Table 5, “Common MCLK Frequencies in Master and Slave Modes,” on page 13 . Changed 8.912 MHz to 8.192 MHz. |
| F5 | Updated master mode MCLK period and output sample rate in “System Clocking and Serial Audio Interface” on page 9 . Updated input sample rate range in “Master Mode Operation” on page 13 . Updated legal text. |

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

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