

Infineon[®] Basic LED Driver

TLD1211SJ

High Side Current Source
1 channel

Typical 85mA load current, up to 2.5A load current using external transistors

Data sheet

Rev. 1.0, 2010-03-26

Automotive



1 Overview

Features

- Adjustable Constant Output Current up to 85 mA
- LED Current of 2.5 A possible by using external Power Transistors
- Voltage Drop across Sense Resistor typ. 0.15 V
- Internal Bandgap Voltage Reference enables High Output Current accuracy
- EN Input for PWM brightness control
- Overvoltage Protection
- Temperature dependent Output Current Reduction
- Very Low Standby Current
- Maximum Operating Voltage 28 V
- Small SMD Package
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-8-16

Applications

- LED Controller for Automotive applications, Low- and High-Power LED
- Universal Constant Current Source
- Interior and Exterior Lighting
- Instrument backlighting
- Illumination

Description

The TLD1211SJ is an integrated adjustable constant current source realized in a bipolar IC technology. The IC is designed to supply LEDs under the severe conditions of automotive applications resulting in constant brightness and extended LED lifetime. The TLD1211SJ is capable to drive high current, high brightness LEDs up to 2.5 A by using additional external output stages as “booster” transistors. For LED currents up to 85mA the IC can be used as a stand alone device and requires only one voltage sense resistor as an external component.

Protection circuits prevent damage to the device in case of overload, short circuit, over voltage, and overtemperature.

Furthermore, the temperature dependent current reduction is able to protect LEDs which are thermally coupled to the IC. The integrated EN input of the TLD1211SJ enables LED brightness control by pulse width modulation.

| Type | Package | Marking |
|-----------|-------------|-----------|
| TLD1211SJ | PG-DSO-8-16 | TLD1211SJ |

2 Block Diagram

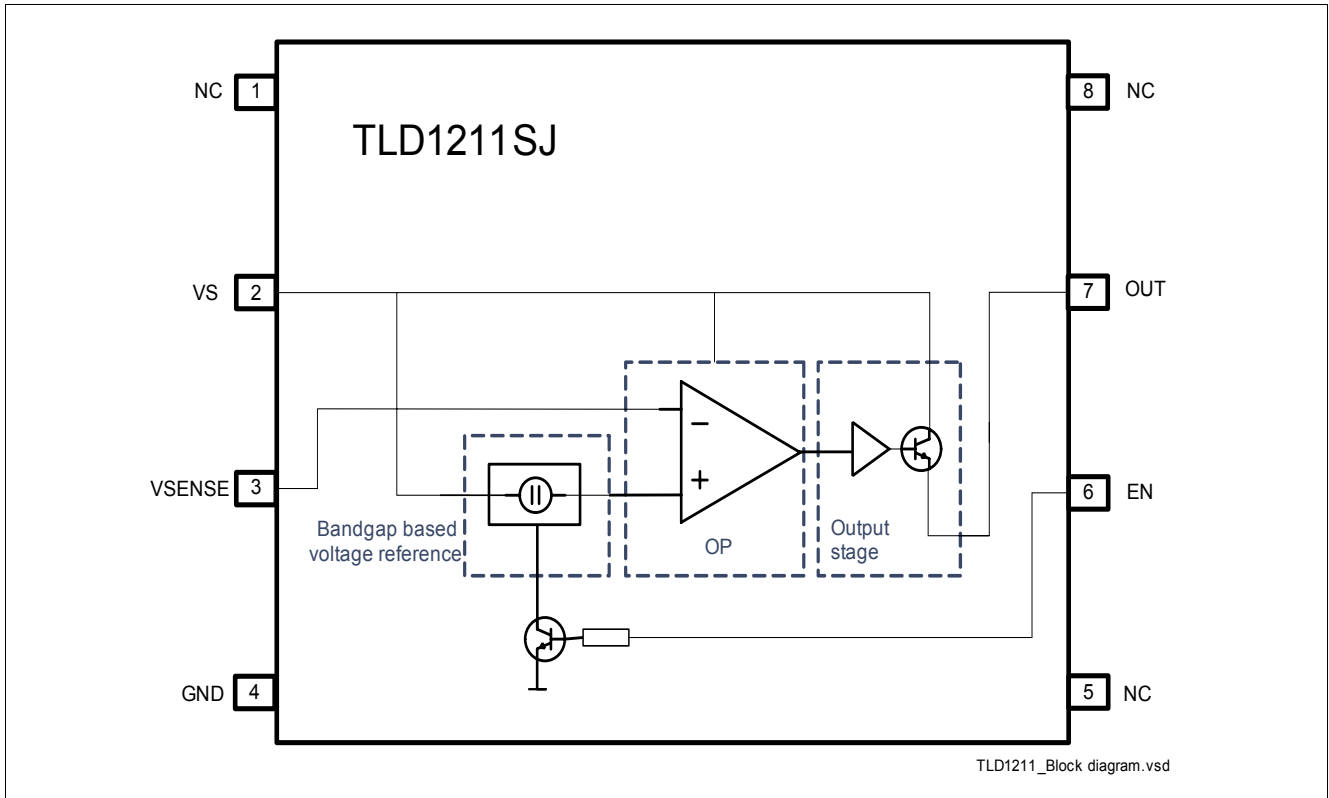


Figure 1 Block Diagram

2.1 Closed Loop Test Setup

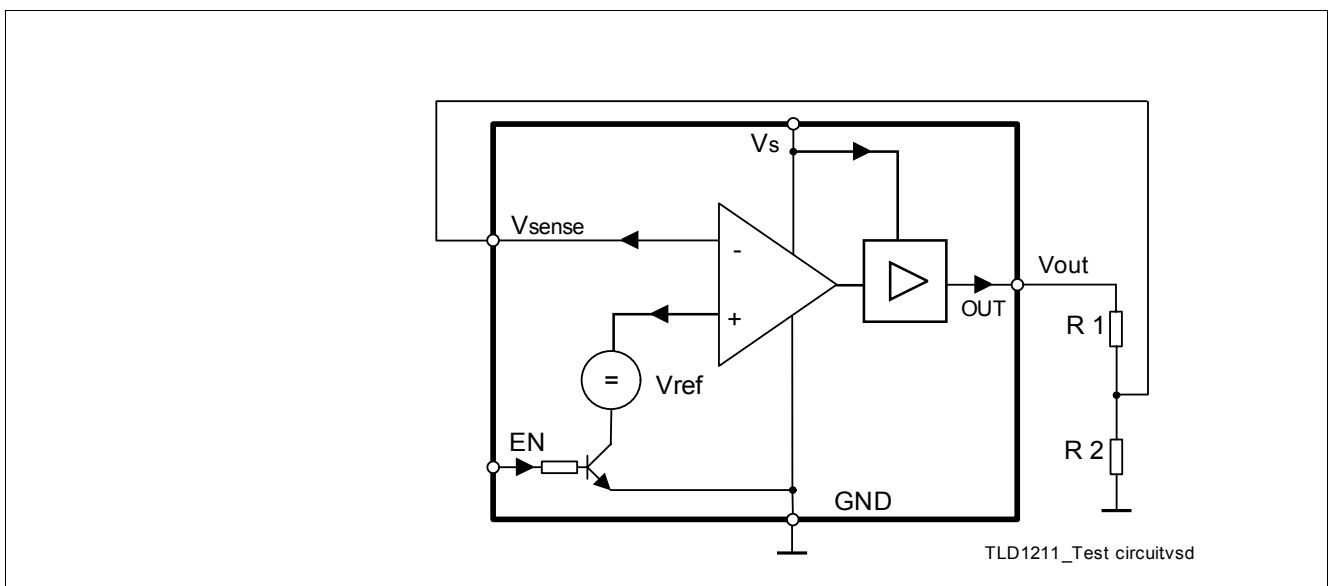


Figure 2 Closed loop Test setup

3 Pin Configuration

3.1 Pin Assignment

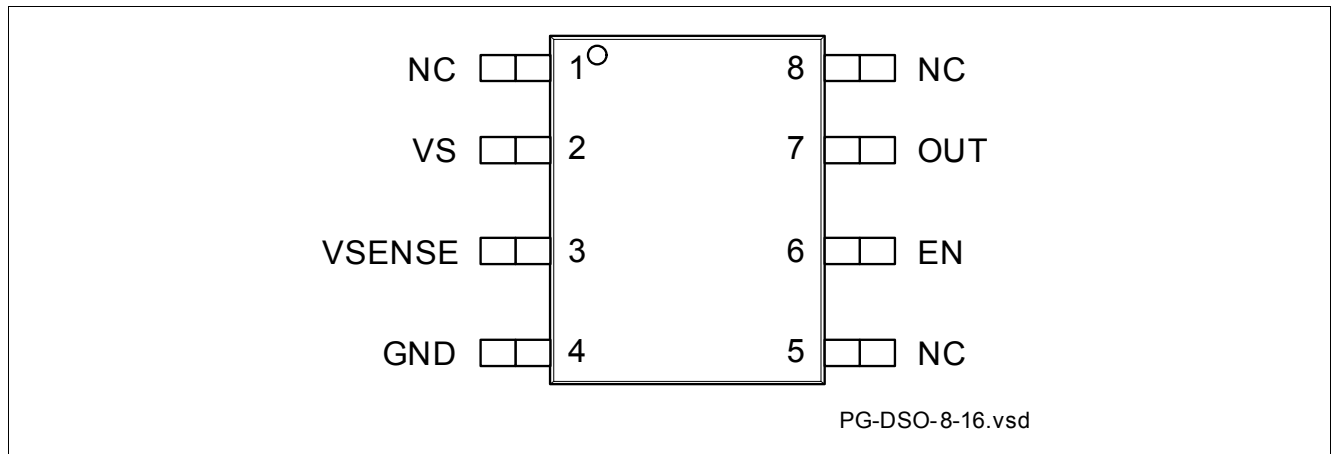


Figure 3 Pin Configuration

3.2 Pin Definition and Functions

| Pin | Symbol | Function |
|-----|-------------|--------------------------------------|
| 1 | NC | Not Connected |
| 2 | V_s | Supply voltage |
| 3 | V_{sense} | Sense input |
| 4 | GND | IC ground, connect with pin 2 on PCB |
| 5 | NC | Not Connected |
| 6 | EN | Enable (<i>PWM input</i>) |
| 7 | OUT | Output |
| 8 | NC | Not Connected |

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings¹⁾

40 °C < T_j < 150 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified

| Pos. | Parameter | Symbol | Limit values | | Unit | Remark |
|-------|---------------------------|----------------|--------------|------|------|--------------------|
| | | | Min. | Max. | | |
| 4.1.1 | Supply voltage | V_s | -0.3 | 45 | V | |
| 4.1.2 | Sense Voltage | V_{sense} | -0.3 | 7 | V | |
| 4.1.3 | EN Voltage | V_{EN} | -0.3 | 7 | V | |
| 4.1.4 | Output current | I_{out} | – | – | mA | internally limited |
| 4.1.5 | Power Dissipation | P_{tot} | 0 | 500 | mW | |
| 4.1.6 | Junction temperature | T_j | -40 | 150 | °C | |
| 4.1.7 | Storage temperature range | T_{STG} | -55 | 150 | °C | |
| 4.1.8 | ESD resistivity | V_{ESD_HBM} | -4000 | 4000 | V | HBM ²⁾ |

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to EIA/JESD 22-A 114B

4.2 Thermal Resistance

Table 2 Thermal Resistance

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-------|--------------------------------------|------------|--------------|------|------|------|---------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 4.2.1 | Junction to Ambient ^{1) 2)} | R_{thJA} | – | 155 | – | K/W | Footprint only |
| | | | – | 96 | – | K/W | 300 mm ² PCB heatsink area |
| | | | – | 86 | – | K/W | 600 mm ² PCB heatsink area |

1) Not subject to production test, specified by design

2) Package was simulated on a FR4 PCB, 80 x 80 x 1.5 mm; 35 µm Cu

4.3 Electrical Characteristics

Table 3 Electrical Characteristics
 $8\text{ V} < V_S < 28\text{ V}$; $-40\text{ °C} < T_J < 150\text{ °C}$, $EN = 5\text{ V}$; $R_1, R_2 = \text{open}$; all voltages with respect to ground;
 positive current defined flowing into pin; unless otherwise specified

| Pos. | Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------|---------------------------------------|-----------------------|--------|------|------|------|---|
| | | | Min. | Typ. | Max. | | |
| 4.3.1 | Operating current during over voltage | $I_{S_{OV}}$ | – | – | 600 | μA | $V_{out} = 0\text{ V}$; $V_S = 42\text{ V}$; $V_{sense} = 0\text{ mV}$ |
| 4.3.2 | Operating current during open load | $I_{S_{open\ load}}$ | 0.5 | 1.4 | 1.7 | mA | $V_{out} = \text{open}$; $V_{sense} = 0\text{ mV}$ |
| 4.3.3 | Standby current | $I_{S_{standby}}$ | – | – | 300 | nA | $EN = 0\text{ V}$; $V_{sense} = 0\text{ mV}$; $T_J < 85\text{ °C}^{(1)}$ |
| 4.3.4 | Standby current | $I_{S_{standby,HOT}}$ | – | – | 30 | μA | $EN = 0\text{ V}$; $V_{sense} = 0\text{ mV}$ |
| 4.3.51 | Output current | $I_{out,ONCOLD}$ | 40 | – | – | mA | $V_S - V_{out} = 3\text{ V}$; $V_{sense} = 0\text{ mV}$; $T_J = -40\text{ °C}$ |
| 4.3.52 | Output current | $I_{out,ON}$ | 65 | 85 | 110 | mA | $V_S - V_{out} = 3\text{ V}$; $V_{sense} = 0\text{ mV}$; $T_J > 0\text{ °C}^{(1)}$; $T_J < 135\text{ °C}^{(1)}$ |
| 4.3.6 | Output current | $I_{out,ONHOT}$ | 60 | – | – | mA | $V_S - V_{out} = 3\text{ V}$; $V_{sense} = 0\text{ mV}$; $T_J = 150\text{ °C}$ |
| 4.3.7 | Output Leakage current | $I_{out,OFF}$ | – | – | 400 | nA | $EN = 0\text{ V}$; $V_{out} = 0\text{ V}$ |
| 4.3.8 | Current of Sense input | I_{sense} | -5 | – | 0.5 | μA | $V_{out} = 0\text{ V}$; $V_{sense} = 200\text{ mV}$ |
| 4.3.9 | Voltage of Sense input | V_{sense} | 135 | 150 | 165 | mV | $R_1 = 390\text{ }Ω$; $R_2 = 10\text{ }Ω$ See Figure 2 ; $T_J < 115\text{ °C}^{(1)}$ |
| 4.3.10 | Over voltage Protection | $V_{s,OV}$ | 28 | 33 | – | V | – |
| 4.3.11 | Drop Voltage | $V_S - V_{out}$ | – | – | 1.3 | V | $I_{out} < 15\text{ mA}$ $V_{sense} = 0\text{ mV}$; $V_S = 8\text{ V}$ |

EN Input

| | | | | | | | |
|--------|--------------------------|--------------|------|----|-----|----|---|
| 4.3.12 | Current of enable input | I_{EN} | 60 | 90 | 130 | μA | $V_{EN} = 5\text{ V}$ |
| 4.3.13 | High Level voltage range | $V_{EN,ON}$ | 1 | – | 5.5 | V | Use resistors at pin to be CMOS/TTL compatible; See Figure 16 |
| 4.3.14 | Low Level voltage range | $V_{EN,OFF}$ | -0.3 | – | 0.3 | V | Use resistors at pin to be CMOS/TTL compatible; See Figure 16 |

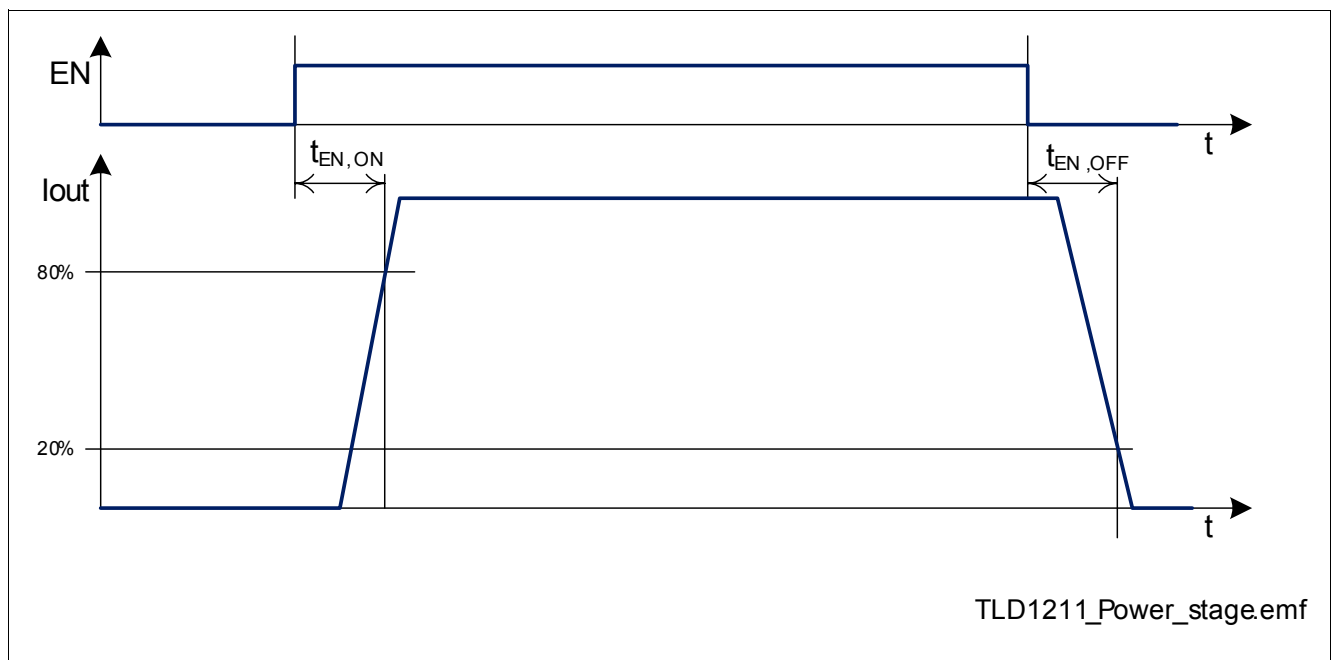
Table 3 Electrical Characteristics (cont'd)

$8\text{ V} < V_S < 28\text{ V}$; $-40\text{ }^\circ\text{C} < T_J < 150\text{ }^\circ\text{C}$, EN = 5 V; $R_1, R_2 = \text{open}$; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified

| Pos. | Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--------|-----------------------------|---------------------|--------|------|------|---------------|--|
| | | | Min. | Typ. | Max. | | |
| 4.3.15 | Turn on time ²⁾ | $t_{\text{EN,ON}}$ | – | – | 65 | μs | $I_{\text{out}100\%} = 15\text{mA}$, See Figure 4 ; $R_1 = 390\ \Omega$; $R_2 = 10\ \Omega$, See Figure 2 |
| 4.3.16 | Turn off time ²⁾ | $t_{\text{EN,OFF}}$ | – | – | 60 | μs | $I_{\text{out}100\%} = 15\text{mA}$; See Figure 4 ; $R_1 = 390\ \Omega$; $R_2 = 10\ \Omega$, See Figure 2 |

1) Not subject to production test, based on temperature characterization

2) When using an external Boost transistor this time is reduced (See also [Figure 16](#))



TLD1211_Power_stage.emf

Figure 4 Timing Diagram

5 Characterization Data

Characterization data based on typical device. TLD1211SJ has been measured in a setup with undefined high thermal resistance.

5.1 Setup 1

Setup according to [Figure 2](#). $R_1 = 390 \Omega$, $R_2 = 10 \Omega$, $V_{EN} = 5 \text{ V}$

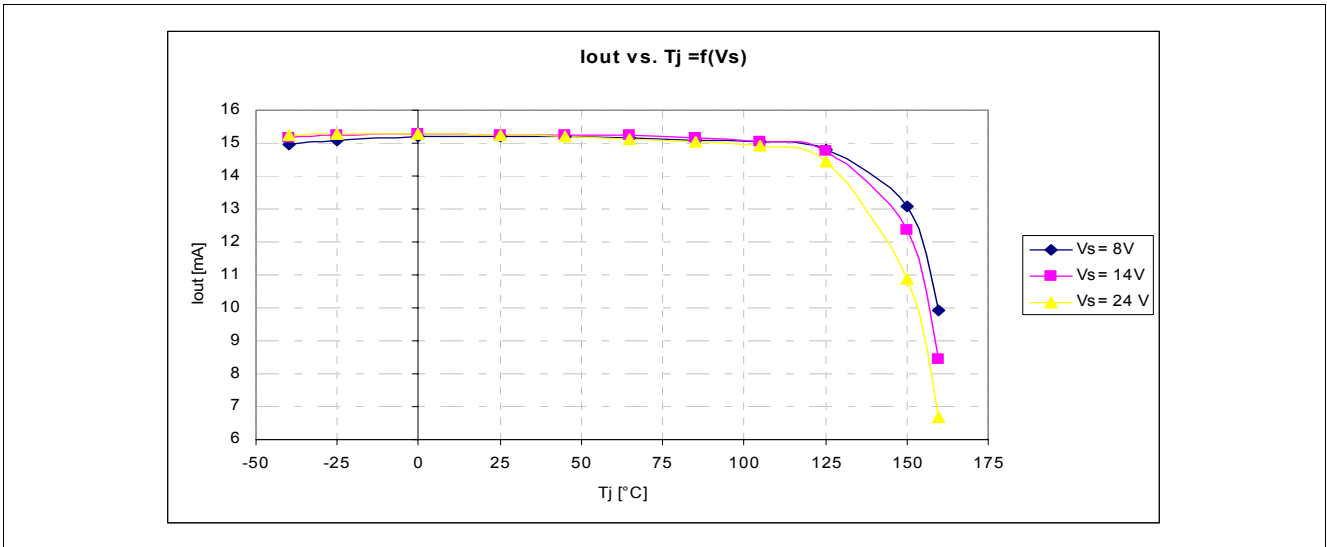


Figure 5 I_{out} vs $T_J = f(V_s)$

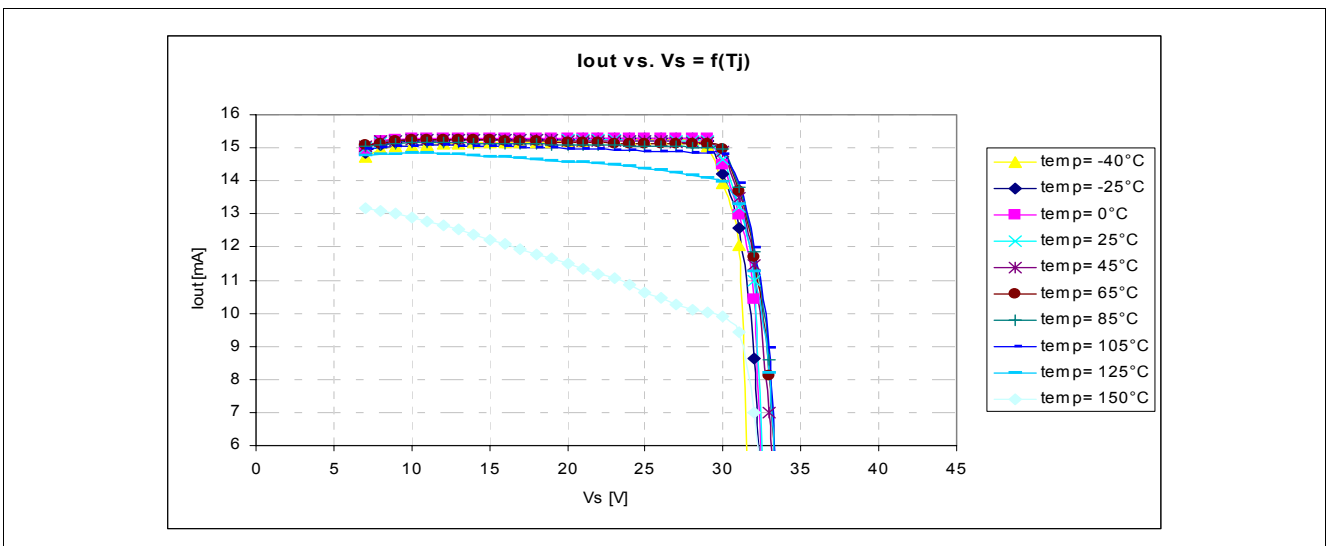


Figure 6 I_{out} vs $V_s = f(T_J)$

5.2 Setup 2

Setup according to **Figure 2**. $R_1 = 0 \Omega$, $R_2 = 0 \Omega$, $V_{out} = 0 V$, $V_{sense} = 0 V$, $V_{EN} = 5 V$

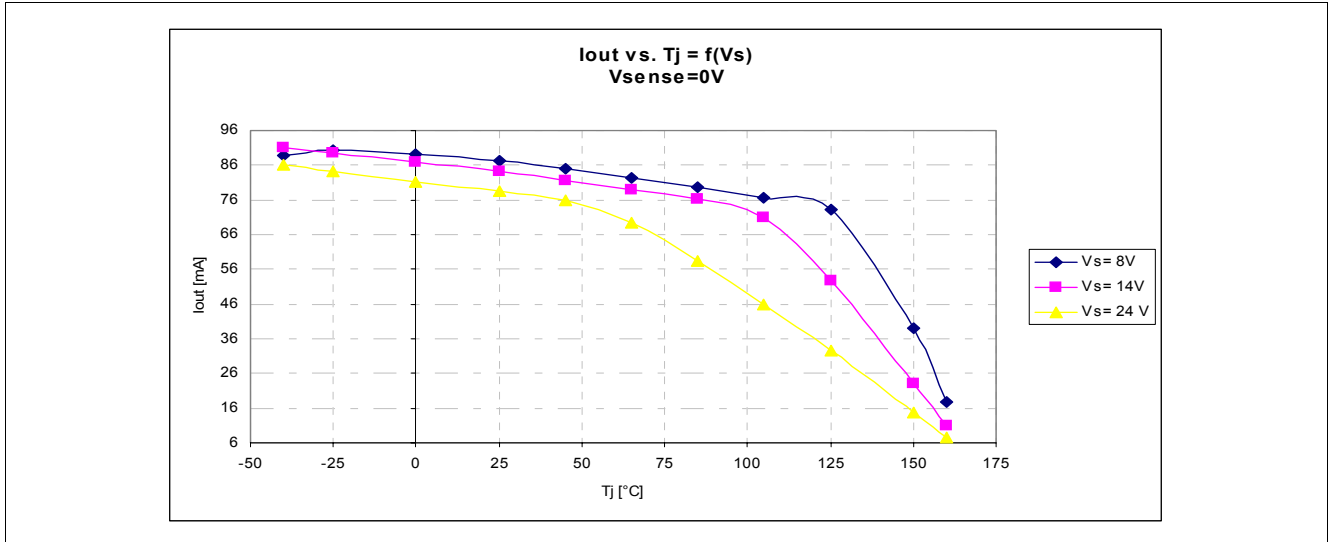


Figure 7 I_{out} vs $T_J = f(V_s)$

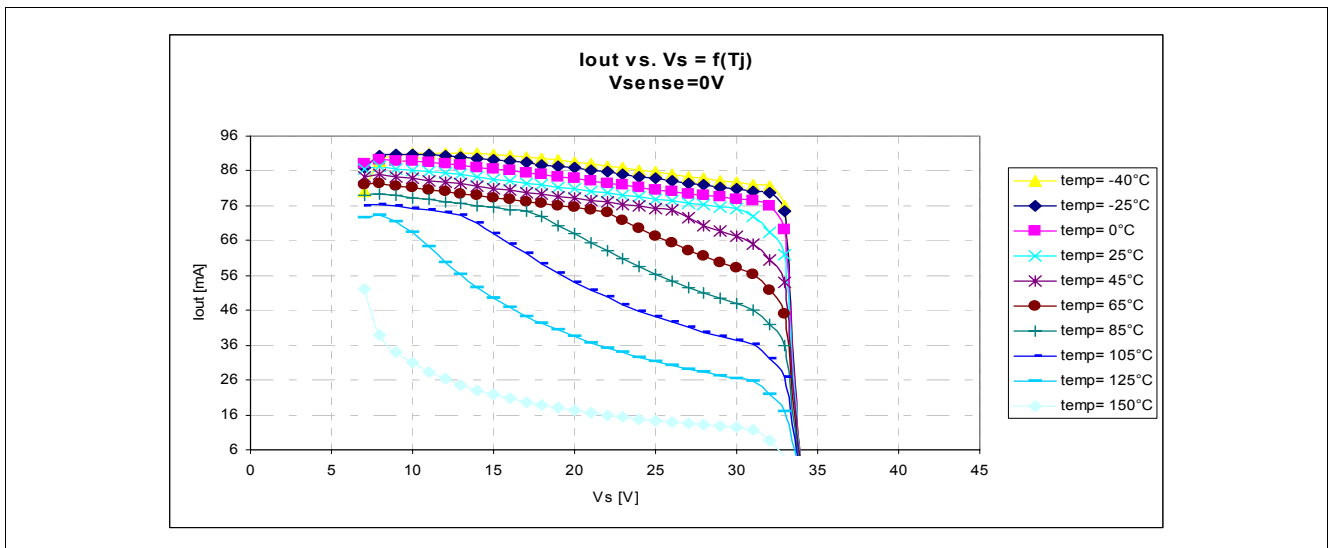


Figure 8 I_{out} vs $V_s = f(T_J)$

5.3 Setup 3

$V_{out} = 0\text{ V}$, V_{sense} = variable, $V_{EN} = 5\text{ V}$

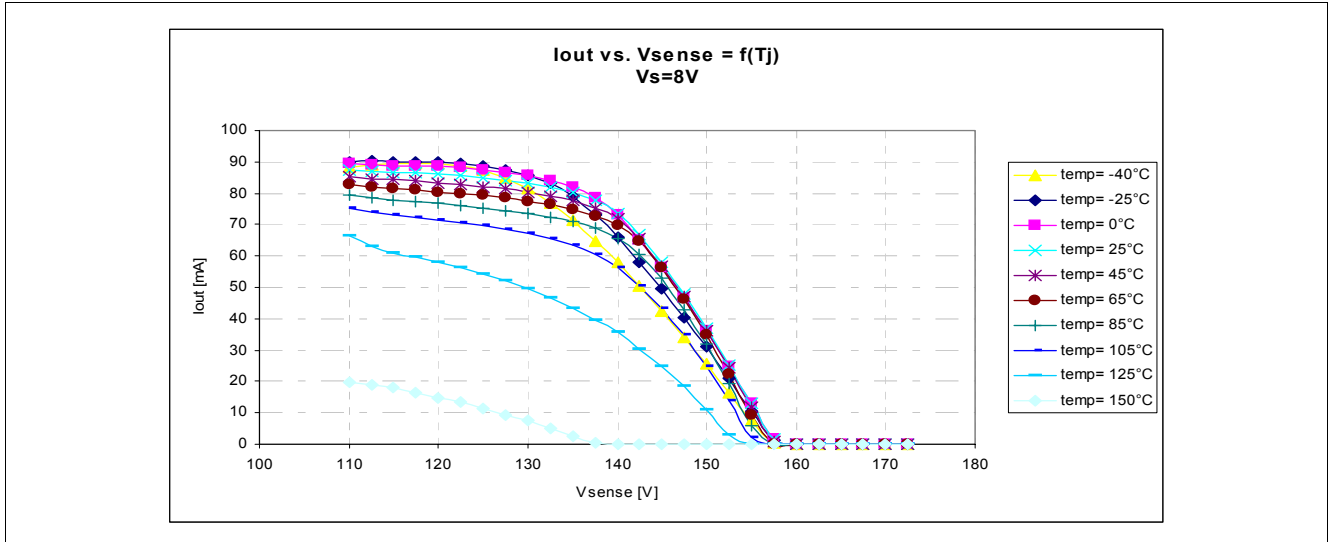


Figure 9 I_{out} vs $V_{sense} = f(T_j)$ at $V_s = 8\text{ V}$

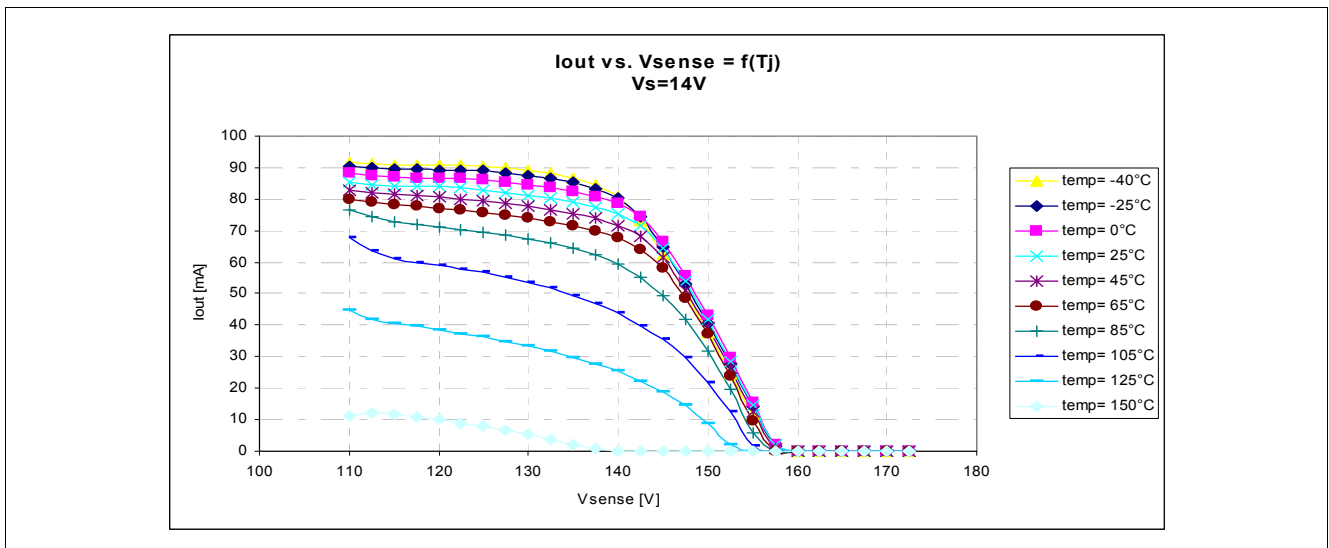
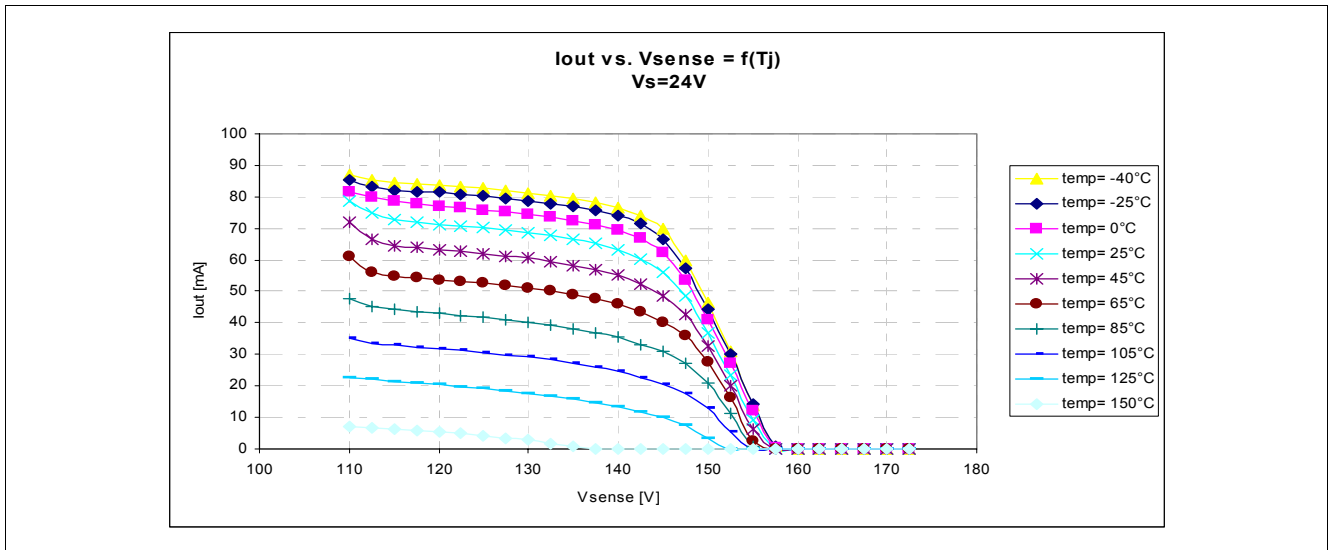
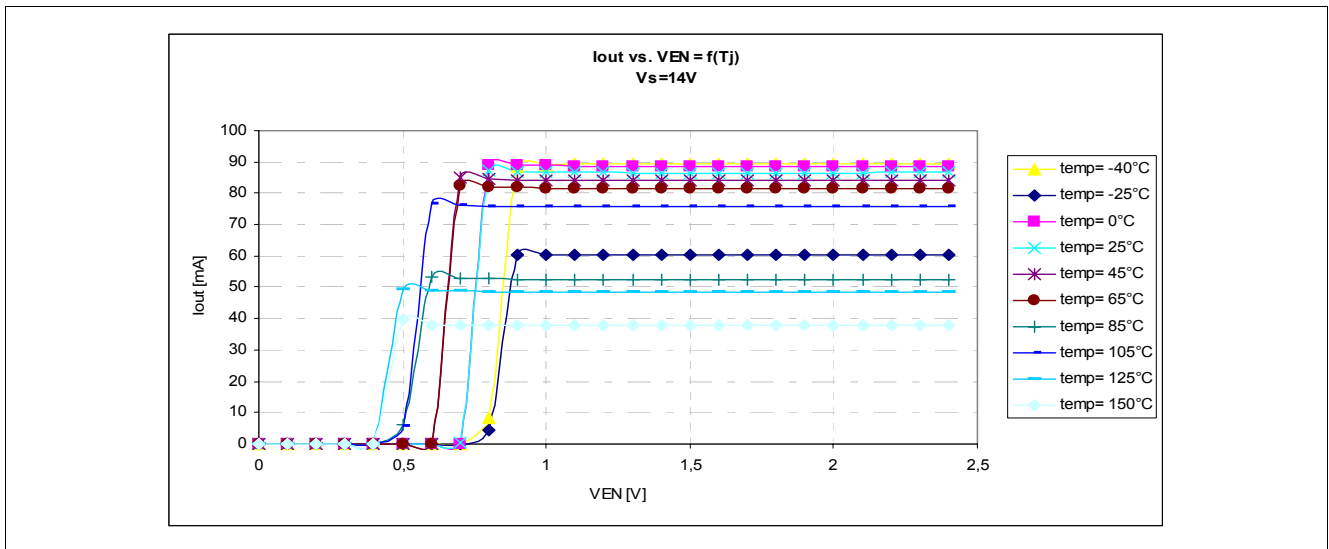


Figure 10 I_{out} vs $V_{sense} = f(T_j)$ at $V_s = 14\text{ V}$



5.4 Setup 4

$V_s = 14\text{ V}$, $V_{out} = 6\text{ V}$, $V_{sense} = 20\text{ mV}$, $V_{EN} = \text{variable}$



5.5 Setup 5

$V_{out} = 0\text{ V}$, $V_{sense} = 0\text{ V}$, $V_{EN} = 0\text{ V}$

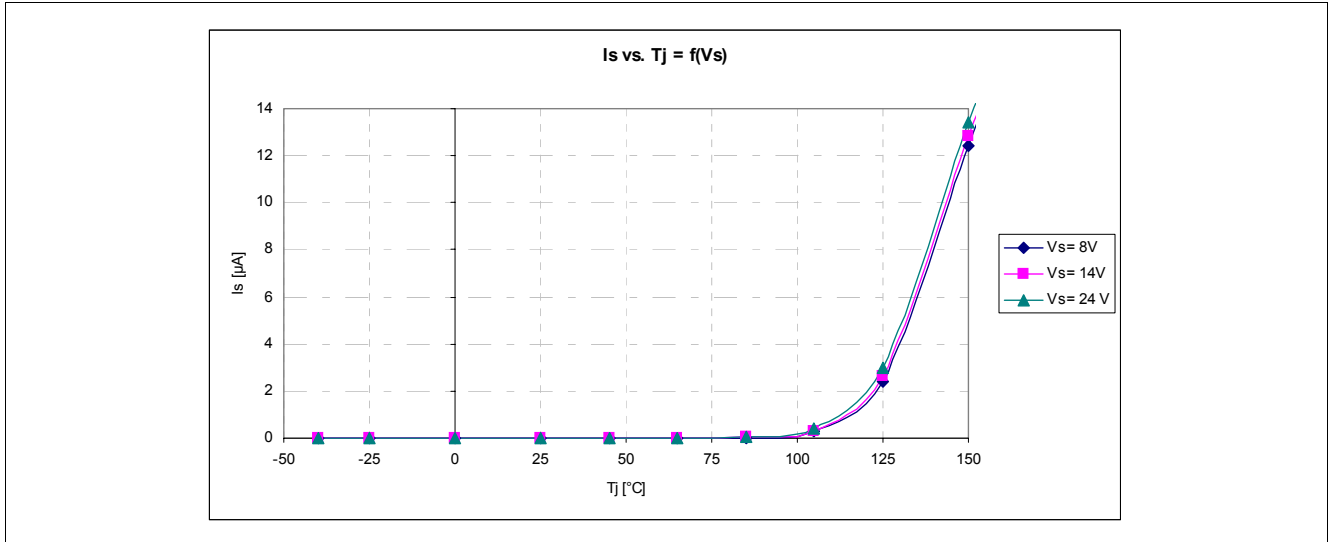


Figure 13 I_s vs $T_j = f(V_s)$

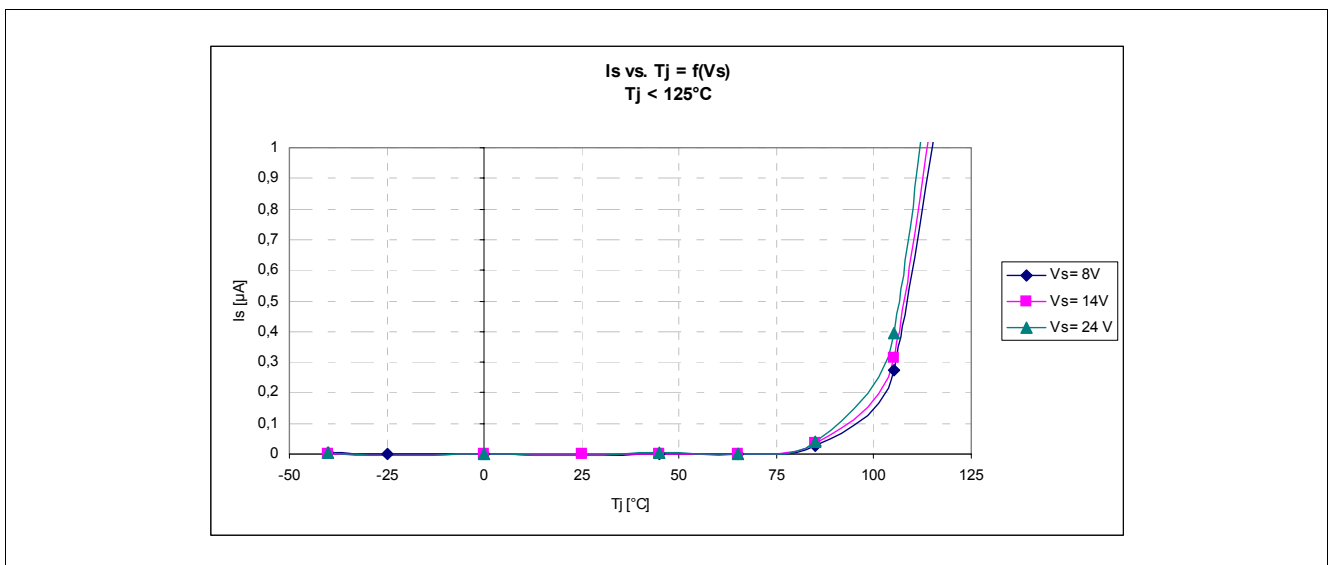


Figure 14 I_s vs $T_j = f(V_s)$, $T_j < 125\text{ °C}$

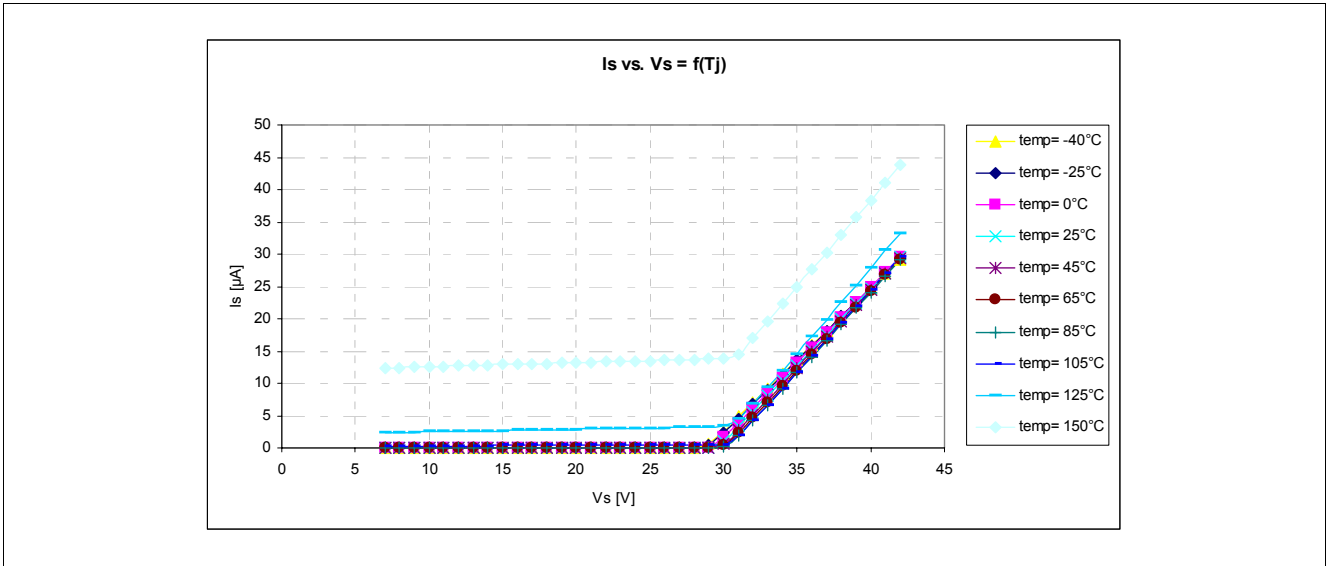


Figure 15 I_s vs $V_s = f(T_J)$

6 Application Information

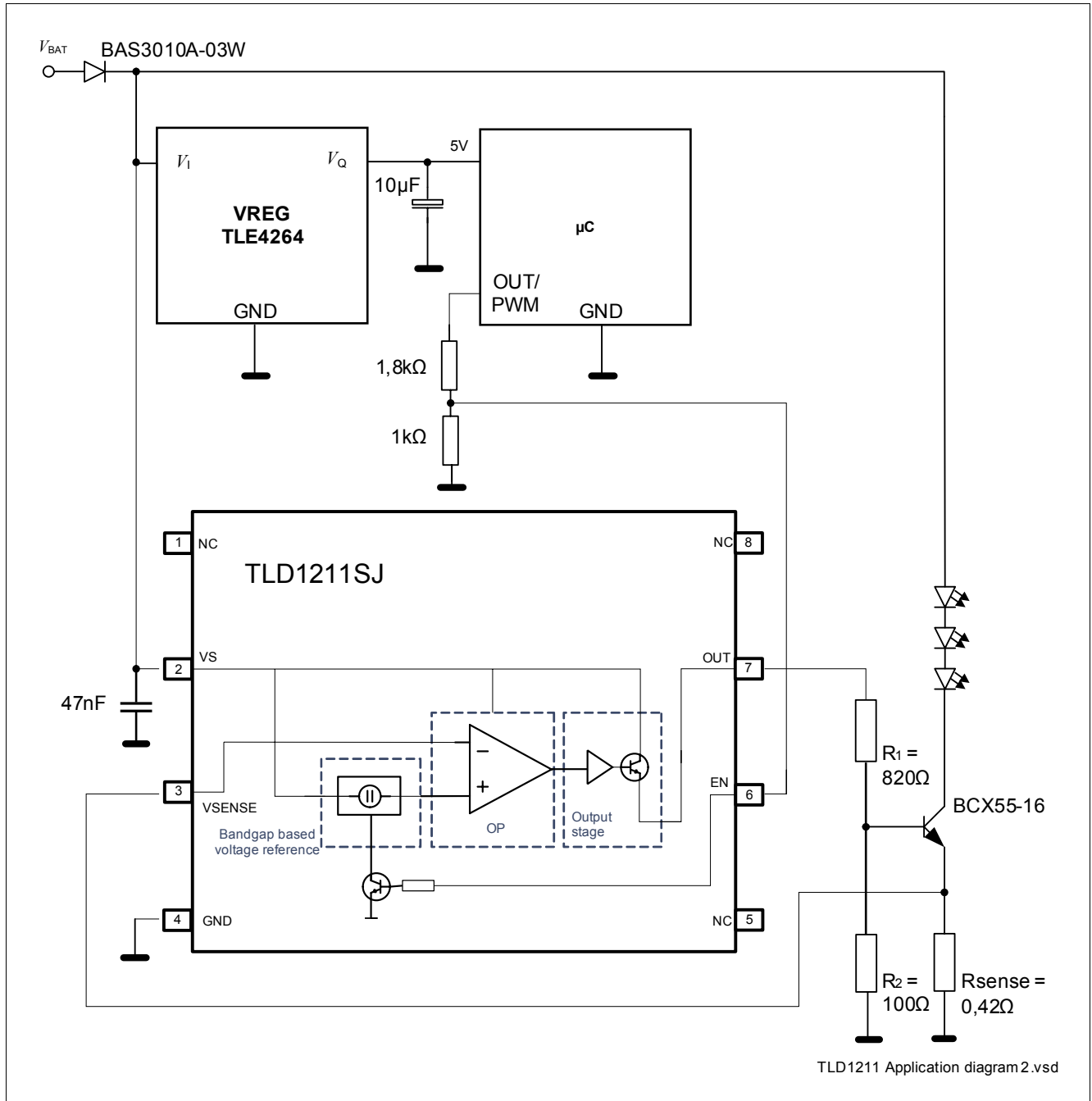


Figure 16 Application Information with External Output Stage

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

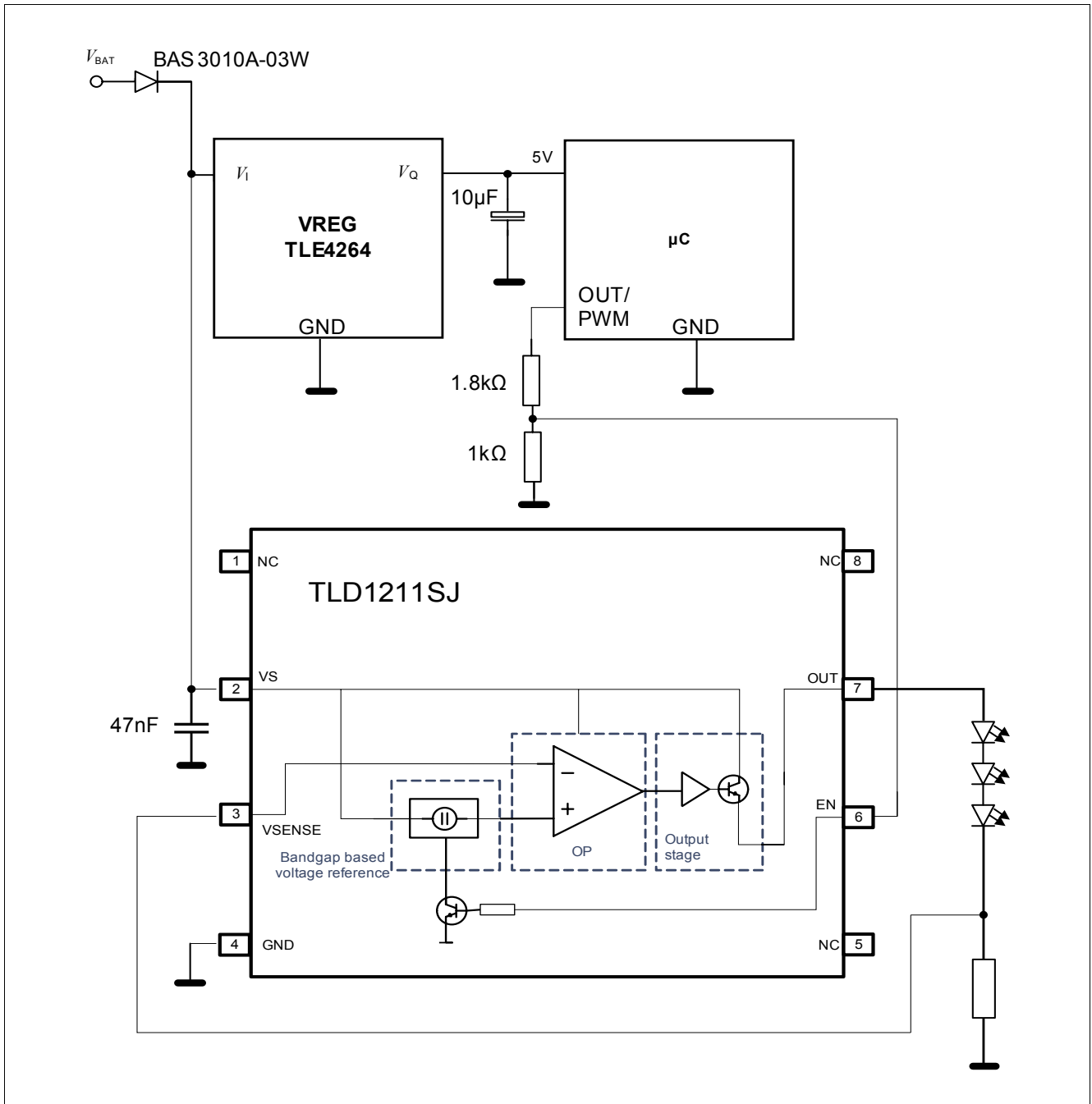


Figure 17 Application Information with Integrated Output Stage Usage

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

7 Package Outlines

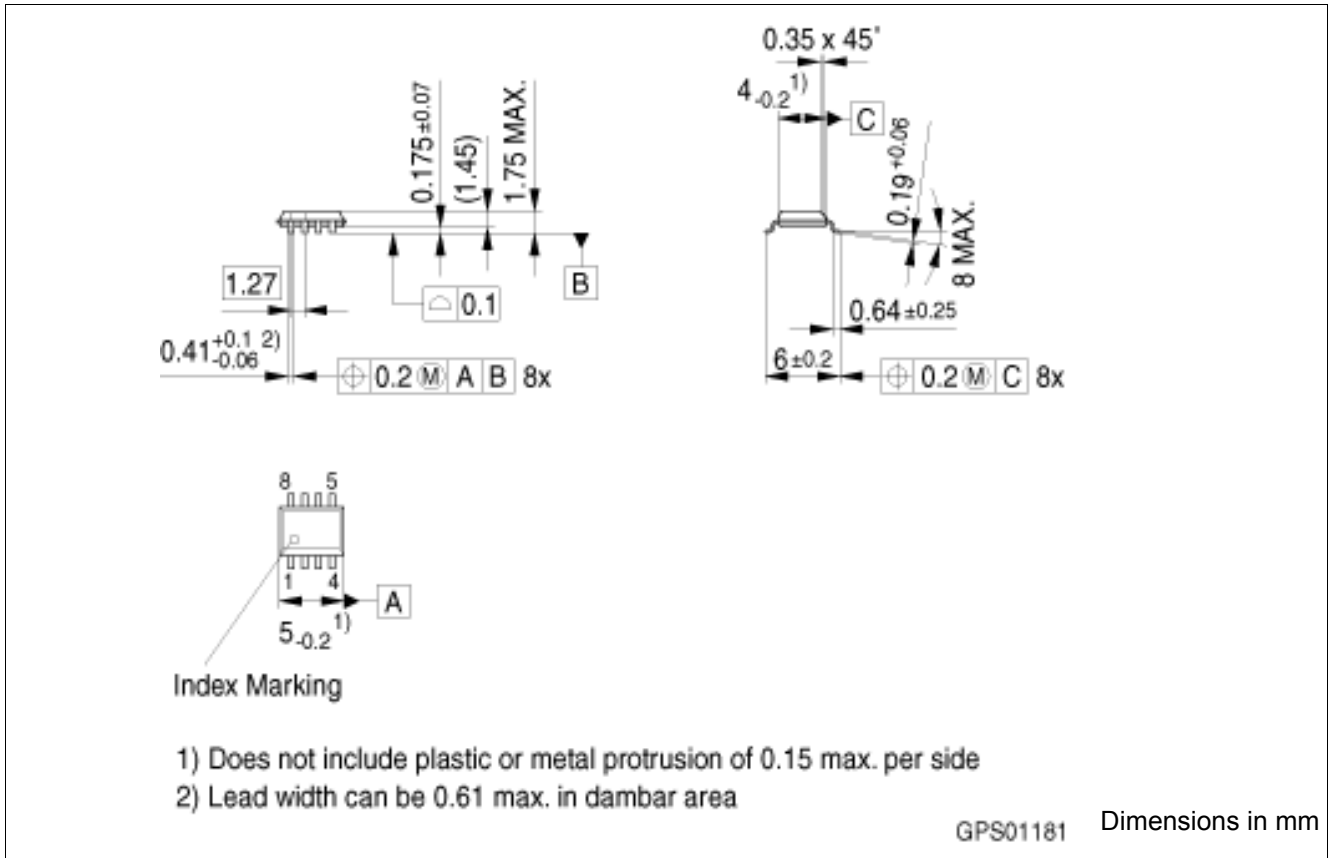


Figure 18 Package Outline; PG-DSO-8-16

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
<http://www.infineon.com/packages>.

8 Revision History

| Revision | Date | Changes |
|----------|------------|------------------|
| 1.0 | 2010-03-26 | Initial revision |

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