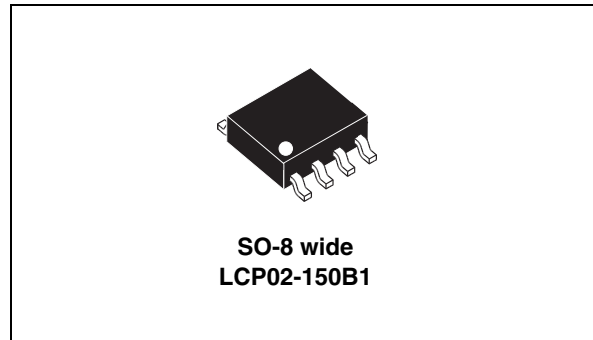


Features

- Protection IC recommended for ringing SLICs
- Wide firing voltage range: -120 V to +120 V
- Low gate triggering current: $I_G = 5 \text{ mA max}$
- Peak pulse current: $I_{PP} = 30 \text{ A (10/1000 } \mu\text{s)}$
- Holding current: $I_H = 150 \text{ mA min.}$
- UL497B approved (file E136224)

Applications

- Dual battery supply voltage SLICs
 - negative battery supply configuration
 - negative and positive battery supply configuration
- Central office (CO)
- Private branch exchange (PBX)
- Digital loop carrier (DLC)
- Asymmetrical digital subscriber line (ADSL G.Lite)
- Fiber in the loop (FITL)
- Wireless local loop (WLL)
- Hybrid fiber coax (HFC)
- ISDN terminal adapter
- Cable modem



Description

The LCP02-150B1 has been developed to protect SLICs operating on both negative and positive battery supplies, as well as high voltage SLICs. It provides crowbar mode protection for both TIP and RING lines. The surge suppression is managed for each wire by two thyristor structures, one dedicated to positive surges the second one for negative surges. Both positive and negative threshold levels are programmable by two gates (G_n and G_p). The use of transistors decreases the battery currents during surge suppression.

LCP02-150B1 can be used to help equipment to meet various standards such as UL1950, IEC 60950 / CSAC22.2, UL1459 and TIA-968-A (formerly FCC part68). A Trisil™ meets UL94 V0 (Trisils are UL497B approved - file: E136224).

TM: Trisil is a trademark of STMicroelectronics

1 Characteristics

Figure 1. Functional diagram

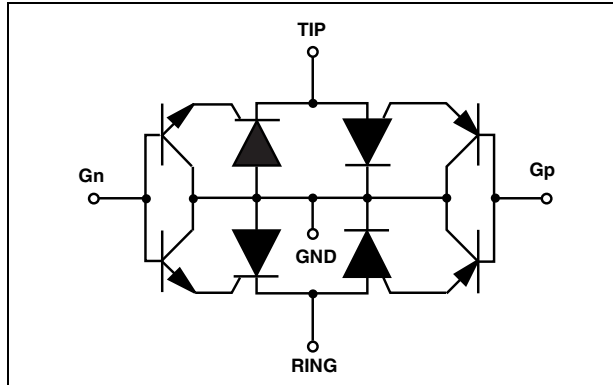


Figure 2. Pin-out configuration

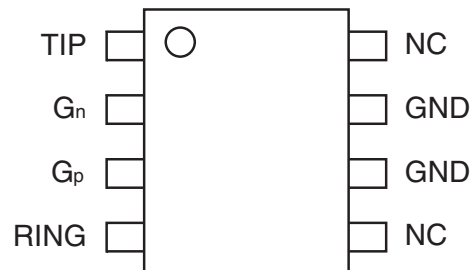
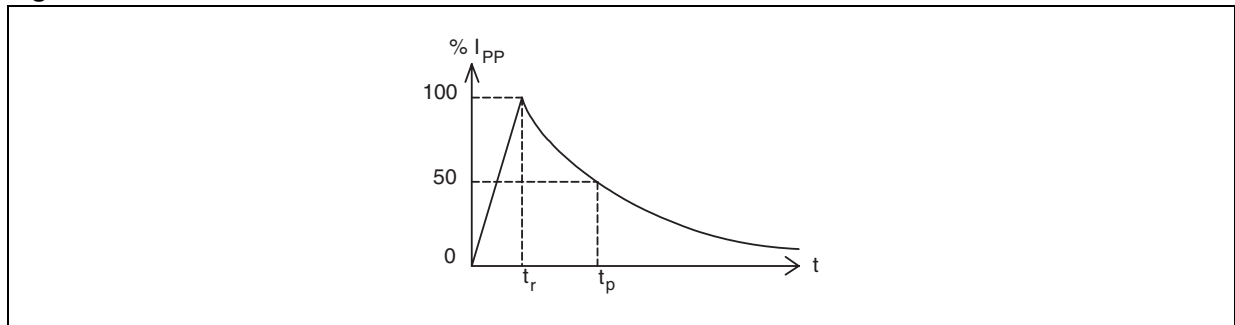


Table 1. Compliant with the following standards

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR1089 core first level	2500 1000	2/10 μ s 10/1000 μ s	500 100	2/10 μ s 10/1000 μ s	20.0 24
GR1089 core second level	5000	2/10 μ s	500	2/10 μ s	40
GR1089 core intra-building	1500	2/10 μ s	100	2/10 μ s	0
ITU-T-K20/K21	6000 4000 1500	10/700 μ s	150 100 37.5	5/310 μ s	94 49 0
ITU-T-K20 (IEC61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
IEC61000-4-5	4000 4000	10/700 μ s 1.2/50 μ s	100 100	5/310 μ s 8/20 μ s	49 0
TIA-968-A (formerly FCC part 68) type A	1500 800	10/160 μ s 10/560 μ s	200 100	10/160 μ s 10/560 μ s	20 15
TIA-968-A (formerly FCC part 68) type B	1000	9/220 μ s	25	5/320 μ s	0

Table 2. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000 μs 5/310 μs 2/10 μs	30 45 100	A
I_{TSM}	Non repetitive surge peak on-state current ($F = 50\text{ Hz}$) I_{TSM} value specified for each line I_{TSM} value can be applied on both lines at the same time (GND capability is twice the line I_{TSM})	$t_p = 0.2\text{ s}$ $t_p = 1\text{ s}$ $t_p = 15\text{ min.}$	9 6 1.9	A
V_{Gn} V_{Gp}	Negative battery voltage range Positive battery voltage range		-120 to 0 0 to +120	V
T_j	Operating junction temperature range		-40 to +125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-55 to +150	$^{\circ}\text{C}$
T_L	Lead solder temperature (10 s duration)		260	$^{\circ}\text{C}$

Figure 3. Pulse waveform**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient	150	$^{\circ}\text{C/W}$

Table 4. Parameters related to the negative suppressor

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{Gn}	Negative gate trigger current	$V_{Gn/GND} = -60\text{ V}$ Measured at 50 Hz		5	mA
I_H	Holding current (see Figure 4)	Go-No Go test, $V_{Gn} = -60\text{ V}$	150		mA
V_{DGL-}	Dynamic switching voltage Gn / Line ⁽¹⁾	$V_{Gn/GND} = -60\text{ V}$ 10/700 μs 2 kV $R_p = 25\text{ }\Omega$ $I_{PP} = 30\text{ A}$ 1.2/50 μs 2 kV $R_p = 25\text{ }\Omega$ $I_{PP} = 30\text{ A}$		8 15	V

1. The V_{DGL} value is the difference between the peak line voltage during the surge and the programmed gate voltage.

Table 5. Parameters related to the positive suppressor

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{Gp}	Positive gate trigger current	$V_{Gp/GND} = 60\text{ V}$, measured at 50 Hz		5	mA
V_{DGL+}	Dynamic switching voltage Gp / Line ⁽¹⁾	$V_{Gp/GND} = 60\text{ V}$ 10/700 μs 2 kV $R_P = 25\ \Omega$ $I_{PP} = 30\text{ A}$ 1.2/50 μs 2 kV $R_P = 25\ \Omega$ $I_{PP} = 30\text{ A}$		8 35	V

1. The V_{DGL} value is the difference between the peak line voltage during the surge and the programmed gate voltage.

Table 6. Parameters related to line/GND

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_R	Reverse leakage current	$T_J = 25\text{ }^\circ\text{C}$ $V_{LINE} = +120\text{ V}$ $V_{Gp/LINE} = +1\text{ V}$ $T_J = 25\text{ }^\circ\text{C}$ $V_{LINE} = -120\text{ V}$ $V_{Gn/LINE} = -1\text{ V}$		5 5	μA
C_{off}	Capacitance LINE/GND	$V_R = -3\text{ V}$, $F = 1\text{ MHz}$, $V_{Gp} = 60\text{ V}$, $V_{Gn} = -60\text{ V}$		60	pF

Table 7. Recommended gate capacitance

Symbol	Component	Min.	Typ.	Max.	Unit
C_G	Gate decoupling capacitance	100	220		nF

Figure 4. Relative variation of holding current versus junction temperature

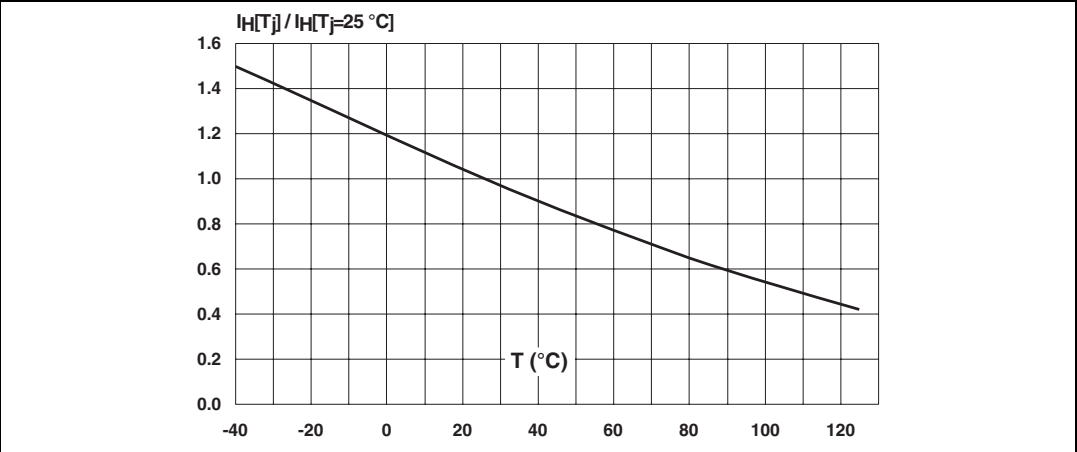


Figure 5. Maximum non repetitive surge peak on state current versus overload duration

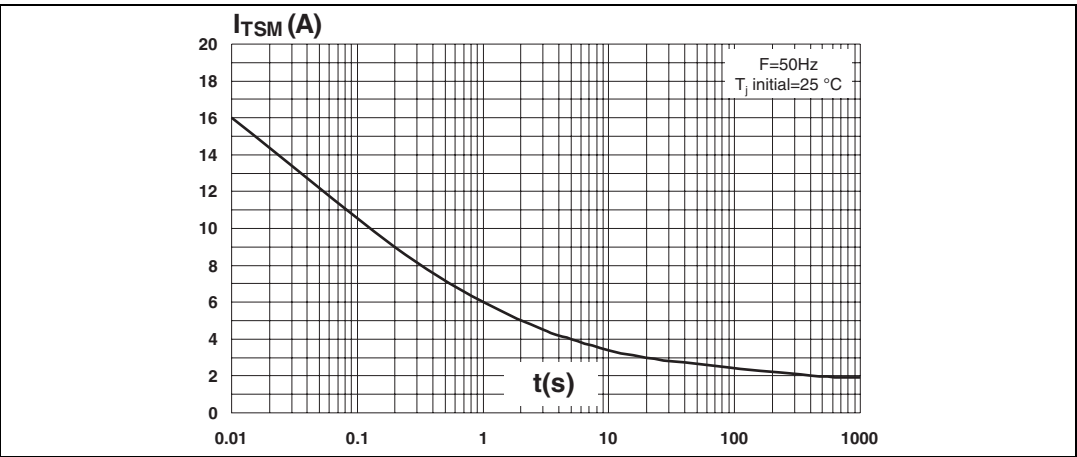
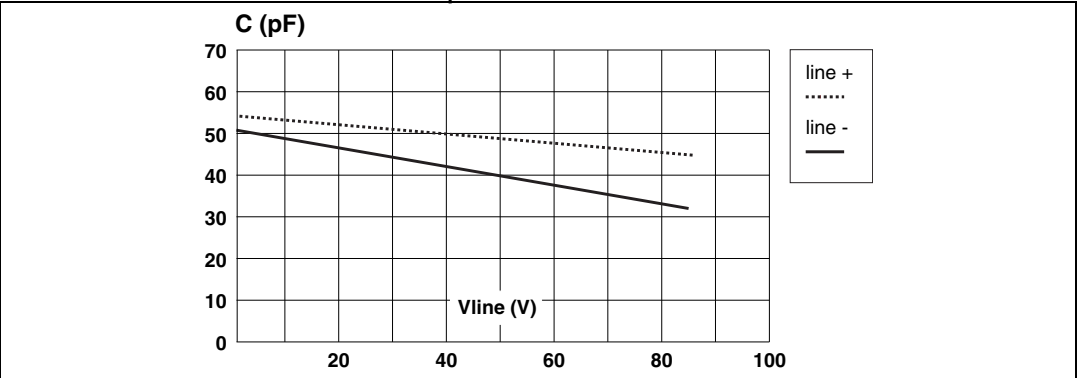


Figure 6. Capacitance versus reverse applied voltage (typical values) with $V_{Gn} = -90\text{ V}$ and $V_{Gp} = +90\text{ V}$



2 Technical information

Figure 7. LCP02 concept behavior

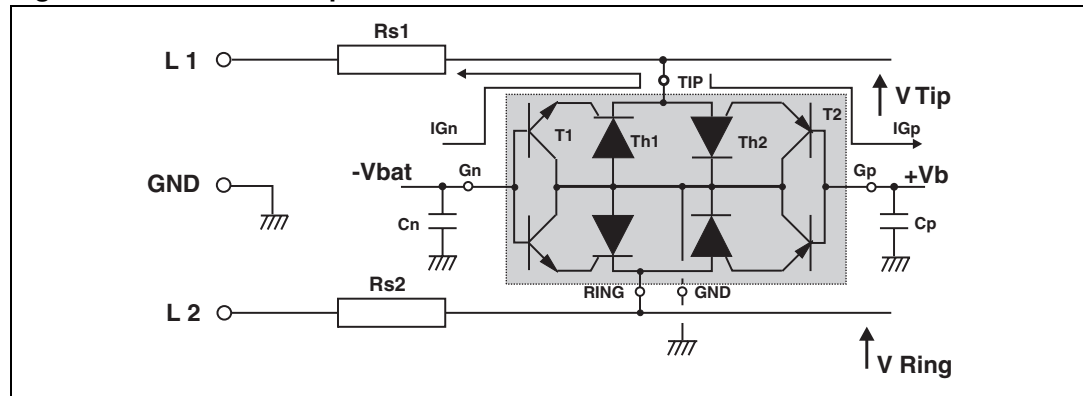


Figure 7 shows the classical protection circuit using the LCP02 crowbar concept. This topology has been developed to protect the new two-battery voltage SLICs. It allows both positive and negative firing thresholds to be programmed. The LCP02 has two gates (Gn and Gp). Gn is biased to negative battery voltage -Vbat, while Gp is biased to the positive battery voltage +Vb.

When a negative surge occurs on one wire (L1 for example), a current I_{Gn} flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1 which fires. All the surge current flows through the ground. After the surge, when the current flowing through Th1 becomes less negative than the negative holding current I_{H-} , Th1 switches off. This holding current I_{H-} is temperature dependant as per *Figure 4*

When a positive surge occurs on one wire (L1 for example), a current I_{Gp} flows through the base of the transistor T2 and then injects a current in the gate of the thyristor Th2 which fires. All the surge current flows through the ground. After the surge, when the current flowing through Th2 becomes less positive than the positive holding current I_{H+} , Th2 switches off. This holding current I_{H+} , typically 20 mA at 25 °C, is temperature dependant and the same *Figure 4* also applies.

The capacitors Cn and Cp are used to speed up the crowbar structure firing during the fast rise or fall edges. This allows minimization of the dynamic breakover voltage at the SLIC TIP and RING inputs during fast surges. Please note that these capacitors are generally available around the SLIC. To be efficient they have to be as close as possible to the LCP02 gate pins (Gn and Gp) and to the reference ground track (or plan). The optimized value for Cn and Cp is 220nF.

The series resistors Rs1 and Rs2 designed in [Figure 7](#) represent the fuse resistors or the PTCs which are needed to withstand the power contact or the power induction tests imposed by the country standards. Taking this factor into account, the actual lightning surge current flowing through the LCP02-150B1 is equal to:

$$I_{\text{surge}} = V_{\text{surge}} / (R_g + R_s)$$

With

V_{surge} = peak surge voltage imposed by the standard.

R_g = series resistor of the surge generator

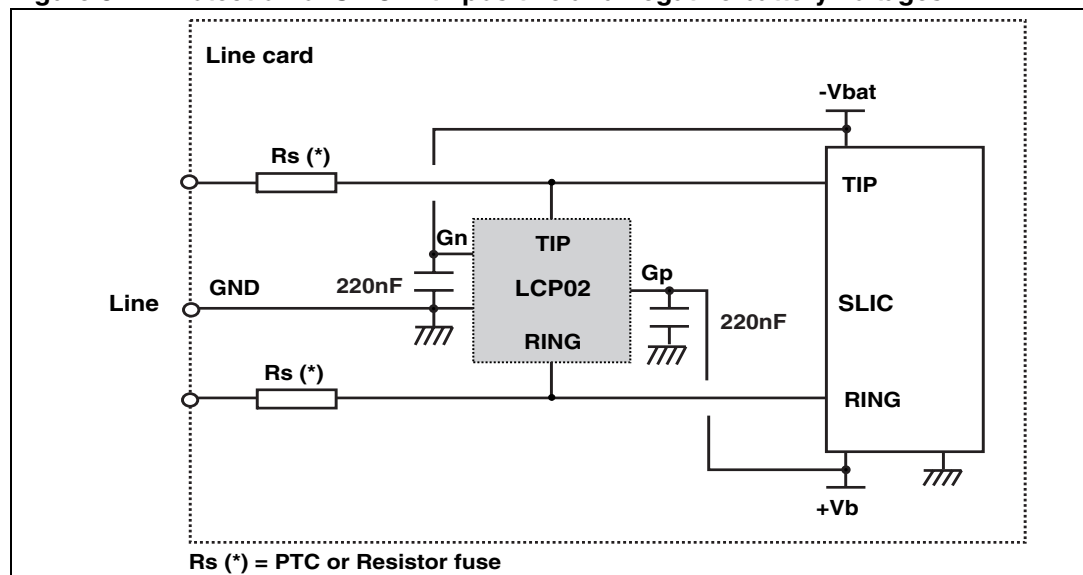
R_s = series resistor of the line card (e.g. PTC)

For a line card with 50 Ω of series resistors which has to be qualified under GR-1089 1000 V 10/1000 μ s surge, the present current through the LCP02-150B1 is equal to:

$$I_{\text{surge}} = 1000 / (10 + 50) = 17 \text{ A}$$

The LCP02-150B1 topology is particularly optimized for the new telecom applications such as fiber in the loop, WLL systems, decentralized central office for example.

Figure 8. Protection of SLIC with positive and negative battery voltages



[Figure 8](#) shows the classical protection topology for SLIC using both positive and negative battery voltages. With such a protection the SLIC is protected against surge over +Vb and lower than -Vbat. In this case, +Vb can be programmed up to +120 V while -Vbat can be programmed down to -120 V.

3 Package information

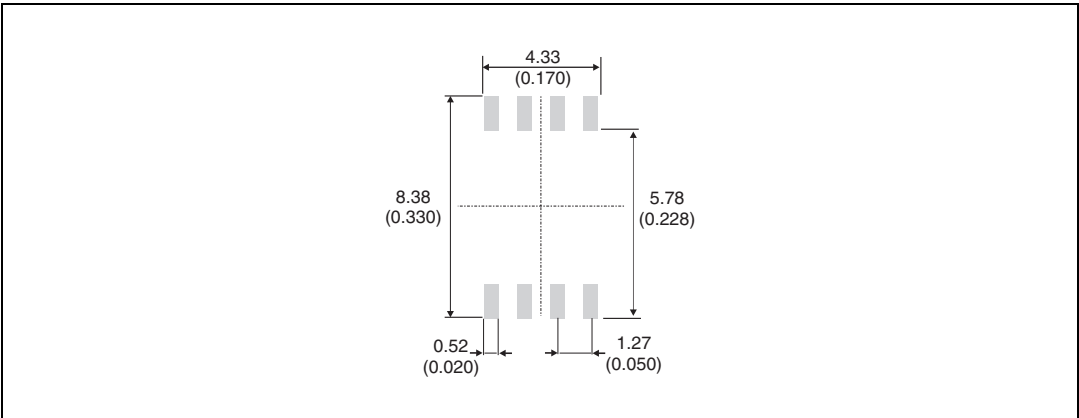
- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 8. SO-8 wide dimensions

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.50			0.099
A1	0.00		0.25	0.000		0.010
A2	1.51		2.00	0.059		0.079
b	0.35	0.40	0.51	0.013	0.016	0.020
c	0.10	0.20	0.35	0.003	0.008	0.014
D	5.14	5.24	5.34	0.202	0.206	0.210
E	5.02		6.22	0.197		0.245
E1	7.62		8.89	0.30		0.35
e		1.27			0.05	
K	0°		10°	0°		10°
L	0.50		0.80	0.019		0.032

Figure 9. SO-8 wide footprint measurements in mm (inches)



4 Ordering information

Table 9. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP02-150B1RL	LCP02	SO-8-Wide	0.13g	1500	Tape and reel

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
Sep-2000	4A	Previous release.
17-Oct-2008	5	Reformatted to current standards. V_{line} updated to 120 V in Table 6 .
28-Jun-2010	6	Removed 1 kV values for V_{DGL-} in Table 4 , and V_{DGL+} in Table 5 . Added symbol and trademark statement for Trisil on the cover page. Updated package dimension graphics.
23-Feb-2012	7	Updated nomenclature for GN to Gn and GP to Gp.
19-Jun-2012	8	Updated dimension D in SO-8 wide

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