

# MC14569B

## Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-Channel and N-Channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

### Features

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 1)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

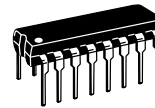
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



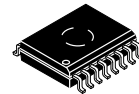
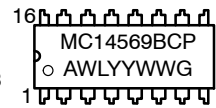
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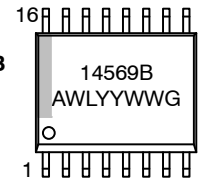
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16 WB  
DW SUFFIX  
CASE 751G



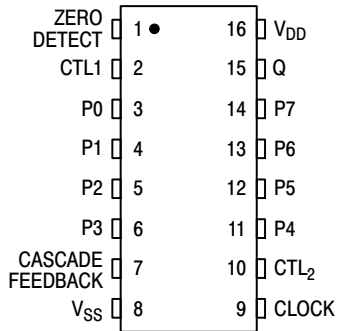
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

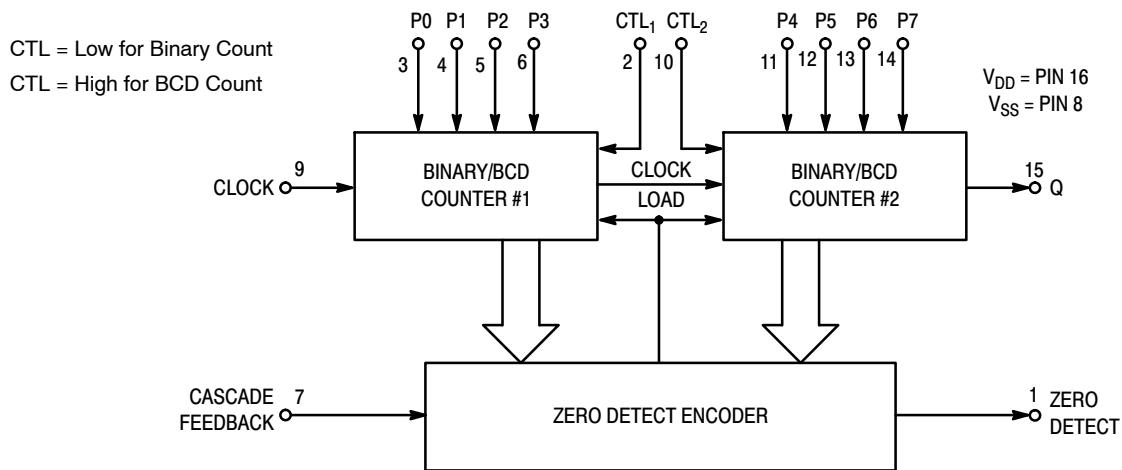
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## PIN ASSIGNMENT



## BLOCK DIAGRAM



## ORDERING INFORMATION

Device	Package	Shipping†
MC14569BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14569BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14569BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level   "1" Level	V <sub>OL</sub>	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
15			-	0.05	-	0	0.05	-	0.05		
	"1" Level	V <sub>OH</sub>	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
10			9.95	-	9.95	10	-	9.95	-		
15			14.95	-	14.95	15	-	14.95	-		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"0" Level	V <sub>IL</sub>	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
15			-	4.0	-	6.75	4.0	-	4.0		
	"1" Level	V <sub>IH</sub>	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
10			7.0	-	7.0	5.50	-	7.0	-		
15			11	-	11	8.25	-	11	-		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source	I <sub>OH</sub>	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
10			-1.6	-	-1.3	-2.25	-	-0.9	-		
15			-4.2	-	-3.4	-8.8	-	-2.4	-		
	Sink	I <sub>OL</sub>	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
10			1.6	-	1.3	2.25	-	0.9	-		
15			4.2	-	3.4	8.8	-	2.4	-		
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	-	5.0	-	0.005	5.0	-	150	μAdc	
		10	-	10	-	0.010	10	-	300		
		15	-	20	-	0.015	20	-	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0 10 15	$I_T = (0.58 \mu\text{A}/\text{kHz}) f + I_{DD}$ $I_T = (1.20 \mu\text{A}/\text{kHz}) f + I_{DD}$ $I_T = (1.95 \mu\text{A}/\text{kHz}) f + I_{DD}$							μAdc	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

Characteristic	Symbol	V <sub>DD</sub> Vdc	All Types			Unit		
			Min	Typ (Note 5)	Max			
Output Rise Time	t <sub>TLH</sub>	5.0	–	100	200	ns		
		10	–	50	100			
		15	–	40	80			
Output Fall Time	t <sub>THL</sub>	5.0	–	100	200	ns		
		10	–	50	100			
		15	–	40	80			
Turn-On Delay Time Zero Detect Output	t <sub>PLH</sub>	5.0	–	420	700	ns		
		10	–	175	300			
		15	–	125	250			
		Q Output	t <sub>PLH</sub>	5.0	–	675	1200	ns
				10	–	285	500	
				15	–	200	400	
Turn-Off Delay Time Zero Detect Output	t <sub>PHL</sub>	5.0	–	380	600	ns		
		10	–	150	300			
		15	–	100	200			
		Q Output	t <sub>PHL</sub>	5.0	–	530	1000	ns
				10	–	225	400	
				15	–	155	300	
Clock Pulse Width	t <sub>WH</sub>	5.0	300	100	–	ns		
		10	150	45	–			
		15	115	30	–			
Clock Pulse Frequency	f <sub>cl</sub>	5.0	–	3.5	2.1	MHz		
		10	–	9.5	5.1			
		15	–	13.0	7.8			
Clock Pulse Rise and Fall Time	t <sub>TLH</sub> , t <sub>THL</sub>	5.0	NO LIMIT			μs		
		10						
		15						

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## SWITCHING WAVEFORMS

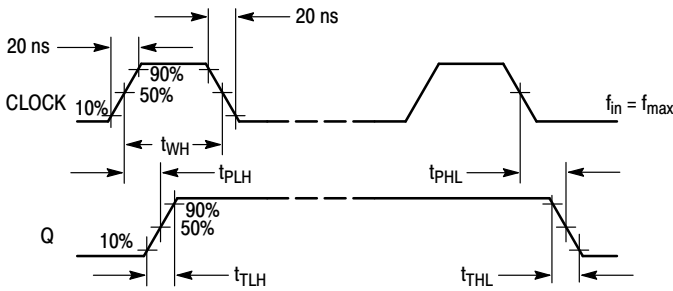


Figure 1.

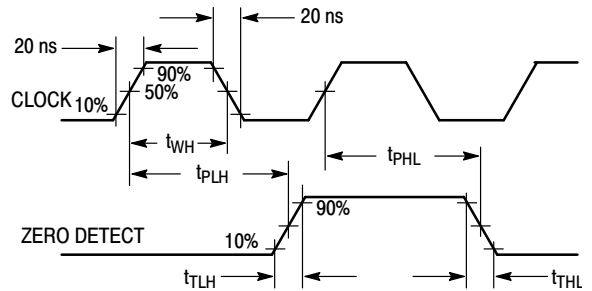


Figure 2.

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## PIN DESCRIPTIONS

### INPUTS

**P0, P1, P2, P3 (Pins 3, 4, 5, 6)** – Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

**P4, P5, P6, P7 (Pins 11, 12, 13, 14)** – Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

**Clock (Pin 9)** – Preset data is decremented by one on each positive transition of this signal.

### OUTPUTS

**Zero Detect (Pin 1)** – This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q (Pin 15)** – Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

### CONTROLS

**Cascade Feedback (Pin 7)** – This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don’t cares.” Refer to Table 1 for output characteristics.

**CTL<sub>1</sub> (Pin 2)** – This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

**CTL<sub>2</sub> (Pin 10)** – This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

### SUPPLY PINS

**V<sub>SS</sub> (Pin 18)** – Negative Supply Voltage. This pin is usually connected to ground.

**V<sub>DD</sub> (Pin 16)** – Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

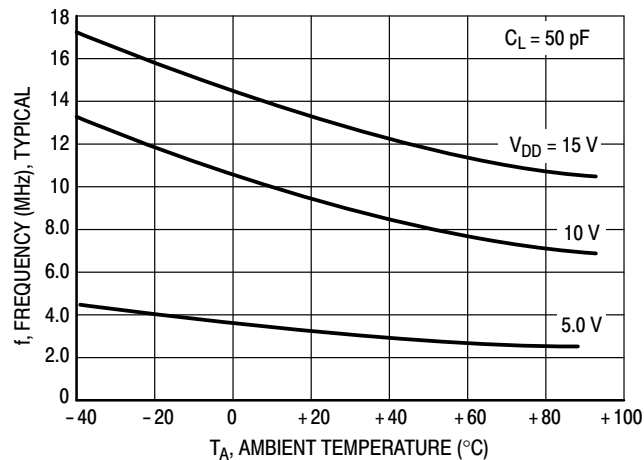
## OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles,

one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V<sub>DD</sub>.





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**Table 3 Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	1	1	0	0	1	19	X		
0	0	1	0	0	0	0	0	20	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	1	1	0	0	0	0	30	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	0	0	0	0	0	40	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	1	0	0	0	0	50	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	0	0	0	0	0	60	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	1	0	0	0	0	70	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓	
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	0	0	0	0	90	90		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	1	1	1	0	0	0	0	150	150		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	1	1	1	1	0	0	1	159	159		
80	40	20	10	8	4	2	1				Bit Value
Counter #2 Binary				Counter #1 BCD							Counting Sequence

X = No Output (Always Low)

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**Table 4 Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	1	1	0	0	0	0	48	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	0	0	0	0	0	0	64	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	0	1	0	0	0	0	80	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	1	1	0	0	0	0	112	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	0	0	0	0	0	128	128	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	0	0	0	0	144	144	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	1	1	1	1	159	159	
$2^7$ 128	$2^6$ 64	$2^5$ 32	$2^4$ 16	$2^3$ 8	$2^2$ 4	$2^1$ 2	$2^0$ 1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

Q Output Active  
↓

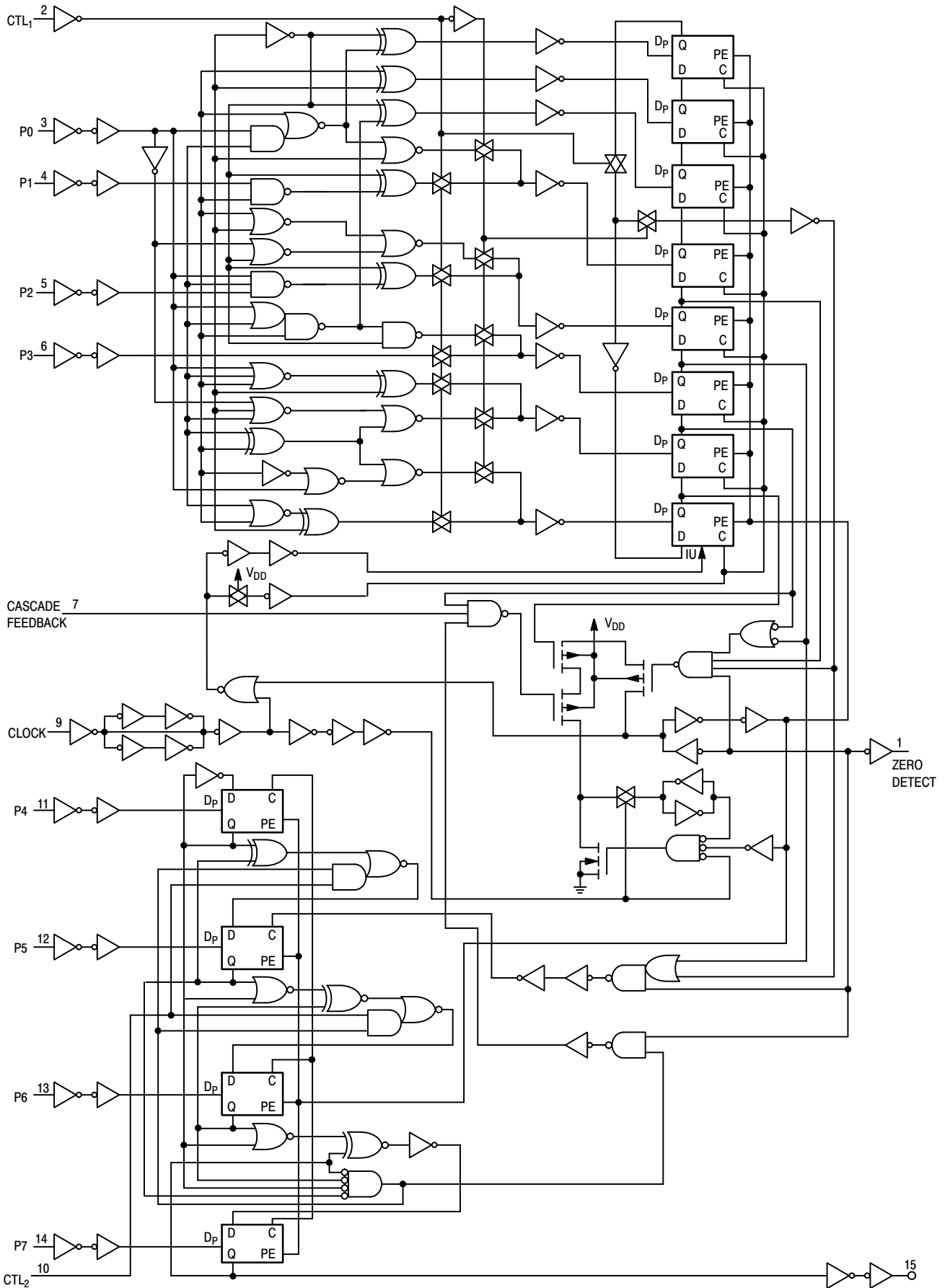
X = No Output (Always Low)





# MC14569B

## LOGIC DIAGRAM



# MC14569B

## TYPICAL APPLICATIONS

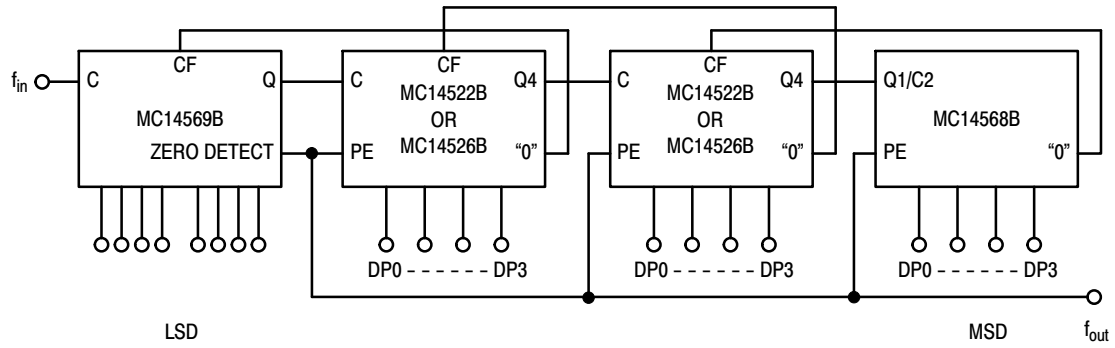


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

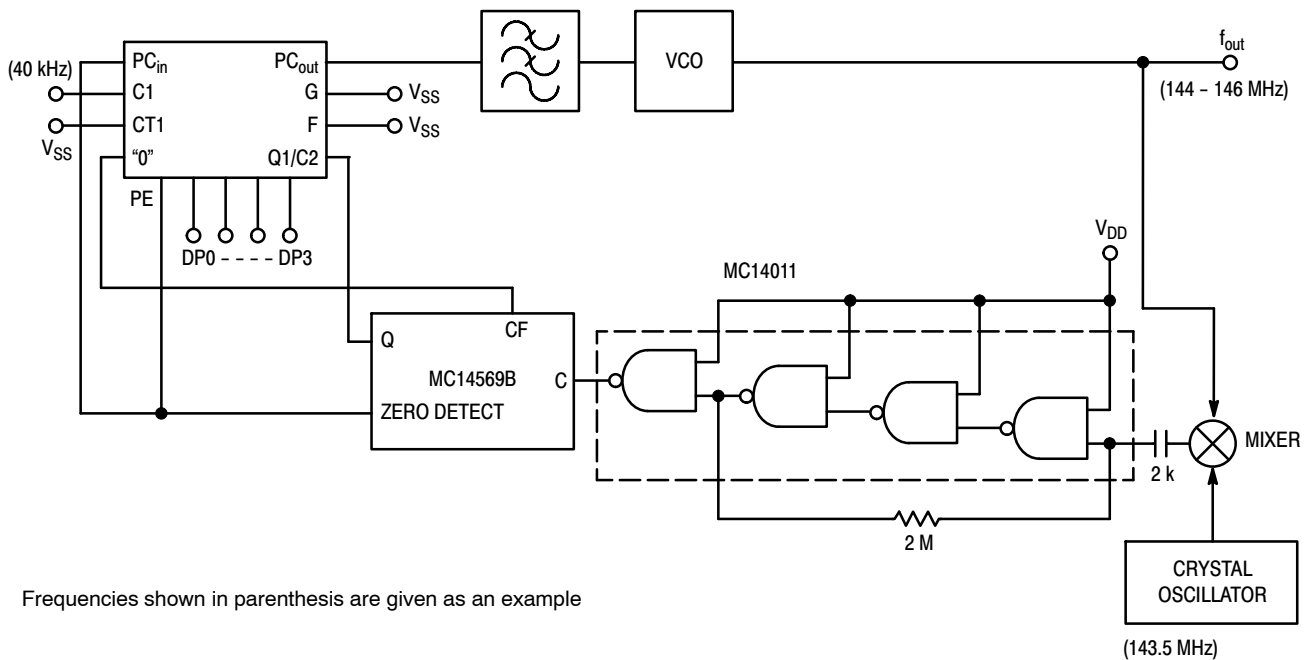
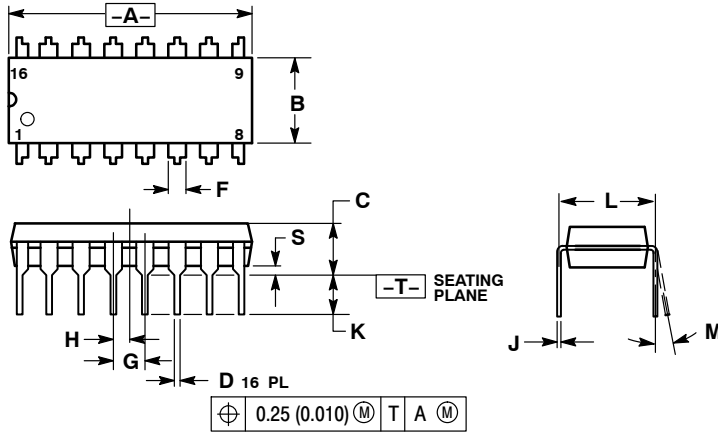


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

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## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE T



NOTES:

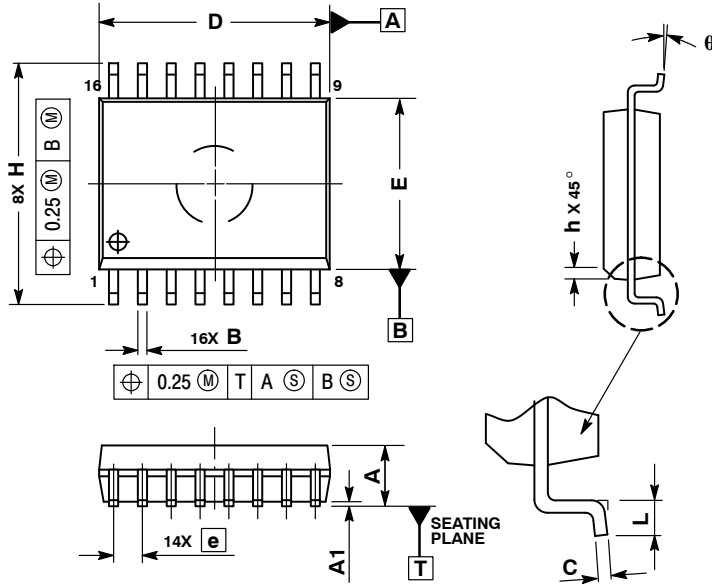
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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## PACKAGE DIMENSIONS

SOIC-16 WB  
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751G-03  
ISSUE C



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0°	7°

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