

Low Charge Injection, 8-Channel, High Voltage Analog Switches with Bleed Resistors

Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation (-10µA max.)
- ▶ Output on-resistance typically (22Ω typ.)
- ▶ Integrated bleed resistors on the outputs
- ▶ Low parasitic capacitances
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical output OFF isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ ON-chip shift register, latch and clear logic circuitry
- ▶ Flexible high voltage supplies

Applications

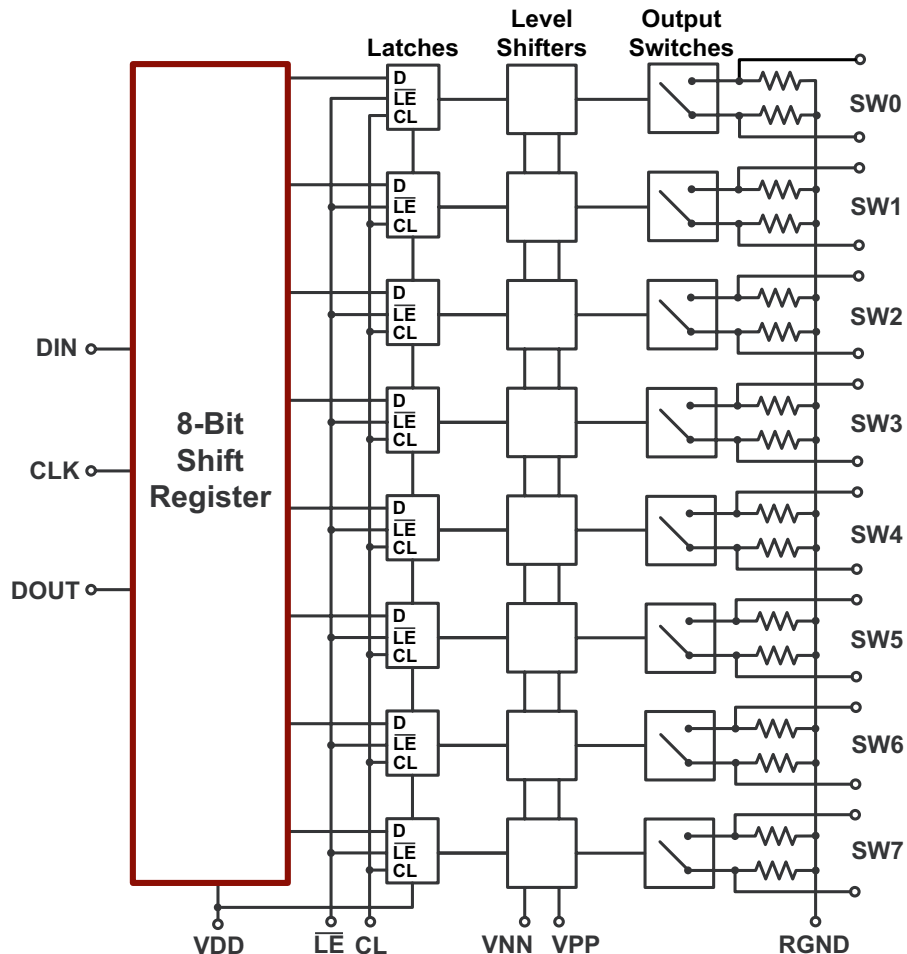
- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers

General Description

The Supertex HV230 is a low charge injection 8-channel, high-voltage, analog switch integrated circuit (IC) with bleed resistors. This device can be used in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers. Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable (\overline{LE}) should be left high until all bits are clocked in. Using HVCMOS® technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

This IC is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/-150V, or +100V/-100V.

Block Diagram

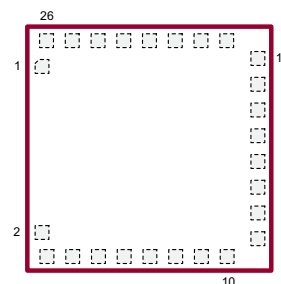


Ordering Information

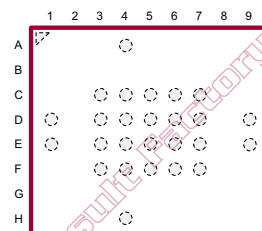
| Part Number | Package Option | Packing |
|-------------|----------------|------------------------|
| HV230G1-G | 26-Lead LLGA | 400/Tray |
| HV230GA-G | 26-Ball fpBGA | Consult factory |

-G denotes a lead (Pb)-free / RoHS compliant package

Pin Configuration



26-Lead LLGA
(top view)



26-Ball fpBGA
(top view)

Absolute Maximum Ratings

| Parameter | Value |
|---------------------------------------|--------------------------|
| V_{DD} logic power supply voltage | -0.5V to +15V |
| $V_{PP} - V_{NN}$ supply voltage | 220V |
| V_{PP} positive high voltage supply | -0.5V to $V_{NN} + 200V$ |
| V_{NN} negative high voltage supply | +0.5V to -200V |
| Logic input voltages | -0.5V to $V_{DD} + 0.3V$ |
| Analog signal range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 3.0A |
| Storage temperature | -65°C to +150°C |
| Power dissipation: | |
| 26-Lead LLGA | 1.0W |
| 26-Ball fpBGA | 1.0W |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

| Package | θ_{ja} |
|---------------|---------------|
| 26-Lead LLGA | 41°C/W |
| 26-Ball fpBGA | - |

Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

26-Lead LLGA



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

26-Ball fpBGA

Operating Conditions

| Sym | Parameter | Value |
|-----------|---|----------------------------------|
| V_{DD} | Logic power supply voltage ^{1,3} | 4.5V to 13.2V |
| V_{PP} | Positive high voltage supply ^{1,3} | 40V to $V_{NN} + 200V$ |
| V_{NN} | Negative high voltage supply ^{1,3} | -40V to -160V |
| V_{IH} | High level input voltage | $V_{DD} - 1.5V$ to V_{DD} |
| V_{IL} | Low-level input voltage | 0V to 1.5V |
| V_{SIG} | Analog signal voltage peak-to-peak ² | $V_{NN} + 10V$ to $V_{PP} - 10V$ |
| T_A | Operating free air temperature | 0°C to 70°C |

Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics (Over operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions | |
|------------------|--|------|-----|-------|-----|-----|-------|-----|------------|--|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | | |
| R_{ONS} | Small signal switch ON-resistance | - | 30 | - | - | 38 | - | 48 | Ω | $I_{SIG} = 5.0mA$ | $V_{PP} = +40V$ |
| | | - | 25 | - | - | 27 | - | 32 | | $I_{SIG} = 200mA$ | $V_{NN} = -160V$ |
| | | - | 25 | - | - | 27 | - | 30 | | $I_{SIG} = 5.0mA$ | $V_{PP} = +100V$ |
| | | - | 18 | - | - | 24 | - | 27 | | $I_{SIG} = 200mA$ | $V_{NN} = -100V$ |
| | | - | 23 | - | - | 25 | - | 30 | | $I_{SIG} = 5.0mA$ | $V_{PP} = +160V$ |
| | | - | 22 | - | - | 25 | - | 27 | | $I_{SIG} = 200mA$ | $V_{NN} = -40V$ |
| ΔR_{ONS} | Small signal switch ON-resistance matching | - | 20 | - | - | 20 | - | 20 | % | $I_{SIG} = 5.0mA, V_{PP} = +100V,$ $V_{NN} = -100V$ | |
| R_{ONL} | Large signal switch ON-resistance | - | - | - | 15 | - | - | - | Ω | $V_{SIG} = V_{PP} - 10V, I_{SIG} = 1.0A$ | |
| R_{INT} | Output switch shunt resistance | - | - | 20 | - | 50 | - | - | K Ω | Output switch to R_{GND} $I_{RINT} = 0.5mA$ | |
| I_{SOL} | Switch OFF leakage per switch | - | 5.0 | - | - | 10 | - | 15 | μA | $V_{SIG} = V_{PP} - 10V$ | |
| V_{OS} | DC offset switch OFF | - | 300 | - | - | 300 | - | 300 | mV | No load | |
| | DC offset switch ON | - | 500 | - | - | 500 | - | 500 | mV | No load | |
| I_{PPQ} | Quiescent V_{PP} supply current | - | - | - | - | 50 | - | - | μA | All switches OFF | |
| I_{NNQ} | Quiescent V_{NN} supply current | - | - | - | - | -50 | - | - | μA | All switches OFF | |
| I_{PPQ} | Quiescent V_{PP} supply current | - | - | - | - | 50 | - | - | μA | All switches ON, $I_{SW} = 5.0mA$ | |
| I_{NNQ} | Quiescent V_{NN} supply current | - | - | - | - | -50 | - | - | μA | All switches ON, $I_{SW} = 5.0mA$ | |
| I_{SW} | Switch output peak current | - | 3.0 | - | - | 2.0 | - | 2.0 | A | V_{SIG} duty cycle -0.1% | |
| f_{SW} | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% | |
| I_{PP} | Supply current | - | 6.5 | - | - | 7.0 | - | 8.0 | mA | $V_{PP} = +40V$ $V_{NN} = -160V$ | All output switches are turning On and Off at 50kHz with no load |
| | | - | 4.0 | - | - | 5.0 | - | 5.5 | | $V_{PP} = +100V$ $V_{NN} = -100V$ | |
| | | - | 4.0 | - | - | 5.0 | - | 5.5 | | $V_{PP} = +160V$ $V_{NN} = -40V$ | |
| I_{NN} | Supply current | - | 6.5 | - | - | 7.0 | - | 8.0 | mA | $V_{PP} = +40V$ $V_{NN} = -160V$ | All output switches are turning On and Off at 50kHz with no load |
| | | - | 4.0 | - | - | 5.0 | - | 5.5 | | $V_{PP} = +100V$ $V_{NN} = -100V$ | |
| | | - | 4.0 | - | - | 5.0 | - | 5.5 | | $V_{PP} = +160V$ $V_{NN} = -40V$ | |
| I_{DD} | Logic supply average current | - | 4.0 | - | - | 4.0 | - | 4.0 | mA | $f_{CLK} = 5.0MHz, V_{DD} = 5.0V$ | |
| I_{DDQ} | Logic supply quiescent current | - | 10 | - | - | 10 | - | 10 | μA | --- | |
| I_{SOR} | Data out source current | 0.45 | - | 0.45 | - | - | 0.40 | - | mA | $V_{OUT} = V_{DD} - 0.7V$ | |
| I_{SINK} | Data out sink current | 0.45 | - | 0.45 | - | - | 0.40 | - | mA | $V_{OUT} = 0.7V$ | |
| C_{IN} | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- | |

AC Electrical Characteristics (Over recommended operating conditions, $V_{DD} = 5.0V$, unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Unit | Conditions |
|---------------|--|-----|-----|-------|-----|-----|-------|-----|---------|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t_{SD} | Set up time before \overline{LE} rises | 150 | - | 150 | - | - | 150 | - | ns | --- |
| t_{WLE} | Time width of \overline{LE} | 150 | - | 150 | - | - | 150 | - | ns | --- |
| t_{DO} | Clock delay time to data out | 55 | 150 | 60 | - | 150 | 70 | 150 | ns | --- |
| t_{WCL} | Time width of CL | 150 | - | 150 | - | - | 150 | - | ns | --- |
| t_{SU} | Set up time data to clock | 15 | - | 15 | - | - | 20 | - | ns | --- |
| t_H | Hold time data from clock | 35 | - | 35 | - | - | 35 | - | ns | --- |
| f_{CLK} | Clock frequency | - | 5.0 | - | - | 5.0 | - | 5.0 | MHz | 50% Duty cycle, $f_{DATA} = f_{CLK}/2$ |
| t_R, t_F | Clock rise and fall times | - | 1.0 | - | - | 1.0 | - | 1.0 | μs | --- |
| t_{ON} | Turn ON time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V, R_L = 10k\Omega$ |
| t_{OFF} | Turn OFF time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V, R_L = 10k\Omega$ |
| dv/dt | Maximum V_{SIG} slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | $V_{PP} = +160V, V_{NN} = -40V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +40V, V_{NN} = -160V$ |
| K_O | OFF isolation | -30 | - | -30 | - | - | -30 | - | dB | $f = 5.0MHz,$ $1.0k\Omega/15pF$ load |
| | | -58 | - | -58 | - | - | -58 | - | | $f = 5.0MHz, 50\Omega$ load |
| K_{CR} | Switch crosstalk | -60 | - | -60 | - | - | -60 | - | dB | $f = 5.0MHz, 50\Omega$ load |
| I_{ID} | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300ns pulse width, 2.0% duty cycle |
| $C_{SG(OFF)}$ | OFF capacitance SW to GND | 5.0 | 17 | 5.0 | - | 17 | 5.0 | 17 | pF | 0V, $f = 1.0MHz$ |
| $C_{SG(ON)}$ | ON capacitance SW to GND | 25 | 50 | 25 | - | 50 | 25 | 50 | pF | 0V, $f = 1.0MHz$ |
| $+V_{SPK}$ | Output voltage spike | - | - | - | - | 150 | - | - | mV | $V_{PP} = +40V, V_{NN} = -160V,$ $R_L = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +100V, V_{NN} = -100V,$ $R_L = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +160V, V_{NN} = -40V,$ $R_L = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |

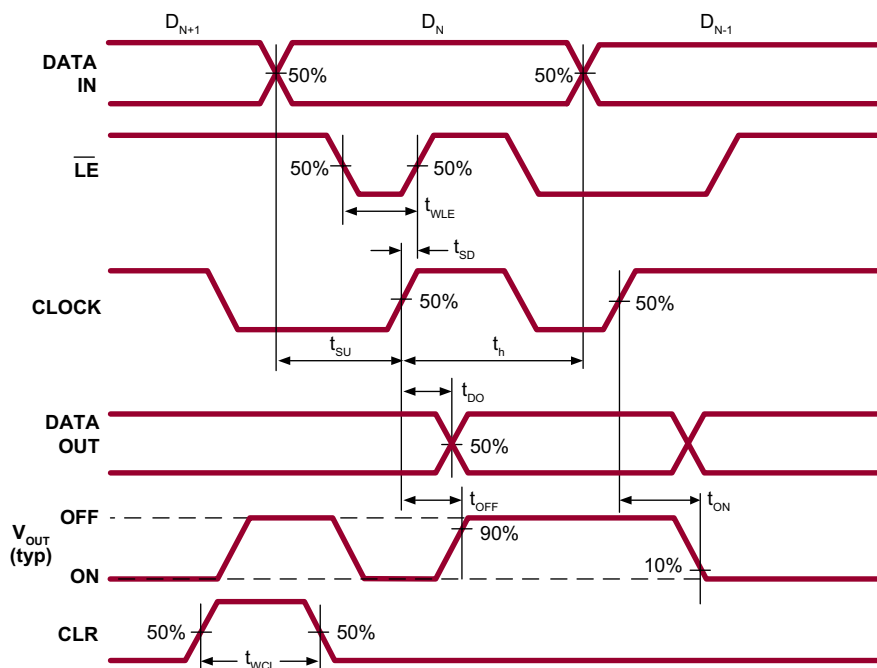
Truth Table

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | \overline{LE} | CLK | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
|----|----|----|----|----|----|----|----|-----------------|-----|---------------------|-----|-----|-----|-----|-----|-----|-----|
| L | | | | | | | | L | L | OFF | | | | | | | |
| H | | | | | | | | L | L | ON | | | | | | | |
| | L | | | | | | | L | L | | OFF | | | | | | |
| | H | | | | | | | L | L | | ON | | | | | | |
| | | L | | | | | | L | L | | | OFF | | | | | |
| | | H | | | | | | L | L | | | ON | | | | | |
| | | | L | | | | | L | L | | | | OFF | | | | |
| | | | H | | | | | L | L | | | | ON | | | | |
| | | | | L | | | | L | L | | | | | OFF | | | |
| | | | | H | | | | L | L | | | | | ON | | | |
| | | | | | L | | | L | L | | | | | | OFF | | |
| | | | | | H | | | L | L | | | | | | ON | | |
| | | | | | | L | | L | L | | | | | | | OFF | |
| | | | | | | H | | L | L | | | | | | | ON | |
| | | | | | | | L | L | L | | | | | | | | OFF |
| | | | | | | | H | L | L | | | | | | | | ON |
| X | X | X | X | X | X | X | X | H | L | Hold Previous State | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | All Switches OFF | | | | | | | |

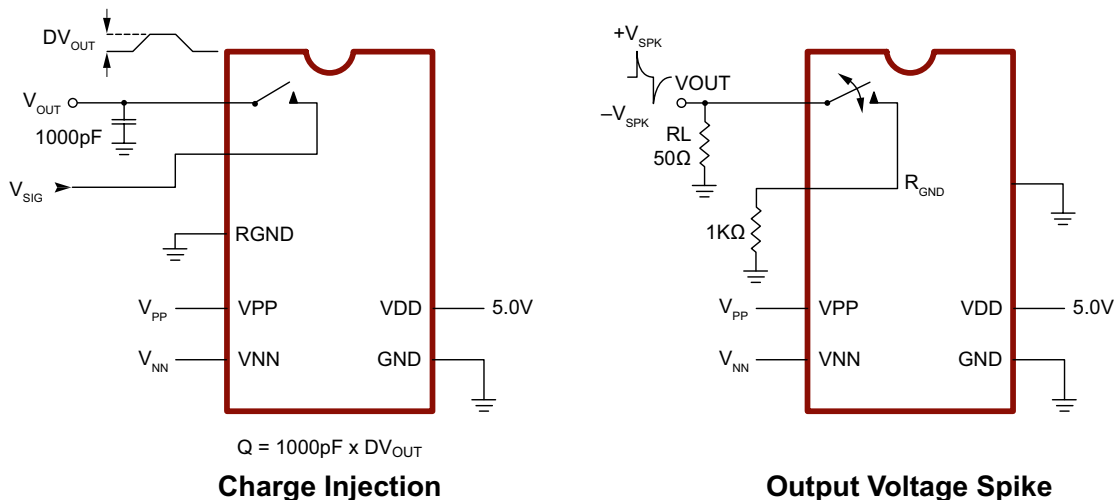
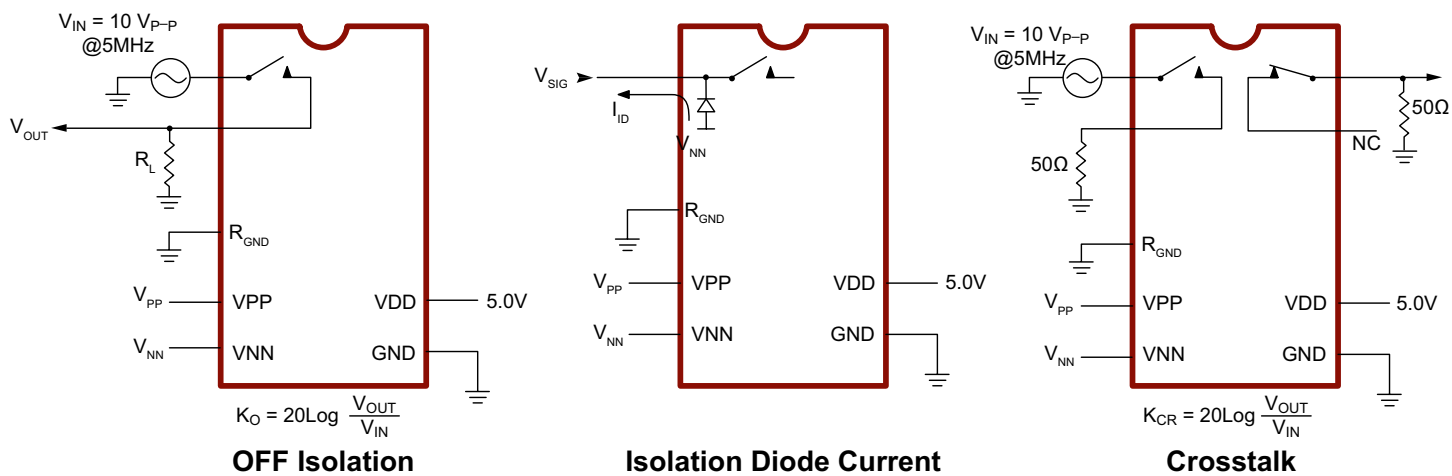
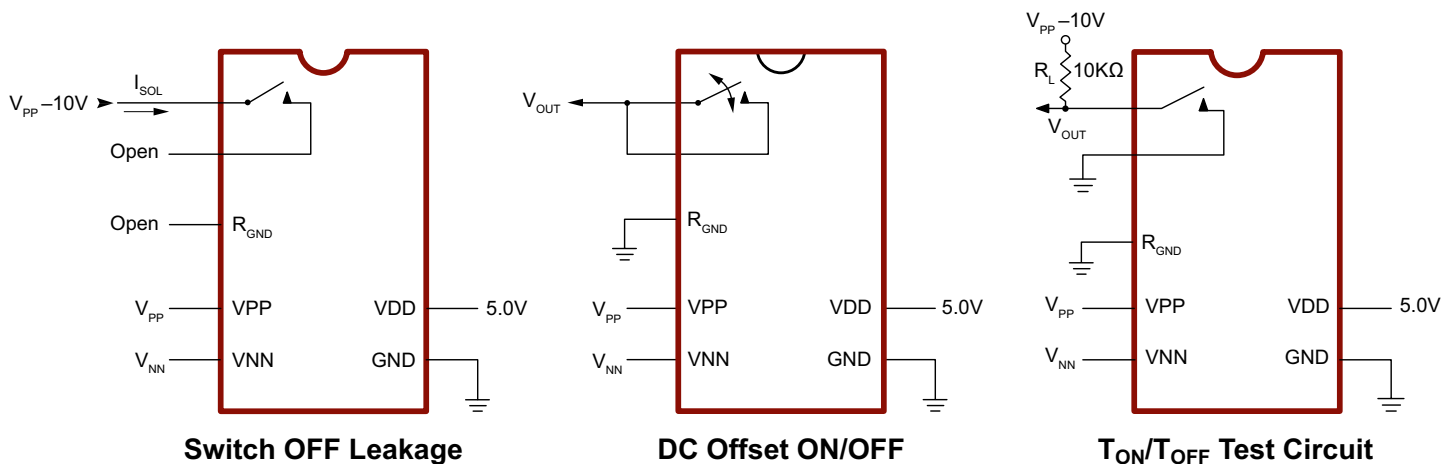
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flow through the latch.
4. D_{OUT} is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if \overline{LE} is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms



Test Circuits



Pin Description (26-Lead LLGA)

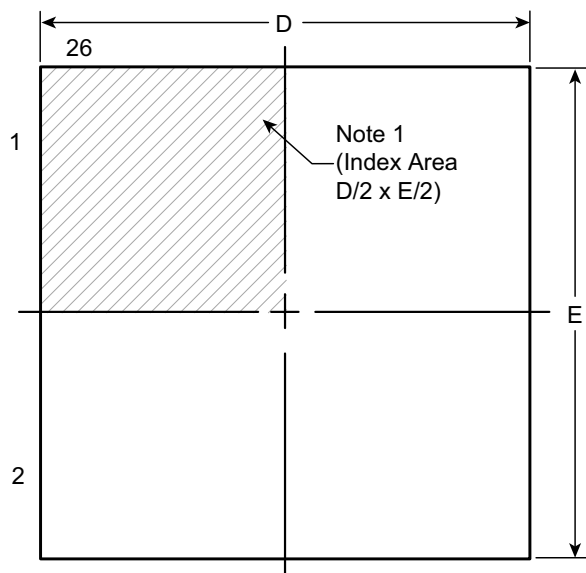
| Pin | Function | Pin | Function |
|-----|----------|-----|------------------------|
| 1 | SW4 | 14 | VDD |
| 2 | SW3 | 15 | DIN |
| 3 | SW3 | 16 | CLK |
| 4 | SW2 | 17 | $\overline{\text{LE}}$ |
| 5 | SW2 | 18 | CL |
| 6 | SW1 | 19 | DOUT |
| 7 | SW1 | 20 | SW7 |
| 8 | SW0 | 21 | SW7 |
| 9 | SW0 | 22 | SW6 |
| 10 | VPP | 23 | SW6 |
| 11 | VNN | 24 | SW5 |
| 12 | RGND | 25 | SW5 |
| 13 | GND | 26 | SW4 |

Pin Description (26-Ball fpBGA)

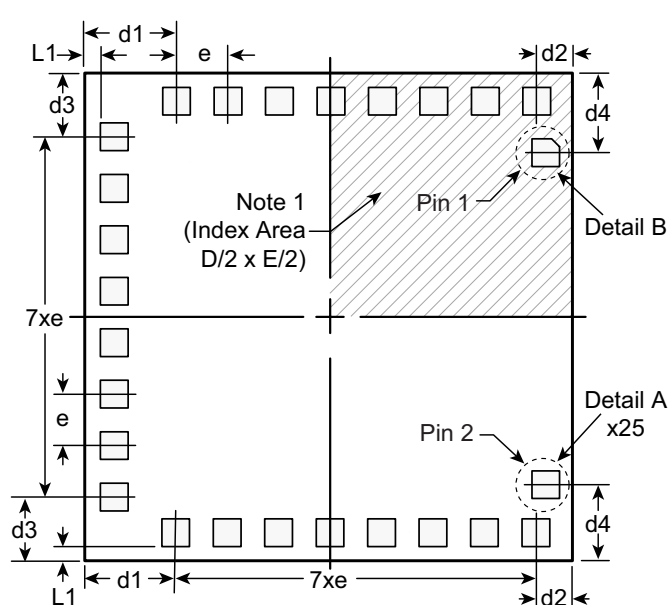
| Ball Location | Function | Ball Location | Function |
|---------------|----------|---------------|------------------------|
| A4 | SW1 | E1 | SW4 |
| C3 | SW2 | E3 | SW4 |
| C4 | SW1 | E4 | SW5 |
| C5 | SW0 | E5 | SW7 |
| C6 | VPP | E6 | $\overline{\text{LE}}$ |
| C7 | VNN | E7 | CLK |
| D1 | SW3 | E9 | DIN |
| D3 | SW3 | F3 | SW5 |
| D4 | SW2 | F4 | SW6 |
| D5 | SW0 | F5 | SW7 |
| D6 | RGND | F6 | DOUT |
| D7 | GND | F7 | CLR |
| D9 | VDD | H4 | SW6 |

26-Lead LLGA Package Outline (G1)

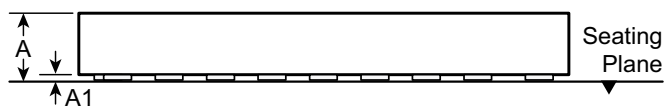
6.00x6.00mm body, 0.60mm height (max), 0.65mm pitch



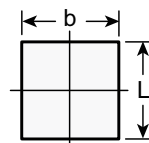
Top View



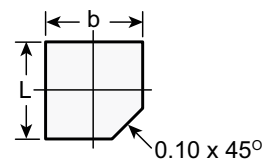
Bottom View



Side View



Detail A



Detail B

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

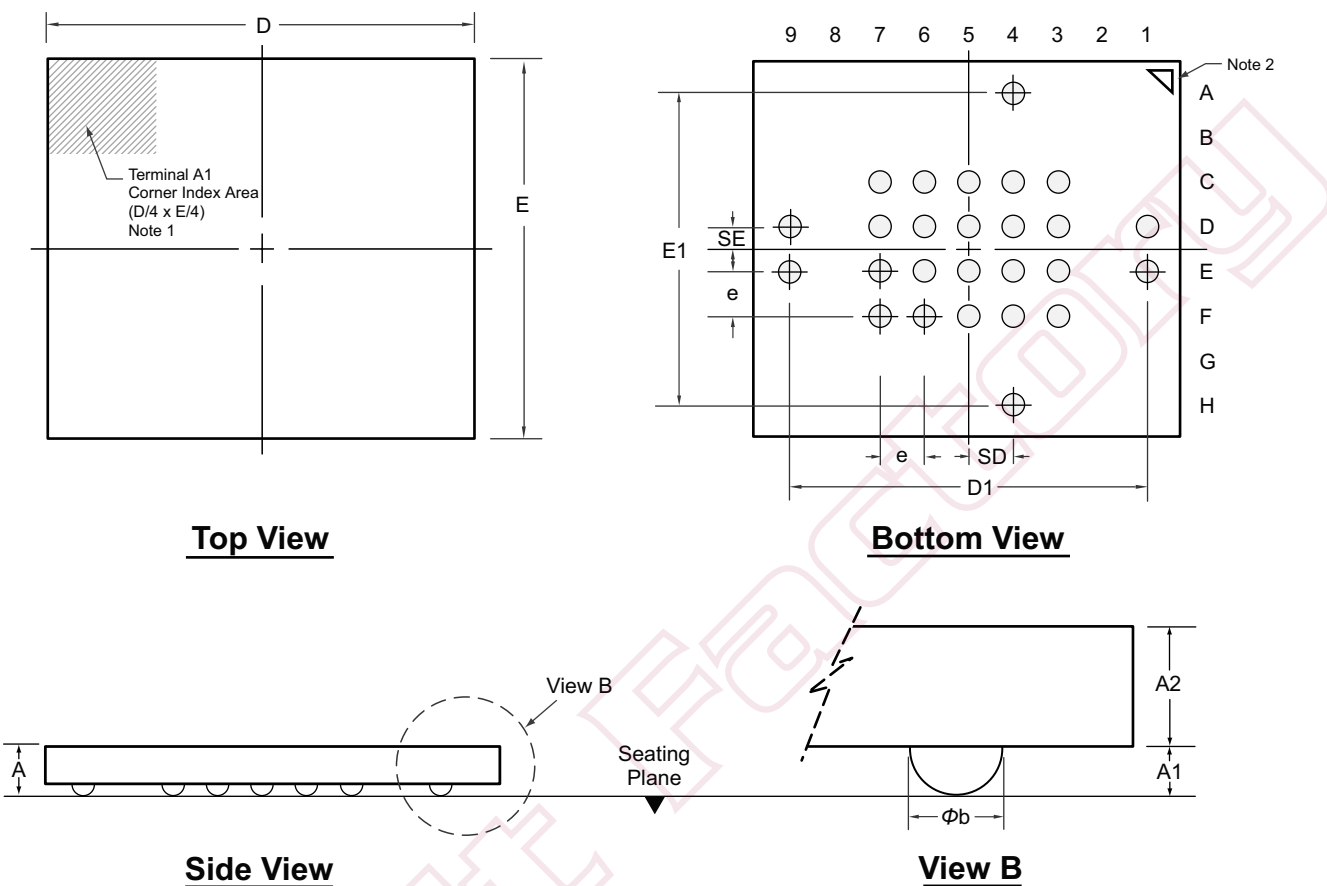
| Symbol | A | A1 | b | D | d1 | d2 | d3 | d4 | E | e | L | L1 | |
|----------------|-----|------|------|------|------|-----------|-----------|-----------|-----------|------|----------|------|----------|
| Dimension (mm) | MIN | 0.50 | 0.00 | 0.25 | 5.90 | 1.050 REF | 0.400 REF | 0.725 REF | 0.925 REF | 5.90 | 0.65 BSC | 0.25 | 0.10 REF |
| | NOM | 0.55 | - | 0.35 | 6.00 | | | | | 6.00 | | 0.35 | |
| | MAX | 0.60 | 0.05 | 0.45 | 6.10 | | | | | 6.10 | | 0.45 | |

Drawings not to scale.

Supertex Doc. #: DSPD-26LLGAG1, Version A090808.

26-Ball fpBGA Package Outline (GA)

6.00x5.35mm body, 1.20mm height (max), 0.65mm pitch



Notes:

1. A Ball A1 identifier must be located in the index area indicated. The Ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Corner A1 identifier (actual shape may vary).

| Symbol | | A | A1 | A2 | ϕ_b | D | D1 | E | E1 | e | SD | SE |
|----------------|-----|-------|------|-------|----------|------|-------------|------|-------------|-------------|-------------|--------------|
| Dimension (mm) | MIN | 0.844 | 0.18 | 0.664 | 0.25 | 5.90 | 5.20 BSC | 5.25 | 4.55 BSC | 0.65 BSC | 0.65 BSC | 0.325 BSC |
| | NOM | 0.994 | 0.23 | 0.764 | 0.30 | 6.00 | | 5.35 | | | | |
| | MAX | 1.200 | 0.28 | 0.864 | 0.35 | 6.10 | | 5.45 | | | | |

Drawings not to scale.
Supertex Doc. #: DSPD-26fpBGAGA, Version A092208.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. (website: <http://www.supertex.com>)



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.