73M1822/73M1922 MicroDAA
Silicon DAA with Serial Interface

Simplifying System Integration™

DATA SHEET

DS_1x22_001 **April 2010**

DESCRIPTION

The 73M1822 MicroDAA™ is the world's first single-package silicon Data Access Arrangement (DAA) for data/fax modem and voice applications. It provides a serial Modem Analog Front End (MAFE) interface to popular DSP/host processors to implement a globally compliant low-cost soft modem solution.

The 73M1822 MicroDAA is available as a two-chip configuration (the 73M1922) that consists of a 73M1902 Host-Side Device and a 73M1912 Line-Side Device. The MicroDAA integrates all codec and DAA functions necessary to achieve reliable PSTN connection worldwide.

The MicroDAA uses a small pulse transformer, which can achieve more than 6 kV isolation. Power may be supplied along with data through this barrier interface to achieve superior performance in weak loop current conditions. Inherently immune to RFI and other forms of common mode interference, the patented MicroDAA technology achieves global DAA compliance with unparalleled flexibility, reliability, and cost structure and requires less than 2 square inches of a single sided PCB.

The MicroDAA supports Caller ID Type I and II, ring detection, tip/ring polarity reversal detection, hook switch control, pulse dialing, regulation of loop current (DC mask), configurable line impedance matching, line in use and parallel pickup detection.

The MicroDAA integrates billing tone filters, external clock reference, audio monitor output, and requires only a small number of low cost and commonly available external components.

The MicroDAA incorporates a configurable sample rate circuit to support soft modem and DSP-based implementations of all speeds up to V.92 (56 Kbps). Sampling rates from 7.2 kHz to 16 kHz can be easily supported.

APPLICATIONS

- V.92 modems
- Satellite Set Top Boxes
- Fax/Multifunction Peripherals (MFP)
- Point of Sale Terminals
- Voicemail Systems
- Industrial and medical telemetry

FEATURES

- Meets FCC, ETSI ES 203 021-2, JATE, NET4 and other PTT standards
- Configurable PSTN termination
- Up to 8 mA minimum line current operation
- 0 dBm Transmit/Receive full scale
- THD –80 dB
- 16-bit codec up to 16 kHz sample rate
- Up to 56 Kbps (V.92) performance
- Configurable sample rates (7.2 – 16 kHz)
- Reference clock range of 9-40 MHz
- Crystal frequency range of 9-27 MHz
- MAFE I/F with Master, Slave and Daisy Chaining
- Billing tone reject filter
- Polarity reversal detection on-chip
- GPIO for user-configurable I/O port
- Call Progress Monitor
- 3.3 V Operation
- Industrial temperature range (-40° to +85° C)
- 6 kV isolation (73M1922)
- 4-5 kV isolation (73M1822)
- 8x8 mm 42-pin QFN (73M1822)
- 20-pin TSSOP or 5x5 mm 32-pin QFN (73M1922)
- RoHS compliant (6/6) lead-free package

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1 Introduction

The 73M1922 MicroDAA is a two-device chip set that consists of a 73M1902 Host-Side Device and a 73M1912 Line-Side Device that can be used in any voice-band PSTN telephone interface application requiring a CODEC. The 73M1822 is a single-package MicroDAA with the same interfaces. Each connects directly between a host processor and the telephone network with a low-cost pulse transformer to provide the required high-voltage isolation. A few low-cost components complete the interface to the network. The pulse transformer transmits encoded digital data rather than analog signals as with other transformer designs. Data is transmitted and received without the usual degradation from common mode noise and magnetic coupling typical of other capacitive and voice-band transformer techniques. The data stream passed between the Host-Side and Line-Side Devices includes the media stream data, control, status and clocking information.

The data sheet describes both the 73M1922 and 73M1822, which will be collectively referred to as the 73M1x22 in this document.

The Host-Side Device uses a serial data port for transferring transmit and receive data, status and control information to a host. This interface is compatible with most DSP and high-performance processor synchronous serial CODEC interfaces.

All media stream data and control information between the Host-Side Device and Line-Side Device of the 73M1822 and 73M1922 are transferred across the pulse transformer. Clocking information used by the Line-Side Device is embedded in the bit stream received from the Host-Side Device and reconstructed by the Line-Side Device of the 73M1822 or 73M1922.

On start up, the Host-Side Device provides power to the Line-Side Device through the transformer. After going off-hook, the Line-Side Device is capable of being powered from the PSTN network. The only physical connections between the devices are the primary side of the pulse transformer that is connected to the Host-Side Device and the secondary side to the Line-Side Device.

Figure 1 shows a reference block diagram of the 73M1922 connected by a pulse transformer and example external line interface circuitry shown for clarification.

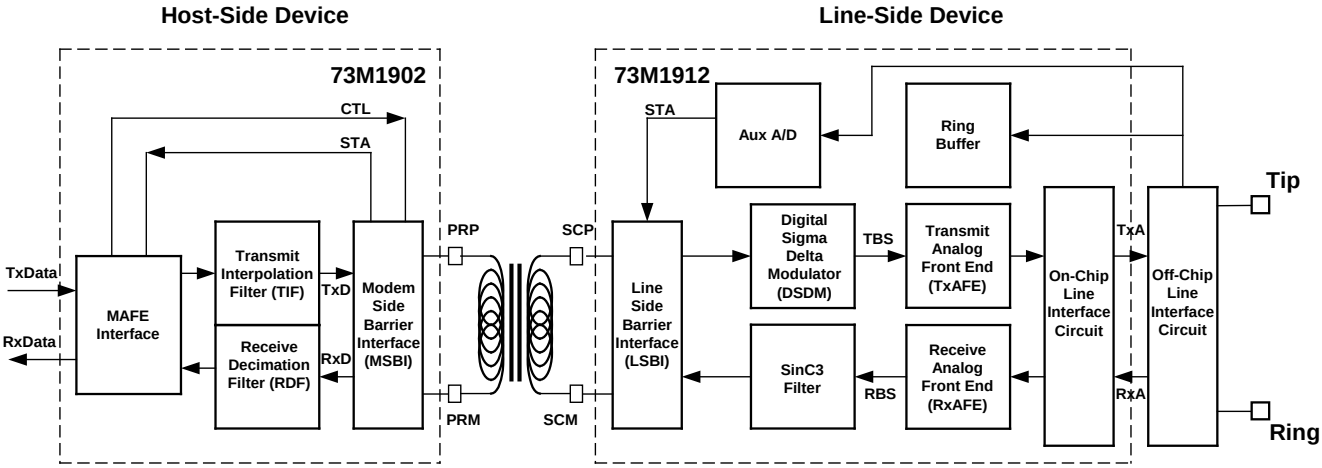


Figure 1: Simple 73M1x22 Reference Block Diagram

The Host-Side Device (73M1902) consists of:

1. Modem Analog Front End (MAFE) Interface Block
2. Transmit Interpolation Filter (TIF)
3. Receive Decimation Filter (RDF)
4. Modem-Side Barrier Interface Circuit (MSBI)

The Line-Side Device (73M1912 / 73M1822) consists of:

1. Digital Sigma Delta Modulator (DSDM)
2. Transmit Analog Front End (TxAFE)
3. Receive Analog Front End (RxAFE) including Sigma Delta Modulator (ASDM)
4. Sinc^3 Filter (Sinc3)
5. On-chip Line Interface Circuit (ONLIC)
6. Line-Side Barrier Interface Circuit (LSBI)

The transmit data (TxData) is interpolated up within TIF (Transmit Interpolation Filter) from the sampling frequency (Fs) to twice the sampling frequency resulting in TxD.

Control information (CTL) is time-division multiplexed with TxD, serialized within MSBI, and sent across the barrier to 73M1912 LIC (Line Interface Circuitry). This is then received and processed within LSBI and separated into TxD and CTL. TxD is digitally sigma-delta modulated to form a serialized Transmit Bit Stream (TBS). The TBS is D/A converted for final transmission to the line. CTL is used to control various features of the Line-Side Device.

On the receive side, the received analog signal from the line is sigma-delta modulated to form a serialized Receive Bit Stream (RBS). RBS is decimated down to twice the sampling frequency as RxD and time-division multiplexed with status Information (STA) from the Auxiliary A/D regarding line condition in LSBI block and transmitted to the Host-Side Device. The MSBI processes this data and separates it into RxD and STA. Rxd is further decimated to down to Fs and sent to the host through the MAFE interface. STA is sent to the host through the MAFE interface using a different time slot.

2 Pinout

The 73M1922 consists of two devices, the 73M1902 and the 73M1912, which are available as 20-pin TSSOP packages and as 32-pin QFN package sets.

2.1 73M1902 20-Pin TSSOP Pinout

Figure 2 shows the 73M1902 20-pin TSSOP pinout.

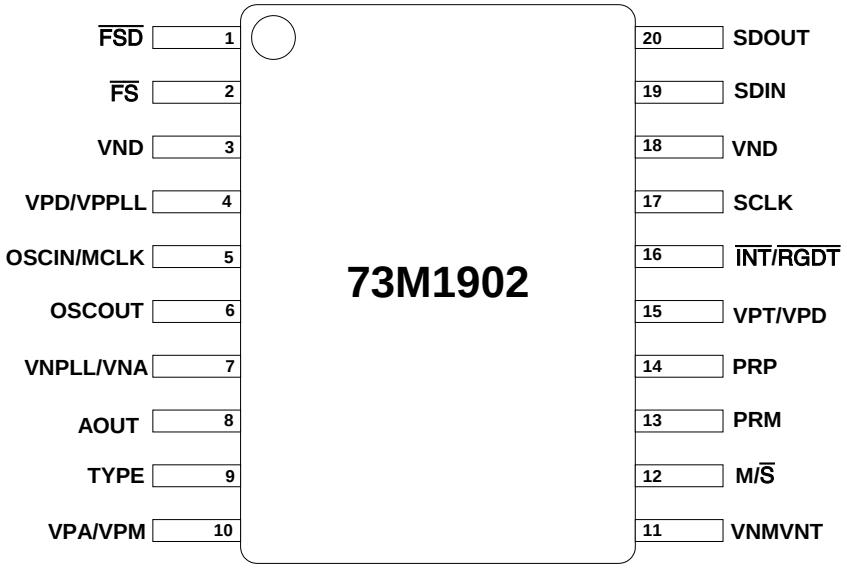


Figure 2: 73M1902 20-Pin TSSOP Pinout

Table 1 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 1: 73M1902 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	$\overline{FSD}$	O	Frame synchronization ($\overline{FS}$) delayed
2	$\overline{FS}$	O	Frame synchronization
3	VND	GND	Negative digital ground
4	VPD/VPPLL	PWR	Positive digital/PLL supply
5	OSCIN/MCLK	I	Crystal oscillator circuit input pin. Input from an external clock source. Crystal frequency range is 9 MHz – 27 MHz.
6	OSCOUT	O	Crystal oscillator output pin. (N.C. with external oscillator)
7	VNA/VNPLL	GND	Negative analog/PLL ground
8	AOUT	O	Call progress audio output
9	TYPE	I	Type of frame sync. 0 = late (mode0), 1 = early (mode1). Weak-pulled high – default = early.
10	VPA/VPM	PWR	Positive analog supply
11	VNM/VNT	GND	Negative barrier interface supply / negative transformer supply
12	M/$\overline{S}$	I	Master/slave control, reset at a transition.
13	PRM	I/O	Pulse transformer primary minus

14	PRP	I/O	Pulse transformer primary plus
15	VPD	PWR	Positive digital supply, positive transformer supply
16	$\overline{\text{INT}}/\overline{\text{RGDT}}$	O	Ring detection indicator or other Interrupts Open drain
17	SCLK	O	Serial interface clock. With continuous SCLK selected, Frequency = 256∗Fs (=1.8432MHz for Fs=7.2kHz, 2.048MHz for Fs=8kHz)
18	VND	GND	Negative digital ground
19	SDIN	I	Serial data input (or output from the controller to 73M1902)
20	SDOUT	O	Serial data output (or input to the controller from 73M1902)

2.2 73M1912 20-Pin TSSOP Pinout

Figure 3 shows the 73M1912 20-pin TSSOP pinout.

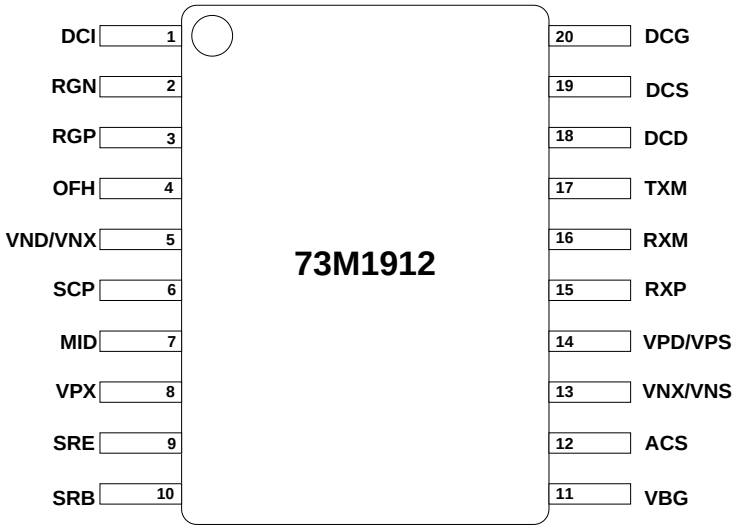


Figure 3: 73M1912 20-Pin TSSOP Pinout

Table 2 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 2: 73M1912 20-Pin TSSOP Pin Definitions

Pin Number	Pin Name	Type	Description
1	DCI	I	DC loop input
2	RGN	I	Ring detect negative voltage input
3	RGP	I	Ring detect positive voltage input
4	OFH	O	Off-hook control
5	VND/VNX	GND	Digital/analog negative supply voltage
6	SCP	I/O	Positive side of the secondary pulse transformer winding
7	MID	I/O	Charge pump midpoint
8	VPX	PWR	Supply from the barrier, connect to VPD
9	SRE	I	Voltage regulator sense
10	SRB	O	Voltage regulator drive
11	VBG	O	VBG bypass, connect to 0.1 µF capacitor to VNS
12	ACS	I	AC current sense
13	VNX/VNS	GND	Digital/analog negative supply voltage
14	VPD/VPS	PWR	Digital/analog positive supply voltage
15	RXP	I	Receive plus – signal input
16	RXM	I	Receive minus – signal input
17	TXM	O	Transmit minus – signal output
18	DCD	O	DC loop drive
19	DCS	I	DC loop current sense
20	DCG	O	DC loop drive

2.3 73M1902 32-Pin QFN Pinout

Figure 4 shows the 73M1902 32-pin QFN pinout.

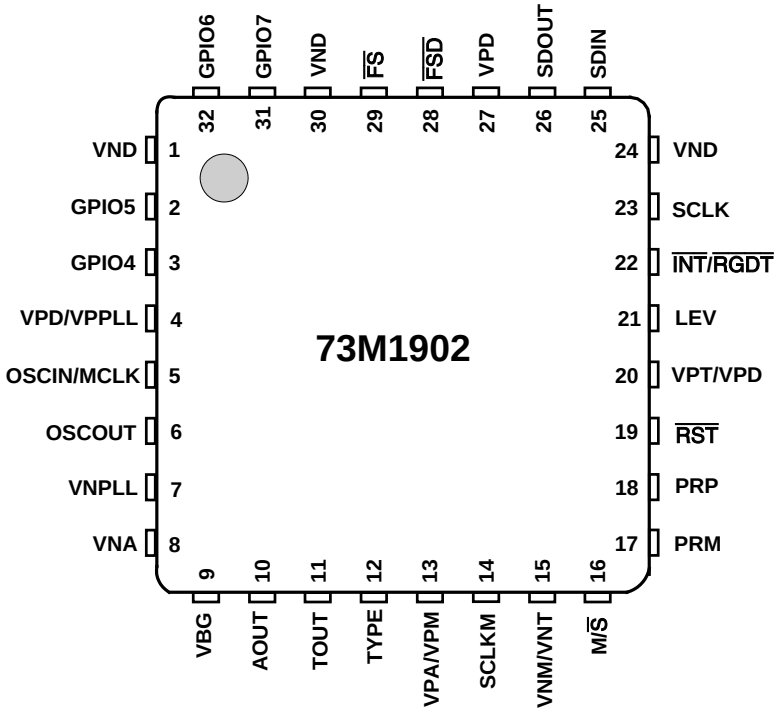


Figure 4: 73M1902 32-Pin QFN Pinout

Table 3 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 3: 73M1902 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	VND	GND	Negative digital ground
2	GPIO5	I/O	Configurable digital input/output pins
3	GPIO4	I/O	Configurable digital input/output pins
4	VPD/VPPLL	PWR	Positive digital/PLL supply
5	OSCIN/MCLK	I	Crystal oscillator circuit input pin. Input from an external clock source. Crystal frequency range supported is 9 MHz – 27 MHz.
6	OSCOUT	O	Crystal oscillator output pin. (N.C. with external oscillator)
7	VNA/VNPLL	GND	Negative analog/PLL ground
8	VNA/VNPLL	GND	Negative analog/PLL ground
9	VBG	O	Band gap voltage reference monitor
10	AOUT	O	Call progress audio output
11	TOUT	O	Digital test output
12	TYPE	I	Type of frame sync. 0 = late (mode0), 1 = early (mode1). Weak-pulled high – default = early.
13	VPA/VPM	PWR	Positive analog supply

Pin Number	Pin Name	Type	Description
14	SCKM	I	Controls the SCLK behavior after $\overline{FS}$. Weak-pulled high – default = continuous SCLK
15	VNM/VNT	GND	Negative barrier interface/transformer supply
16	M/$\overline{S}$	I	Master/slave control, reset at a transition
17	PRM	I/O	Pulse transformer primary minus
18	PRP	I/O	Pulse transformer primary plus
19	$\overline{RST}$	I	Factory test mode – leave open
20	VPD	PWR	Positive digital supply, positive transformer supply
21	LEV	O	Test output (CMOS level)
22	$\overline{INT}$/$\overline{RGDT}$	O	Ring detection indicator or other Interrupts. Open drain
23	SCLK	O	Serial interface clock. With continuous SCLK selected, Frequency = 256∗Fs (=1.8432MHz for Fs=7.2kHz, 2.048MHz for Fs=8kHz)
24	VND	GND	Negative digital ground
25	SDIN	I	Serial data input (or output from the controller to 73M1902)
26	SDOUT	O	Serial data output (or input to the controller from 73M1902)
27	VPD	PWR	Positive digital supply, positive transformer supply
28	$\overline{FSD}$	O	FS delayed
29	$\overline{FS}$	O	Frame synchronization
30	VND	GND	Negative digital ground
31	GPIO7	I/O	Configurable digital input/output pins
32	GPIO6	I/O	Configurable digital input/output pins

2.4 73M1912 32-Pin QFN Pinout

Figure 5 shows the 73M1912 32-pin QFN pinout.

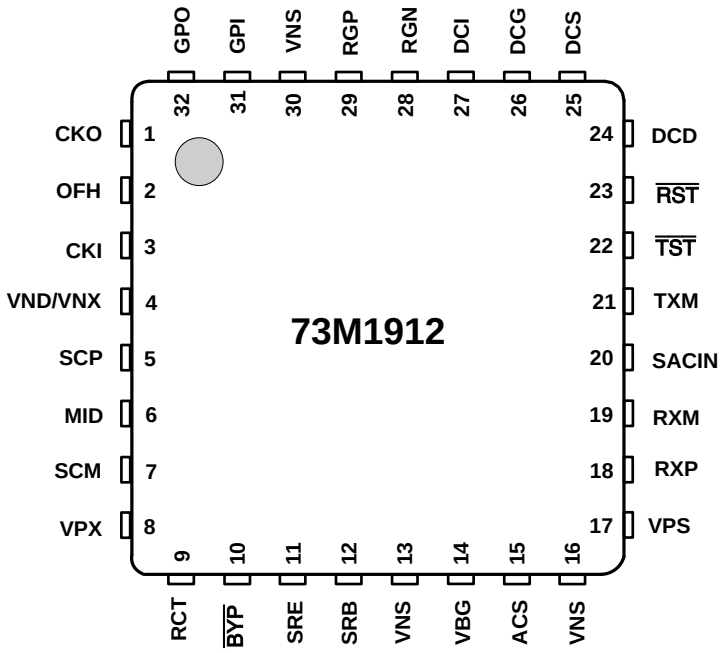


Figure 5: 73M1912 32-Pin QFN Pinout

Table 4 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 4: 73M1912 32-Pin QFN Pin Definitions

Pin Number	Pin Name	Type	Description
1	CKO	O	Test point for recovered clock
2	OFH	O	Off-hook control
3	CKI	I	Test input for clock
4	VND/VNX	GND	Digital/analog negative supply voltage
5	SCP	I/O	Positive side of the secondary pulse transformer winding
6	MID	I/O	Charge pump midpoint
7	SCM	I/O	Negative side of the secondary pulse transformer winding
8	VPX	PWR	Supply from the barrier side, connect to VPD
9	RCT	I	External rectification – disables internal rectifier when low, leave open
10	$\overline{\text{BYP}}$	I	Factory test mode – leave open
11	SRE	I	Voltage regulator sense
12	SRB	O	Voltage regulator drive
13	VNS	GND	Analog/digital negative supply voltage
14	VBG	O	VBG bypass, connect to 0.1µF capacitor to VPS
15	ACS	I	AC current sense
16	VNS	GND	Analog/digital negative supply voltage

Pin Number	Pin Name	Type	Description
17	VPS	PWR	Analog/digital positive supply voltage
18	RXP	I	Receive plus – signal input
19	RXM	I	Receive minus – signal input
20	SACIN	I	Caller ID mode AC impedance connection
21	TXM	O	Transmit minus – transhybrid cancellation output
22	$\overline{TST}$	I	Factory test mode – leave open
23	$\overline{RST}$	I	Factory test mode – leave open
24	DCD	O	DC loop drive
25	DCS	I	DC loop current sense
26	DCG	O	DC loop drive
27	DCI	I	DC loop input
28	RGN	I	Ring detect negative voltage input
29	RGP	I	Ring detect positive voltage input
30	VNS	GND	Analog/digital negative supply voltage
31	GPI	I	General purpose input (test pin)
32	GPO	O	General purpose output (test pin)

2.5 73M1822 Pinout

Figure 6 shows the 73M1822 42-pin pinout.

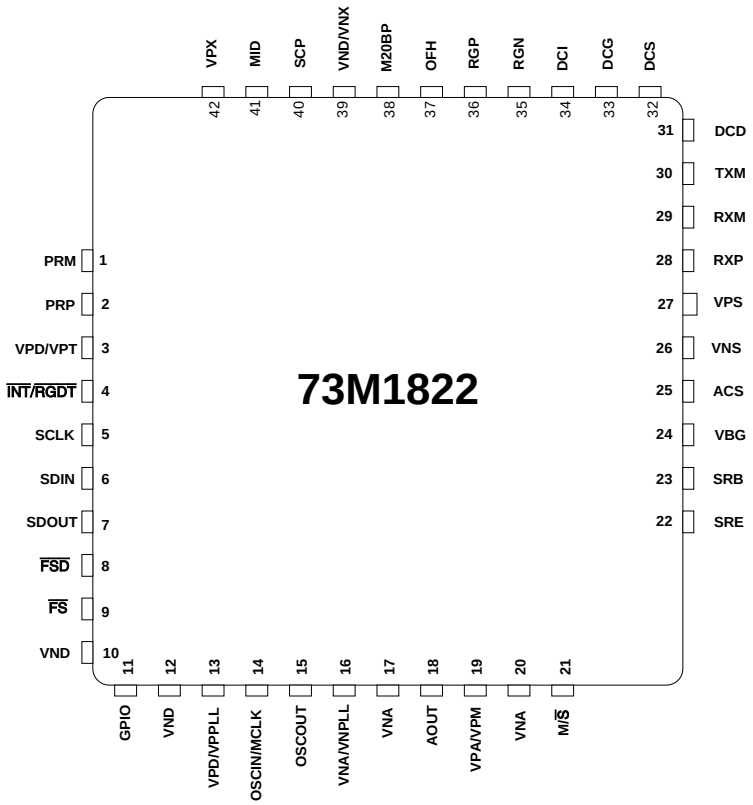


Figure 6: 73M1822 42-Pin Pinout

Table 5 describes the pin functions for the device. Decoupling capacitors on the power supplies should be included for each pair of supply pins.

Table 5: 73M1822 Pin Definitions

Pin Number	Pin Name	Type	Description
1	PRP	I/O	Pulse transformer primary plus
2	PRM	I/O	Pulse transformer primary minus
3	VPD/VPT	PWR	Positive digital/transformer supply
4	$\overline{\text{INT}}/\overline{\text{RGDT}}$	O	Ring detection indicator or other Interrupts Open drain
5	SCLK	O	Serial interface clock. With continuous SCLK selected, Frequency = 256∗Fs (=1.8432 MHz for Fs=7.2 kHz, 2.048 MHz for Fs=8 kHz)
6	SDIN	I	Serial data input (or output from the controller to the 73M1822)
7	SDOUT	O	Serial data output (or input to the controller from the 73M1822)
8	$\overline{\text{FSD}}$	O	FS delayed
9	$\overline{\text{FS}}$	O	Frame synchronization
10	VND	GND	Negative digital ground
11	GPIO	I/O	Configurable digital input/output pins
12	VND	GND	Negative digital ground
13	VPD/VPPLL	PWR	Positive digital supply

Pin Number	Pin Name	Type	Description
14	OSCIN/MCLK	I	Crystal oscillator circuit input pin. Input from an external clock source. Crystal frequency range supported is 9 MHz – 27 MHz.
15	OSCOUT	O	Crystal oscillator output pin. (N.C. with external oscillator)
16	VNA/VNPLL	GND	Negative PLL ground
17	VNA	GND	Negative analog ground
18	AOUT	O	Call progress audio output
19	VPA/VPM	PWR	Positive analog supply
20	VNM/VNT	GND	Negative transformer supply
21	M/$\overline{S}$	I	Master or slave selection / reset - active during transition
22	SRE	I	S/Sh regulator sense
23	SRB	O	S/Sh regulator drive
24	VBG	O	VBG bypass, connect to 0.1uF capacitor to VPS
25	ACS	I	AC current sense
26	VNS	GND	LIC analog/digital negative ground
27	VPS	PWR	LIC analog/digital positive supply voltage
28	RXP	I	Receive plus -signal input
29	RXM	I	Receive minus - signal input
30	TXM	O	Transmit minus - signal output
31	DCD	O	DCD for integrated Darlington
32	DCS	I	DC loop current sense
33	DCG	O	DC loop drive
34	DCI	I	DC loop input
35	RGM	I	Ring minus voltage input
36	RGP	I	Ring plus voltage input
37	OFH	O	Off-hook control
38	M20BP	I	Substrate connection. Connect to VNX.
39	VND/VNX	GND	LIC digital/analog negative ground
40	SCP	I/O	Positive side of the secondary pulse transformer winding
41	MID	I/O	Charge pump -normally left open
42	VPX	PWR	LIC supply from the barrier side

2.6 Exposed Bottom Pad on 73M1x66B QFN Packages

✓ The 73M1822 and 73M1922 QFN packages have exposed pads on the underside that are intended for device manufacturing purposes. These exposed pads are not intended for thermal relief (heat dissipation) and should not be soldered to the PCB. Soldering of the exposed pad could also compromise electrical isolation/insulation requirements for proper voltage isolation. Avoid any PCB traces or through-hole vias on the PCB beneath the exposed pad area.

3 Electrical Characteristics and Specifications

3.1 Isolation Barrier Characteristics

Table 6 provides the characteristics of the 73M1x22 Isolation Barrier.

Table 6: Isolation Barrier Characteristics at 8 kHz Sample Rate

Parameter	Rating
Barrier frequency	768 kHz
Data transfer rate across the barrier	1.536 Mbps

3.2 Electrical Specifications

This section provides the absolute maximum ratings, the recommended operating conditions and the DC characteristics.

3.2.1 Absolute Maximum Ratings

Table 7 lists the maximum operating conditions for the 73M1x22. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to the extremes of the absolute maximum rating for extended periods may affect device reliability.

Table 7: Absolute Maximum Device Ratings

Parameter	Min	Max	Unit
Supply voltage	-0.5	4.0	V
Pin input voltage (except OSCIN)	-0.5	6.0	V
Pin input voltage (OSCIN)	-0.5 to VDD	0.5	V

3.2.2 Recommended Operating Conditions

Function operation should be restricted to the recommended operating conditions specified in Table 8.

Table 8: Recommended Operating Conditions

Parameter	Min	Max	Unit
Supply voltage (VDD) with respect to VSS	3.0 V	3.6	V
Operating temperature	0	85	°C

3.2.3 DC Characteristics

Table 9 lists the 73M1x22 DC characteristics.

Table 9: DC Characteristics

Parameter		Condition	Min	Nom	Max	Unit
Input low voltage	VIL	–	-0.5	–	0.2 ∗ VDD	V
Input high voltage (except OSCIN)	VIH1	–	0.7 VDD	–	5.5	V
Input High Voltage OSCIN	VIH2	–	0.7 VDD	–	VDD + 0.5	V
Output low voltage (except OXCOUT, $\overline{FS}$, SCLK, SDOUT)	VOL	IOL=4 mA	–	–	0.45	V
Output low voltage OSCOUT	VOLOSC	IOL=3 mA	–	–	0.7	V
Output Low Voltage $\overline{FS}$, SCLK, SDOUT	VOL	IOL = 1mA	–	–	0.45	V
Output high voltage (except OSCOUT, $\overline{FS}$, $\overline{FSD}$, SCLK, SDOUT)	VOH	IOH=-4 mA	VDD - 0.45	–	–	V
Output High Voltage OSCOUT	VOHOSC	IOH =-3.0 mA	VDD - 0.9	–	–	V
Output high voltage $\overline{FS}$, $\overline{FSD}$, SCLK, SDOUT	VOH	IOH=-1 mA	VDD - 0.45	–	–	V
Input low leakage current	IIL1	VSS < Vin < VIL1	10	–	40	µA
Input high leakage current	IIH1	VIH1 < Vin < 5.5		–	1	µA
Input Leakage Current OSCIN	IIL2	VSS < Vin < VIL2	1	–	30	µA
Input High Leakage Current OSCIN	IIH2	VIH2 < Vin < VDD	1	–	10	µA
IDD current at 3.0 V – 3.6 V Nominal at 3.3 V						
Active digital current	$IDD1_{dig}$	–	–	1.0	1.5	mA
Active PLL current	$IDD1_{pll}$	–	–	1.0	1.5	mA
Active analog current	$IDD1_{ana}$	–	–	12	17	mA
IDD total current*	IDD1	–	–	15	20	mA
IDD total current*	IDD2	–	–	20	30	mA
IDD current PWDN=1	IDD2	–	–	1.0	5	µA
IDD current SLEEP=1 (Ext Ref Clk)	IDD3	–	–	0.5	1.0	mA
IDD current IDL2=1 (Ext Ref Clk)	IDD4	–	–	10	15	mA
IDD current ENFEH=0 (Ext Ref Clk)	IDD5	–	–	1.0	1.5	mA

*Note: IDD1 is with the secondary of the barrier left open.
IDD2 is with the secondary of the barrier connected to the 73M1912 fully powered.

3.3 Serial Interface Timing Specification

The 73M1x22 has a synchronous serial interface, called the MAFE interface, to transfer data to and from a host. Table 10 provides the timing specification for the MAFE interface.

Table 10: Serial Data Port Timing at 8 kHz Sample Rate

Parameter	Min	Nom	Max	Unit
SCLK period (Tsclk)	–	1/1.536 MHz	–	ns
SCLK to $\overline{FS}$ delay (td1) – mode1	–	–	20	ns
SCLK to $\overline{FS}$ delay (td2) – mode1	–	–	20	ns
SCLK to SDOUT delay (td3) with 10 pf load	–	–	20	ns
Setup time SDIN to SCLK (tsu)	15	–	–	ns
Hold time SDIN to SCLK (th)	10	–	–	ns
SCLK to $\overline{FS}$ delay (td4) – mode 0	–	–	20	ns
SCLK to $\overline{FS}$ delay (td5) – mode 0	–	–	20	ns

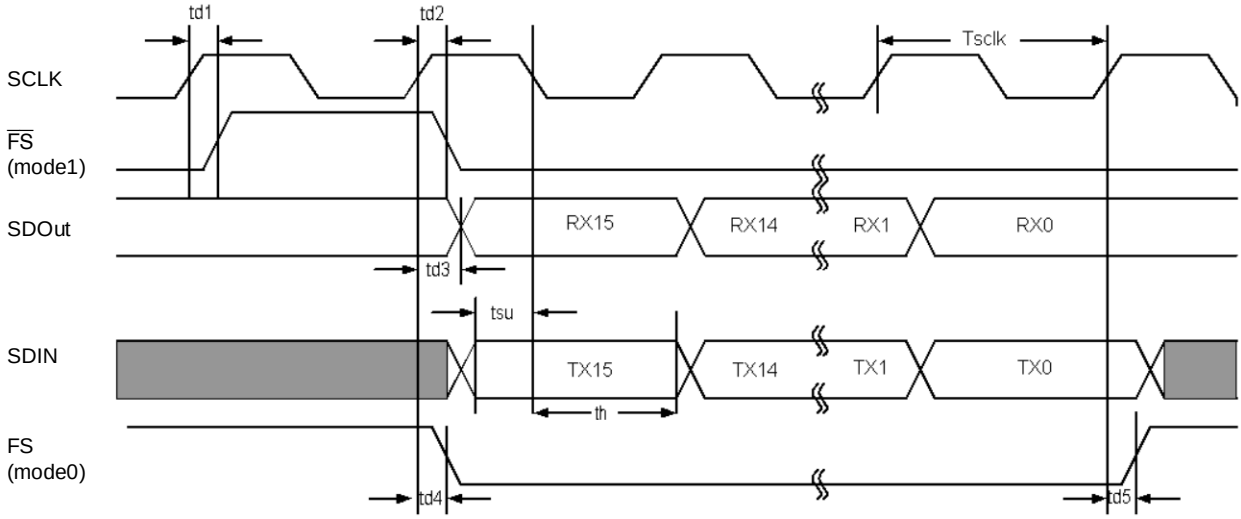


Figure 7: MAFE Timing Diagram

3.4 Analog Specifications

This section provides the electrical characterizations of the 73M1x22 analog circuitry.

3.4.1 DC Specifications

VBG is to be connected to an external bypass capacitor with a minimum value of 0.1 µF. This pin is not intended for any other external use.

Table 11: Reference Voltage Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	VDD=3.0 V – 3.6 V	0.9	1.19	1.4	V
VBG Noise	300 Hz – 3.3 kHz	–	-86	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB

3.4.2 Call Progress Monitor

The Call Progress Monitor monitors activities on the line. The audio output contains both transmit and receive data with a configurable level individually set by Register 0x10.

Figure 8 shows the frequency response of the Call Progress Monitor Filter based upon the characteristics of the device plus the external circuitry as shown.

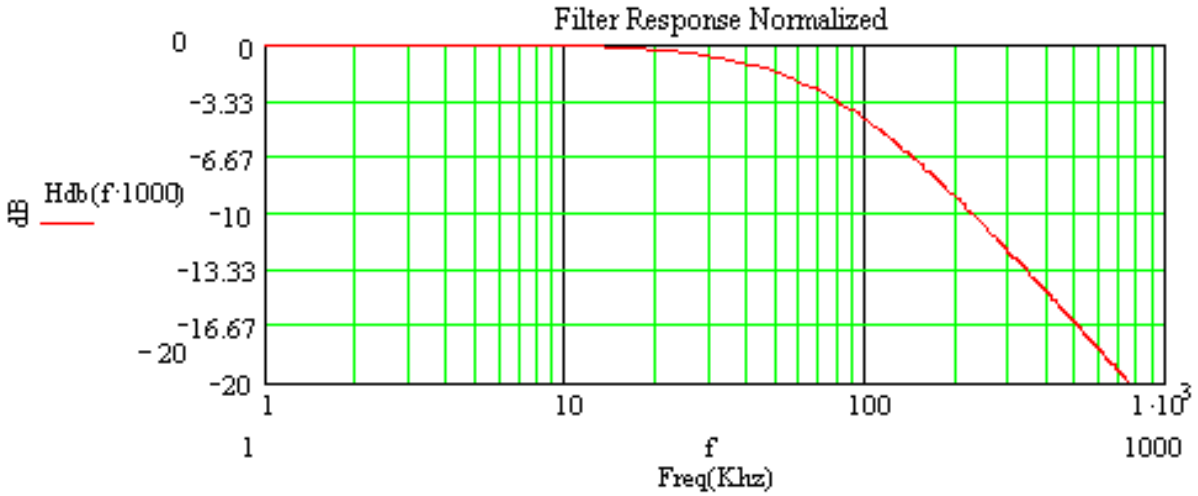


Figure 8: Call Progress Monitor Frequency Response

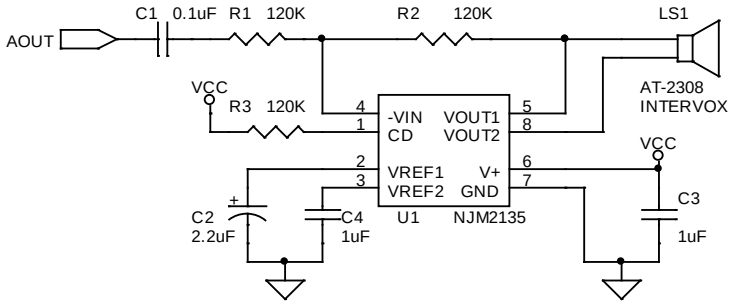


Figure 9: Demo Board Circuit Connecting AOUT to a Speaker

Table 12: Component Values for the Speaker Driver

Quantity	Reference	Part Description	Part
1	C1	Ceramic capacitor	0.1 µF
1	C2	Ceramic capacitor	2.2 µF (optional)
2	C3, C4	Ceramic capacitor	1 µF
1	LS1	Sound transducer	Speaker (Intervox)
3	R1, R2, R3	1/8 W resistor	120 kΩ
1	U1	Audio amplifier	NJM2135 (New Japan Radio)

All measurements are at the AOUT pin with CMVSEL=0. Note that when CMVSEL=1, the peak signal at AOUT is increased to approximately 1.11 Vpk.

Table 13: Call Progress Monitor Specification

Parameter	Test Condition	Min	Nom	Max	Units
AOUT for transmit	1 kHz full swing code word at SDIN pin CMRXG=11(Mute) Observe AOUT pin	–	–	–	–
	CMTXG=00	–	0.98	–	Vpk
	CMTXG=01 relative to CMTXG=00	–	-6	–	dB
	CMTXG=10 relative to CMTXG=00	–	-12	–	dB
	CMTXG=11(Mute)	–	Mute	–	dB
AOUT transmit THD	CMTXG=00	–	40	–	dB
AOUT for receive	1.0 Vpk, 1 kHz at the line or 0.5 Vpk at RXP/RXM with RXG=10 (+6 dB) CMTXG=11(Mute) Observe AOUT pin	–	–	–	–
	CMRXG=00	–	0.96	–	Vpk
	CMRXG=01 relative to CMRXG=00	–	-6	–	dB
	CMRXG=10 relative to CMRXG=00	–	-12	–	dB
	CMRXG=11(Mute)	–	Mute	–	dB
AOUT receive THD	CMRXG=00	–	40	–	dB
AOUT output impedance	–	–	10	–	kΩ

3.5 73M1x22 Line-Side Electrical Specifications (73M1912)

Table 14 lists the absolute maximum ratings for the line side. Operation outside these rating limits may cause permanent damage to this device.

Table 14: Line-Side Absolute Maximum Ratings

Parameter	Min	Max	Unit
Pin input voltage from VPX to VNX	-0.5	6.0	V
Pin input voltage (all other pins) to VNS	-0.5	4.0	V

3.6 Reference and Regulation

Table 15 lists the VBG specifications. VBG should be connected to an external bypass capacitor with a minimum value of 0.1µF. This pin is not intended for any other external use.

The following conditions apply: VPX=5 V; Barrier Powered Mode; Barrier Data Rate across the Barrier=1.5 Mbps; VBG connected to 0.1 µF external cap.

Table 15: VBG Specifications

Parameter	Test Condition	Min	Nom	Max	Units
VBG	See conditions above.	–	1.19	–	V
VBG Noise	300 Hz – 3.3 kHz	–	-86*	-80	dBm_{600}
VBG PSRR	300 Hz – 30 kHz	40	–	–	dB
VPS	VPX=5.5 V	–	3.15	–	V
VPS PSRR	VPX=4.5 V to 5.5 V	–	40	–	dB

3.7 AC Signal Levels

Table 16 shows the maximum transmit levels that the 73M1912 Line-Side Device is capable of delivering.

Table 16: Maximum Transmit Levels

Transmit Type	Maximum Level at the Line (dBm)	Peak to RMS Ratio	RMS Voltage on the Line (V)	Peak Voltage on the Line (V)
V.90	-12.0	4	0.195	0.778
QAM	-7.3	2.31	0.334	0.772
DPSK	-5.1	1.81	0.431	0.779
FSK	-3.0	1.41	0.548	0.775
DTMF (high tone)	-7.8	1.41	0.316	0.446
DTMF (low tone)	-9.8	1.41	0.251	0.354

3.8 DC Transfer Characteristics

Table 17 lists the maximum DC output levels. All tests are driven at pin DCI and measured at pin DCS. DCEN=1 and pin DCI is shorted to pin DCS. ILM=0 unless stated otherwise.

Table 17: Maximum DC Transmit Levels

Parameter	Test Condition	Min	Nom	Max	Units
V_{DCON} (DC "On" Voltage)	DCIV=00	0.69	0.73	0.78	V
	DCIV=01	0.89	0.94	0.99	V
	DCIV=10	1.01	1.06	1.11	V
	DCIV=11	1.13	1.18	1.23	V
With ENAC=0	DCIV=XX	0.27	0.31	0.35	V
DC Gain	$V_{DCON}<V_{DCI}<0.4V+V_{DCON}$	-0.25	0 .0	+0.25	dB
I_{DCI} before ILIM	ILM=1 $V_{DCI}=0.28V+V_{DCON}$	–	–	1	µA
I_{DCI} after ILIM	ILM=1 $V_{DCI}=0.44V+V_{DCON}$	20	–	–	µA
*Noise	At the line with 300 Ω(ac) (0.15 - 4.0 kHz)	–	-85	-80	dBm

3.9 Transmit Path

Table 18 lists the transmit path characteristics. A pattern for a sinusoid of 1 kHz, full scale (code word of +/- 32,767) from the 73M1x22 is forced and ACS is measured with R10=255 Ω. Test conditions are: ACZ=00 (600 Ω termination), THEN=1, ATEN=1, DAA=01, TXBST=0.

Table 18: Transmit Path

Parameter	Test Condition	Min	Nom	Max	Units
Offset voltage	50% 1's density relative to 1.4 V Nom	–	25	–	mV
Tx gain	DAA=00	–	+2	–	dB
	DAA=01	–	0	–	dB
	DAA=10	–	-4	–	dB
	DAA=11	–	-8	–	dB
AC swing	DAA=01	0.39	0.425	0.45	Vpk
	DAA=00	–	0.535	–	Vpk
	TXBST=1, DAA=xx	–	0.850	–	Vpk
	ACZ=01	–	0.2751	–	Vpk
	ACZ=10	–	0.295	–	Vpk
	ACZ=11	–	0.265	–	Vpk
Idle noise	300 Hz – 4 kHz	–	-81	–	dBm
THD	300 Hz – 4 kHz	–	-80	–	dB
Intermod distortion 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-85	–	dB
PSRR	-30 dBm signal at VPX in Mixed Mode; 300 Hz – 30 kHz	–	–	40*	dB
Pass band ripple	150 Hz – 3.3 kHz	-0.125	–	+0.125	dB
	Gain relative to 1 kHz	–	–	–	dB
	0.5 kHz	–	0.17	–	dB
	1.0 kHz	–	0	–	dB
	2.0 kHz	–	0.193	–	dB
	3.3 kHz	–	-0.12	–	dB
Aliased image	Fs +/- 1 kHz, relative to 1 kHz	–	-75	–	dB

3.10 Receive Path

Table 19 list the receive path characteristics. All test inputs are driven by a signal generator at the collector of Q5.

Table 19: Receive Path

Parameter	Test Condition	Min	Nom	Max	Units
Differential input resistance	RXP/RXM	–	1000	–	kΩ
Input level	Differential, RXP/RXM	–	1.0	1.16	Vpk
Input level	Common mode, RXP/RXM	–	1.37		V
Overall ΣΔ ADC modulation gain inclusive of 73M1902 processing	Normalized to VRef=1.40 V. RXG=00; RXM=0	43	47	51	µV/bit
Offset voltage		–	13	70	mV
Rx gain	RXG=00	–	0	–	dB
	RXG=01	2	3	4	dB
	RXG=10	5	6	7	dB
	RXG=11	8	9	10	dB
	RXBST=1, RXG=00	17.5	19.5	21.0	dB
Overall receive frequency response inclusive of 73M1902 processing	Relative to 1 kHz	–	–	–	
	0.3 kHz – 3.3 kHz	-0.25	0	+0.25	dB
	Fs (8 kHz)	–	-75	–	dB
Idle noise	300 Hz – 4 kHz	–	-81	–	dBm
THD	RXG[1:0]=00	–	-80	–	dB
	RXBST=1	–	-60	–	
Intermod distortion 1.0 kHz and 1.2 kHz summed	300 Hz – 4 kHz	–	-80	–	dB
Crosstalk	1 Vpk 1 kHz sine wave at TXP; FFT on Rx ADC samples, first four harmonics reflected to the line.	–	-85	–	dBm
CMRR	RXP=RXM 1 Vpk	40	–	–	dB
PSRR	-30 dBm signal at VPX in Barrier Powered Mode; 300 Hz – 30 kHz.	–	–	40*	dB

3.11 Transmit Hybrid Cancellation

Table 20 lists the transmit hybrid cancellation characteristics. Unless stated otherwise, test conditions are: ACZ=00 (600 Ω termination), THEN=1, ATEN=1, DAA=01, TXBST=0. TXM is externally fed back into the 73M1912 to effect cancellation of transmit signal.

Table 20: Transmit Hybrid Cancellation Characteristics

Parameter	Test Condition	Min	Nom	Max	Units
Transmit hybrid cancellation	Measure RxD in HIC	–	26	–	dB
Offset voltage	50% 1's Density	–	25	50	mV
AC swing	1 kHz sinusoid at Tip and Ring	0.85	0.95	1.05	Vpk
Idle noise	300 Hz – 4 kHz at Tip and Ring	–	-81	–	dBm

3.12 Receive Notch Filter

Table 21 lists the receive notch filter characteristics. All measurements taken with RLPNEN=1, TXEN=0, RXG=00, ATEN=1. RXP is driven with 1 Vpk signal.

Table 21: Receive Notch Filter

Parameter	Test Condition	Min	Nom	Max	Unit
Magnitude response	**RLPNH=0 (12 kHz Notch)**				
	300 Hz	–	0.0	–	dB
	1 kHz	–	+0.03	–	dB
	3 kHz	–	+0.04	–	dB
	16 kHz	-20	-50	–	dB
	Passband Ripple (0.3 kHz – 3.4 kHz)	–	+/- 0.15	–	dB
Delay		–	28.8	–	µs
	300 Hz	–	28.93	–	µs
	1 kHz	–	30.25	–	µs
	3 kHz	–	41.62	–	µs
	12 kHz	–	9.95	–	µs
Magnitude response	**RLPNH=1 (16 kHz Notch)**				
	300 Hz	–	0.0	–	dB
	1 kHz	–	+0.04	–	
	3 kHz	–	+0.11	–	dB
	12 kHz	-20	-50	–	dB
	Passband Ripple (0.3 kHz – 3.4 kHz)	–	+/- 0.15	–	dB
Delay		–	30.53	–	µs
	300 Hz	–	30.66	–	µs
	1 kHz	–	31.93	–	µs
	3 kHz	–	42.26	–	µs
	16 kHz		4.74	–	µs

3.13 Detectors

This section provides electrical characteristics for the following detectors:

- Over-Voltage.
- Over-Current.
- Under-Voltage.
- Over-Load.

3.13.1 Over-Voltage Detector

The values in Table 22 were measured in IDL2 mode between RGP and RGN.

Table 22: Over-Voltage Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over voltage levels	OVDTH=0	0.52	0.6	0.68	V
	OVDTH=1	0.59	0.7	0.77	V

3.13.2 Over-Current Detector

The values in Table 23 were measured in Barrier Powered Mode.

Table 23: Over-Current Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over current level	Measured at DCS.	0.85	0.96	1.10	V

3.13.3 Under-Voltage Detector

The values in Table 24 were measured in Barrier Powered Mode. In the recommended schematic (see Figure 10 and Figure 11), disconnect Q5 collector and connect to an external power supply, VPE, through a 600 Ω resistor.

Table 24: Under-Voltage Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Under voltage detect	Measure VPE when UVD is detected as VPE is decreased.	5.6	–	6.5	V

3.13.4 Over-Load Detector

The values in Table 25 were measured in Barrier Powered Mode.

Table 25: Over-Load Detector

Parameter	Test Condition	Min	Nom	Max	Unit
Over load level	Measured at DCI with 1 kHz.	0.6	0.75	0.9	Vpk

4 Applications Information

This section provides general usage information for the design and implementation of the 73M1x22. The documents listed in Section **Error! Reference source not found.** provide more detailed information. Always consult with Teridian Semiconductor for the latest recommendations before finalizing a design.

4.1 Example Schematic of the 73M1922 and 73M1822

Figure 10 shows a reference schematic for the 73M1922. Figure 11 shows a reference schematic of the 73M1822. Note that minor changes may occur to the reference material from time to time and the reader is encouraged to contact Teridian for the latest information. For more information about schematic and layout design, see the *73M1822/73M1922 Schematic and Layout Guidelines*.

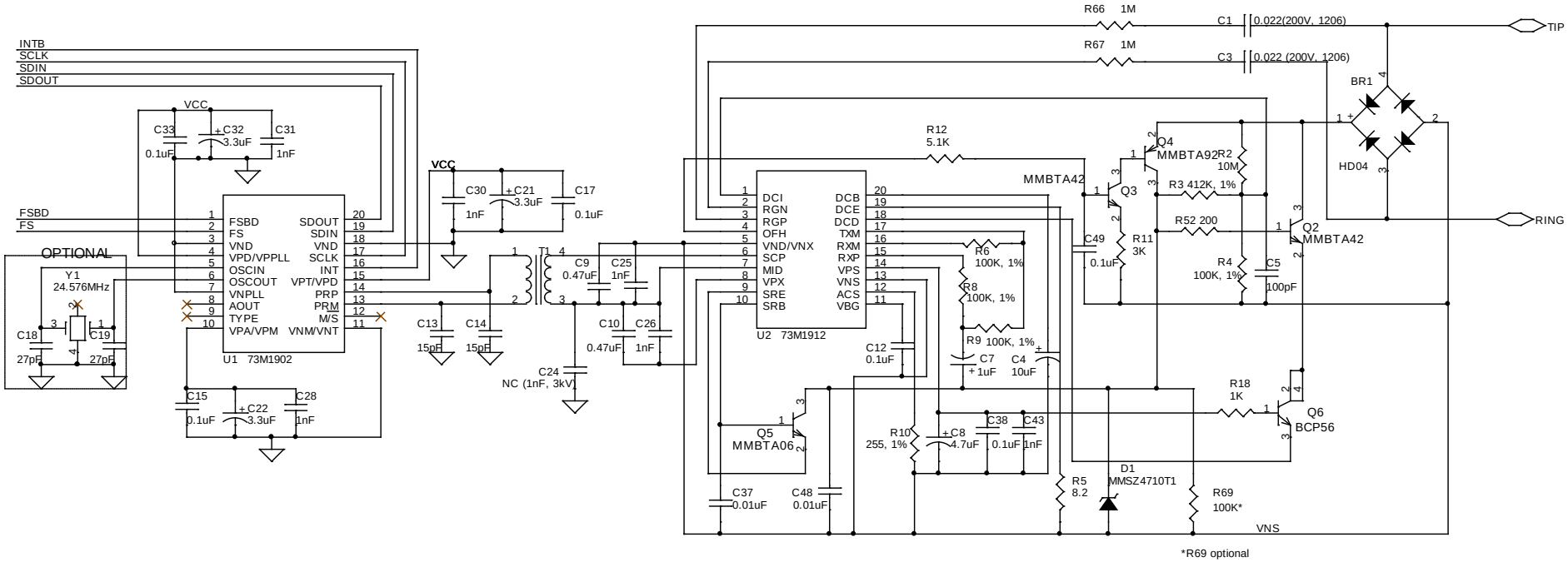


Figure 10: Recommended Circuit for the 73M1922

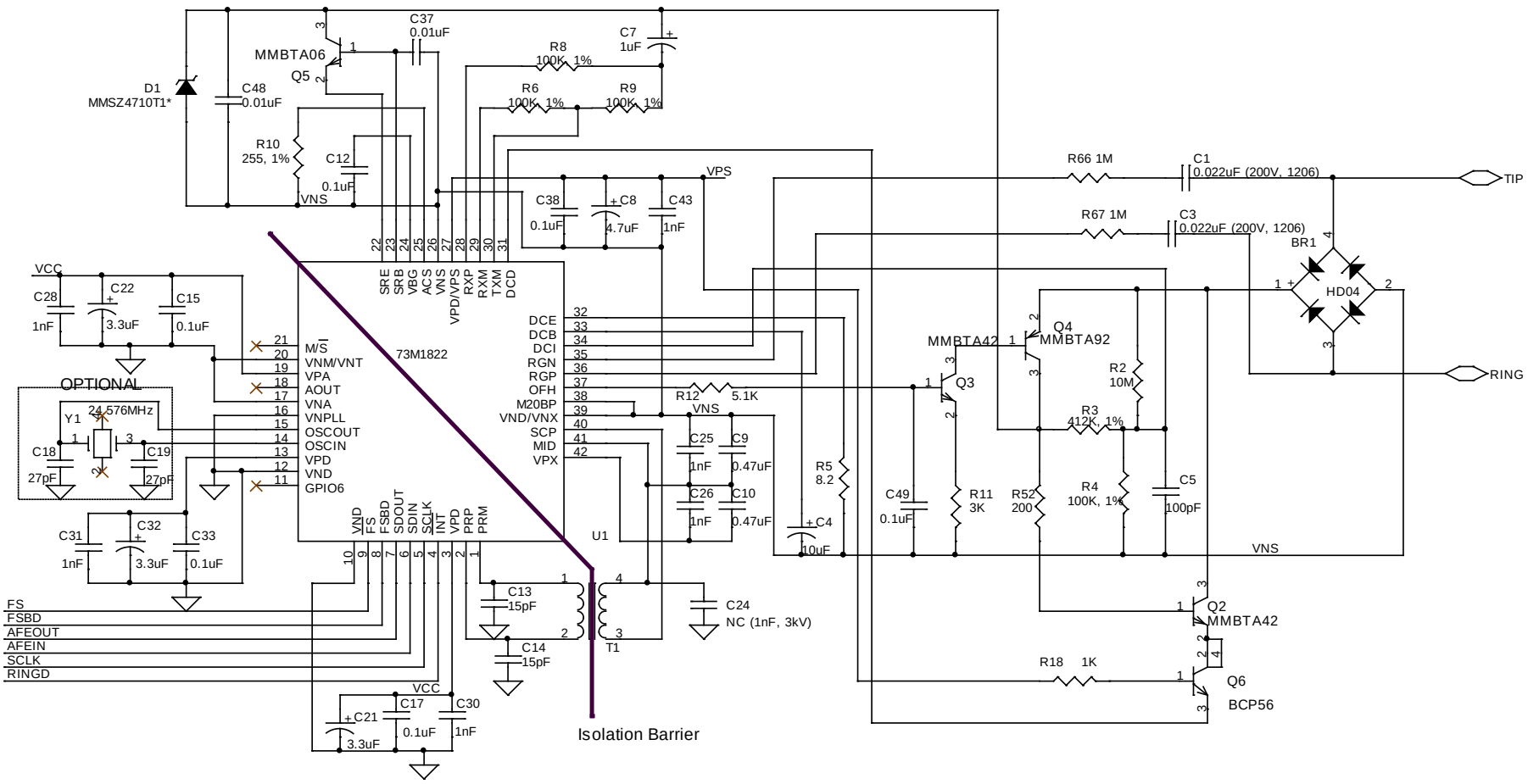


Figure 11: Recommended Circuit for the 73M1822

4.2 Bill of Materials

Table 26 provides the 73M1x22 bill of materials for the reference schematics provided in Figure 10 and Figure 11.

Table 26: Reference Bill of Materials for 73M1822/73M1922

Reference	Part Description	Example Source	Example MFR P/N
BR1	HD04 rectifier bridge, 0.8A, 400V	Diodes Inc.	HD04-T
C1, C3	0.022µF 200V, X7R, 1206	Panasonic	ECJ-3FB2D223K
C4	10µF 6.3V, tantalum, 0805	AVX, Panasonic	TCP0J106M8RA
C5	100pF 50V, ceramic, 0603	Taiyo Yuden	UMK107CH101JZ-T
C7	1µF 6.3V, tantalum, 0805	Rohm	TCP0J105M8R
C8	4.7µF, 6.3V, X5R, ±10%, ceramic, 0805	Panasonic	ECJ-2YB0J475K
C9, C10	0.47µF, 6.3V, X5R, ±10%, ceramic, 0603	Panasonic	ECJ-1VB0J474K
C12, C15, C17, C33, C38, C49	0.1µF, 16V, X7R, ±10%, ceramic, 603	Panasonic, Kemet	C0603C104K8RACTU
C13, C14	15pF 50V, ceramic, 0603	Panasonic	ECJ-1VC1H150J
C18, C19	27pF 50V, ceramic, 0603	Panasonic	ECJ-1VC1H270J
C21, C22, C32	3.3µF, 6.3V, X5R, ±10%, ceramic, 0805	Panasonic	ECJ-2YB0J335K
C24	NC (1nF, 3kV)		
C25, C26, C28, C30, C31, C43	1nF 10V, X7R, ceramic, 0603	Panasonic	C0603C102K8RACTU
C37, C48	0.01µF, 50V, X7R, ±10%, ceramic, 603	AVX, Panasonic, UTC	06035C103KAT2A
D1	25V, 500mW Zener diode	ON Semi, Diodes, Inc.	MMSZ4710T1
Q2, Q3	A42, NPN 300 V transistor SOT23	Diodes, Central Semi	MMBTA42LT1G
Q4	A92, PNP 300 V transistor SOT23	Diodes, On Semi	MMBTA92LT1G
Q5	A06, NPN 80 V transistor SOT23	Fairchild, On Semi	MMBTA06LT1G
Q6	NPN 80 V transistor SOT223	Fairchild, On Semi	BCP56
R2	10M 1%, 1/8W resistor 0805	Panasonic, Yageo	RC0603FR-0710ML
R3	412 K, 1%, 1/16W resistor 0603	Panasonic	ERJ-3EKF4123V
R4, R6, R8, R9	100K, 1%, 1/16W resistor 0603	Panasonic	ERJ-3EKF1003V
R5	8.2, 1%, 1/8W resistor 0805	Vishay	CRCW08058R20FNEA
R10	255, 1%, 1/16W resistor 0603	Panasonic	RC0603FR-07255RL
R11	3 K, 1/16 W resistor 0603	Panasonic, Yageo	RC0603FR-073K0L
R12	5.1 K, 1/16 W resistor 0603	Panasonic, Yageo	RC0603FR-075K1L
R18	1 K, 1/16W resistor 0603	Panasonic	ERJ-3EKF1001V
R52	200, 1/16W resistor 0603	Panasonic	ERJ-3EKF2000V
R66, R67	1 M,1/8W resistor 0805	Panasonic, Yageo	RC0805FR-071ML
R69*	100K typ. 5%, 1/10W resistor 0603	Yageo	RC0603JR-07100KL
T1	Pulse transformer	See Table 28.	
Y1	24.576 MHz crystal (fundamental)	ECS/Abracon	–

* Optional – see the *73M1822/73M1922 Schematic and Layout Guidelines* for details.

4.3 Over-Voltage and EMI Protection

Over-voltage/over-current protection is required to meet worst-case conditions for target countries. UL1950, EN60950, IEC 60950, ITU-T K.20/K.21 and GR-1089-CORE specifications define the protection requirements for many countries. A single design can be implemented to meet all these requirements.

Figure 12 shows a recommended protection circuit topology. Fuse (F1) should be rated for 600 V operation and the bidirectional thyristor (E1) should have a minimum break-over of 275 V and be able to survive a 100 A fast transient. In addition to over-voltage and current protection, the line-interface designer should make provisions to prevent EMI emissions and susceptibility. Figure 12 also illustrates how L1, L2, C35, C36 and C42 can provide this suppression. The ferrite beads, L1 and L2, should be capable of passing 200 mA and have an impedance of 2000 Ω at 100 MHz. C35, C36 and C42 should be 220 pF and rated for a breakdown voltage greater than the highest isolation voltage that is required for country compatibility. C35 and C36 should be returned to an earth ground. EMI suppression is dependent on the physical design of the overall circuit and not all the suppression components may be needed in every design and application. The values shown are typical and should be optimized for a particular design.

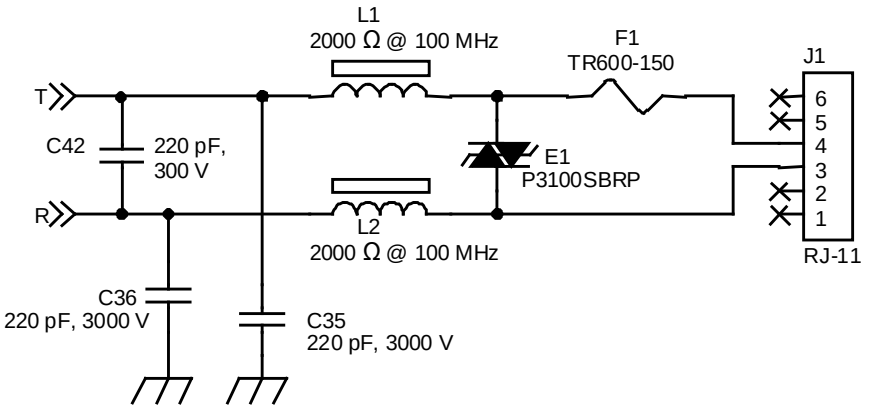


Figure 12: Suggested Over-voltage Protection and EMI Suppression Circuit

Table 27: Reference Bill of Materials for Figure 12

Reference	Part Description	Source	Example MFR P/N
E1	Bidirectional thyristor, 275V/ 100A	Diodes, Inc.	TB3100H-13-H
F1	150mA, 600V PTC resettable fuse	Bourns	MF-R015/600 or equivalent
L1,L2	2 KΩ @ 100 MHz, 200 mA min, 0805	Steward/TDK	MPZ2012S601A
C36, C35	220 pF, 3000 V	TDK	C4532COG3F221K
C42	220 pF, 300 V	Vishay	VJ1206Y221KXEAT5Z

4.4 Isolation Barrier Pulse Transformer

The isolation element used by the 73M1x22 is a standard digital pulse transformer. Several vendors supply compatible transformers with up to 6000 V ratings. Since the transformer is the only component crossing the isolation barrier other than EMI capacitors that may be required, it solely determines the isolation between the PSTN and the 73M1922 digital interface. This method of isolation is significantly superior to other isolation techniques with major advantages in high common mode voltage operation, lower radiated noise (EMI) and improved operation in noisy environments. Table 28 lists some pulse transformers compatible with the 73M1x22. The table also includes lower-voltage transformers that offer low-cost alternatives if such voltages are sufficient.

Table 28: Compatible Pulse Transformer Sources

Company	Number
Sumida	ESMIT 4180
Wurth Electronics Midcom Inc.	750110001
UMEC	TG-UTB01543S
Datatronics	PT79280
AAsupreme	P95003

Table 29 lists some of the typical transformer specifications used by the 731x22. Contact the manufacturer directly for product information.

Table 29: Transformer Characteristics

Parameter	Test Condition	Min	Nom	Max	Tolerance	Unit
Inductance	100 kHz, 10 mVAC, 1-2, Ls.	54	60	200	–	µH
Interwinding Capacitance	–	–	–	6	–	pF
Turn Ratio	–	–	1:1	–	±2 %	N/A
DC Resistance	Primary	–	–	0.25	–	Ω
	Secondary	–	–	0.25	–	Ω
Dielectric Breakdown Voltage	1 sec	2000	3750	–	–	Vrms
ET Constant	–	–	1.2	–	–	Vµs
Surge Test	1.2 x 50 µs	2800	6000	–	–	Vpeak
Operating Temperature	–	-40	–	85	–	°C

5 Control and Status Registers

Table 30 shows the register map of addressable registers for the 73M1822 and 73M1922. The shaded cells in the register map indicate read only and cannot be modified. Reserved bits should be left in their default state. Accessing unspecified registers should be avoided. Each register and bit is described in detail in the following sections.

For registers 0x12 through 0x1F, which are located in the Line-Side Device, there is a minimum time between consecutive write transactions of 300 µs.

Table 30: Control and Status Register Map

Address (hex)	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	00h/9Ch	DSYEN	NSLAVE2	NSLAVE1	NSLAVE0	MSIDEN	MSID	SCK32	Reserved
02	00h	TMEN	Reserved	Reserved	Reserved	Reserved	ENLPW	SPOS	HC
03	F0h	GPIO7	GPIO6	GPIO5	GPIO4	RGMON	DET	SYNL	RGDT
04	F7h	DIR7	DIR6	DIR5	DIR4	REVHSD3	REVHSD2	REVHSD1	REVHSD0
05	0Bh	ENGPIO7	ENGPIO6	ENGPIO5	ENGPIO4	ENAPOL	ENDET	ENSYNL	ENRGDT
06	00h	POL7	POL6	POL5	POL4	Reserved	Reserved	Reserved	Reserved
07	00h	Reserved	Reserved	Reserved	Reserved	DTST3	DTST2	DTST1	DTST0
08	DAh	PSEQ7	PSEQ6	PSEQ5	PSEQ4	PSEQ3	PSEQ2	PSEQ1	PSEQ0
09	EFh	PRST2	PRST1	PRST0	PDVSR4	PDVSR3	PDVSR2	PDVSR1	PDVSR0
0A	31h	ICHP3	ICHP2	ICHP1	ICHP0	Reserved	KVCOH2	KVCOH1	KVCOH0
0B	2Ah	Reserved	NDVSR6	NDVSR5	NDVSR4	NDVSR3	NDVSR2	NDVSR1	NDVSR0
0C	06h	NSEQ7	NSEQ6	NSEQ5	NSEQ4	NSEQ3	NSEQ2	NSEQ1	NSEQ0
0D	42h	LOKDET	SLHS	Reserved	Reserved	CHNGFS	NRST2	NRST1	NRST0
0E	00h	FRCVCO	PWDNPLL	Reserved	Reserved	Reserved	Reserved	RGTH1	RGTH0
0F	2Ch	ENFEH	PWDN	SLEEP	Reserved	XIB1	XIB0	Reserved	Reserved
10	00h	Reserved	Reserved	Reserved	CMVSEL	CMTXG1	CMTXG0	CMRXG1	CMRXG0
12	00h	OFH	ENDC	ENAC	ENSHL	$\overline{\text{ENLVD}}$	ENFEL	ENDT	ENNOM
13	00h	DCIV1	DCIV0	ILM	ACCEN	PLDM	OVDTH	IDISPD1	IDISPD0
14	00h	TXBST	DAA1	DAA0	Reserved	RXBST	RLPNH	RXG1	RXG0
15	00h	Reserved	DISNTR	Reserved	CIDM	THEN	ENUVD	ENOVD	ENOID
16	01h	TXEN	RXEN	RLPNEN	ATEN	FSCTR3	FSCTR2	FSCTR1	FSCTR0
17	00h	APWS	Reserved	Reserved	ACZ1	ACZ0	Reserved	Reserved	Reserved
18	01h	TEST3	TEST2	TEST1	TEST0	Reserved	Reserved	Reserved	Reserved
19	00h	POLL	MATCH	Reserved	IDL2	INDX3	INDX2	INDX1	INDX0
1A	00h	RNG7	RNG6	RNG5	RNG4	RNG3	RNG2	RNG1	RNG0
1B	00h	LV7	LV6	LV5	LV4	LV3	LV2	LV1	Reserved
1C	00h	LC6	LC5	LC4	LC3	LC2	LC1	LC0	Reserved
1D	90h	REVLSD3	REVLSD2	REVLSD1	REVLSD0	Reserved	Reserved	Reserved	Reserved
1E	00h	ILMON	UVDET	OVDET	OIDET	SLLS	Reserved	Reserved	Reserved
1F	00h	POLVAL7	POLVAL6	POLVAL5	POLVAL4	POLVAL3	POLVAL2	POLVAL1	POLVAL0

Throughout this document, type W is read/write, type WO is write only and type R is read only. Registers and bits are defined as 0x16[3:0], where 0x16 is the register address and the numbers in square brackets specify the address bits. The bit order is [msb – lsb] for a field. For example, [3:0] means bits 3 through 0 of a particular field.

Table 31: Alphabetical Bit Map

Bit Name	Register	Page	Default	Type	Category
ACCEN	0x13[4]	68	0	W	DAA Control Function
ACZ1/0	0x17[4:3]	67	00	W	DAA Control Function
APWS	0x17[7]	67	0	W	DAA Control Function
ATEN	0x16[4]	66	0	W	DAA Control Function
CHNGFS	0x0D[3]	45	0	W	PLL System Timing Control
CIDM	0x15[4]	72	0	W	DAA Control Function
CMRXG1/0	0x10[1:0]	40	00	W	Call Progress Monitor
CMTXG1/0	0x10[3:2]	40	00	W	Call Progress Monitor
CMVSEL	0x10[4]	40	0	W	Call Progress Monitor
DAA1/0	0x14[6:5]	55	00	WO	Signal Control Function
DCIV1/0	0x13[7:6]	66	00	WO	DAA Control Function
DET	0x03[2]	73	0	R	Line Sensing Control
DIR4	0x04[4]	39	1	W	GPIO Control
DIR5	0x04[5]	39	1	W	GPIO Control
DIR6	0x04[6]	39	1	W	GPIO Control
DIR7	0x04[7]	39	1	W	GPIO Control
DISNTR	0x15[6]	59	0	WO	Barrier Control Function
DTST0	0x07[0]	76	0	W	Loopback Control
DTST1	0x07[1]	76	0	W	Loopback Control
DTST2	0x07[2]	76	0	W	Loopback Control
DTST3	0x07[3]	76	0	W	Loopback Control
DSYEN	0x01[7]	51	0/1	W	Slave Control
ENAC	0x12[5]	68	0	WO	Current Limiting Detection Control and Status
ENAPOL	0x05[3]	59	1	W	Barrier Control Function
ENDC	0x12[6]	68	0	WO	Current Limiting Detection Control and Status
ENDET	0x05[2]	73	0	W	Line Sensing Control
ENDT	0x12[1]	73	0	WO	Line Sensing Control
ENFEH	0x0F[7]	38	0	W	Power Control Function
ENFEL	0x12[2]	68	0	WO	Current Limiting Detection Control and Status
ENGPIO7	0x05[7]	39	0	W	GPIO Control
ENGPIO6	0x05[6]	39	0	W	GPIO Control
ENGPIO5	0x05[5]	39	0	W	GPIO Control
ENGPIO4	0x05[4]	39	0	W	GPIO Control
$\overline{\text{ENLPW}}$	0x02[2]	59	0	W	Barrier Control Function
$\overline{\text{ENLVD}}$	0x12[3]	68	0	WO	DAA Control Function
ENNOM	0x12[0]	65	0	WO	DAA Control Function
ENOID	0x15[0]	74	0	WO	Over-Current Detection Control and Status
ENOVD	0x15[1]	74	0	WO	Over-Voltage Detection Control and Status
ENRGDT	0x05[0]	72	1	W	Ring Detection Status Function
ENSHL	0x12[4]	68	0	WO	DAA Control Function
ENSYNL	0x05[1]	59	1	W	Barrier Control Function
ENUVD	0x15[2]	73	0	WO	Under-Voltage Detection Control and Status
FRCVCO	0x0E[7]	38	0	W	Device Clock Management
FSCTR	0x16[3:0]	67	0001	W	DAA Control Function
GPIO4	0x03[4]	39	1	W	GPIO Control
GPIO5	0x03[5]	39	1	W	GPIO Control
GPIO6	0x03[6]	39	1	W	GPIO Control
GPIO7	0x03[7]	39	1	W	GPIO Control
HC	0x02[0]	51	0	W	MAFE Configuration
ICHP	0x0A[7:4]	45	1100	W	PLL System Timing Control
IDL2	0x19[4]	38	0	W	Power Control Function

Bit Name	Register	Page	Default	Type	Category
IDISPD0	0x13[0]	65	0	WO	DAA Control Function
IDISPD1	0x13[1]	65	0	WO	DAA Control Function
ILM	0x13[5]	66	0	WO	DAA Control Function
ILMON	0x1E[7]	66	0	R	DAA Control Function
INDX	0x19[3:0]	36	0	W	Line-Side Device Register Polling
KVCOH	0x0A[2:0]	45	001	W	PLL System Timing Control
LC	0x1C[7:1]	73	0	R	Auxiliary A/D Converter Status
LOKDET	0x0D[7]	45	0	R	PLL System Timing Control
LV	0x1B[7:1]	73	0	R	Auxiliary A/D Converter Status
MATCH	0x19[6]	36	0	R	Line-Side Device Register Polling
MSID	0x01[2]	51	0/1	W	Slave Control
MSIDEN	0x01[3]	51	0/1	W	Slave Control
NDVSR	0x0B[6:0]	45	101010	W	PLL System Timing Control
NRST	0x0D[2:0]	45	000	W	PLL System Timing Control
NSEQ	0x0C[7:0]	45	0000110	W	PLL System Timing Control
NSLAVE	0x01[6:4]	51	0/1	W	Slave Control
OFH	0x12[7]	65	0	WO	DAA Control Function
OIDET	0x1E[4]	74	0	R	Over-Current Detection Control and Status
OVDET	0x1E[5]	74	0	R	Over-Voltage Detection Control and Status
OVDTH	0x13[2]	74	0	WO	Over-Voltage Detection Control and Status
PDVSR	0x09[4:0]	45	01111	W	PLL System Timing Control
PLDM	0x13[3]	65	0	WO	DAA Control Function
POL7	0x06[7]	39	0	W	GPIO Control
POL6	0x06[6]	39	0	W	GPIO Control
POL5	0x06[5]	39	0	W	GPIO Control
POL4	0x06[4]	39	0	W	GPIO Control
POLL	0x19[7]	36	0	W	Line-Side Device Register Polling
POLVAL	0x1F[7:0]	36	0	R	Line-Side Device Register Polling
PRST	0x09[7:5]	45	111	W	PLL System Timing Control
PSEQ	0x08[7:0]	45	11011010	W	PLL System Timing Control
PWDN	0x0F[6]	38	0	W	Power Control Function
PWDNPLL	0x0E[6]	38	0	R	Device Clock Management
REVHSD	0x04[3:0]	37	0111	R	Device Revision
REVLSD	0x1D[7:4]	37	1001	R	Device Revision
RGDT	0x03[0]	72	0	R	Ring Detection Status Function
RGMON	0x03[3]	72	0	R	Ring Detection Status Function
RGTH1/0	0x0E[1:0]	72	0	W	Ring Detection Status Function
RLPNEN	0x16[5]	67	0	W	DAA Control Function
RLPNH	0x14[2]	67	0	W	DAA Control Function
RNG	0x1A[7:0]	73	0	R	Auxiliary A/D Converter Status
RXBST	0x14[3]	55	0	WO	Signal Control Function
RXEN	0x16[6]	55	0	WO	Signal Control Function
RXG0	0x14[0]	55	0	WO	Signal Control Function
RXG1	0x14[1]	55	0	WO	Signal Control Function
SCK32	0x01[1]	51	0	W	Slave Control
SLEEP	0x0F[5]	38	1	W	Power Control Function
SLHS	0x0D[6]	59	1	R	Barrier Control Function
SLLS	0x1E[3]	59	0	W	Barrier Control Function
SPOS	0x02[1]	51	0	W	MAFE Configuration
SYNL	0x03[1]	59	0	R	Barrier Control Function
THEN	0x15[3]	67	0	W	DAA Control Function
TMEN	0x02[7]	76	0	W	Loopback Controls
TEST	0x18[7:4]	76	0	W	Loopback Controls
TXBST	0x14[7]	55	0	WO	Signal Control Function
TXEN	0x16[7]	55	0	WO	Signal Control Function
UVDET	0x1E[6]	73	0	R	DAA Control Function
XIB	0x0F[3:2]	38	11	W	Device Clock Management

5.1 Line-Side Device Register Polling

The Register Map as read from a 73M1x22 Host-Side Device consists of two groups. The first is the Host-Side Device registers (0x00 through 0x11) and the second is a copy of the Line-Side Device registers (0x12 through 0x1F).

As an extra degree of integrity the 73M1x22 supports the ability to manually monitor the registers of its Line-Side Device. This is achieved by using the Manual Poll Function. The Line-Side registers that can be polled are 0x12 through 0x18.

The method is to write the offset address of the Line-Side Device register to be read into the INDX field. The value of this is the offset from 0x12; that is, Register 0x12 is 0x0, 0x13 is 0x1, etc. The next step is to set the POLL bit, which causes the device to read the requested register from the Line-Side Device. The value of the requested Line-Side Device register is written into POLVAL (0x1F). This value is compared with that of the Host-Side copy and if they are the same then the MATCH bit is set.

The values presented at MATCH and POLVAL are valid approximately 600 µs (depending upon the clock) after a poll request, and are valid only after the POLL bit has been reset by the Host-Side Device.

Function Mnemonic	Register Location	Type	Description
INDX	0x19[3:0]	W	Index Address of the register to be manually polled with the results placed in POLVAL. This address should be cleared after the poll. Default = 0.
MATCH	0x19[6]	R	Polling Match 0 = No match. (Default) 1 = This read-only bit indicates that there is match with the corresponding polled register in the Host-Side Device. The result of the polling function can be read only after the POLL bit is reset to zero by the 73M1x22.
POLL	0x19[7]	W	Polling Enable 0 = Polling disabled. (Default) 1 = Manually polls the control register in the Line-Side Device whose address is given by INDX. The POLL bit remains high until the MATCH result is available at which time it will be reset to 0 and the MATCH bit status can be read.
POLVAL	0x1F[7:0]	R	Polling Value When 73M1x22 is polled, the content of the Line-Side Device Register given by the offset address in INDX is placed in this register. Default = 0. This register can be read after the POLL bit has been reset to zero, indicating the result is ready.

6 Hardware Control Functions

This section describes the 73M1x22 capabilities with respect to its configuration and hardware pin control. This includes features such as Interrupt Control, Power Management, Clock Control, General Purpose Input/Output (GPIO) and control of the Call Progress Monitor.

6.1 Device Revision

The 73M1922 provides the device revision number for the Host-Side Device and the Line-Side Device.

For the 73M1822B07 and 73M1922A01 (73M1902B04) Host-Side Device, the current revision is 0111.

For the 73M1822B07 and 73M1922A01 (73M1912B07) Line-Side Device, the current revision is 1001.

Function Mnemonic	Register Location	Type	Description
REVHSDn	0x04[3:0]	R	Revision Host-Side Device These read only status bits indicate the revision of the 73M1x22 Host-Side Device.
REVLSDn	0x1D[7:4]	R	Revision Line-Side Device These read-only status bits provide the Device ID for the 73M1x22 Line-Side Device. Before the barrier synchronization, the value is 0000. After the barrier synchronization, the value represents the Device ID of the Line-Side Device (73M1912).

6.2 Interrupt Control

The 73M1x22 supports a single interrupt that can be asserted under several configurable conditions. These include status of GPIOs, RGMON, DET, SYNL and RGDT.

All interrupt sources that are enabled are OR'ed together to create the INT output signal. GPIO ports that are configured to be output will not generate interrupts.

When the INT pin goes active (low), the host should read the interrupt source Register 0x03, which is then cleared after the read operation. An interrupt during wake-on-ring should be interpreted as the detection of a valid ring signal.

Address 0x03

Reset State E0h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO7	GPIO6	GPIO5	GPIO4	RGMON	DET	SYNL	RGDT

6.3 Power Management

The 73M1x22 supports three modes of power control for the device.

Normal mode	The 73M1x22 operates normally.
Sleep mode	The device PLL is turned off and the internal clock is driven by Xtal. SCK=1/8 Xtal. Control and status registers maintain their content.
Power Down	The device is shut down altogether. In this mode the MAFE is disabled together with the Xtal oscillator. To restart the normal operations, RESET or power on reset is required.

Function Mnemonic	Register Location	Type	Description
SLEEP	0x0F[5]	W	Sleep Mode 0 = Disable Sleep Mode. 1 = Enable Sleep Mode. (Default)
PWDN	0x0F[6]	W	Power Down Mode 0 = Disable Power Down Mode. (Default) 1 = Enable Power Down Mode.
IDL2	0x19[4]	W	Ring Detect Functions 0 = Disable ring detect monitoring A/D function. (Default) 1 = Enable ring detect monitoring A/D function.
ENFEH	0x0F[7]	W	Enable Front End Host 1 = Enable Front End of the 73M1902 Host-Side Device. 0 = Disable Front End of the 73M1902 Host-Side Device. (Default)

6.4 Device Clock Management

Function Mnemonic	Register Location	Type	Description
FRCVCO	0x0E[7]	W	Force VCO 0 = The system clock is driven from the Xtal oscillator. (Default) 1 = The system clock is derived from locked PLL. This is set to 0 upon reset, Sleep or Power Down mode enabled.
PWDNPLL	0x0E[6]	R	PLL Powered Down 0 = PLL is not powered down. (Default) 1 = PLL is powered down.
XIB	0x0F[3:2]	W	Crystal Oscillator Bias Current Control 00 = Crystal oscillator bias current at 120 µA 01 = Crystal oscillator bias current at 180 µA 10 = Crystal oscillator bias current at 270 µA 11 = Crystal oscillator bias current at 450 µA (Default) If OSCIN is used as a clock input, XIB = 00 setting should be used to save power (=167 µA at 27.648 MHz).

6.5 GPIO Registers

The 73M1922 32-pin QFN package provides four I/O pins (GPIO7, GPIO6, GPIO5 and GPIO4). The 73M1822 (42-pin QFN package) provides one user GPIO pin (GPIO6).

✓ GPIO pins are not available on the 20-pin package version of the 73M1922.

Each pin can be configured independently as either an input or an output.

At power on and after a reset, the GPIO pins are initialized to a high impedance state to avoid unwanted current contention and consumption. The input structures are protected from floating inputs, and no output levels are driven by any of the GPIO pins.

The GPIO pins are configured as inputs or outputs by writing to the I/O Direction register (DIR).

The mapping of GPIO pins is designed to correspond to the bit location in their control and status registers.

The 73M1922 supports the ability to generate an interrupt on the INT pin. The source can be configured to generate on a rising or a trailing edge. Only GPIO ports that are configured as inputs can be used to generate interrupts.

Function Mnemonic	Register Location	Type	Description
DIR	0x04[7:4]	W	I/O Direction These control bits are used to designate the GPIO[7:4] pins as either inputs or outputs. 0 = GPIO pin is programmed to be an output. 1 = GPIO pin is programmed to be an input. (Default)
GPIOn	0x03[7:4]	W	GPIO Status These bits reflect the status of the GPIO7, GPIO6, GPIO5 and GPIO4 pins. If DIR bit is reset, reading this field will return the logical value of the appropriate GPIOn pin as an input. If DIR bit is set the pins will output the logical value as written.
ENGPIOn	0x05[7:4]	W	GPIO Interrupt Enable Each of the GPIO enable bits in this register enables the corresponding GPIO bit as an edge-triggered interrupt source. If a GPIO bit is set to one, an edge (which edge depends on the value in the GIP register) of the corresponding GPIO pin will cause the INT pin to go active low, and the edge detectors will be rearmed when the GPIO data register is read.
POLn	0x06[7:4]	W	GPIO Interrupt Edge Selection Define the interrupt source as being either on a rising or a falling edge of the corresponding GPIO pin. 0 = A rising edge will trigger an interrupt from the corresponding pin. (Default) 1 = A falling edge will trigger an interrupt from the corresponding pin.

6.6 Call Progress Monitor

For the purpose of monitoring activities on the line, a Call Progress Monitor is provided in the 73M1x22. This audio output contains both transmit and receive data with configurable levels.

Function Mnemonic	Register Location	Type	Description
CMVSEL	0x10[4]	W	Call Progress Monitor Voltage Reference Select Quiescent DC voltage select at AOUT. 0 = 1.5 Vdc. (Default) 1 = VCC/2 Vdc.
CMTXG	0x10[3:2]	W	Transmit Path Gain Setting 00 — 0 dB (for TBS full swing, AOUT =1.08 Vpk) (Default) 01 — -6 dB 10 — -12 dB 11 — MUTE
CMRXG	0x10[1:0]	W	Receive Path Gain Setting 00 — 0 dB (for RBS full swing, AOUT =1.08 Vpk) (Default) 01 — -6 dB 10 — -12 dB 11 — MUTE

7 Clock and Sample Rate Management

The Host-Side Device has an on-chip crystal oscillator, prescaler and PLL/NCO to allow a choice of a wide range of sample rates and crystal choices. Note the following acronyms are used in this section:

F_S Sampling frequency
NCO Numerically-Controlled Oscillator

7.1 Clock Generation with HIC (73M1902)

The clock generation for the entire chip consists of crystal oscillator, Prescaler NCO, NCO based PLL and a clock divider as shown in Figure 13.

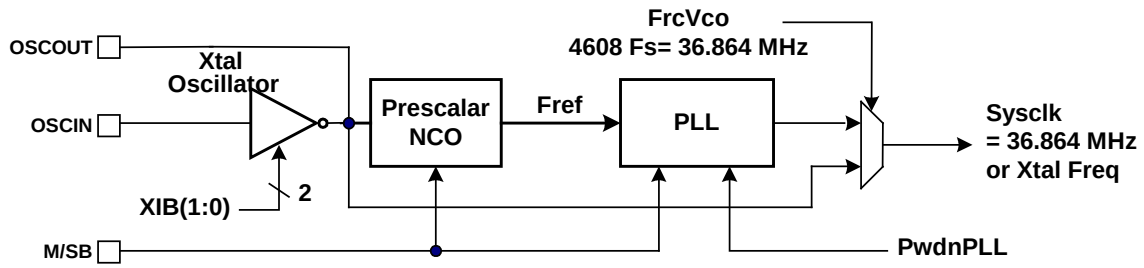


Figure 13: Clock Generation Block Diagram (assumes 8 kHz sample rate)

7.2 Crystal Oscillator

The crystal oscillator is designed to operate with a wide choice of crystals (from 9 MHz to 27 MHz). It is a common source configuration with current source loading to reduce power consumption. The current source levels are configurable in 4 steps by using the XIB bits (Register 0x0F[3:2]) for optimum power performance. On reset the oscillator runs at its full current level. The Host can then step down the current level by setting the XIB bits to an appropriate value that is adequate to achieve stable oscillation with minimal EMI generation.

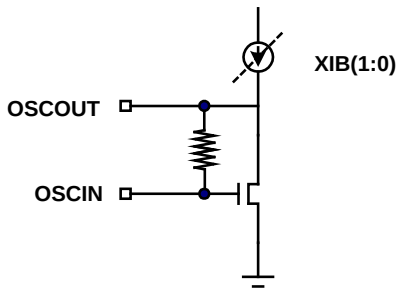


Figure 14: Crystal Oscillator with Configurable Load Current

Table 5: Crystal Oscillator Load Current versus XIB

XIB	Load Current
00	120 µA
01	180 µA
10	270 µA
11	450 µA

7.3 PLL Prescaler

The prescaler converts the crystal oscillator frequency, Fxtal, to a convenient frequency to be used as a reference frequency, Fref, for the PLL. A set of three numbers must be entered through the serial port – PDVSR (5 bit), PRST (3 bit) and PSEQ (8 bit) as follows:

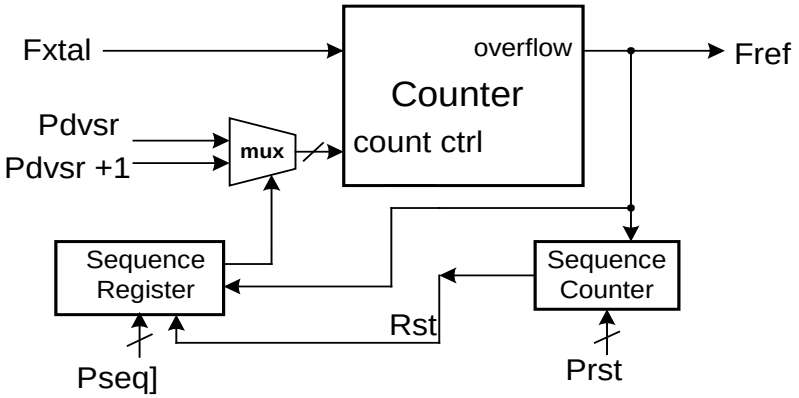


Figure 15: Prescaler Block Diagram

PDVSR = Integer [Fref/Fxtal];
PRST = Denominator of the ratio (Fref/Fxtal) minus 1 when it is expressed as a ratio of two smallest integers = Nnco1/Dnco1;
PSEQ = Divide Sequence

The prescaler should be designed such that the output frequency, Fref, is in the range of 2 ~ 4 MHz.

7.4 PLL Circuit

Figure 16 illustrates a block diagram of the on-chip PLL circuit.

The architecture of the 73M1x22 requires that the PLL output frequency, Fvco, be related to the sampling rate, Fs, by Fvco = 2 x 2304 x Fs. The NCO must function as a divider whose divide ratio equals Fref/Fvco. Just as in the NCO prescaler, a set of three numbers must be entered through a serial port to affect this divide – NDVSR (7 bits), NRST (3 bits) and NSEQ (8 bits) as follows:

NDVSR = Integer [Fref/Fxtal];
NRST = Denominator of the ratio (Fvco/Fref), Dnco1, minus 1, when it is expressed as a ratio of two smallest integers = Nnco1/Dnco1;
NSEQ = Divide Sequence

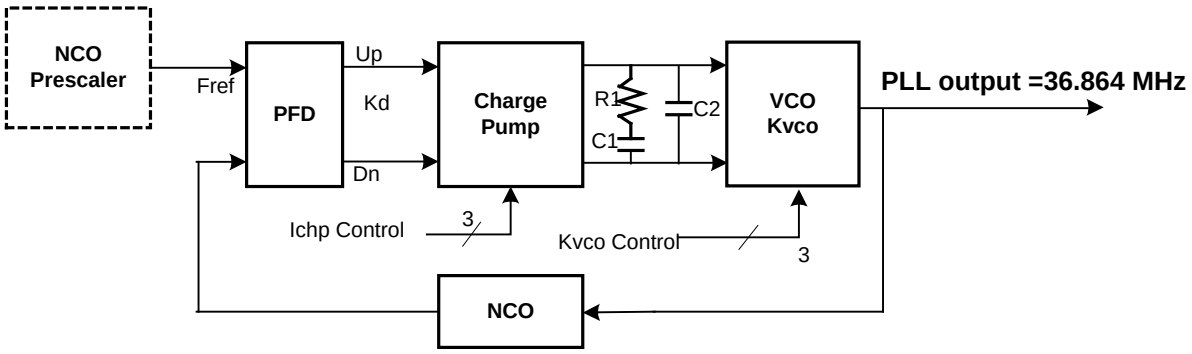


Figure 16: PLL Block Diagram

Upon the system reset, the system clock is equal to Fxtal/9. The system clock will remain at Fxtal until the host forces the transition no sooner the second Frame Synch period after the write to Register0D. When

this happens, the system clock will transition to PLLclk without any glitches through a specially designed de-glitch mux.

The following tables show the register values for several common clock or crystal frequencies and sample rates. By using these tables, computing the values for the registers is not necessary in most cases.

Table 32: Clock Generation Register Settings for Fxtal = 27 MHz

Bit, Reg Address / Fs (kHz)	PSEQ 0x08	PRST, PDVSR 0x09	ICHP, KVCO_H 0x0A	NDVSR 0x0B	NSEQ 0x0C	NRST 0x0D	Ichp (µA)	KVCO (2:0)
7.2	0xDA	0xEF	0x20	0x13	0x10	0x04	8	0
8.0	0xDA	0xEF	0x31	0x15	0x04	0x02	10	1
9.6	0xDA	0xEF	0x32	0x19	0x1A	0x04	10	2
12.0	0xDA	0xEF	0x24	0x20	XX	0x00	8	4
14.4	0xDA	0xEF	0x46	0x26	0x14	0x04	12	6
16.0	0xA4	0xE9	0x17	0x19	0x1A	0x04	6	7

Table 33: Clock Generation Register Settings for Fxtal = 24.576 MHz

Bit, Reg Address / Fs (kHz)	PSEQ 0x08	PRST, PDVSR 0x09	ICHP, KVCO_H 0x0A	NDVSR 0x0B	NSEQ 0x0C	NRST 0x0D	Ichp (µA)	KVCO (2:0)
7.2	XX	0x0A	0x10	0x0D	0x02	0x01	6	0
8.0	XX	0x0A	0x11	0x0F	XX	0x00	6	1
9.6	XX	0x0A	0x22	0x12	XX	0x00	8	2
12.0	XX	0x0A	0x14	0x16	0x02	0x01	6	4
14.4	XX	0x0A	0x26	0x1B	XX	0x00	8	6
16.0	XX	0x08	0x17	0x18	XX	0x00	6	7

Table 34: Clock Generation Register Settings for Fxtal = 9.216 MHz

Bit, Reg Address / Fs (kHz)	PSEQ 0x08	PRST, PDVSR 0x09	ICHP, KVCO_H 0x0A	NDVSR 0x0B	NSEQ 0x0C	NRST 0x0D	Ichp (µA)	KVCO (2:0)
7.2	XX	0x04	0x20	0x0E	0x14	0x04	8	0
8.0	XX	0x04	0x31	0x10	XX	0x00	10	1
9.6	XX	0x04	0x32	0x13	0x10	0x04	10	2
12.0	XX	0x04	0x24	0x18	XX	0x00	8	4
14.4	XX	0x08	0x66	0x39	0x1A	0x04	16	6
16.0	XX	0x03	0x17	0x18	XX	0xC0	6	7

Table 35: Clock Generation Register Settings for Fxtal = 24.000 MHz

Bit, Reg Address / Fs (kHz)	PSEQ 0x08	PRST, PDVSR 0x09	ICHP, KVCO_H 0x0A	NDVSR 0x0B	NSEQ 0x0C	NRST 0x0D	Ichp (µA)	KVCO (2:0)
7.2	0xDA	0xEF	0x30	0x 5	0x1A	0x04	10	0
8.0	0x02	0x2C	0x31	0x13	0x10	0x04	10	1
9.6	0xDA	0xEF	0x42	0x1C	0x1E	0x04	12	2
12	0x08	0x66	0x14	0x0E	0x14	0x04	6	4
14.4	0x54	0xCA	0x46	0x1C	0x3E	0x05	12	6
16.0	0xA4	0xE9	0x17	0x1C	0x1E	0xC4	6	7

Table 36: Clock Generation Register Settings for Fxtal = 25.35 MHz

Bit, Reg Address / Fs(kHz)	PSEQ 0x08	PRST, PDVSR 0x09	ICHP, KVCO_H 0x0A	NDVSR 0x0B	NSEQ 0x0C	NRST 0x0D	Ichp (µA)	KVCO (2:0)
7.2	0x92	0xF4	0x50	0x1A	0x06	0x02	14	0
16	0x40	0xCA	0x17	0x1D	0x02	0xC1	6	7

7.5 PLL System Timing Control

Table 48 describes the registers used for PLL system timing control.

Table 37: PLL System Timing Controls

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>PSEQ</td><td>0x08[7:0]</td><td>W</td><td>Sequence of the divisor. If PRST=0, this register is ignored.</td></tr>
<tr><td>PRST</td><td>0x09[7:5]</td><td>W</td><td>Rate at which the sequence register is reset.</td></tr>
<tr><td>PDVSR</td><td>0x09[4:0]</td><td>W</td><td>Divisor value. Default is 01111.</td></tr>
<tr><td>ICHP</td><td>0x0A[7:4]</td><td>W</td><td>The sizes of the charge pump current in the PLL.</td></tr>
<tr><td>KVCOH</td><td>0x0A[2:0]</td><td>W</td><td>The magnitude of KVCO associated with the VCO within PLL. The following table shows proper KVCOH values per each desired PLL VOC frequency.
<table>
<tr><th>KVCOH2</th><th>KVCOH1</th><th>KVCOH0</th><th>Fvco</th><th>Kvco</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>33 MHz</td><td>38 MHz/V</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>36 MHz</td><td>38 MHz/V</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>44 MHz</td><td>40 MHz/V</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>48 MHz</td><td>40 MHz/V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>57 MHz</td><td>63 MHz/V</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>61 MHz</td><td>63 MHz/V</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>69 MHz</td><td>69 MHz/V</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>73 MHz</td><td>69 MHz/V</td></tr>
</table></td></tr>
<tr><td>NDVSR</td><td>0x0B[6:0]</td><td>W</td><td>Divisor value. If NRST=0, this register is ignored.</td></tr>
<tr><td>NSEQ</td><td>0x0C[7:0]</td><td>W</td><td>Divisor sequence.</td></tr>
<tr><td>LOKDET</td><td>0x0D[7]</td><td>R</td><td>Phase Locked Loop Lock Detect
0 = PLL is not locked. (Default)
1 = PLL is locked to PCLK.</td></tr>
<tr><td>CHNGFS</td><td>0x0D[3]</td><td>W</td><td>Sample Rate Change Sequence Enable
0 = No Fs change sequence generated. (Default)
1 = Fs change sequence is enabled.

Setting this bit to 1 minimizes the barrier power loss period during the sample rate changes. This bit is recommended to be set to 1 for the applications requiring dynamic sample rate changes such as V.34 and V.90 modems, etc.</td></tr>
<tr><td>NRST</td><td>0x0D[2:0]</td><td>W</td><td>Represents the rate at which the NCO sequence register is reset.</td></tr>
</table>

8 MAFE Serial Interface

The serial data port is a bi-directional port that is supported by most host processors. This is a simple four-wire interface consisting of a clock, frame sync, data in and data out. The typical I^2S (Inter-IC Sound, NXP semiconductor) bus can be easily converted into a MAFE-compatible interface. Although the 73M1x22 is a peripheral to the host processor, the device can be either a master or slave to the host. The M/$\overline{S}$ pin dictates what is in control of the serial port. If the M/$\overline{S}$ pin is a logic 1 (default), the device is the master; if a logic 0, then it is a slave.

The 73M1x22 chip set can be configured to use one of two framing modes. The active low frame synchronization ($\overline{FS}$) signal is pin configurable by the TYPE pin. When the TYPE pin is unconnected or pulled up to logic "1" (mode 1), an early $\overline{FS}$ is generated in the bit clock prior to the first data bit transmitted or received. When this pin is pulled down to ground (mode 0), a late FS operates as a chip select; the $\overline{FS}$ signal is active for all bits that are transmitted or received. The TYPE input is sampled during the device reset and is ignored at all other times. The final state of the TYPE pin as the $\overline{TEST1}$ pin is de-asserted determines the frame synchronization mode used. In master mode, $\overline{FS}$ is an output and generated by the MicroDAA at the frame sync (or sample) rate, Fs. In daisy chain/slave mode, regardless of the type, the master device will only support early mode. The slave device can be of either an early or late type. For every data Fs, 16 bits are transmitted and 16 bits are received.

✓ The standard 73M1822 device supports the late frame sync mode only. If a need for a frame sync early mode is required, contact the Teridian Marketing department for details.

8.1 Data and Control Frame Formats

The serial bit stream of a data frame from the SDOUT pin are defined as follows:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX15	RX14	RX13	RX12	RX11	RX10	RX9	RX8	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0

Figure 17 shows data and control frames with early and late frame synch.

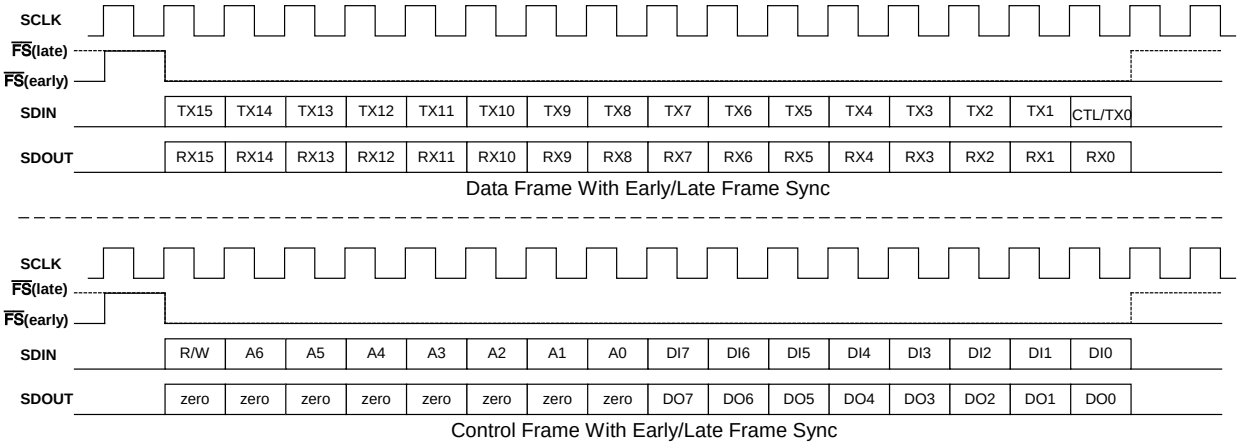


Figure 17: Serial Port Timing Diagram

If the HC bit (Register 0x02[0]) is reset to 0 (default), CTL (Bit 0 of TX data) is used for the host to request a control frame. The 16-bit serial data bit stream received on the SDIN is defined as follows:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	CTL

If the CTL bit in the TX data stream is set high by the host, a control frame will be initiated before the next data frame. A control frame allows the host controller to read or write status and control to the 73M1x22.

If the HC bit (Register 0x02[0]) is set to 1, a control frame is initiated between every pair of data frames. The 16-bit serial data bit stream received on the SDIN is defined as follows:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX15	TX14	TX13	TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0

In both cases, Bit 15 is transmitted/received first in time. Bits RX[15:0] are the receive code word. Bits TX[17:0] are the transmit code word.

The serial bit stream of a control frame on the SDIN pin is defined as:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/$\overline{W}$	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

The serial bit stream of a control frame on the SDOUT pin is defined as:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0

If the R/W (Bit 15 of the control word) bit is set to a 0, the data byte transmitted on the SDOUT pin is all zeros and the data received on the SDIN pin is written to the register pointed to by the received address bits (A6-A0). If the R/W bit is set to a 1, there is no write to any register and the data byte transmitted on the SDOUT pin is the data contained in the register pointed to by address bits A6-A0. Only one control frame can occur between any two data frames.

8.2 Data and Control Frame Timing

Figure 18 illustrates data and control frames timing of 8 kHz sample rate.

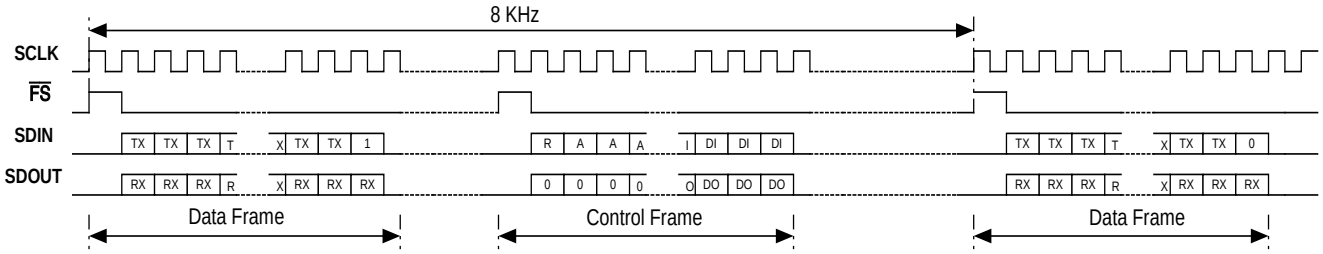


Figure 18: Data and Control Frames Timing Diagram

The position of a control data frame is controlled by the SPOS bit (Register 0x02[1]). If SPOS is zero, the control frames occur midway between data frames, i.e., the time between data frames are equal. If SPOS is set to 1, the control frame is ¼ of the way between consecutive data frames, i.e., the control frame is closer to the first data frame. This is illustrated in Figure 19. The SPOS bit has no effect in Slave or Daisy Chain mode

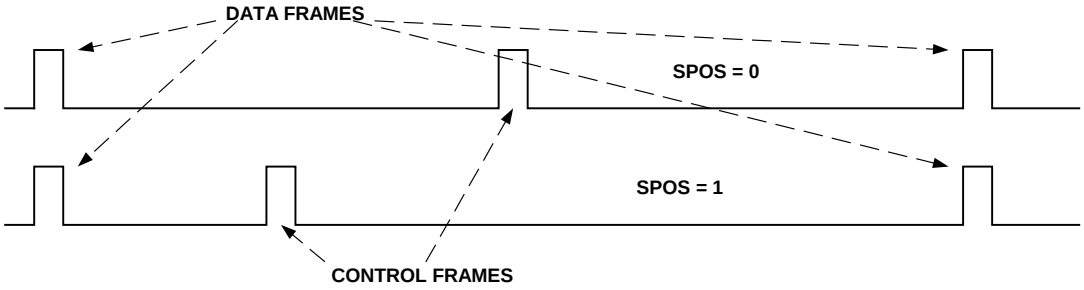


Figure 19: Control Frame Position versus SPOS

The SDOUT and $\overline{FS}$ pins change values following a rising edge of SCLK. The SDIN pin is sampled on the falling edge of SCLK.

8.3 Serial Clock Operation

SCLK is a continuous clock running at 256∗Fs (Fs = Sample rate frequency). On the 32-pin version of 73M1922, the SCKM (Pin 14), which is weakly pulled high internally, can be connected to ground to stop the SCLK after 32 clock cycles. This is illustrated in Figure 20.

✓ The 73M1822 and 73M1922 20-pin TSSOP packages only support the continuous SCLK configuration.

Table 38: Behavior of SCLK under SCKM

SCKM Pin	Number of SCLK Cycles before Being Shut Off
High	Continuous
Low	32

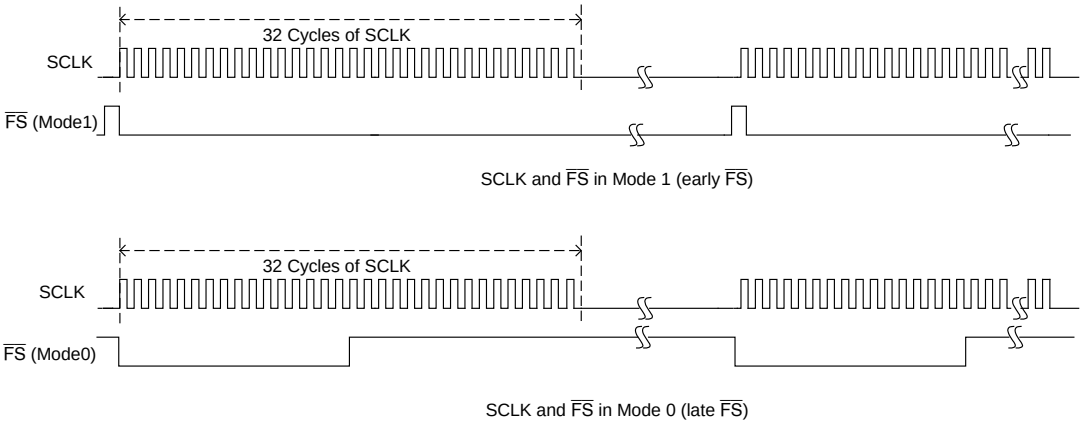


Figure 20: SCLK and $\overline{FS}$ with SCKM = 0

8.4 MicroDAA IN Master/Slave Configuration

The 73M1x22 can be configured as a Slave by resetting the M/$\overline{S}$ pin to 0. In this mode, $\overline{FS}$ of the slave device(s) becomes an input from $\overline{FSD}$ output of the Master or previous slave device. $\overline{FSD}$ is $\overline{FS}$ delayed by 16 SCLK cycles. This delay can be adjusted between 16 and 32 by setting the SCK32 bit (Register 0x01[1] bit for the number of total devices less than or equal to 4. For more slaves, the SCK32 bit should be reset. This is illustrated in Figure 21 and Figure 22. $\overline{FSD}$ is always of Late Type (or "Framed").

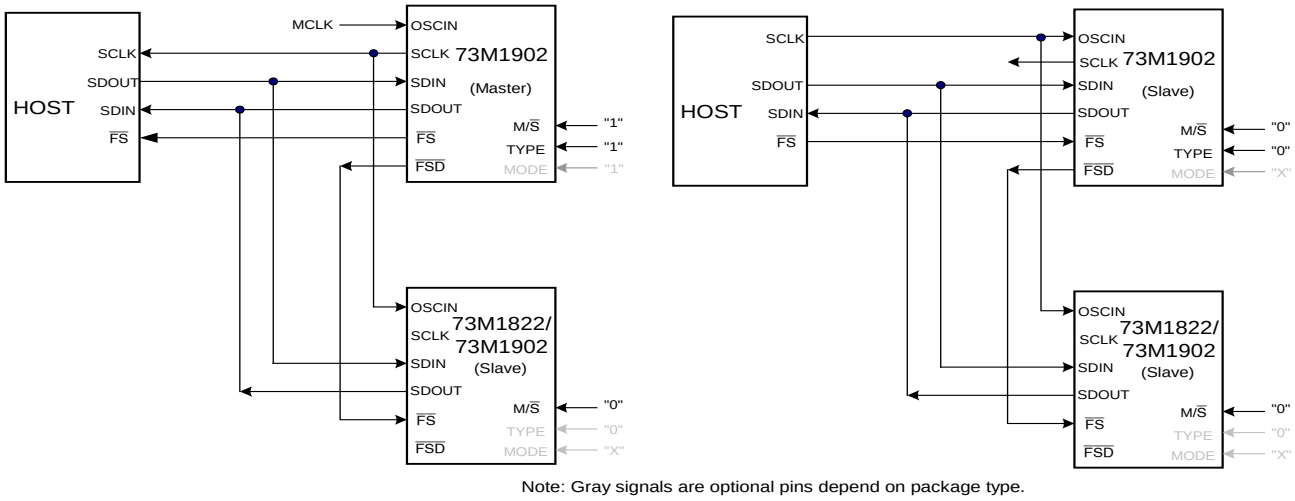


Figure 21: Example Connections for Master and Slave Operation

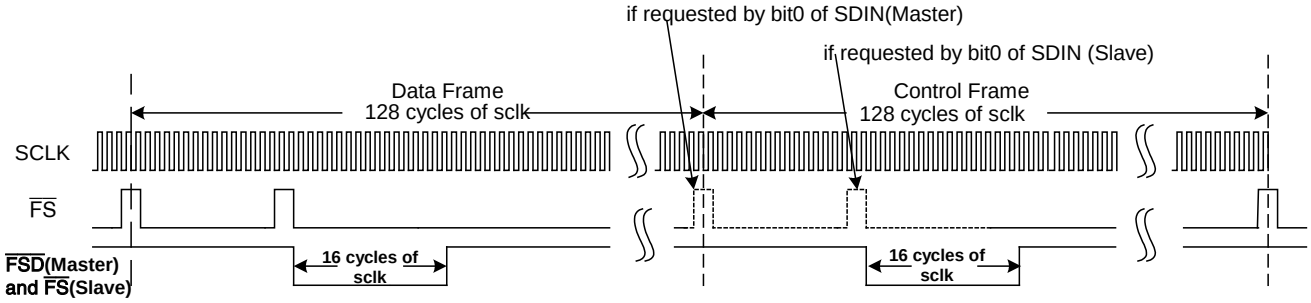


Figure 22: Master/Slave Serial Timing Diagram

8.5 73M1x22 Reset

The 73M1x22 can be initialized to a default state by pulling the $\overline{RST}$ pin low for 100 ns or longer. The device will be ready within 100 µs after the removal of reset pulse. The M/$\overline{S}$ pin is used to provide reset in the 73M1822 and 72M1902 20-pin TSSOP packaged parts. The reset signal is also bi-directional and edge triggered, so either a low-to-high or high-to-low transition will generate a reset. Ensure the final state of M/$\overline{S}$ is the master or slave mode that is desired. M/$\overline{S}$ is used as follows:

Slave Mode

Transition the M/$\overline{S}$ pin high to low after the power supply has reached the minimum VDD level. If active reset signal is used on power up, only a high-to-low transition is needed; if a reset is needed after power up, a low-to-high-to-low toggle of M/$\overline{S}$ is used. The serial port should be ignored during this time.

Master Mode

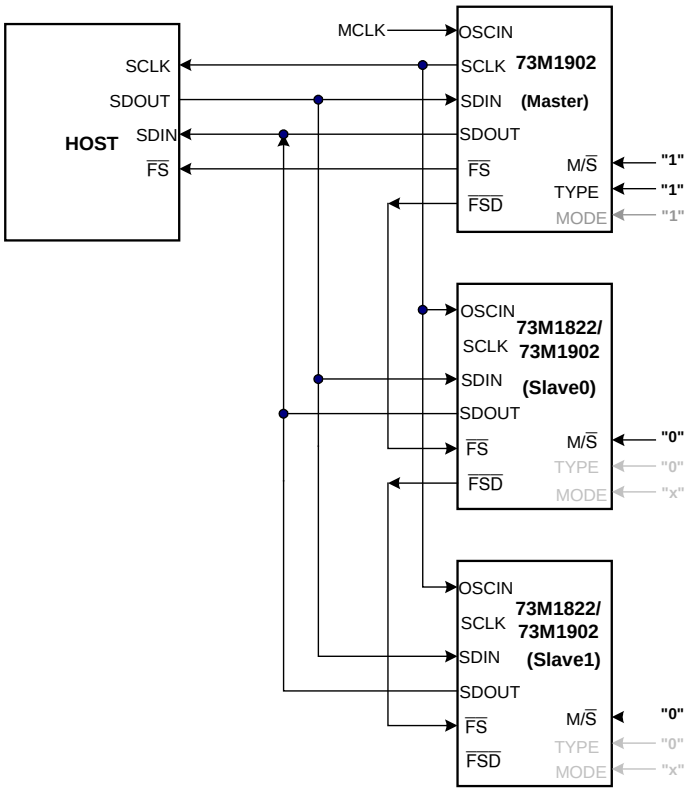
Transition the M/$\overline{S}$ pin low to high. The transition from low to high should be after the minimum VDD level is reached. If an active reset signal is used on power up only a low-to-high transition is needed; if a reset is needed after power up, a high-to-low-to-high toggle of M/$\overline{S}$ is required. The serial port should be ignored during this time.

8.6 73M1x22 in Daisy Chain Configuration

An internal register controls the daisy chain mode. $\overline{FS}$ pin of a slave device is an input from the FSD pin of the preceding device. In this arrangement, the HC bit (Register 0x02[0]) is ignored and the Software control is automatically enabled. Setting CTL (bit 0 of the SDIN data stream) to 1 does the control frame request. The delayed $\overline{FS}$, $\overline{FSD}$, is fed to the subsequent slave device as $\overline{FS}$. $\overline{FSD}$ is delayed from FS and always 16 SCLK periods wide. There are 256 SCLK pulses between frame syncs. A maximum of 7 slaves can be supported.

To aid the host in identifying the master data frame, the least significant bit of the 16-bit word (from SDOUT) from the master can be forced to "1" and the least significant bit of the 16-bit word from the slave(s) to "0" by controlling the MSID bits (Register 0x01[2]) of each device. In the cascade mode, the number of slaves supported must be specified in the NSLAVE bits (Register 0x01[6:4]).

It is important to note that slave devices OSCIN comes from the SCLK pin of the Master device. If a device is configured as a Slave (M/$\overline{S}$=0), the internal PLL is automatically programmed for the correct operation regardless of the external PLL programming. Figure 23 and Figure 24 illustrate the daisy chain configuration.



Gray pins are optional depending on the package type.

Figure 23: Daisy Chaining a Master and Two Slaves

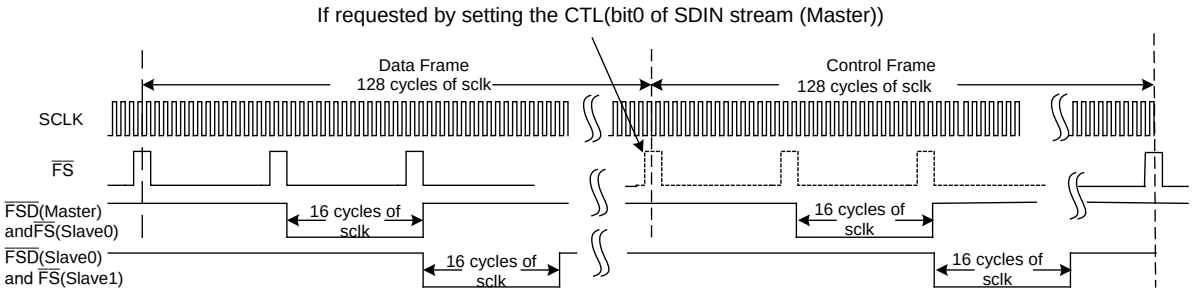


Figure 24: Timing Diagram with One Master and Two Slaves

8.7 MAFE Configuration Registers

The 73M1x22 allows MAFE control frame generation via software control or automatically by the hardware. Using the software-controlled control frame, host resources can be saved by removing the redundant control frame generated by the hardware control.

Function Mnemonic	Register Location	Type	Description
SPOS	0x02[1]	W	SPOS 0 = Control frames occur half way between data frames. (Default) 1 = Control frames occur after one quarter of the time between data frames has elapsed.
HC	0x02[0]	W	Hardware Controlled Control Frame Enable 0 = Control frame is under host software control, the lsb of SDIN data stream becomes a control frame request bit and control frames happen only on request. The actual value of bit 0 of SDIN data stream is forced to 0. (Default) 1 = Control frame generation is under hardware control, bit 0 of SDIN data stream becomes bit 0 of the transmit word and control frames occur automatically after every data frame.

8.8 Slave Registers

The 73M1x22 allows a daisy chain of up to seven slave devices on the same bus. In this configuration, only one device on the bus can be a master and the rest are slaves.

Function Mnemonic	Register Location	Type	Description
DSYEN	0x01[7]	W	Daisy Chain Configuration Enable 0 = Disable Daisy Chain. 1 = Enable Daisy Chain.
NSLAVE	0x01[6:4]	W	Number of Slaves in Daisy Chain Mode Specifies the number of slaves supported. The maximum number is 7. There are two default values. The default in Master Mode is 000. The default in Slave Mode is 001.
MSIDEN	0x01[3]	W	Master/Slave Identification Enable When enabled in a daisy chain configuration, the MSID control bit forces the least significant bit of the SDOUT data stream. 0 = MSID feature disabled. 1 = MSID feature enabled. (Default)
MSID	0x01[2]	W	Master/Slave Identification When MSIDEN = 1, in a daisy chain configuration (DSYEN = 1), this bit allows selecting the value of bit 0 of the SDOUT data stream. 0 = The least significant bit of SDOUT is forced to 0. 1 = The least significant bit of SDOUT is forced to 1. (Default) If DSYEN = 0, MSID has no impact on the least significant bit of the SDOUT data stream. (Default)
SCK32	0x01[1]	W	Daisy Chain $\overline{FSD}$ Latency Control 0 = $\overline{FS}$ to $\overline{FSD}$ delay is 32 SCLK periods. (Default) 1 = $\overline{FS}$ to $\overline{FSD}$ delay is 16 SCLK periods. This bit must be set when there are four or more slave devices. When a master is driving a slave, only Early Type is allowed.

9 Signal Processing

9.1 Transmit Path Signal Processing

9.1.1 General Description

In the transmit path, data is first sent by the host DSP through a serial interface to the 73M1822 / 73M1922 then interpolated by a transmit interpolation filter, serialized and transmitted across to the Line-Side Device, which is floating relative to the Host-Side Device earth ground. The data received on the Line-Side Device is then de-serialized and digitally sigma-delta modulated to a one-bit data stream of 1.536 Mbps (for a sample frequency of 8 kHz). The signal is further filtered first by a switched capacitor filter and then a continuous anti-aliasing circuit.

The frequency response and bandwidth of the transmit path is dependent on the sampling frequency (Fs). Figure 22 and Figure 23 show the normalized frequency response of the transmit path. For Fs = 8 kHz, the 0.2 dB pass-band ripple frequency is from DC to 3.422 kHz. The 3 dB bandwidth is 3.65 kHz.

9.1.2 Total Transmit Path Response

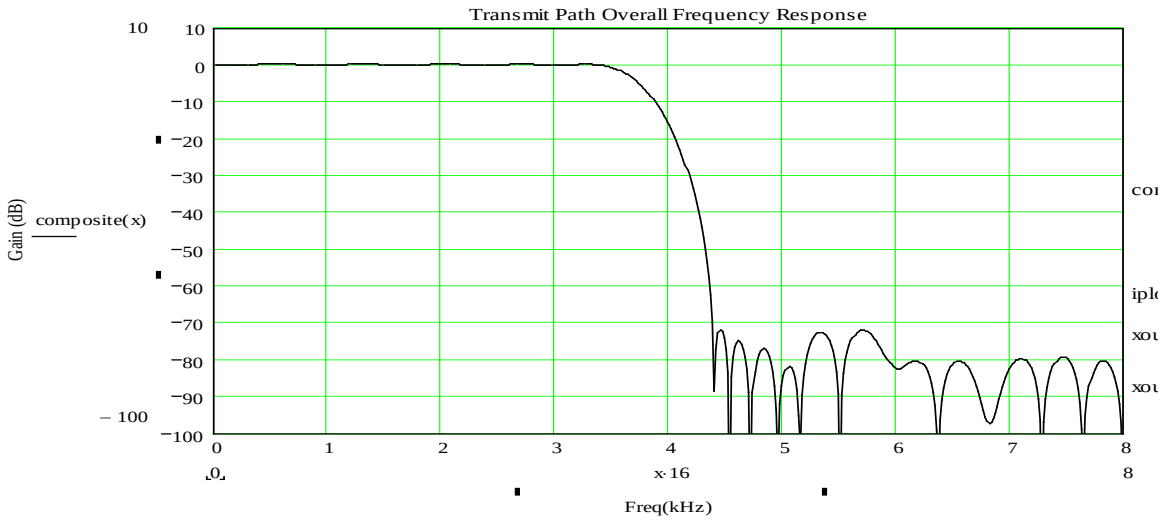


Figure 25: Transmit Path Overall Frequency Response to Fs (8 kHz)

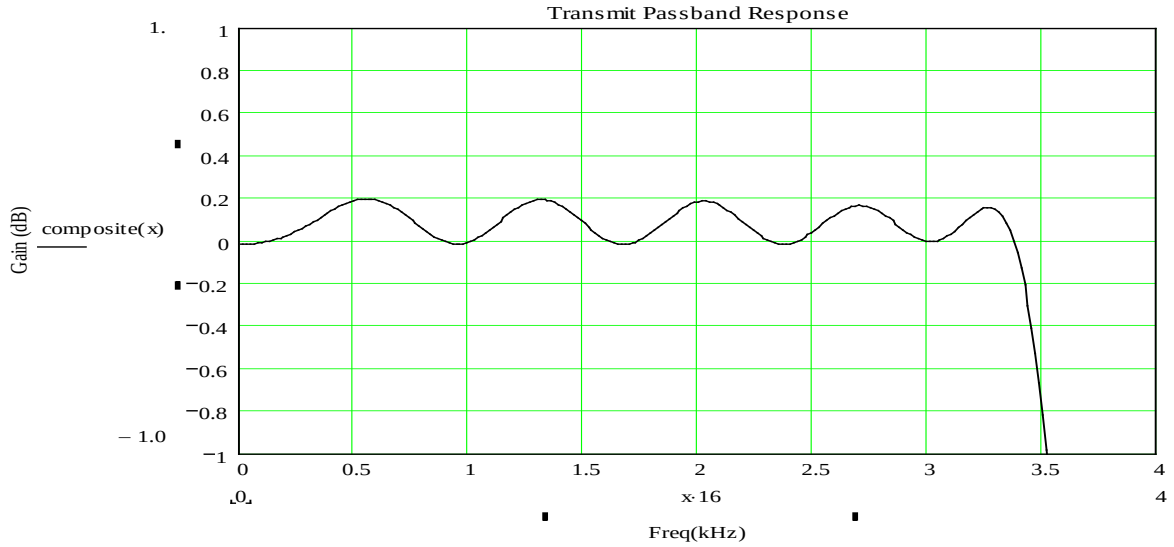


Figure 26: Pass-Band Response of the Transmit Path

9.1.3 73M1x22 Transmit Spectrum

Figure 27 shows the transmit spectrum observed on the line from dc to 32 kHz for a sample frequency (Fs) of 8 kHz. The transmit signal is band-limited (by default) to Fs/2=4 kHz and is flat (with 0.2 dB ripple) to 3.65 kHz and is marked as Txdb(x) in the figure.

Also shown, and marked as signaldb(x), is the baseband signal from 1 kHz to 2 kHz. The aliases of signaldb(x) are shown as aliasdb(x) and are attenuated significantly with better than 80 dB attenuation at 8 kHz, better than 60 dB at 16 kHz, better than 100 dB at 24 kHz, etc.

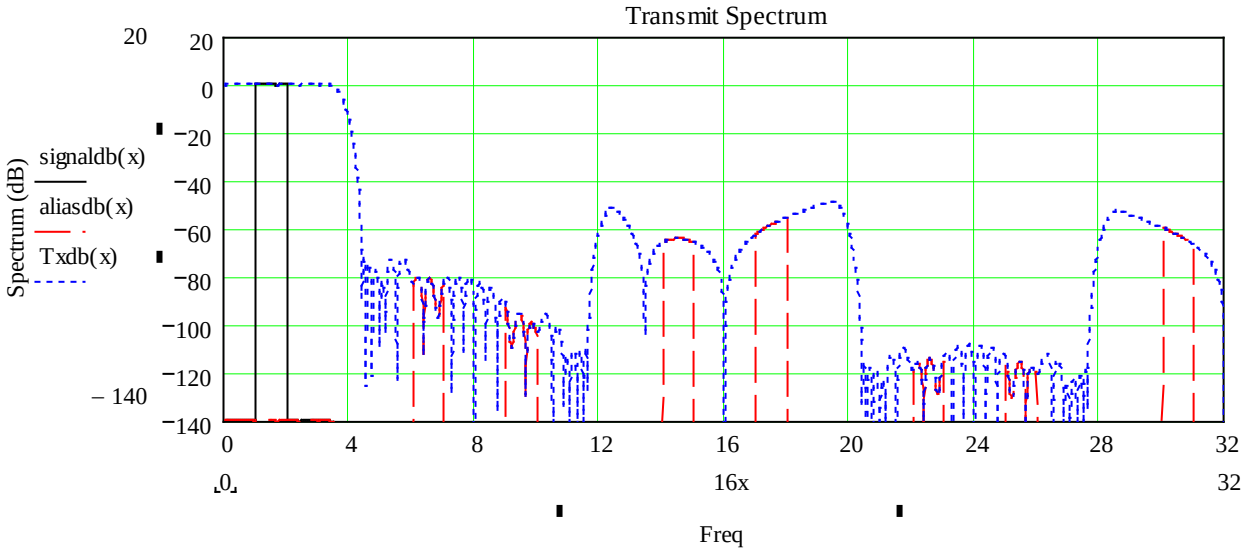


Figure 27: Transmit Spectrum to 32 kHz

9.2 Receive Path Signal Processing

9.2.1 General Description

In the receive path, the signal from the telephone line is input to the anti-aliasing filter and passed through a selectable low pass (notch) filter, which can be used to attenuate in-band Billing Tones. The analog signal is digitized by a sigma-delta analog to digital converter. The resulting high frequency one-bit data stream is decimated and sent to the Host-Side Device via the barrier. Another decimation FIR filter in the Host-Side Device filters the received data and sends it to the host DSP for processing.

The frequency response and bandwidth of the receive path is dependent on the sampling frequency (Fs). Figure 28 and Figure 29 show the normalized frequency response of the receive path, including the effect of the decimation filter in the 73M1902/73M1822 HIC.

For Fs=8 kHz, the 0.2 dB pass-band ripple frequency is from DC to 3.342 kHz. The 3 dB bandwidth is 3.56 kHz.

9.2.2 Total Receive Path Response

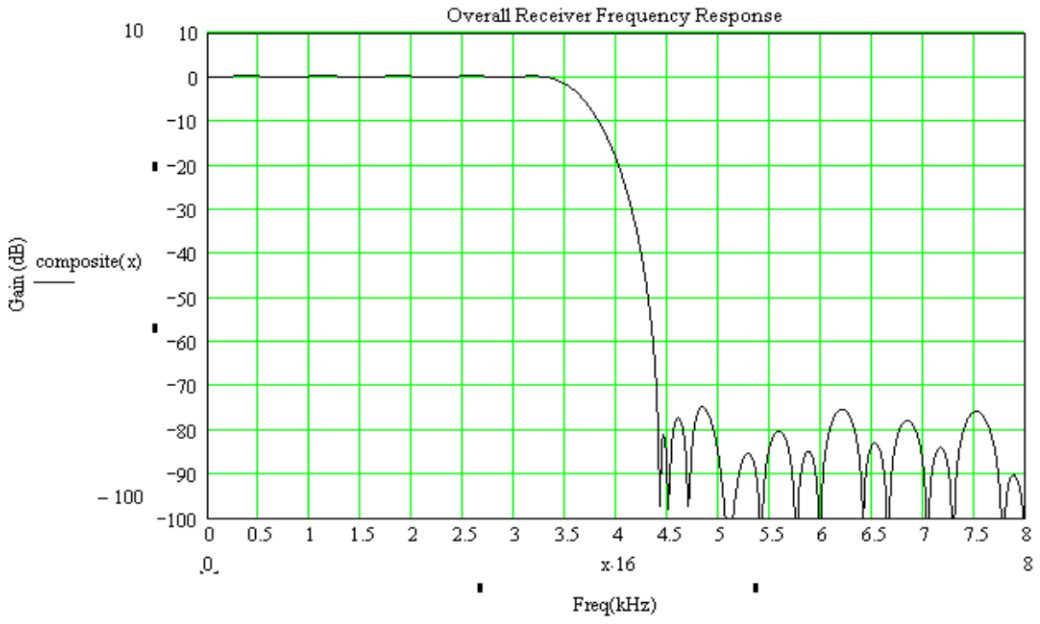


Figure 28: Overall Frequency Response of the Receive Path

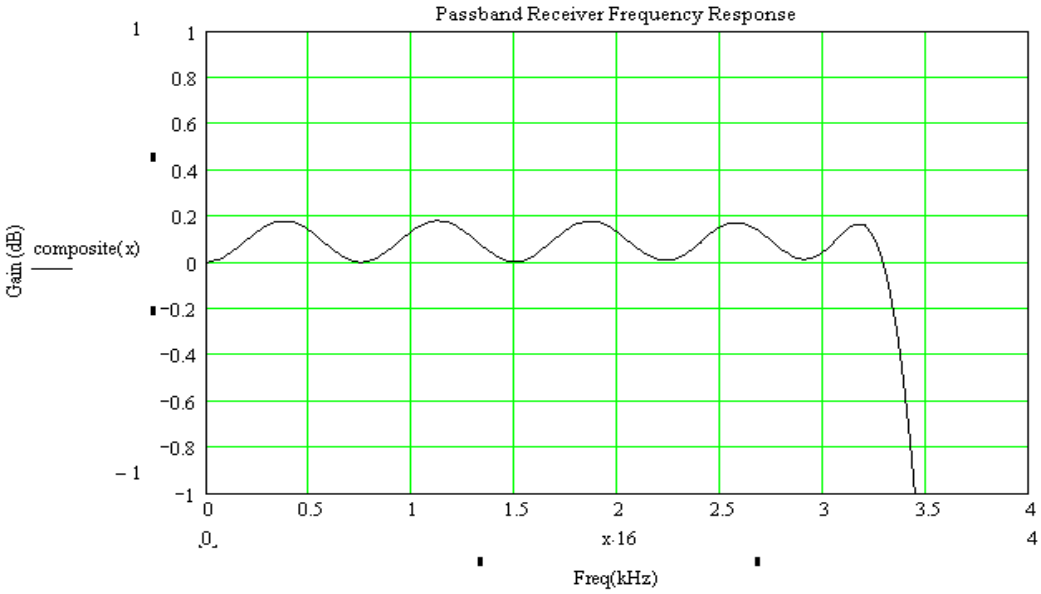


Figure 29: Pass-band Response of the Overall Receive Path

9.3 Signal Control Functions

Table 39: Signal Control Functions

Function Mnemonic	Register Location	Type	Description
TXBST	0x14[7]	WO	Transmit Boost Used in conjunction with DAA to manage transmit level. If set to 1, Transmit signal is increased by 6 dB. See Section 9.3.1.
DAA	0x14[6:5]	WO	DAA Tx Gain Used in conjunction with TXBST to manage transmit level. See Section 9.3.1.
RXBST	0x14[3]	W	Received Boost If set to 1, Receive signal is increased by 20 dB. Default is 0.
RXG	0x14[1:0]	WO	Receive Gain Sets the receive path gain/attenuation. See Table 41.
TXEN	0x16[7]	WO	Transmit Path Enable 1 = Enable Transmit Path. 0 = Disable Transmit Path. (Default)
RXEN	0x16[6]	WO	Receive Path Enable 1 = Enable Receive Path. 0 = Disable Receive Path. (Default)

9.3.1 Transmit and Receive Level Control

On the transmit side, 0 dBm transmit programming at the MAFE interface results in ~0 dBm on the line. On the receive side, 0 dBm receive signal on the line results in ~0 dBm at the MAFE interface.

On the transmit side there are three bits to adjust the transmit level: TXBST (Register 0x14[7]), DAA(1:0) (Register 0x14[6:5]).

Table 40: Transmit Gain Control

TXBST	DAA1	DAA0	Gain, nom.	Units
0	0	0	+2.0	dB
0	0	1	0.0	dB
0	1	0	-4.0	dB
0	1	1	-8.0	dB
1	0	0	+8.0	dB
1	0	1	+6.0	dB
1	1	0	+2.0	dB
1	1	1	-2.0	dB

On the receive side, there are two RXG bits RXG(1:0) (Register 0x14[1:0]) to control the receive gain. The RXG bits need to be set to 00. When the received line signal exceeds the voltage specified in *ITU-T Recommendation G.712 (2001)*, the receive gain must be reduced to prevent saturation and clipping within the receive signal processing path.

Table 41: Receive Gain Control

RXG1	RXG0	Gain nom	Units
0	0	0.0	dB
0	1	+3.0	dB
1	0	+6.0	dB
1	1	+9.0	dB

10 Barrier Information

10.1 Isolation Barrier

The 73M1x22 uses the Teridian MicroDAA proprietary isolation method based upon low cost pulse transformer coupling. This technique provides several advantages over other methods, including lower BOM cost, reduced component count, and significantly enhances common mode noise immunity, lower radiated noise (EMI), and improved operation in noisy environments. The MicroDAA technology has additional and enhanced functionality such as the support of powering the Line-Side DAA circuit from the Host-Side Device. This allows operation on leased lines circuits and on low current conditions commonly encountered in long loops. The MicroDAA can also operate entirely from line power when sufficient loop current is available.

Since the transformer is the only component crossing the isolation barrier, it solely determines the isolation between the PSTN and the 73M1x22 digital interface. Several vendors can supply compatible transformers with ratings up to 6000 V.

10.2 Barrier Powered Options

The 73M1x22 has the ability to be used either in a Line Powered Mode or one where the Line-Side Device can be powered across the barrier from the Host-Side Device. The power on default for the 73M1x22 is Barrier Powered Mode.

10.2.1 Barrier Powered Operation

In this default mode of operation the 73M1x22 Host-Side Device drives the pulse transformer in such a way that power pulses are time division multiplexed into the transmit bit stream (half the time) that is rectified by circuitry in the Line-Side Device and uses this energy to power itself.

10.2.2 Line Powered Operations

If there is sufficient current available from the PSTN line, the 73M1x22 can be programmed to use line power instead of across the barrier.

10.3 Synchronization of the Barrier

Since the communication across the barrier is digital, synchronization of data across the barrier is of absolute importance. To that end, the devices implement special procedures to ensure reliability across the barrier.

When loss of synchronization is detected, the SLHS bit is set to 1 and likewise SYNL is also set to 1 and initiates an interrupt to the host. Once the SYNL bit is asserted a new barrier synchronization sequence will automatically begin.

Once read, the SLHS bit is reset, but will be set again if the synchronization loss continues.

Upon power up, the following sequence should be used to ensure barrier synchronization:

1. The Line-Side Device (73M1902) starts in Barrier Powered Mode and transmits a preamble to aid the PLL locking of the
   Line-Side Device.
2. When PLL Lock detect is achieved, the Line-Side Device transmits status data to the Host-Side Device.
3. When the Line-Side status Data is detected by the Host-Side Device, the barrier is considered to be in synchronization by the Host-Side Device.
4. If the auto-poll mode is enabled, the Device ID is transmitted, which is followed by transmit data.
5. Upon detection of the Device ID, the Line-Side Device considers the Barrier to be in synchronization in host-to-line side direction.
6. Line-Side Device starts sending Receive Data.
7. If the Auto-Poll bit is enabled, the Host-Side Device will have polled the Device ID of the Line-Side Device. If the barrier is synchronized, then Register 0x1D[7:4], will be 1100. If not synchronized, then 0000.

10.4 Auxiliary A/D Converter

Line monitoring and sensing is performed with an 8-bit auxiliary A/D converter integrated in the 73M1922/73M1822. The input signals are connected to RGP and RGN pins. In certain applications, this A/D can be used to sample signals unrelated to PSTN DAA functions. In this type of application, it is necessary to isolate the input signal with optical or other means since the 73M1x22 is connected directly to the PSTN and is susceptible to high voltage surge. Under normal conditions, RGP and RGN are AC coupled to the line through high-voltage (250 V) capacitors.

10.5 Auto-Poll

Once the MSBI acquires synchronization, the MSBI state machine automatically sends a polling command to the 73M1x12 LIC. More specifically, the Host-Side Device (73M1902) requests that the Line-Side Device (73M1912) transmits its revision ID to the contents of Register 0x1D[7:4] in the 73M1902. The “revision ID” part of that specific register is cleared upon power up or upon loss of synchronization. After this auto-poll sequence, the host should read Register 0x1D[7:4] and determine if the “revision ID” field is all zeros or not. If it is not all zeros, this implies synchronization is established between the Host-Side Device and Line-Side Device.

The auto-poll mechanism can be disabled by setting the ENAPOL bit (Register 0x05[3]).

10.6 Barrier Control Functions

Table 42: Barrier Control Functions

Function Mnemonic	Register Location	Type	Description
ENLPW	0x02[2]	W	Enable Line Power 0 = Barrier Powered Mode is selected. (Default) 1 = Line Powered Mode is selected. ✓ Bit $\overline{\text{ENLVD}}$ must have the value of 0 before switching from Line Powered Mode to Barrier Powered Mode. Otherwise level detection is disabled and the transition to Barrier Powered Mode will not occur.
SYNL	0x03[1]	R	Barrier Synchronization Loss 0 = Indicates synchronization of data across the barrier. 1 = Indicates a loss of synchronization of data across the barrier. This status bit is reset when read. This is a maskable interrupt. It is enabled by the ENSYNL bit.
ENAPOL	0x05[3]	W	Enable Automatic Polling 0 = Disables automatic polling. 1 = Initiates automatic polling of the 73M1x22 Line-Side Device ID upon the establishment of the barrier SYN. (Default) If SYN is lost, the Device ID will be reset to 0000.
ENSYNL	0x05[1]	W	Enable Synchronization Loss Detection Interrupt 0 = Disables Synch Loss Detection Interrupt. 1 = Enables Synch Loss Detection Interrupt. (Default) When the 73M1x22 detects a loss of synchronization in the Host-Side Barrier Interface, SYNL 0x03[1] will be set and reset when read.
SLHS	0x0D[6]	R	Synchronization Loss Host Side This bit indicates the status of the Barrier Interface as seen from the Host-Side. 0 = Host-Side Barrier Interface is synchronized. 1 = Host-Side Barrier Interface lost synchronization. (Default) Once read, the SLHS bit is reset, but will be set again if the synchronization loss continues.
DISNTR	0x15[6]	WO	Disable No-Transition Timer If enabled, the No-Transition Timer is a safety feature. If the barrier fails, i.e. no transition is detected for 400 µs, the Line-Side Device resets itself and goes on hook to prevent line holding in a failure condition. 0 = Enables No-Transition Timer of 400 µs. (Default) 1 = Disables No-Transition Timer.
SLLS	0x1E[2]	W	Synchronization Loss Line Side 0 = TXRDY will continuously be generated following Synchronization Loss so as to allow SLLS information to be transferred across the barrier. This causes an automatic transfer of 1Eh. (Default) 1 = Synchronization is lost in the Line-Side Device due to Header.

10.7 Line-Side Device Operating Modes

The architecture of the 73M1x22 is unique in that the isolation barrier device, an inexpensive pulse transformer, is used to provide power and also bidirectional data between the Host-Side Device and the Line-Side Device. When the 73M1x22 is on hook, all the power for the Line-Side Device is provided over the barrier interface. After the Line-Side Device goes off hook, the telco line supplies approximately 8 mA to the Line-Side Device while the host provides the remainder across the barrier. It is also possible to power the Line-Side Device entirely from the line provided there is at least 17 mA of loop current available. Setting the ENLPW bit enables this mode and turns off the power supplied across the barrier. There is a penalty in using this mode in that the noise and dynamic range are about 6 dB worse than with the Barrier Powered Mode. It is therefore recommended that the Line Powered Mode be reserved for applications where the absolute minimum power from the host side is a priority and the reduction in performance can be tolerated.

Figure 30 shows the AC and DC circuits of the Line-Side Device.

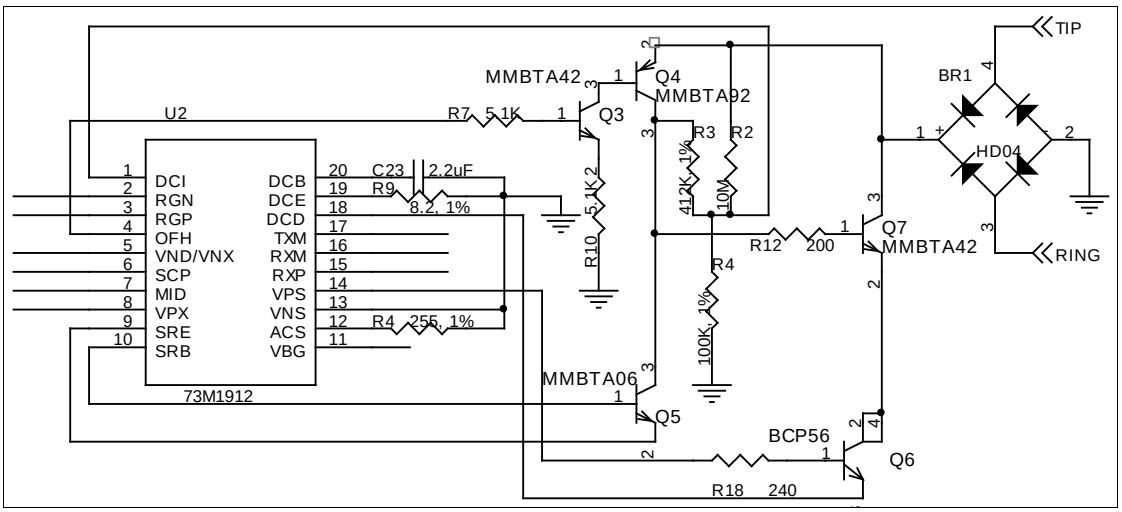


Figure 30: Line-Side Device AC and DC Circuits

The DCVI bits control the voltage versus current characteristics of the 73M1x22 by monitoring the voltage at the line divided down by the ratios of (R3+R4)/R4 (5:1) during off-hook and (R2+R4)/R4 (101:1) during on-hook period measured at the DCI pin. This voltage does not include the voltage across the Q4 and the bridge. When both the ENAC and ENDC bits are set (the hold mode), the DCVI characteristics follow approximately a 50 Ω load line offset by a factor determined by the DCVI bits. If ENDC=1 and ENAC=0, the 73M1x22 is in the seize mode and the DC voltage characteristic will be reduced to meet the Australian seize voltage requirements regardless of the setting of the DCVI bits.

10.8 Fail-Safe Operation of the Line-Side Device

The 73M1x22 provides additional protection against improper operation during error and harmful external events. These include power or communication failure with the Line-Side Device and the detection of abnormal voltages and currents on the line. The basis of this protection is to ensure that under these conditions the device is in the On-Hook state and the isolation is provided.

The following events will cause the 73M1x22 Line-Side Device to go to the On-Hook state if it is Off-Hook:

1. A Power-On Reset occurs while Off-Hook.
2. The non-transition timer function (see DISNTR) is triggered by the absence of any signal transitions for more than 400 µs on the barrier interface, indicating a problem with communications.
3. The power supply to the Line-Side Device is below normal operating levels.

11 Configurable Direct Access Arrangement (DAA)

The 73M1x22 line-side device integrates most of the circuitry to implement a PSTN line interface or DAA that is capable of being globally compliant with a single bill of materials. The 73M1x22 supports the following DAA functions:

- Pulse dialing
- On and Off Hook switch control
- Loop current (DC-IV) regulation
- Line impedance matching
- Ring detection
- Tip and Ring voltage polarity reversal detection
- Billing tone rejection
- Trans-hybrid cancellation

The device is able to support Barrier-powered mode in which the PSTN loop current may be as low as 8 mA.

11.1 Pulse Dialing

The 73M1x22 supports Pulse Dialing. See Section 11.6 for the description applicable control and status bits and Section **Error! Reference source not found.** for a description of a recommended procedure.

11.2 DC Termination

DC Termination or Loop Current (DC-IV) regulation is managed by the 73M1x22 Line-Side Device by configuring the appropriate registers. No additional components are necessary.

The 73M1x22 provides a DC transconductance circuit that regulates the tip to ring voltage depending on the DC current supplied by the line. There are four settings that can be used to set the voltage to current ratio.

Figure 31 shows the DC-IV characteristics of the 73M1x22 with special regions of interest.

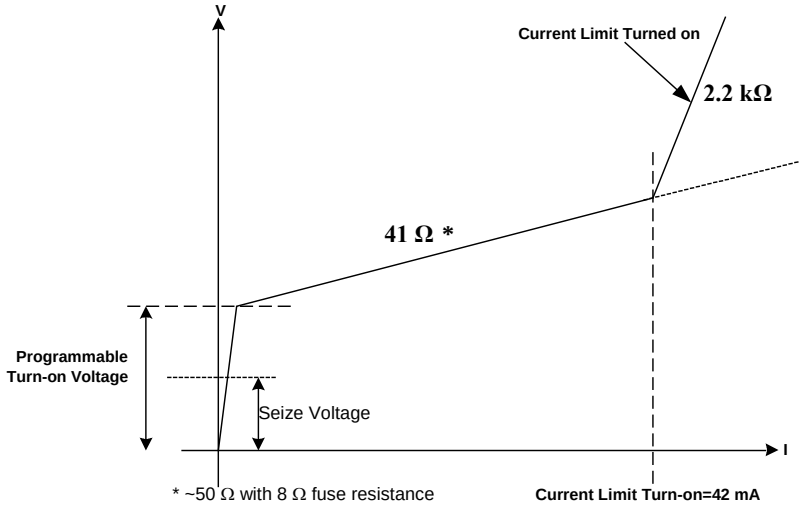


Figure 31: DC-IV Characteristics

The 73M1x22 can:

- Shift the characteristics by setting the turn-on voltage.
- Enable a current limit of 42 mA.

The 73M1x22 meets a wide range of different countries' requirements under software control. See Section 11.7.

There are two operating states for the DC-IV circuits: Hold and Seize.

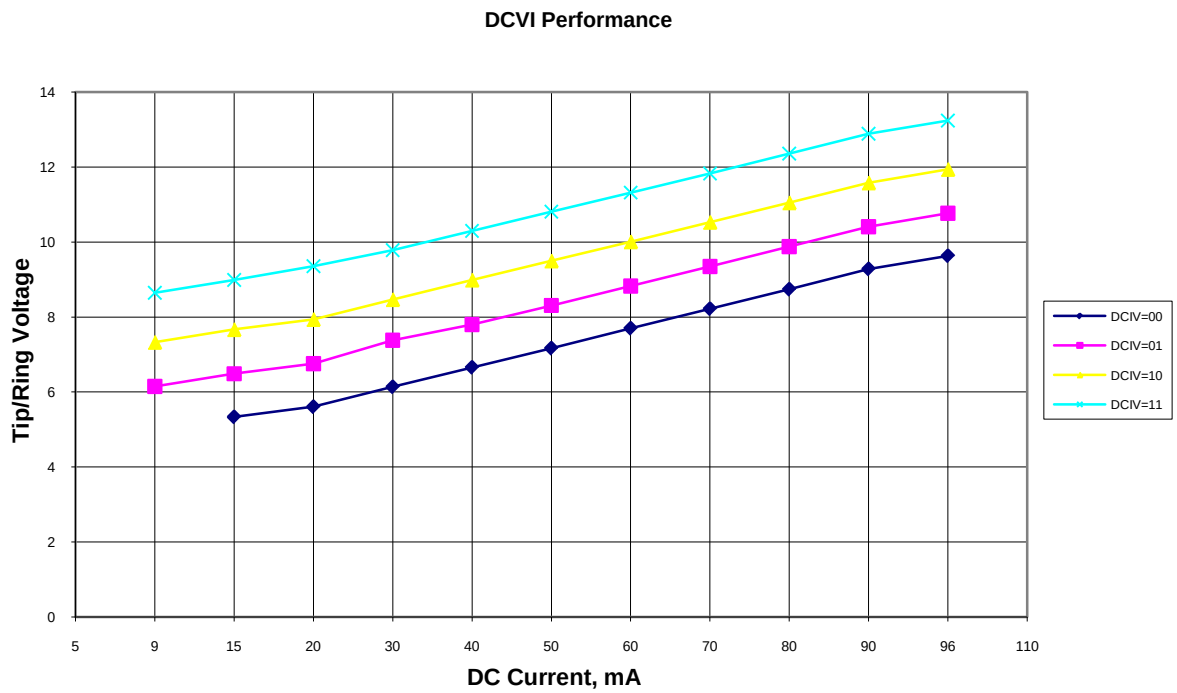


Figure 32: Tip-Ring Voltage versus Current Using Different DCIV Settings

The Hold state is the nominal operational point for the DC-IV circuits. The response shown in Figure 31 is for the Hold state (both DC and AC transconductance circuits are enabled). The slope of the DC-IV characteristics is approximately 50 Ω when the series resistance of a typical PPTC resettable fuse is taken into account.

The Seize state is a condition that is used by some central offices to determine an off-hook condition. In this state an additional load is added to the nominal operational DC-IV characteristics used during the Hold state

In the Seize state (only the DC transconductance circuit is enabled), the turn-on voltage is reduced on the line independent of the DC-IV control bits. See the description of the DCIV bit in Section 11.6.

An example of the use of the Seize state is that of Australia in which requires this stat for the first 300 ms immediately after going off hook.

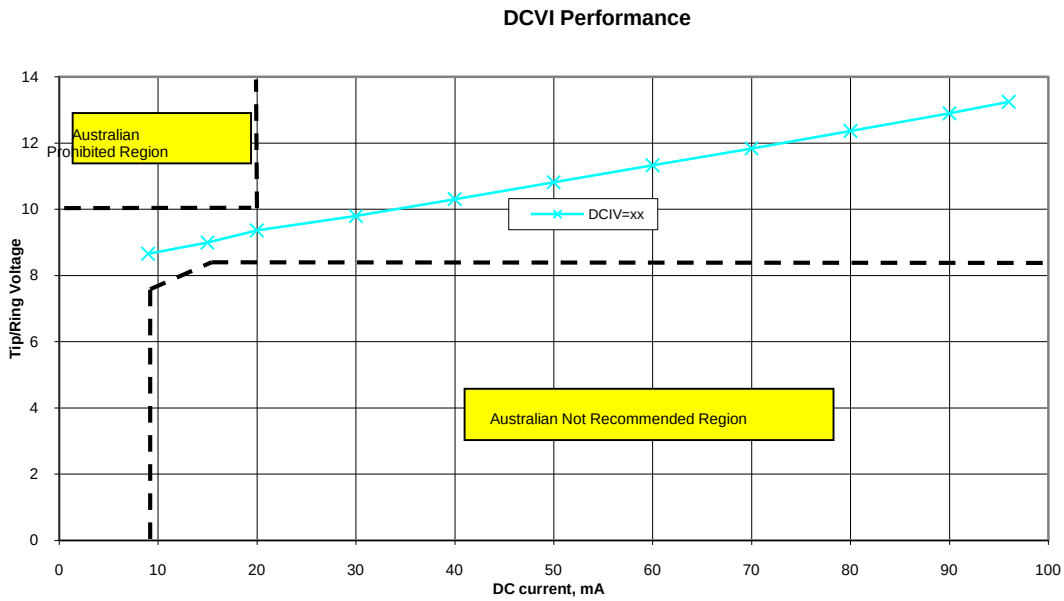


Figure 33: Voltage versus Current in the Seize Mode is the Same for All DCIV Settings

To facilitate the quick capture of the loop, the bandwidth of the DC loop is high upon power up. On the completion of DC loop capture, it should be lowered to avoid the interaction of DC and AC loops. See the description of the ENNOM bit in Section 11.6.

11.2.1 Current Limit Detection

If the DAA Current Limiting feature is enabled and the device detects a limited condition, then a status bit is set to give an indication of this event.

11.3 AC Termination

International DAA functionality is supported without any external termination components through the following functions:

- Enable/Disable AC termination ATEN bit at Register 0x16[4].
- Select AC termination impedance using the ACZ bits at Register 0x17[4:3]

ACZ Active Termination Loop Setting
00 = 600Ω (USA, Japan)
01 = 270Ω + 750Ω || 150nF (ETSI ES 203 021-2)
10 = 200Ω + 680Ω || 100nF (China)
11 = 220Ω + 820Ω || 115nF (Australia)

The AC impedance presented to the line can be altered as described in the AC Termination Register (Register 0x17). This is a part of a feedback loop that monitors the line and feeds an appropriate AC current back to line, such that the desired impedance looking into the RXP pin (of the 73M1912 LIC) is realized. Figure 34 shows magnitude response of the impedance matching filter for the case of ETSI ES 203 021-2. It is approximately equal to the inverse of the frequency characteristics of the impedance being realized.

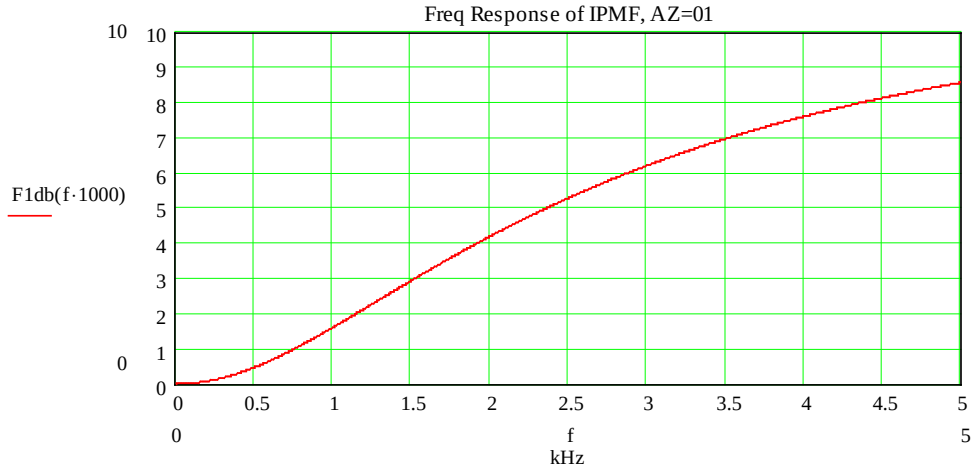


Figure 34: Magnitude Response of IPMF, ACZ=01 (ETSI ES 203 021-2)

11.4 Billing Tone Rejection

Some countries use a large amplitude out-of-band tone to measure call duration to allow remote central offices to determine the duration of a call for billing purposes. To avoid saturation and distortion of the input caused by these tones, it is important to be able to reject them. Typical values of frequency are 12 kHz or16 kHz.

The 73M1x22 has an integrated notch filter that attenuates either of these tones. By enabling this filter and selecting the position of the notch frequency such tones will be attenuated.

Figure 35 shows the magnitude response of the filter with a notch at either 12 kHz or 16 kHz.

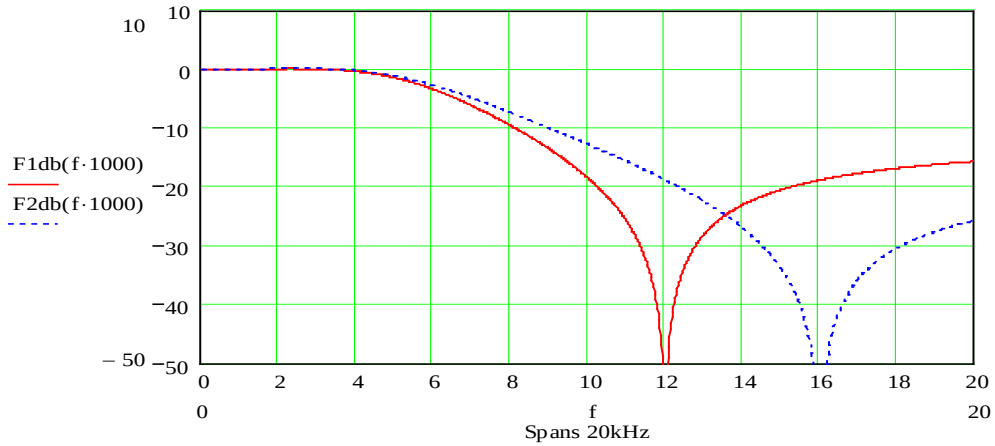


Figure 35: Magnitude Response of Billing Tone Notch Filter

In addition to the notch filter, the 73M1x22 can indicate the presence of an overload condition when a line's AC voltage exceeds 3.5 Vpk.

11.5 Trans-Hybrid Cancellation

A Transmit Bit Stream (TBS) emulating a sinusoid of 1 kHz, full scale (code word of +/- 32,767) is applied to SDIN and the residual signal is measured at SDOUT. Unless stated otherwise, test conditions are: ACZ=00 (600 Ω termination), THEN=1, ATEN=0, DAA=01, TXBST=0. TXM is externally fed back into the Line-Side Device (73M1912) to effect cancellation of transmit signal.

Table 43: Trans-Hybrid Cancellation

Parameter	Test Condition	Min	Nom	Max	Units
Transmit hybrid cancellation	Measure RxD in HIC		26		dB
Offset voltage	50% 1's Density		25	50	mV
AC swing	1kHz sinusoid at Tip and Ring	0.85	0.95	1.05	Vpk
Idle noise	300 Hz – 4 kHz at Tip and Ring		-81		dBm

11.6 Direct Access Arrangement Control Functions

These Transmit Control Registers contain control information to set up the line side of the 73M1x22. Included are DC-IV characteristics, off-hook control, etc.

Table 44: DAA Control Functions

Function Mnemonic	Register Location	Type	Description
OFH	0x12[7]	WO	Off-Hook Enable This bit controls the state of the Hook signal. 0 = On-Hook. (Default) 1 = Off-Hook.
PLDM	0x13[3]	WO	Pulse Dialing Mode Enable Alleviates the strict timing requirements for the Host having to control ENDC and OFH during pulse dialing. With PLDM = 1, the Host only has to toggle OFH to perform pulse dialing. 0 = Pulse Dialing Mode is disabled. (Default) 1 = Pulse Dialing Mode is enabled.
IDISPD	0x13[1:0]	WO	Discharge and Pulse Dialing Controls the DC discharge current and how fast the loop turns off. Affects pulse dialing waveform. Controls the amount of discharge current during hook switch transitions. 0 = Minimum current. (Default) 1 = Maximum current. It is recommended to set IDISPD to 1 prior to hook switching operations.
ENNOM	0x12[0]	WO	Enable Nominal Operation 0 = Speeds up the on and off hook transitions time by increasing the DC loop bandwidth of the DC transconductance circuit in the 73M1x22. This can be used for pulse dialing. In addition, ENNOM=0 prevents the reset of all bits in Register 0x12. (Default) 1 = Enter Nominal Operation. Reduces the loop bandwidth of the DC transconductance circuit. Allows reset of Register 0x12 caused by bits UVDT, OVDT or OIDT.

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>DCIV</td><td>0x13[7:6]</td><td>WO</td><td>DC Current Voltage Characteristic Control
Hold state with ENDC and ENAC=1, 20 mA DC loop current except if the DC-IV curve is shifted to a value given by these bits. This assumes that there is a 5:1 attenuation of off-hook.

<table>
<tr><th>DCIV1</th><th>DCIV0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>DC Loop On Voltage of 0.73V (5.60 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>0</td><td>1</td><td>DC Loop On Voltage of 0.977 V (6.75 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>1</td><td>0</td><td>DC Loop On Voltage of 1.232 V (7.65 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
<tr><td>1</td><td>1</td><td>DC Loop On Voltage of 1.488 V (9.35 V at Tip/Ring assuming a 5:1 step down of off-hook voltage)</td></tr>
</table>

*seize state with ENDC=1 and ENAC=0, 20 mA loop current.
xx=DC Loop On Voltage of 0.281V (3.9 V at Tip/Ring assuming 5:1 step down of off-hook voltage)</td></tr>
<tr><td colspan="4">Current Limiting Detection Control and Status</td></tr>
<tr><td>ILM</td><td>0x13[5]</td><td>WO</td><td>Current Limit Enable
This control enables or disables loop current limit.
0 = No current limit. (Default)
1 = 42 mA current limit enabled.</td></tr>
<tr><td>ILMON</td><td>0x1E[7]</td><td>R</td><td>Current Limit Mode On
This status bit is effective only when the ILM bit is set to 1.
0 = Loop current is lower than 42 mA.
1 = Loop current is higher than 42 mA and the current limiting mode is active.</td></tr>
<tr><td>THDCEN</td><td>0x13[4]</td><td>W</td><td>Enables the cancellation of AC signals within DCGM circuit
0 = Disables AC cancellation.
1 = Enables the cancellation of AC from DCGM circuit.</td></tr>
<tr><td>ATEN</td><td>0x16[4]</td><td>W</td><td>Active Termination Loop Enable
Enables or disables Active Termination Loop.
0 = Disable. (Default)
1 = Enable Active Termination Loop.
Normal operation requires this bit to be set to always enable a termination circuit.</td></tr>
</table>

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>FSCTR</td><td>0x16[3:0]</td><td>W</td><td>Filter Sample Rate Selection.
Since impedance matching is done thru the use of a switched capacitor filter, the realized impedance is exact only if Sample Rate Frequency (Fs) matches to the Sample Rate specified in FSCTR(3:0). When the actual sample rate is not any one of the followings in the table, a setting closest to the actual Fs should be chosen to minimize mismatching errors. These setting will affect both in AC Impedance Matching Filter (IPMF) and Receiver Low Pass Notch Filter (RLPN) both.
<table>
<tr><th colspan="4">Control Bits</th><th colspan="2">Fs Assumed (kHz)</th></tr>
<tr><th>FSCTR3</th><th>FSCTR2</th><th>FSCTR 1</th><th>FSCTR 0</th><th>IPMF</th><th>RLPN</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>7.2</td><td>7.2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8</td><td>8</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>9</td><td>9.6</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>9.6</td><td>9.6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>10.286</td><td>9.6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>11.2</td><td>12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>12</td><td>12</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>12.8</td><td>12</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>14.4</td><td>14.4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>X</td><td colspan="2">Not allowed</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>X</td><td colspan="2">Not allowed</td></tr>
</table></td></tr>
<tr><td>ACZ</td><td>0x17[4:3]</td><td>W</td><td>Active Termination Loop
Controls the selection of the active termination loops per the table shown below. ATEN must be set to 1 for selection to be enabled.
<table>
<tr><th>ACZ Field</th><th>Active Termination Loop Setting</th></tr>
<tr><td>00</td><td>600 Ω (Default)</td></tr>
<tr><td>01</td><td>270 Ω + 750 Ω || 150 nF(ETSI ES 203 021-2)</td></tr>
<tr><td>10</td><td>200 Ω + 680 Ω || 100 nF (China)</td></tr>
<tr><td>11</td><td>220 Ω + 820 Ω || 115 nF (Australia)</td></tr>
</table></td></tr>
<tr><td>APWS</td><td>0x17[7]</td><td>W</td><td>Analog Power Save Enable
0 = Saves analog power in LIC of 73M1822 or 73M1912.
1 = Full analog power in LIC of 73M1822 or 73M1912.</td></tr>
<tr><td>RLPNEN</td><td>0x16[5]</td><td>W</td><td>Receive Low Pass Notch Enable
0 = Billing Tone Receive Low Pass Notch (RLPN) filter bypassed. (Default)
1 = RLPN Filter Enabled. See RLPNH for notch frequency selection.</td></tr>
<tr><td>RLPNH</td><td>0x14[2]</td><td>W</td><td>Receive Low Pass Notch
0 = Selects Receive Low Pass Notch (RLPN) at 12 kHz. (Default)
1 = Selects RLPN at 16 kHz. See RLPNEN at register address 0x16[5] to enable filter.</td></tr>
<tr><td>THEN</td><td>0x15[3]</td><td>W</td><td>Enable Transhybrid Circuit
The rejection of the transmit signal from the receive signal path.
0 = Transhybrid Circuit disabled. (Default)
1 = Transhybrid Circuit enabled.
This bit should always be set for optimal performance.</td></tr>
</table>

Function Mnemonic	Register Location	Type	Description
ACCEN	0x13[4]	W	AC Cancellation Enable Cancels the AC signals from the DC transconductance circuit. 0 = No AC cancellation. (Default) 1 = Enables the cancellation of AC from the DC transconductance circuit. This should be set for normal operation.
ENAC	0x12[5]	WO	Enable AC Transconductance Circuit 0 = Shut Down AC Transconductance Circuit. Aux A/D input = Ring Detect Buffer (RGN) / Line Voltage (DCI). Seize state for going off hook. (Default) 1 = Enable AC Transconductance Circuit. Aux A/D input = Line Current (DCS) / Line Voltage (DCI).
ENDC	0x12[6]	WO	Enable DC Transconductance Circuit 0 = Shut down Transconductance Circuit. (Default) 1 = Enable Transconductance Circuit.
ENSHL	0x12[4]	WO	Enable Shunt Loading 0 = Disable shunt loading. (Default) 1 = Enable shunt loading of the line.
ENFEL	0x12[2]	WO	Enable Front End Line-Side Circuit 0 = Power down Front End Line-Side circuits. (Default) 1 = Enable Front End blocks excluding DCGM, ACGM, shunt regulator.
$\overline{\text{ENLVD}}$	0x12[3]	WO	LeV Detection (OVDT, UVDT, OIDT monitors) 0 = Enable LeV detection. (Default) 1 = Disable LeV detection (used in line-powered mode to save power). This bit will be 0 when Line Powered Mode is detected (ENLPW is set in Register 0x02[2]) and set to 1 when an interrupt occurs within the Line-Side Device. This bit must be reset prior to switching back to Barrier Powered Mode.

11.7 International Register Settings Table for DC and AC Terminations

Table 45 lists the recommended ACZ and DCIV register settings for various countries. Other parameters can also be set in addition to the AC and DC termination. These settings along with the reference schematic (see Figure 10 and Figure 11) can realize a single design for global usage without country-specific modifications. For more information on worldwide approvals, refer to the *73M1922 World-Wide Design Guide Application Note*.

Table 45: Recommended Register Settings for International Compatibility

Country	ACZ	DCIV	Country	ACZ	DCIV	Country	ACZ	DCIV
Argentina	00	10	Hungary[1]	01	10	Pakistan	00	10
Australia	11	11	Iceland[2]	01	10	Peru	00	10
Austria[1]	01	10	India	00	10	Philippines	00	10
Bahrain	00	10	Indonesia	00	10	Poland[1]	01	10
Belgium[1]	01	10	Ireland[1]	01	10	Portugal[1]	01	10
Bolivia	00	10	Israel	00	10	Romania[1]	01	10
Brazil	00	10	Italy[1]	01	10	Russia	00	10
Bulgaria[1]	01	10	Japan	00	00	Saudi Arabia	00	10
Canada	00	10	Jordan	00	10	Singapore	00	10
Chile	00	10	Kazakhstan	00	10	Slovakia[1]	01	10
China	00	10	Kuwait	00	10	Slovenia[1]	01	10
Columbia	00	10	Latvia[1]	01	10	South Africa	11	10
Croatia	01	10	Lebanon	00	10	South Korea	00	10
Cyprus[1]	01	10	Leichtenstein[2]	01	10	Spain[1]	01	10
Czech Rep[1]	01	10	Lithuania[1]	01	10	Sweden[1]	01	10
Denmark[1]	01	10	Luxembourg[1]	01	10	Switzerland[2]	01	10
Ecuador	00	10	Macao	00	10	Syria	00	10
Egypt	00	10	Malaysia	00	10	Taiwan	00	10
El Salvador	00	10	Malta[1]	01	10	ES 203 021-2	01	10
Estonia[1]	01	10	Mexico	00	10	Thailand	00	10
Finland[1]	01	10	Morocco	00	10	Turkey	00	10
France[1]	01	10	Netherlands[1]	01	10	UAE	00	10
Germany[1]	01	10	New Zealand	11	10	UK[1]	01	10
Greece[1]	01	10	Nigeria	00	10	Ukraine	00	00
Guam	00	10	Norway[2]	01	10	USA	00	10
Hong Kong	00	10	Oman	00	10	Yemen	00	10

[1] These countries are members of the European Union, where there are no longer any regulatory requirements for AC impedance. The suggested setting complies with ETSI ES 203 021-2. Other settings can be used if desired.

[2] These countries are members of the European Free Trade Association, and their regulations generally follow the European Union model. The suggested setting complies with ETSI ES 203 021-2.

12 Line Sensing and Status

12.1 Auxiliary A/D Converter

An 8-bit auxiliary A/D converter integrated in the 73M1x22 provides line monitoring and sensing capabilities. The A/D converter input signals are connected to the RGP and RGN pins of the device. It is possible to use this A/D converter to sample signals unrelated to PSTN DAA functions. However, in this application, it is necessary to isolate the input signal with optical or other means since the 73M1x22 is connected directly to the PSTN. Under normal conditions, RGP and RGN are AC coupled to the line through high voltage (250 V) capacitors.

Through the use of this auxiliary A/D converter, the following line status sensing features are supported by the 73M1x22:

- Ring detection.
- PSTN line already in use detection.
- Off-hook detection that a parallel phone has been picked-up – parallel pick-up detection (PPU).
- On-hook detection of DC loop voltage polarity reversals.
- On-hook detection of Type II Caller ID.

12.2 Ring Detection

Ring Detection is provided through circuitry connected to the device pins RGP and RGN. Any large voltage transition (ringing or line reversal) will be a source for the “Wake up” signal to the 73M1x22. Upon reception of a wake-up signal, the 73M1x22 passes the detected signal to the host where it is to be qualified for frequency and cadence (on and off timing of the ring tone bursts) as a valid ring signal.

12.3 Line In Use Detection (LIU)

If the 73M1x22 is preparing to go off-hook and dial, it is required to be aware whether the phone line is already in use by another device. If the 73M1x22 determines that the phone line is presently in use, it can avoid going off-hook and interrupting the call in progress. The timing of the 73M1x22 off-hook transition can be delayed until the 73M1x22 determines that the phone line is available. LIU sensing is done at pin DCIN with the Aux A/D.

12.4 Parallel Pick Up (PPU)

Parallel Pick Up is a means for the 73M1x22 to determine and notify a host in the case when the DAA is off-hook and a second or parallel connected device during the course of a connection is also made to go off-hook.

12.5 Polarity Reversal Detection

A third type of line sensing requirement is associated with Caller ID protocols found in Japan and some European countries. In these countries, the Caller ID signals are sent prior to the start of normal ringing. A polarity reversal is used to indicate to the 73M1x22 that transmission of Caller ID information is about to begin. The detection of a polarity reversal takes place while the 73M1x22 is in the on-hook state.

12.6 Off-hook Detection of Caller ID Type II

It is also possible to receive Caller ID signals while the telephone is in use, referred to as Type II CID. This requires the 73M1x12 to constantly monitor the line for signals, such as special in-band or CAS tones, while the 73M1x22 is in the off-hook state. This is done through the normal receive path.

12.7 Voltage and Current Detection

The 73M1x22 is capable of detecting the following circumstances:

- Under voltage on the line
- Over voltage on the line
- Over current

These 73M1x22 built-in mechanisms provide protection to both the device itself and the external line circuitry.

If enabled, Over Voltage and Over Current detection will cause the 73M1x22 to go on-hook without the intervention of the host.

If configured in Line Powered mode, the detection of an Under-voltage condition causes the 73M1x22 to switch automatically to Barrier Powered Operation (see Section 10.2.1). This is done without the intervention of the host.

For each of the detection functions there are enable control and detection status. For each of the functions there is a master detection function enable bit that is to be set in order for the functions to work.

12.8 Under Voltage Detection (UVD)

Under Voltage Detection is an important feature of 73M1x22. It is intended to determine if the phone line is not capable of supplying the current that the 73M1x22 requires from the line for proper operation. If this function is enabled and If the line is not capable of providing this current, the UVD condition will be asserted and can become a source of interrupt from 73M1x22 to its connected host.

12.9 Over Voltage Detection (OVD)

If enabled, Over Voltage Detection is indicated if the device senses that the line voltage exceeds a defined threshold. The device allows the selection of choice of either 60 Vpk or 70 Vpk (depending upon the attenuation ratio, typically this is 100:1).

If enabled the 73M1x22 will automatically go on-hook if over voltage is detected.

12.10 AC Signal Over Load Detection

This is the same feature as used for the detection of billing tones (see Section 11.4). In this most generic sense, this detector provides an indicator that the AC signal on the line exceeds a value of 3.5 Vpk.

12.11 Over Current Detection (OID)

When the line current exceeds the safe operating range of the 73M1x22 or the external transistors, the device indicates this condition. If enabled, the 73M1x22 will automatically go on-hook if an over current event is detected.

12.12 Line Status Functions Control Functions

These registers contain control information to set up and use the 73M1x22 line sensing functions.

Table 46: Line Sensing Control Functions

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>RXBST</td><td>0x14[3]</td><td>WO</td><td>Received Boost
If set to 1, Receive signal is increased by 20 dB. Default is 0. This is used to amplify signals that are passed through the auxiliary A/D when On-Hook.</td></tr>
<tr><td>CIDM</td><td>0x15[4]</td><td>W</td><td>Caller ID Mode
0 = Disable Caller ID Mode. (Default)
1 = Enables Caller ID Mode by coupling the signal from the RGN/RGP pins to the receive filter input. A 20 dB gain boost is included in the signal path. The RXBST bit should also be set to allow the total nominal gain of 40 dB in the Caller ID path. The normal signal path is disconnected.</td></tr>
<tr><td colspan="4">Ring Detection Status Bits</td></tr>
<tr><td>RGTH</td><td>0x0E[1:0]</td><td>W</td><td>Ring Detect Threshold
Controls the Ring Detect Threshold assuming a 100:1 reduction of Ring Voltage into RGP/RGN pins.
<table>
<tr><th>RGTH1</th><th>RGTH0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Ring Detect disabled. For ring detection to occur, these bits must be programmed to a non-zero state.</td></tr>
<tr><td>0</td><td>1</td><td>0.15 Vpk equivalent to ±15 Vpk at Auxiliary A/D input.</td></tr>
<tr><td>1</td><td>0</td><td>0.30 Vpk equivalent to ±30 Vpk at Auxiliary A/D input.</td></tr>
<tr><td>1</td><td>1</td><td>0.45 Vpk equivalent to ±45 Vpk at Auxiliary A/D input.</td></tr>
</table></td></tr>
<tr><td>RGMON</td><td>0x03[3]</td><td>R</td><td>Ringing Monitor
Bit 3 monitors the activity of Ringing for further cadence check by the host:
0 = Silent (Default)
1 = Ringing
This bit is not latched. This status bit is reset when read.</td></tr>
<tr><td>RGDT</td><td>0x03[0]</td><td>R</td><td>Ring or Line Reversal Detection
Voltage greater than the Ring Detect Threshold was detected at RGP/RGN. This value is latched upon the event and cleared on read. The threshold is determined by RGTH. This is a maskable interrupt. It is enabled by the ENRGDT bit.
0 = No Latched Ring or Line Reversal Detection event. (Default)
1 = A Latched Ring or Line Reversal Detection event.</td></tr>
<tr><td>ENRGDT</td><td>0x05[0]</td><td>W</td><td>Enable Ring Detection Interrupt
This control bit enables the ring detection interrupt.
0 = Ring Detection Interrupt Disabled.
1 = Ring Detection Interrupt Enabled. (Default)
When 73M1922 detects an incoming ring signal, this bit will be set, if enabled, and reset when read.</td></tr>
</table>

Auxiliary A/D Converter Status Bits			
RNG	0x1A[7:0]	R	Result of Auxiliary A/D measuring the attenuated ring voltage. Note: 1 lsb=1.31/128=~10.23 mV; 1's compliment. Example: 00100000 → 327 mV or Ring Voltage=32.7 V
LV	0x1B[7:1]	R	Line Voltage On and Off Hook LV contains the seven most significant bits of an 8-bit A/D representation of the voltage of the input of pin DCI. The voltage at the DCI pin is equal to the decimal value of LV bits [7:1] x 21.87 mV. For example, if the value of 0100000 is read from LV bits [7:1], this has a decimal value of 32, therefore DCI voltage equals 32 x 21.87 = 700 mV. Note that the voltage at the DCI pin is the voltage divided by 5 (off hook) or 100 (on hook). When offhook the diode bridge, switch saturation voltage, etc. should also be added to calculate the voltage at tip and ring.
LC	0x1C[7:1]	R	Loop Current in DC Path Result of Auxiliary A/D measuring the Loop Current (7-bit resolution, least significant bits only). Note LC0=1 lsb=1.31/128=~10.23 mV=1.25 mA; magnitude only. The value of the resistor between the rectifier bridge and the DCS pin is assumed to be 8.2 Ω. Example: 0000011 → 30.7 mV/RE=3.74 mA; 0010000 → 20 mA Note: The AC path also has ~7 mA of loop current that should be added to get the total loop current provided by the line.
Line Sensing Control			
DET	0x03[2]	R	Detection of Voltage or Current Fault 0 = None of the three conditions is detected. (Default) 1 = Indicates the detection of one of three conditions: Under Voltage, Over Voltage and Over Current. This status bit is reset when read. This is a maskable interrupt. It is enabled by the ENDET bit.
ENDET	0x05[2]	W	Enables Line Sensing Interrupt on Host Side Device This bit controls whether an interrupt is generated based upon the detection of Under Voltage, Over Voltage and Over Current. 0 = Disable detector interrupt. (Default) 1 = Enable detector interrupt.
ENDT	0x12[1]	WO	Enable Detectors on Line Side Device 0 = UVDT, OVDT and OIDT conditions are ignored. (Default) 1 = Enables UVDT, OVDT and OIDT in the Line-Side Device and allows them to be used in the Host-Side Device.
Under-Voltage Detection Control and Status			
ENUVD	0x15[2]	WO	Enable Under Voltage Detector on Line Side Device 1 = Under Voltage Detector Enabled. When enabled, the ENNOM bit is temporarily set to the wide bandwidth mode if an under-voltage condition detected to allow fast reacquisition of the line.
UVDET	0x1E[6]	R	Under-Voltage Detection on Line Side Device 0 = Under Voltage condition is not detected at VPS. (Default) 1 = Under Voltage condition is detected at VPS.

Over-Voltage Detection Control and Status			
ENOVD	0x15[1]	WO	Enable Over-Voltage Detector on Line Side Device 1 = Over Voltage Detector Enabled (not latched). Over voltage detector is enabled if ENOVD, ENFEL and ENNOM all equal 1.
OVDET	0x1E[5]	R	Over-Voltage Detected on Line Side Device 0 = Over Voltage condition is not detected at RGP/RGN inputs. (Default) 1 = Over Voltage Condition is detected at RGP/RGN inputs.
OVDTH	0x13[2]	WO	Over-Voltage Threshold Setting 0 = Over Voltage Threshold is 0.6 Vpk at the chip or 60 Vp on the line. (Default) 1 = Over Voltage Threshold is 0.7 Vpk at the chip or 70 Vp on the line.
Over-Current Detection Control and Status			
ENOID	0x15[0]	WO	Enable Over-Current Detector on Line Side Device 0 = Over-Current Detector is not enabled. (Default) 1 = Over-Current Detector is enabled.
OIDET	0x1E[4]	R	Over-Current (I) Detector on Line Side Device 0 = Over-Current (I) condition is not detected. (Default) 1 = Over-Current (I) condition is detected at the DCS pin when Loop Current is > 125 mA if ILM=0, or > 55 mA if ILM=1.

13 Loopback and Testing Modes

Figure 36 show the five loopback modes available in the 73M1x22.

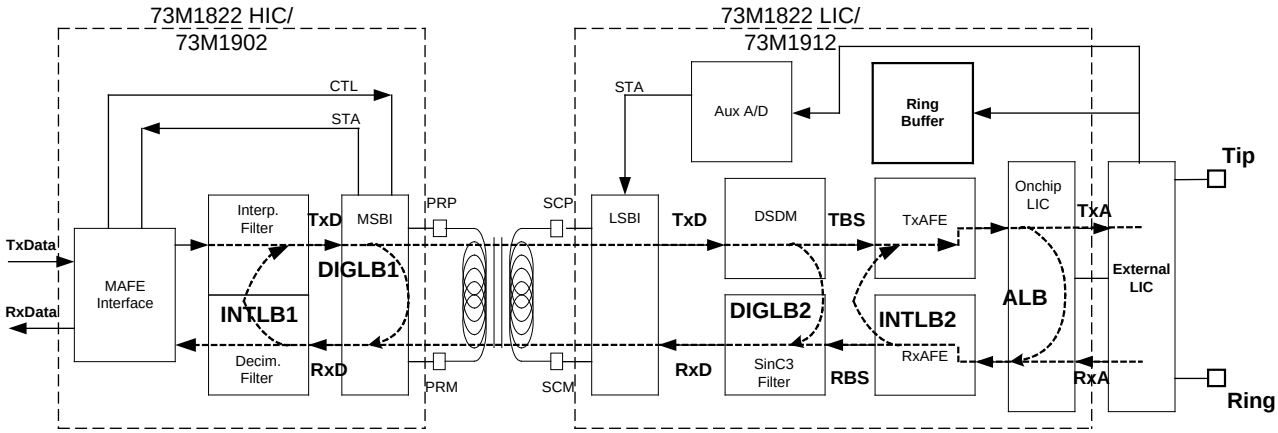


Figure 36: Loopback Modes Highlighted

Table 47 describes how the above control bits interact to provide each of the six loopback modes.

Table 47: Loopback Modes

TEST	TMEN	DTST	Loopback Mode	Mnemonic
0000	0	00	Normal mode. (Default)	No Loops
0000	1	10	Digital Loopback mode. Interpolated TxData (TxD) is looped back to the Decimated RxData input (RxD).	DIGLB1
0000	1	11	Remote Analog Loopback. Received RxD is looped back as TxD and transmitted back to the 73M1922 Line-Side Device; RxD is D/A converted to yield the analog transmit signal (TxA).	INTLB1
0001	0	00	Digital Loopback mode. Transmit Bit Stream (TBS) is looped back to receive digital channel and received (DIGLB2).	DIGLB2
0010	0	00	Remote Analog Loopback. Receive analog signal is converted to Received Bit Stream (RBS) and is looped back to TBS and the analog transmit channel (INTLB2).	INTLB2
0011	0	00	Analog Loopback. The transmit data is connected to the receiver at the analog interface and received (ALB).	ALB

13.1 Loopback Controls

Table 48 describes the registers used for loopback control.

Table 48: Loopback Controls

<table>
<tr><th>Function Mnemonic</th><th>Register Location</th><th>Type</th><th>Description</th></tr>
<tr><td>TMEN</td><td>0x02[7]</td><td>W</td><td>Test Mode Enable
Used to enable the activation of the test loops controlled by the DTST bits (DIGLB1 and INTLB1).
0 = No DTST loops enable. (Default)
1 = DTST loops enable.

✓ TMEN has to be set to 1 before the setting of the DTST bits.</td></tr>
<tr><td>DTST</td><td>0x07[3:0]</td><td>W</td><td>These control bits enable DIGLB1 and INTLB1.

✓ Prior to writing to these bits, TMEN must be set to 1.
<table>
<tr><th>DTST1</th><th>DTST0</th><th>Selected Test Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (Default)</td></tr>
<tr><td>1</td><td>0</td><td>DIGLB1</td></tr>
<tr><td>1</td><td>1</td><td>INTLB1</td></tr>
</table></td></tr>
<tr><td>TEST</td><td>0x18[7:4]</td><td>W</td><td>This four-bit field is used to enable the loopback mode per the following table:
<table>
<tr><th>TEST</th><th>Loopback Mode</th></tr>
<tr><td>0000</td><td>Normal mode. (Default)
Transmit and receive channels are independent.</td></tr>
<tr><td>0001</td><td>Digital loopback mode. Transmit Bit Stream (TBS) is looped back to receive digital channel and received (DIGLB2).</td></tr>
<tr><td>0010</td><td>Remote Analog loopback. Receive analog signal is converted to Received Bit Stream (RBS) and is looped back to TBS and the analog transmit channel (INTLB2).</td></tr>
<tr><td>0011</td><td>Analog loopback. The transmit data is connected to the receiver at the analog interface and received (ALB).</td></tr>
</table></td></tr>
</table>

14 Performance

This section provides an overview of typical performance characteristics measured using a 73M1x22 production device on a Teridian Reference Board. The measurements were made at the tip and ring pins.

14.1 DC VI Characteristics

14.1.1 Off-Hook Tip and Ring DC Characteristics

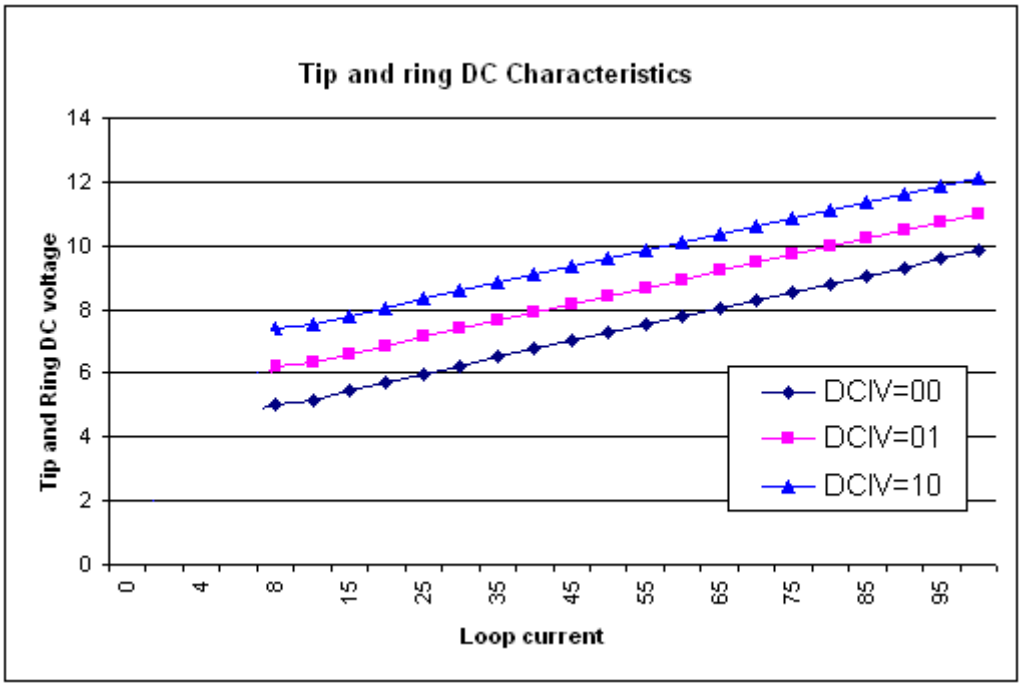


Figure 37: Off-Hook Tip and Ring DC Characteristics

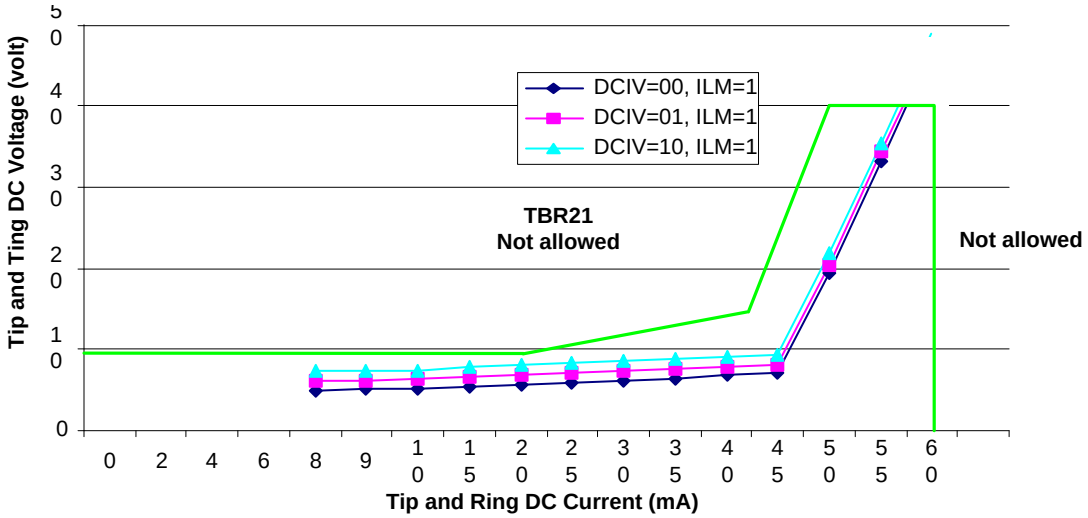


Figure 38: ES 203 021-2 DC Mask with Current Limit Enabled

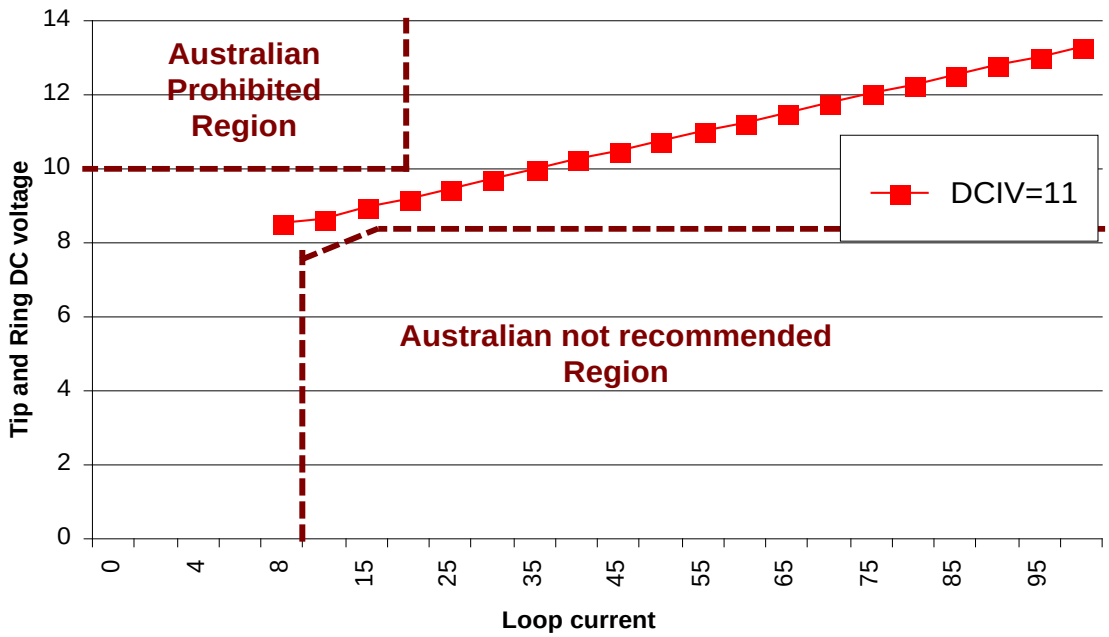


Figure 39: Australian Hold State Characteristics

14.2 Receive

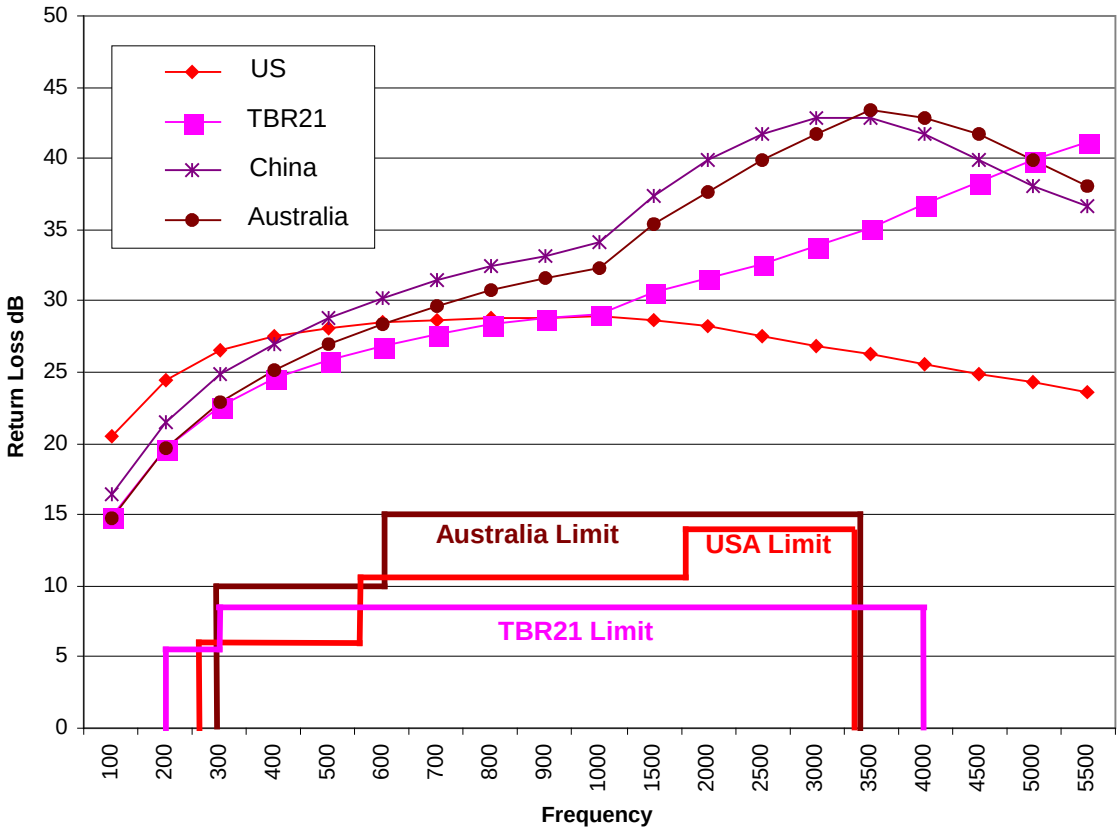
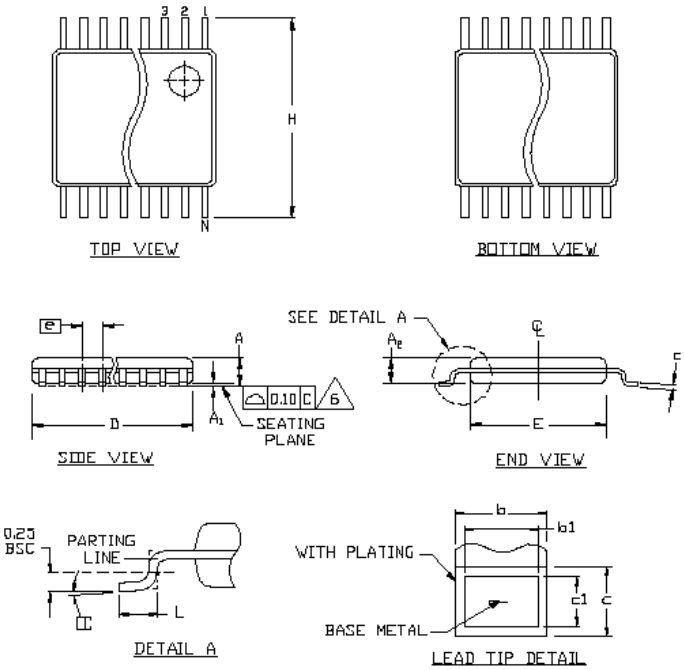


Figure 40: Return Loss

15 Package Layout



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

Figure 41: 20-Pin TSSOP Package Dimensions

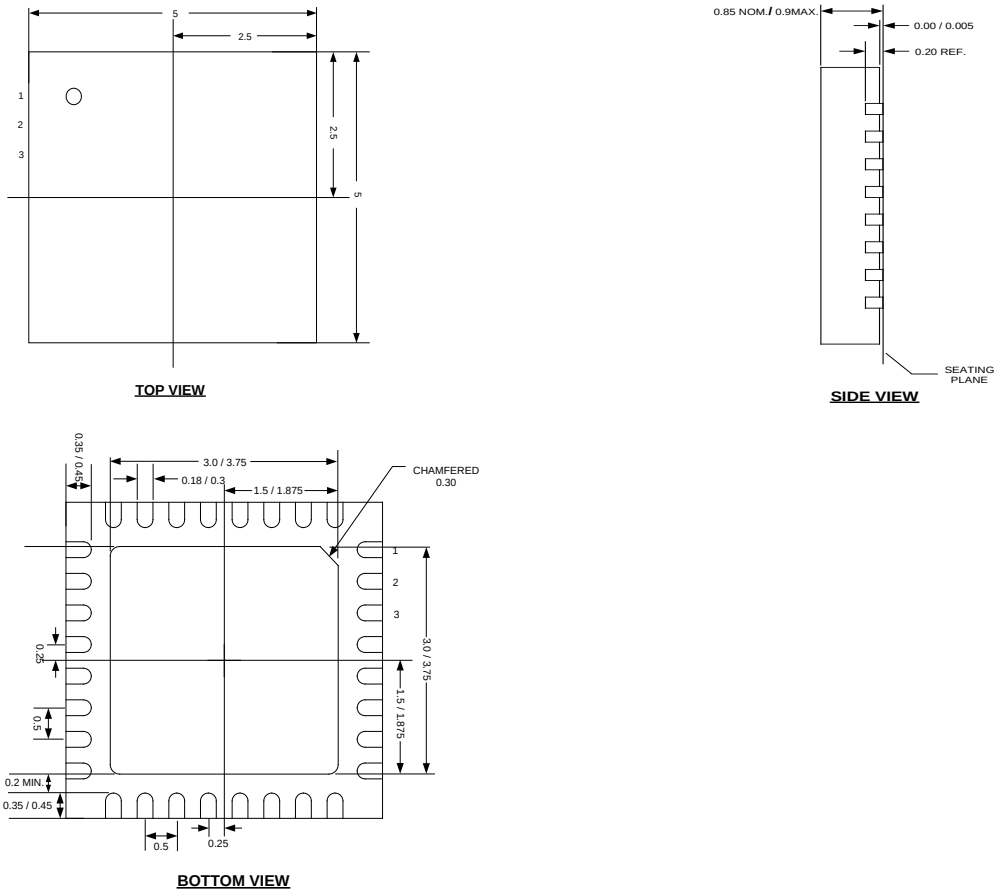
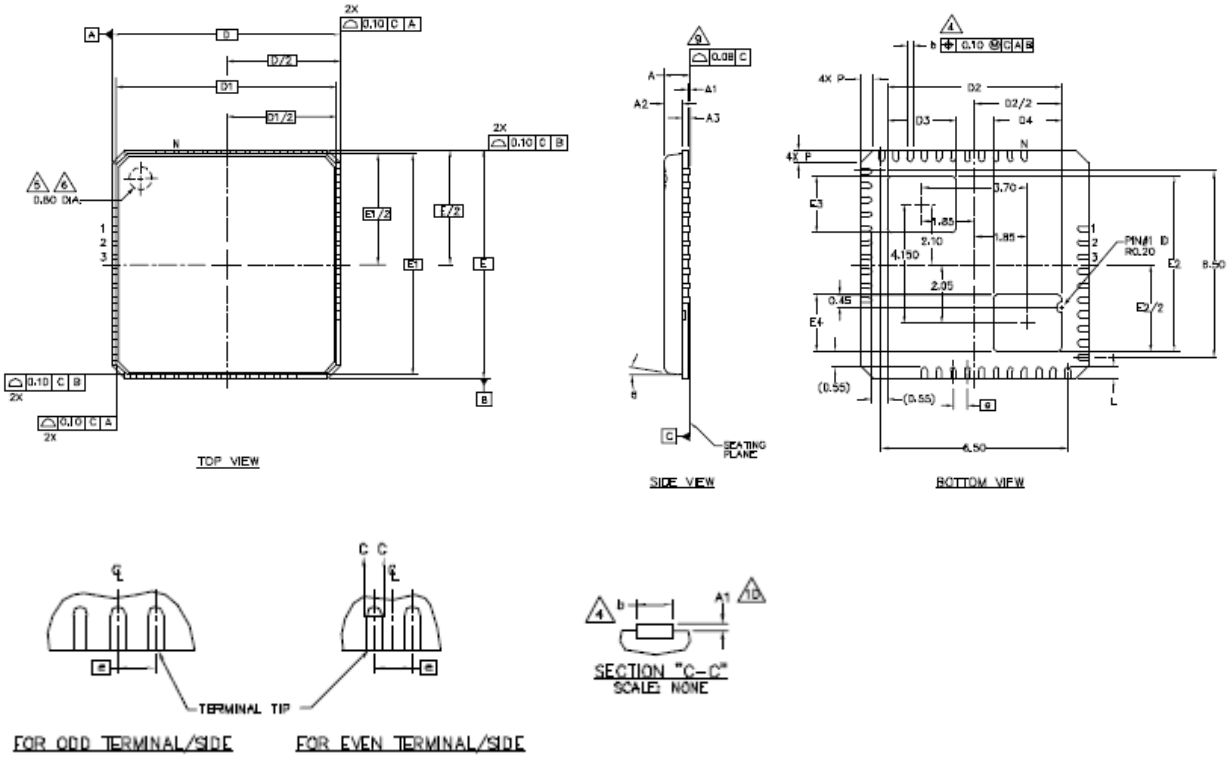


Figure 42: 32-Pin QFN Package Dimensions



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. APPLIED ONLY FOR TERMINALS.

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.85	0.90	
A1	0.00	0.01	0.05	9
A2	–	0.65	0.70	
A3	0.20 REF.			
e	0.50 BSC			
N	42			
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D	8.00 BSC			
D1	7.75 BSC			
E	8.00 BSC			
E1	7.75 BSC			
θ			12°	
P	0.24	0.42	0.60	

SYMBOLS	D2			E2			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	5.95	6.10	6.25	6.00	6.15	6.30	
SYMBOLS	D3			E3			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	2.25	2.40	2.55	1.85	2.00	2.15	
SYMBOLS	D4			E4			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	2.25	2.40	2.55	1.85	2.00	2.15	

Figure 43: 42-Pin QFN Package Dimensions

16 Ordering Information

Table 49 lists the order numbers and packaging marks used to identify 73M1822 and 73M1922 products.

Table 49: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark	Host/Line
73M1922 32-Pin QFN, Lead free	73M1922-IM/F	73M1912-M 73M1902-M	Line-Side IC Host-Side IC
73M1922 32-Pin QFN, Lead free, Tape and Reel	73M1922-IMR/F	73M1912-M 73M1902-M	Line-Side IC Host-Side IC
73M1922 20-Pin TSSOP, Lead free	73M1922-IVT/F	73M1912VT 73M1902A	Line-Side IC Host-Side IC
73M1922 20-Pin TSSOP, Lead free Tape and Reel	73M1922-IVTR/F	73M1912VT 73M1902A	Line-Side IC Host-Side IC
73M1822 42-Pin QFN, Lead free	73M1822-IM/F	73M1822A-IM	
73M1822 42-Pin QFN, Lead free, Tape and Reel	73M1822-IMR/F	73M1822A-IM	

17 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73M1822 or 73M1922, contact us at:

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Revision History

Revision	Date	Description
1.0	10/26/2007	First publication.
1.1	11/7/2007	
1.1.1	4/11/2008	
1.2	8/28/2008	
1.3	3/23/2009	
1.4	8/6/2009	
1.5	10/16/2009	
1.6	4/7/2010	Changed the values in Table 17. Replaced the schematics in Figure 10 and Figure 11. Updated the Bill of Materials in Table 27. Added the ACCEN bit to Table 30 and Table 31. Corrected the Types (R, W, WO) in Table 31. Added clarification to the description of the PLDM bit. Added clarification to the description of the RGDT bit.

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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