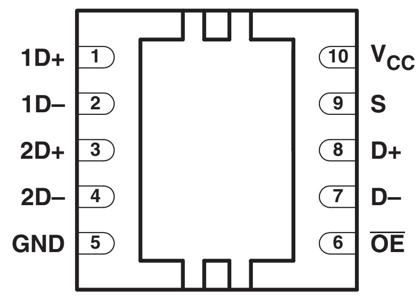
HIGH-SPEED USB 2.0 (480-Mbps) 1:2 MULTIPLEXER/DEMULTIPLEXER SWITCH WITH SINGLE ENABLE AND IEC LEVEL 3 ESD PROTECTION

Check for Samples: TS3USB221E

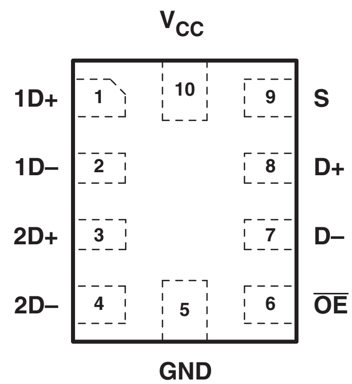
FEATURES

- V_{CC} Operation of 2.5 V to 3.3 V
- Switch I/Os Accept Signals Up to 5.5 V
- 1.8-V Compatible Control-Pin Inputs
- Low-Power Mode When $\overline{OE}$ Is Disabled (1 μA)
- r_{ON} = 6 Ω Maximum
- Δr_{ON} = 0.2 Ω Typical
- $C_{io(on)}$ = 7 pF Maximum
- Low Power Consumption (30 μA Maximum)
- ESD Performance Tested Per JESD 22
  - 7000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O Port to GND
  - 12-kV Human Body Model (A114-B, Class II)
  - ±7-kV Contact Discharge (IEC 61000-4-2)
- High Bandwidth (1 GHz Typical)

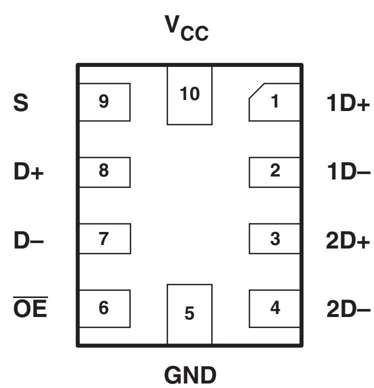
DRC PACKAGE
(TOP VIEW)



RSE PACKAGE
(TOP VIEW)



RSE PACKAGE
(BOTTOM VIEW)



APPLICATIONS

- Routes Signals for USB 1.0, 1.1, and 2.0

DESCRIPTION/ ORDERING INFORMATION

The TS3USB221E is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221E integrates ESD protection cells on all pins, is available in a SON package (3 mm × 3 mm) as well as in a tiny μQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SON – DRC	Reel of 3000	TS3USB221EDRCR	ZVM
	QFN (µQFN) – RSE	Reel of 3000	TS3USB221ERSER	LGR or LGO

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. PIN DESCRIPTION

NAME	DESCRIPTION
$\overline{OE}$	Bus-switch enable
S	Select input
D	Bus A
nD	Bus B

Table 2. TRUTH TABLE

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

BLOCK DIAGRAM

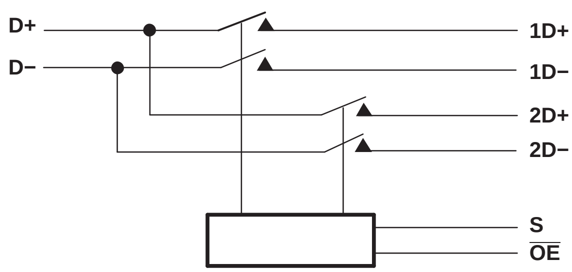
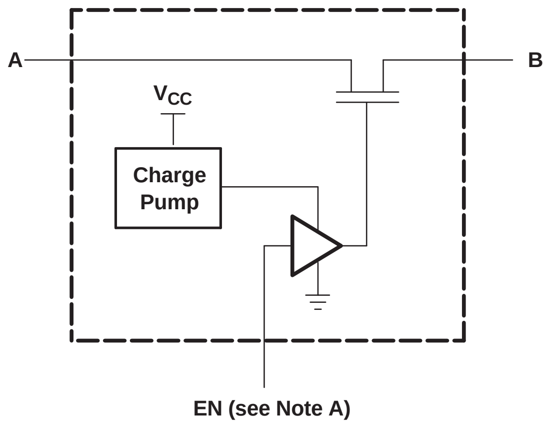


Figure 1. SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



A. EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current(5)			±120	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	DRC package(7)		48.7	°C/W
		RSE package		243	
		ZXU package		128	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) Package Preview

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0.46 × V_{CC}		V
		V_{CC} = 2.7 V to 3.6 V	0.46 × V_{CC}		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.25 × V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V		0.25 × V_{CC}	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS[1]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V, 2.7 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V, 2.7 V, 0 V,	V_{IN} = 0 V to 3.6 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V, 2.7 V, V_O = 0 V to 5.25 V, V_I = 0 V,	V_{IN} = V_{CC} or GND, Switch OFF				±1	µA
$I_{(OFF)}$		V_{CC} = 0 V	$V_{I/O}$ = 0 V to 5.25 V				±2	µA
			$V_{I/O}$ = 0 V to 3.6 V				±2	
			$V_{I/O}$ = 0 V to 2.7 V				±1	
I_{CC}		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND,	$I_{I/O}$ = 0 V, Switch ON or OFF				30	µA
I_{CC} (low power mode)		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND	Switch disabled ($\overline{OE}$ in high state)				1	µA
I_{CC} [4]	Control inputs	One input at 1.8 V, Other inputs at V_{CC} or GND	V_{CC} = 3.6 V				20	µA
			V_{CC} = 2.7 V				0.5	
C_{in}	Control inputs	V_{CC} = 3.3 V, 2.5 V,	V_{IN} = 3.3 V or 0 V			1.5	2.5	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch OFF		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch ON		6	7.5	pF
r_{ON} [5]		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		3	6	Ω
			V_I = 2.4 V,	I_O = –15 mA		3.4	6	
Δr_{ON}		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		0.2		Ω
			V_I = 1.7,	I_O = –15 mA		0.2		
$r_{ON(flat)}$		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		1		Ω
			V_I = 1.7,	I_O = –15 mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP[1]	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	–40	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	–40	dB
BW	Bandwidth (–3 dB)	R_L = 50	1	GHz

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

DYNAMIC ELECTRICAL CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 , f = 250 MHz	-39	dB
O_{IRR}	OFF isolation	R_L = 50 , f = 250 MHz	-40	dB
BW	Bandwidth (3 dB)	R_L = 50	1	GHz

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.

SWITCHING CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL}– t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

SWITCHING CHARACTERISTICS

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ±10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL}– t_{PLH})(2)			0.1	0.2	ns

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

APPLICATION INFORMATION

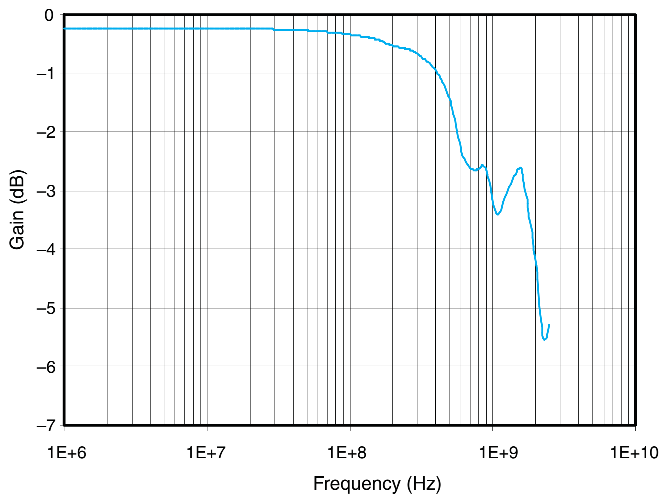


Figure 2. Gain vs Frequency

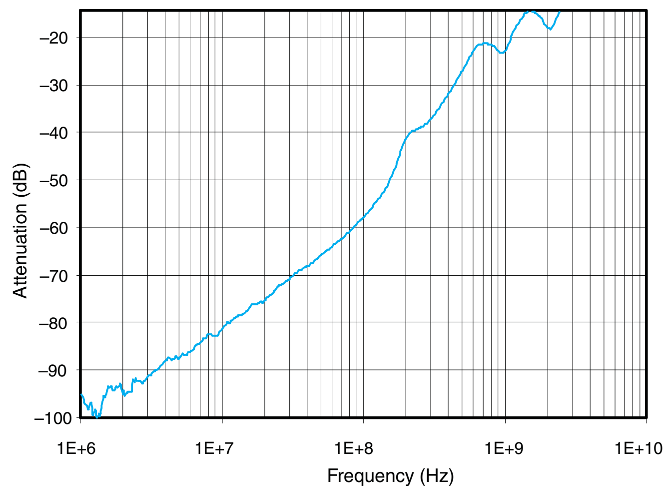


Figure 3. OFF Isolation vs Frequency

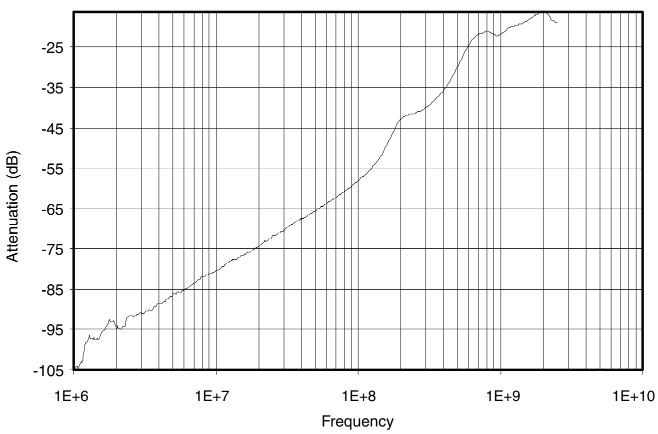


Figure 4. Crosstalk vs Frequency

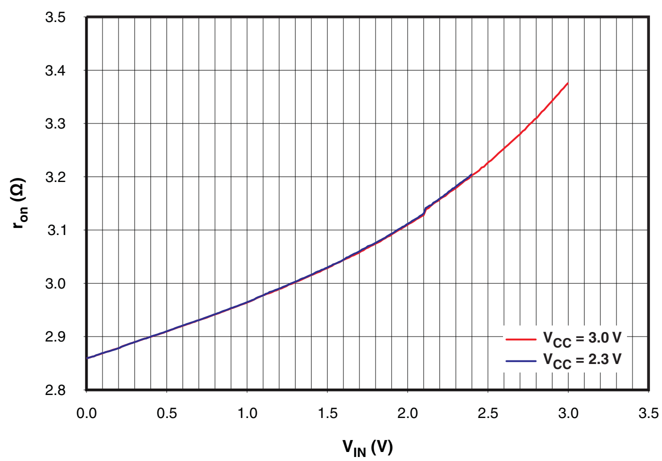


Figure 5. r_{on} vs V_{IN} (I_{OUT} = –15 mA)

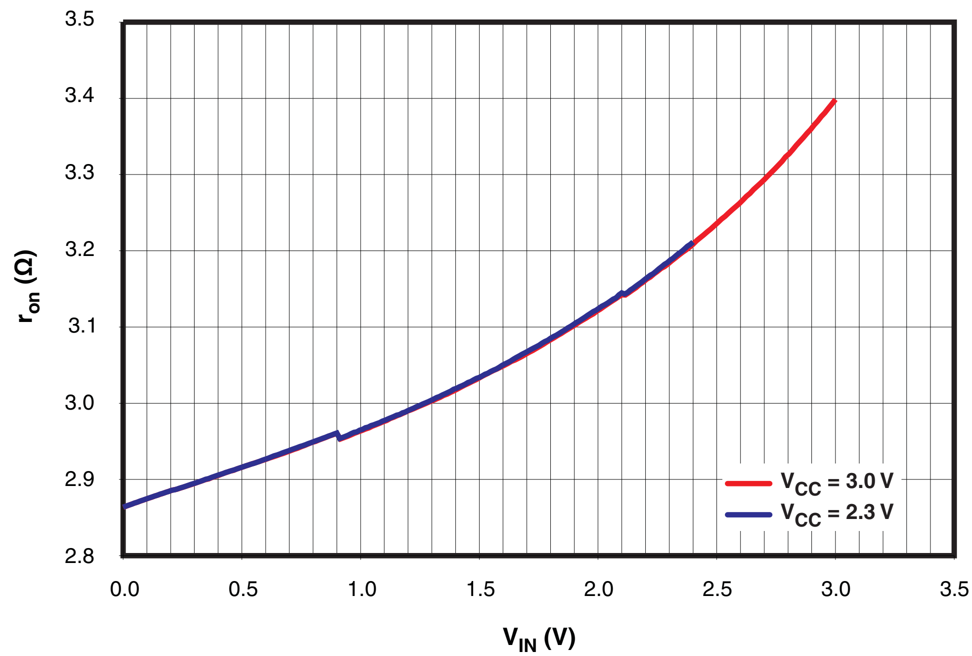


Figure 6. r_{on} vs V_{IN} (I_{OUT} = –30 mA)

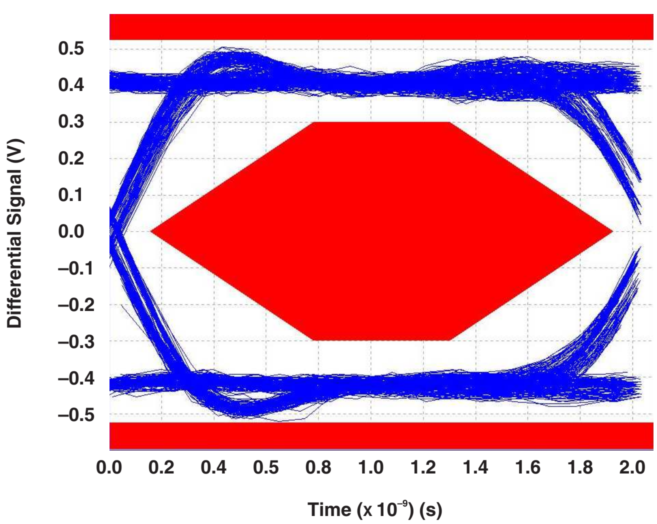


Figure 7. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

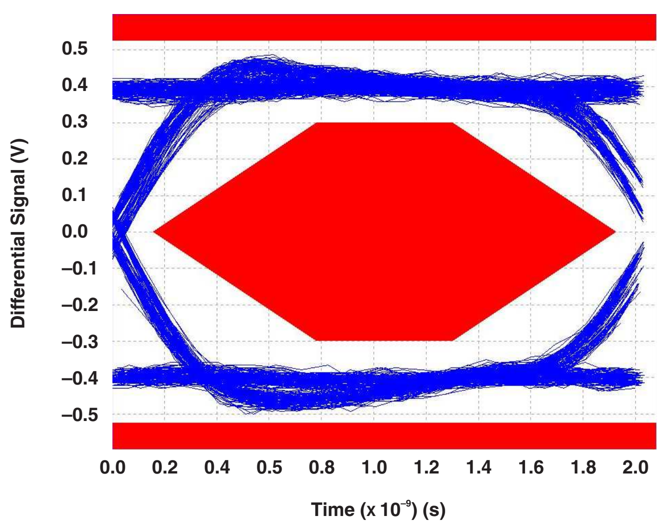


Figure 8. Eye Pattern: 480-Mbps USB Signal With Switch 1D Path

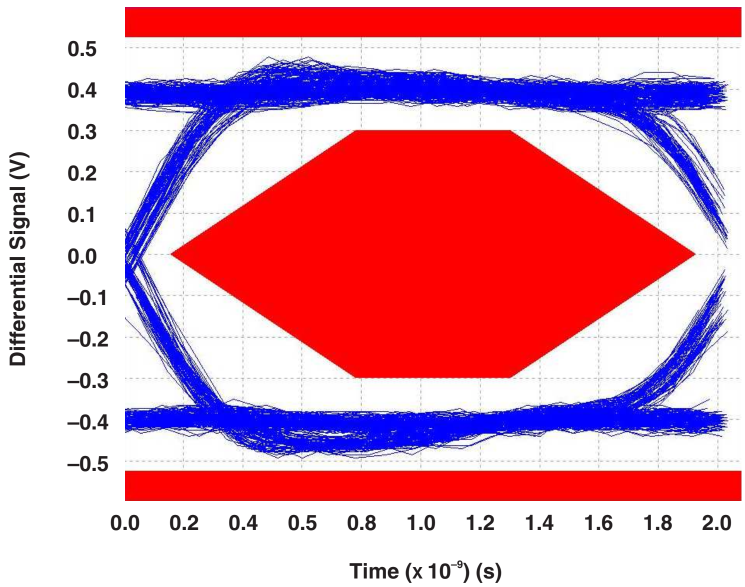
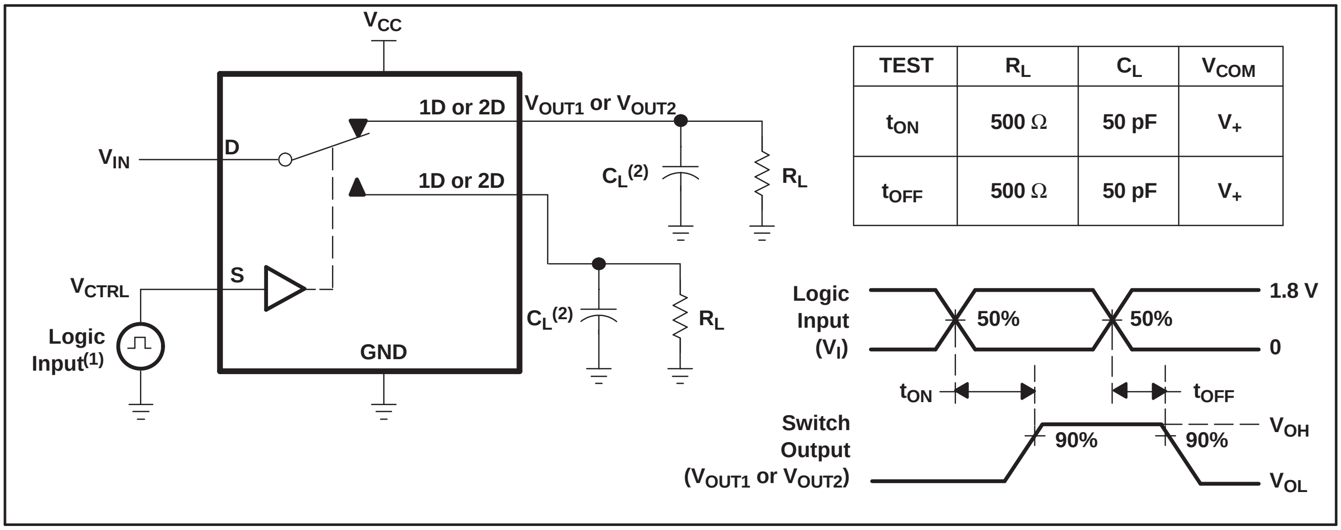


Figure 9. Eye Pattern: 480-Mbps USB Signal With Switch 2D Path

PARAMETER MEASUREMENT INFORMATION



TEST	R_L	C_L	V_{COM}
t_{ON}	500 Ω	50 pF	V_+
t_{OFF}	500 Ω	50 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 10. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

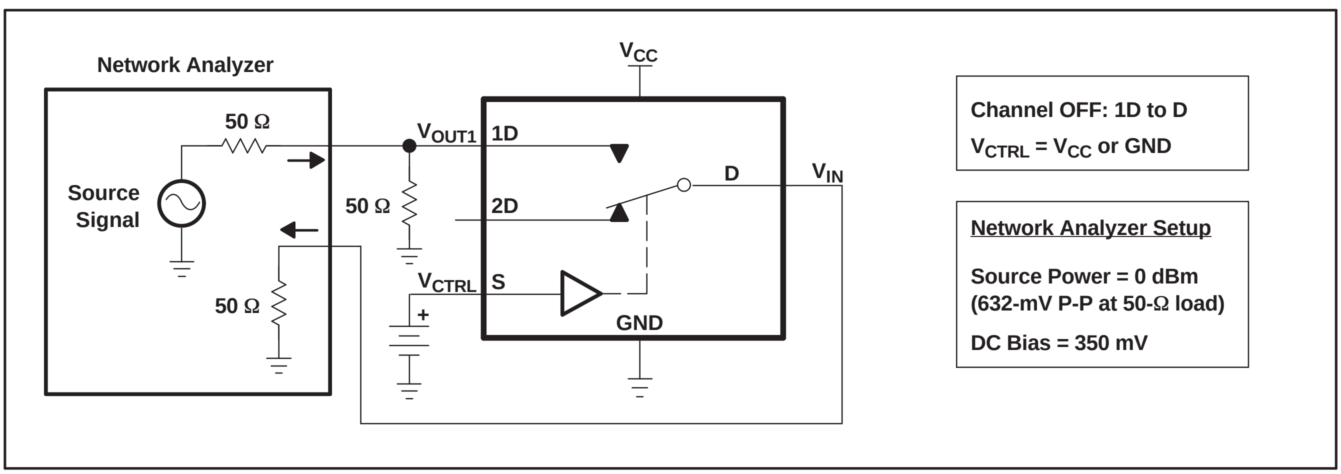


Figure 11. OFF Isolation (O_{ISO})

PARAMETER MEASUREMENT INFORMATION (continued)

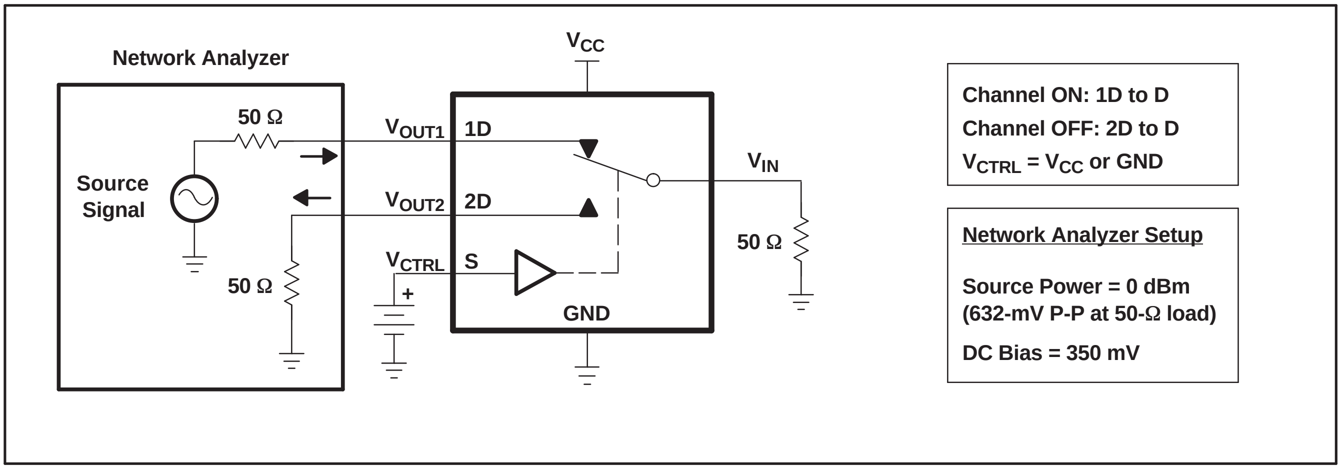


Figure 12. Crosstalk (X_{TALK})

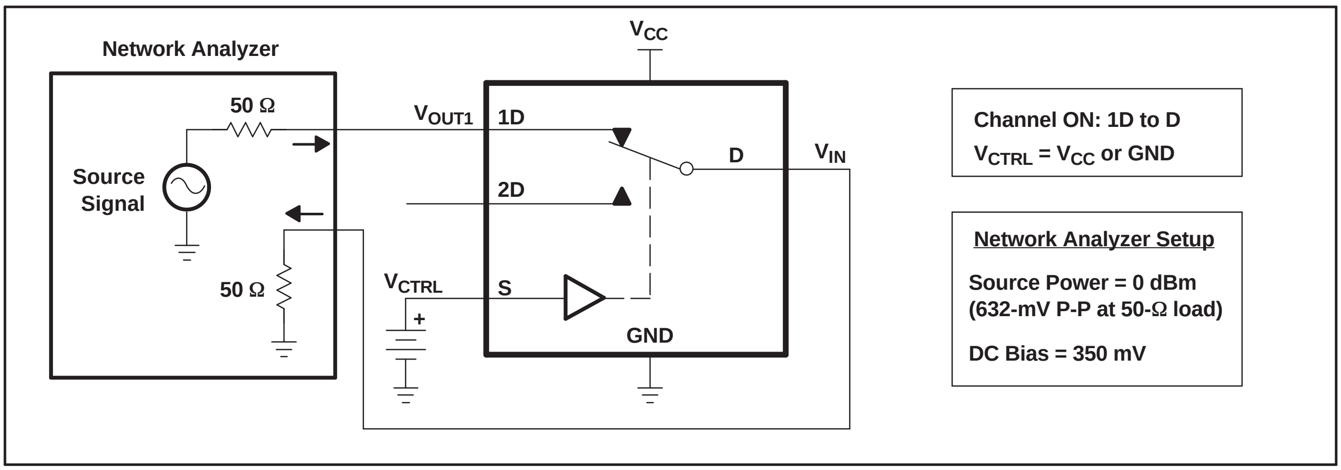


Figure 13. Bandwidth (BW)

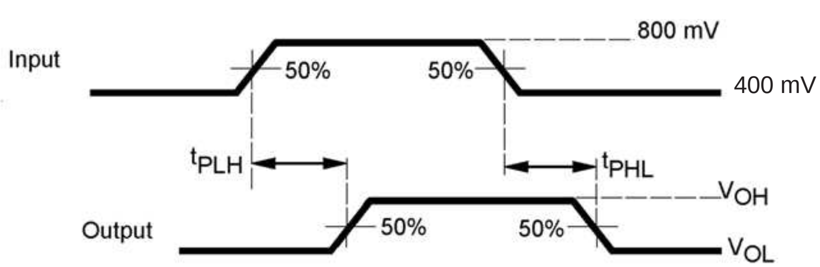


Figure 14. Propagation Delay

PARAMETER MEASUREMENT INFORMATION (continued)

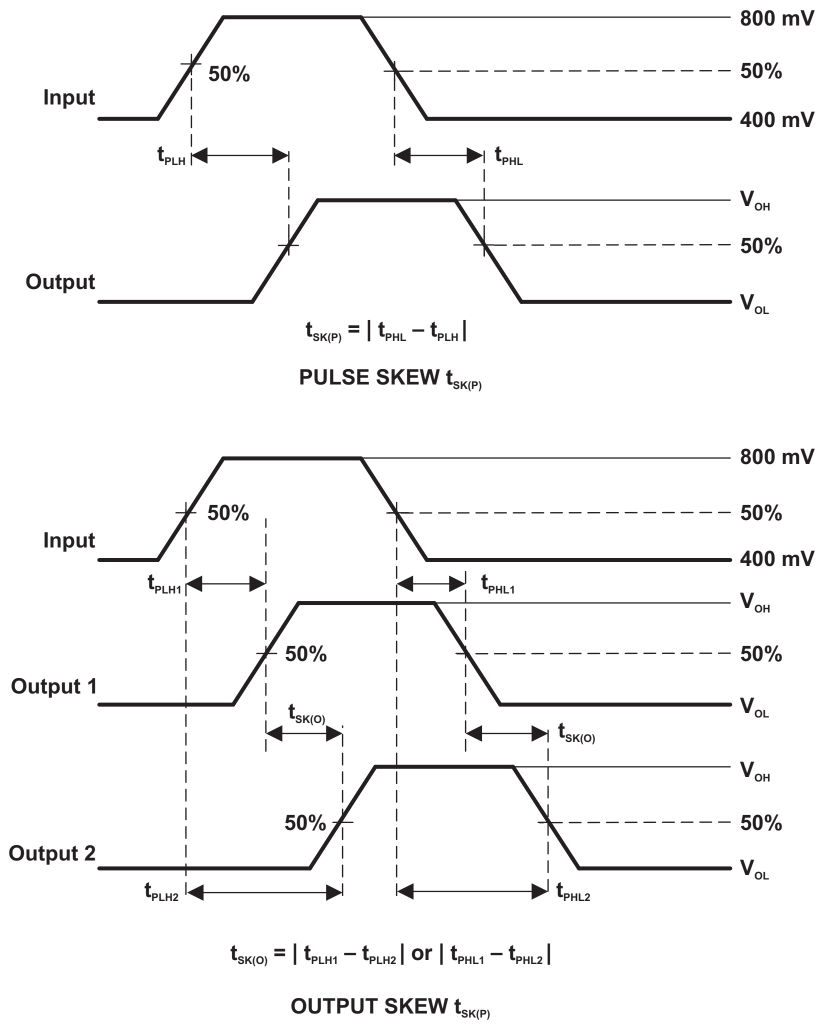


Figure 15. Skew Test

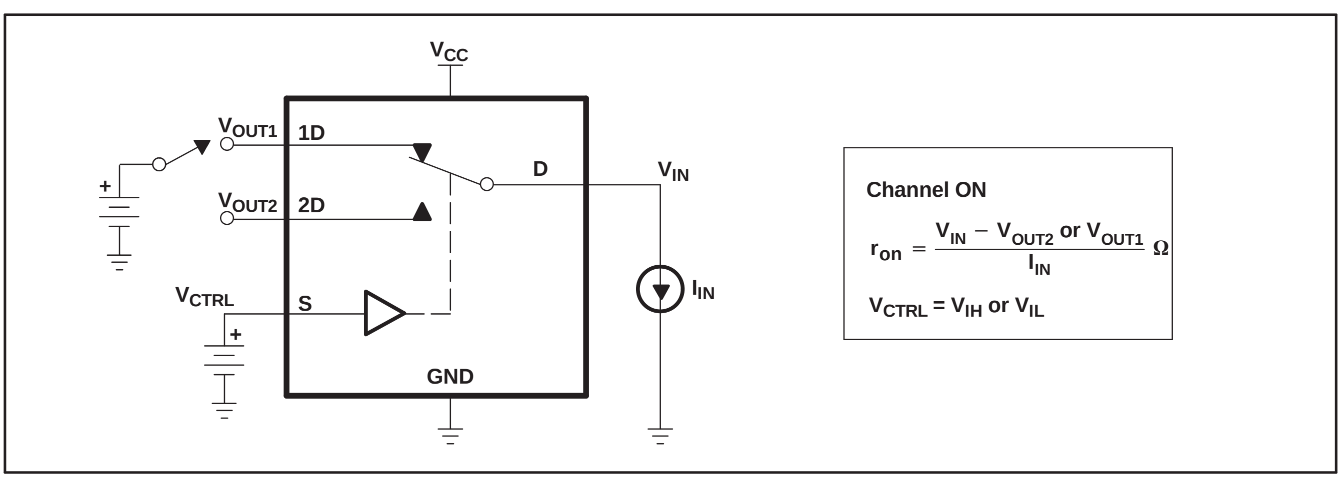


Figure 16. ON-State Resistance (r_{on})

PARAMETER MEASUREMENT INFORMATION (continued)

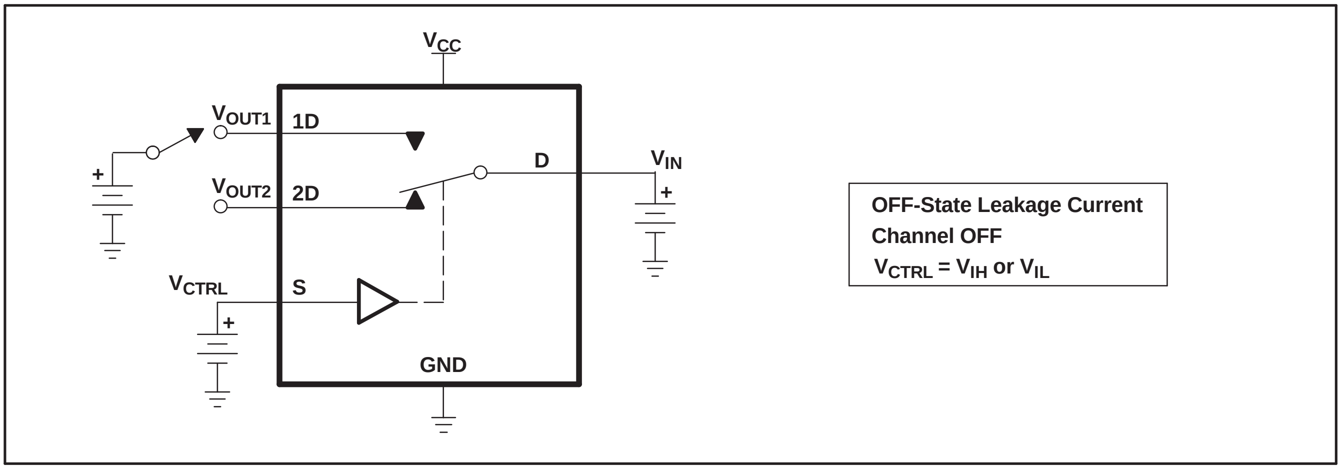


Figure 17. OFF-State Leakage Current

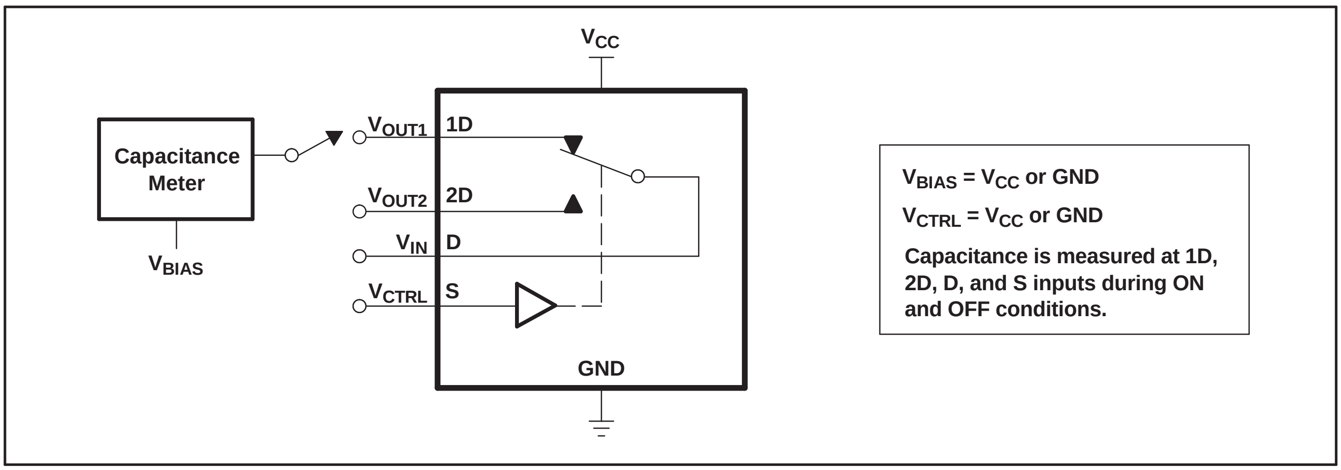


Figure 18. Capacitance

REVISION HISTORY

Changes from Revision A (February 2010) to Revision B	Page
• Update TOP-SIDE MARKING for RSE package.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS3USB221EDRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVM	Samples
TS3USB221ERSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(LGO ~ LGR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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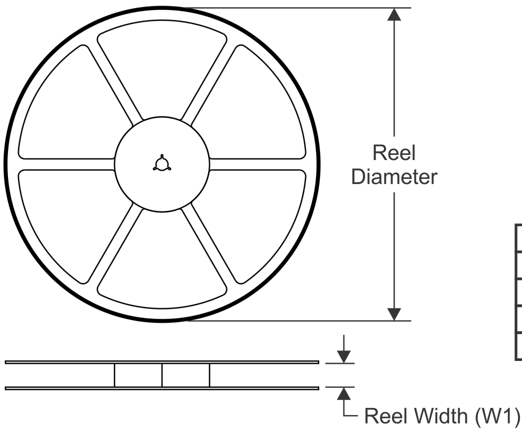
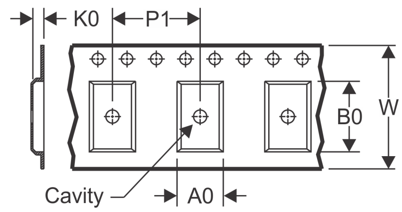
TAPE AND REEL INFORMATION

REEL DIMENSIONS

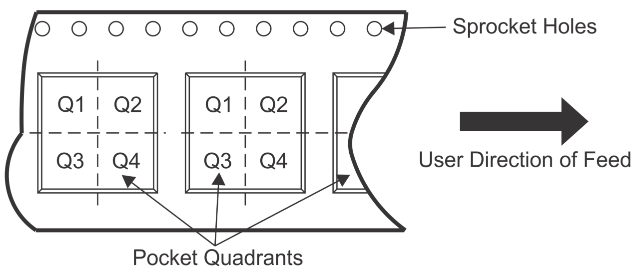


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

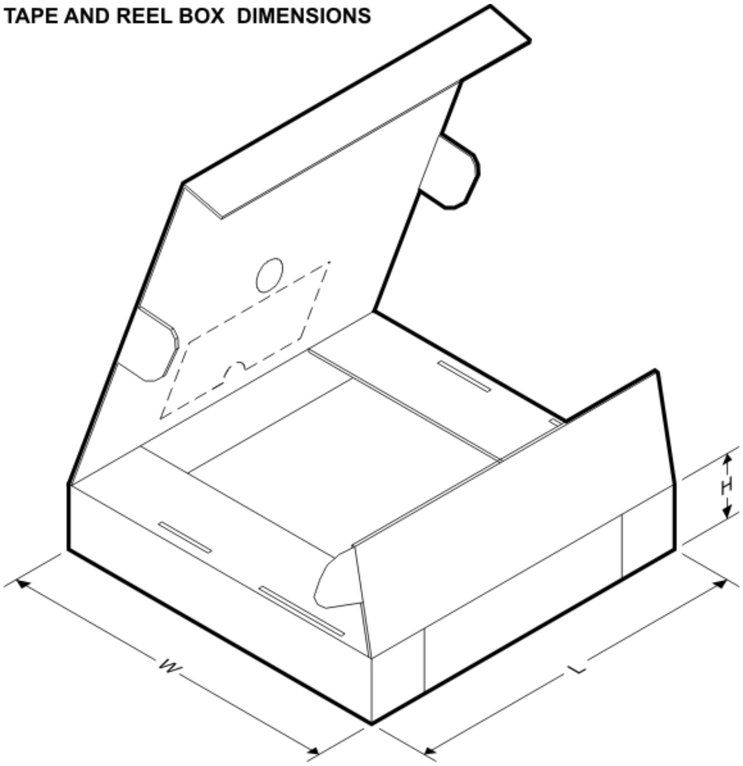
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221EDRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3USB221ERSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
TS3USB221ERSER	UQFN	RSE	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

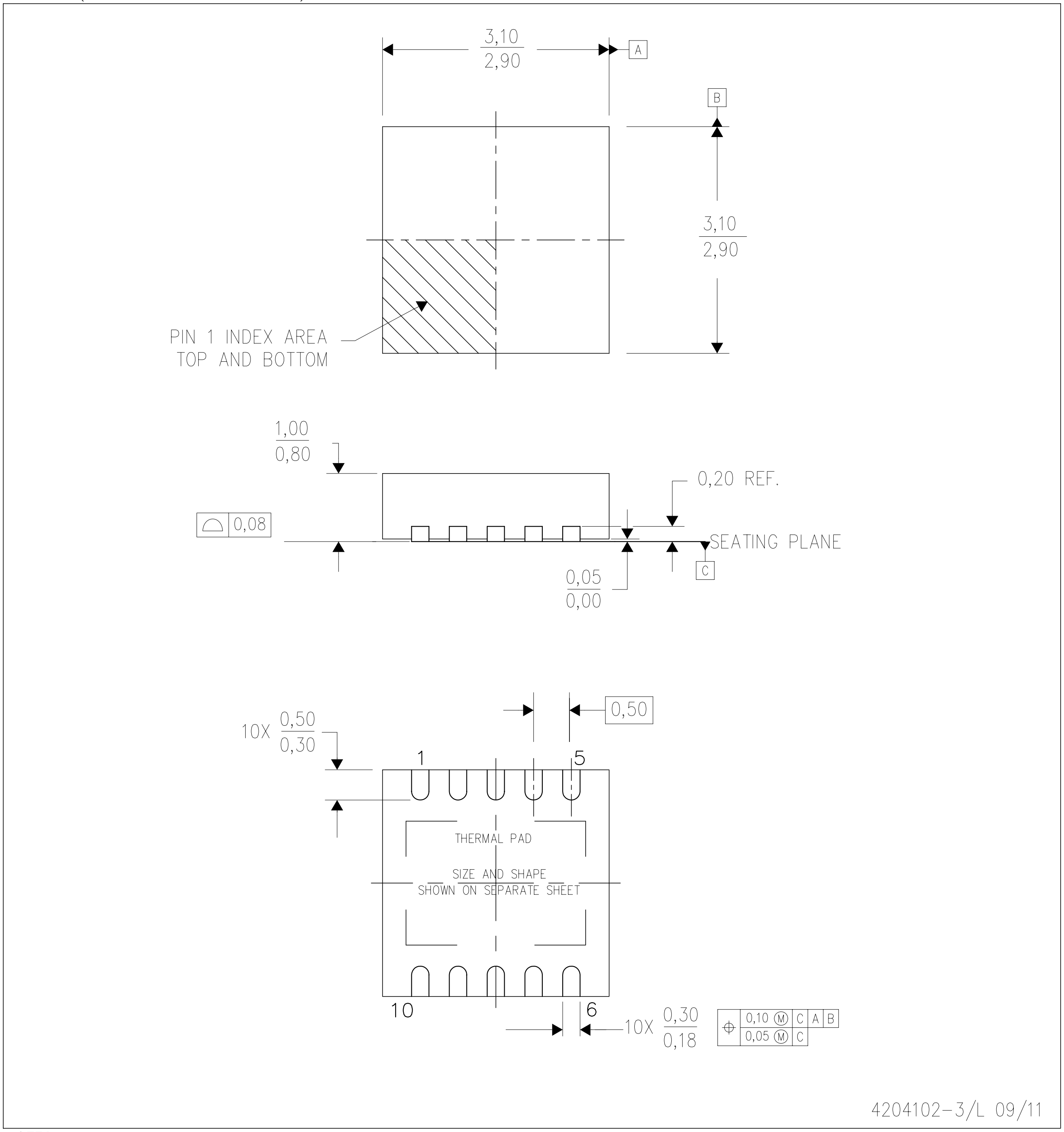
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221EDRCR	SON	DRC	10	3000	367.0	367.0	35.0
TS3USB221ERSER	UQFN	RSE	10	3000	202.0	201.0	28.0
TS3USB221ERSER	UQFN	RSE	10	3000	203.0	203.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

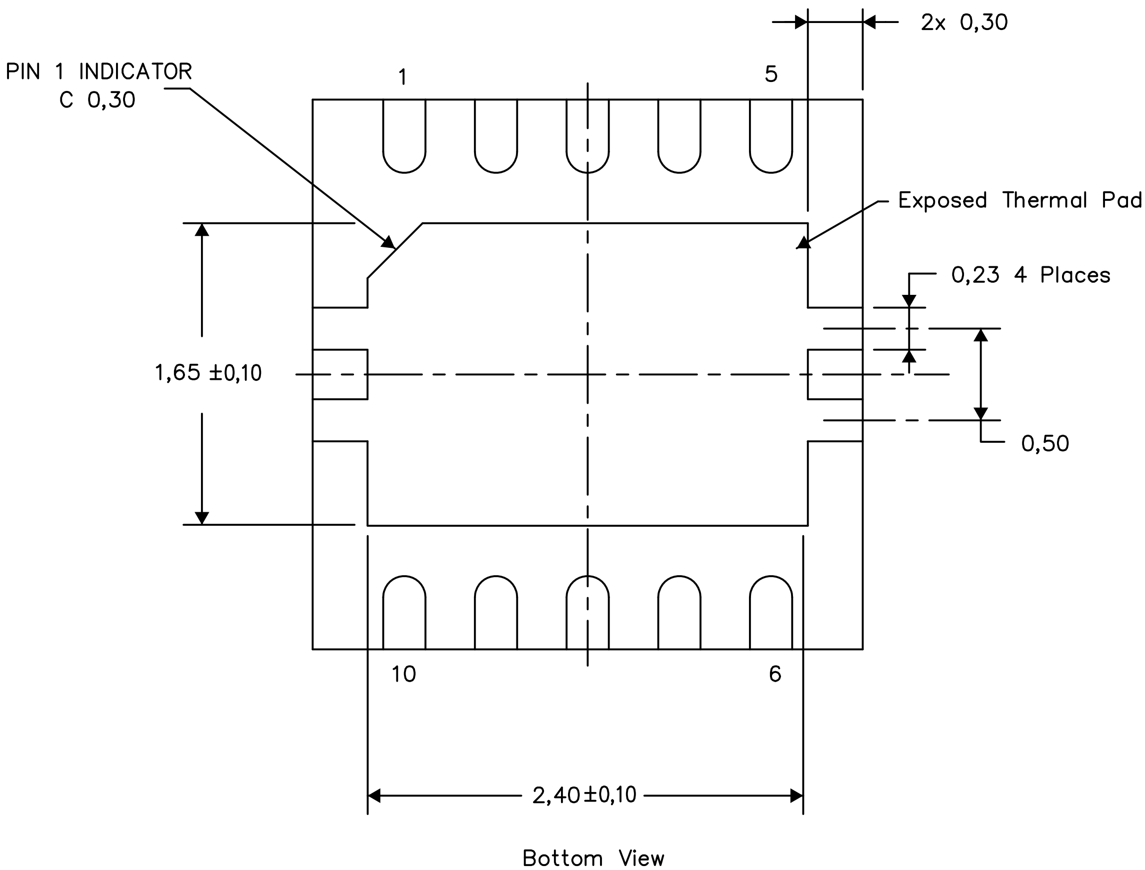
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

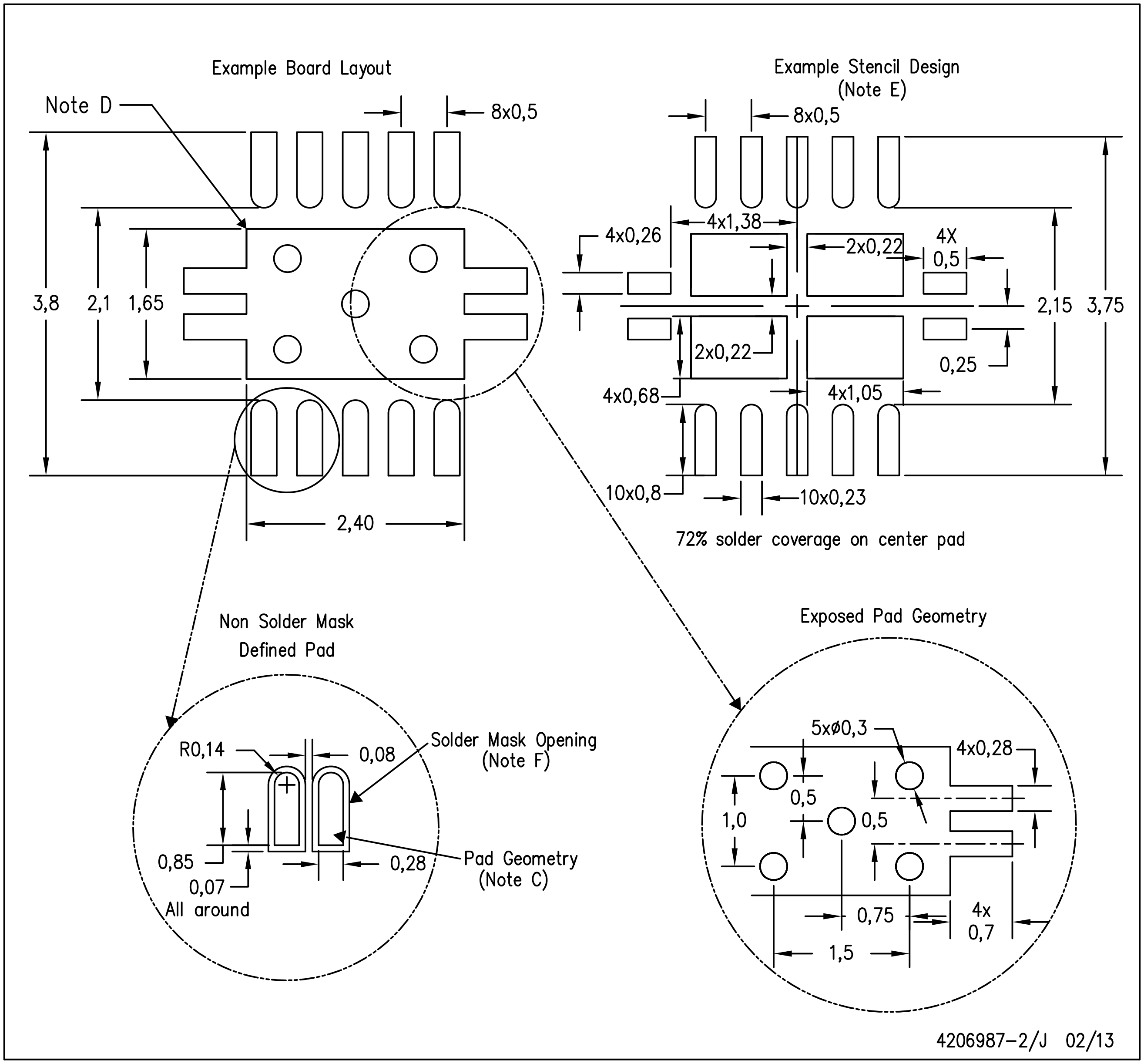


Exposed Thermal Pad Dimensions

4206565–3/R 03/13

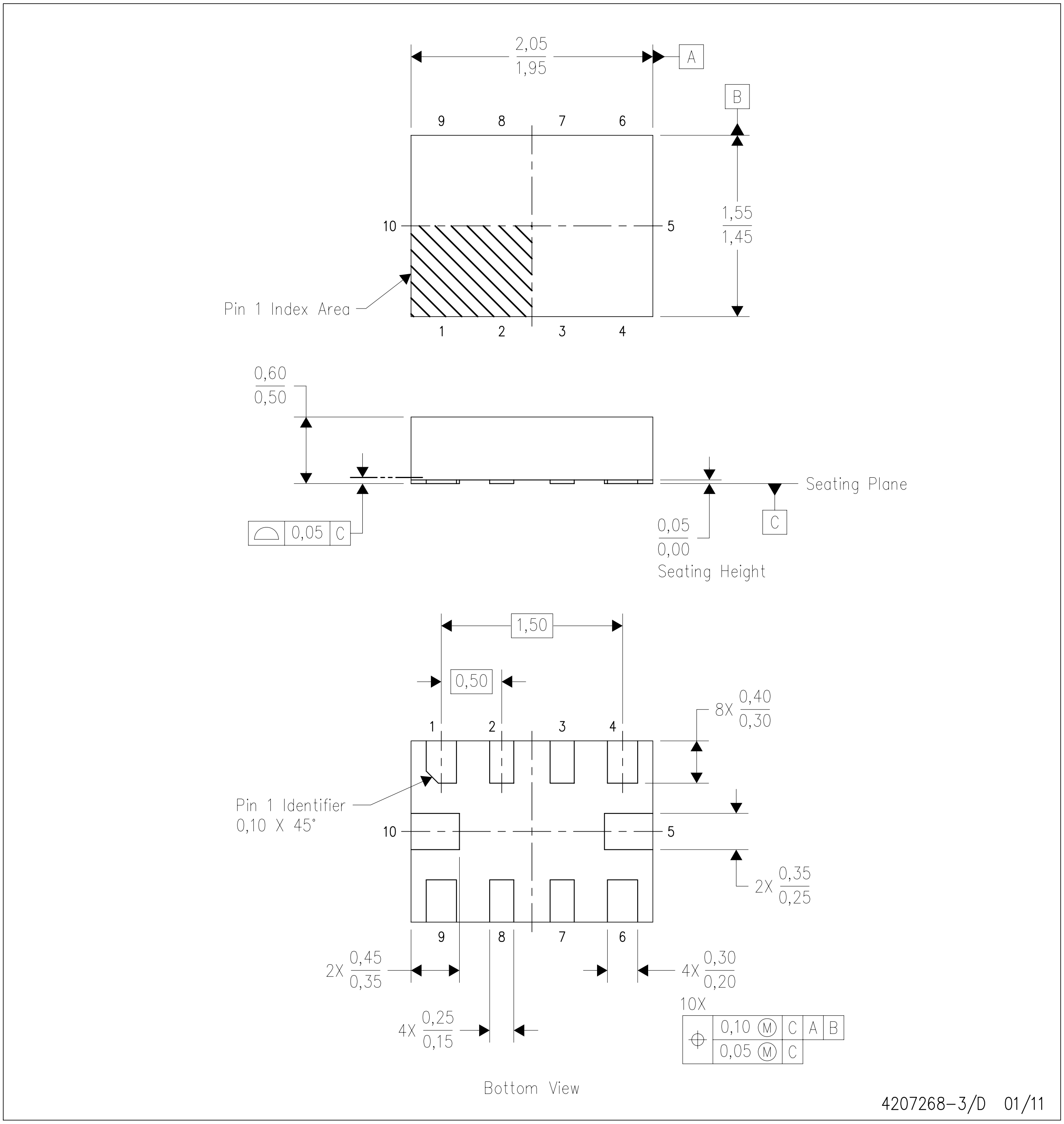
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



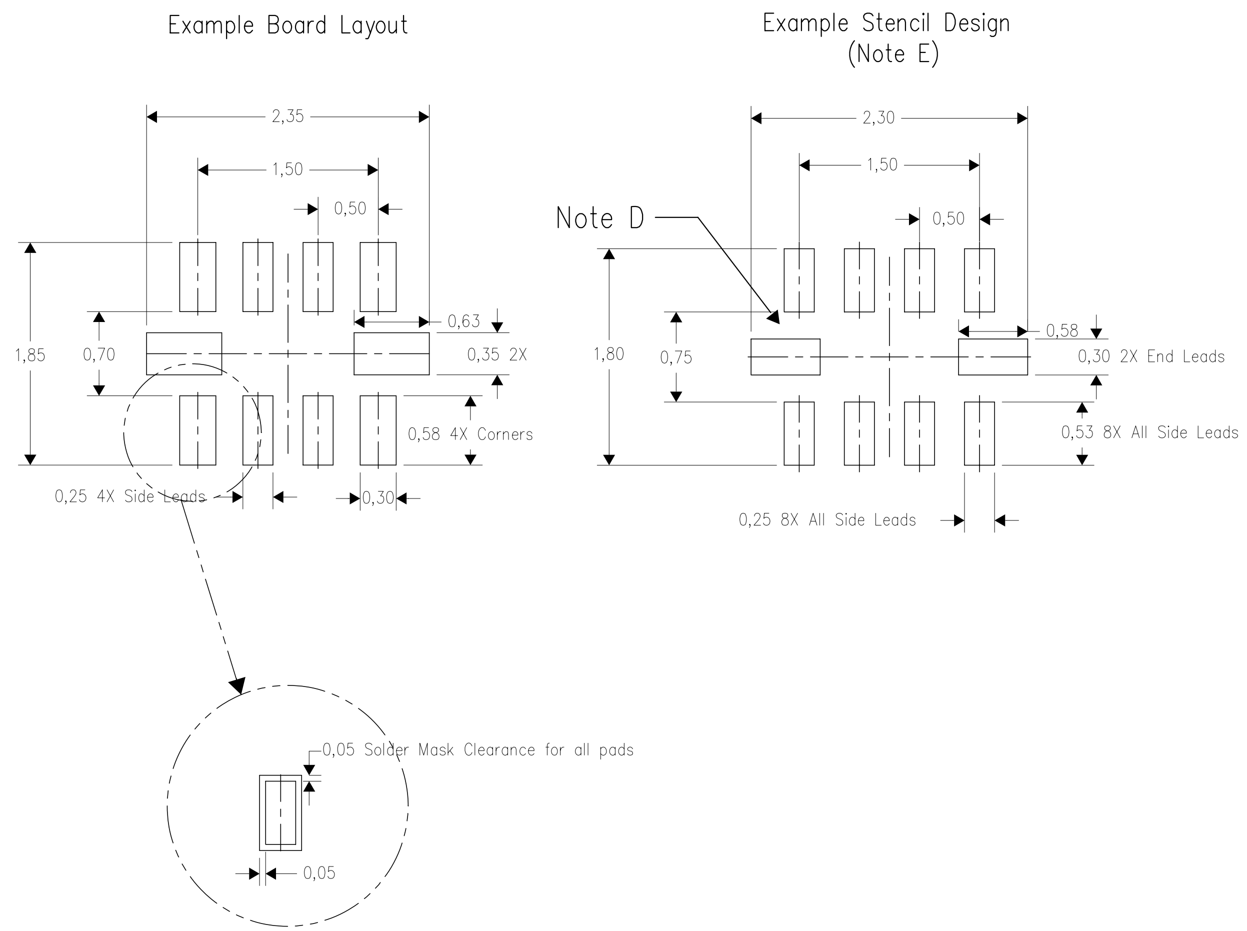
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSE (R-PUQFN-N10) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. This package complies to JEDEC MO-288 variation UEFD.

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4208106–3/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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