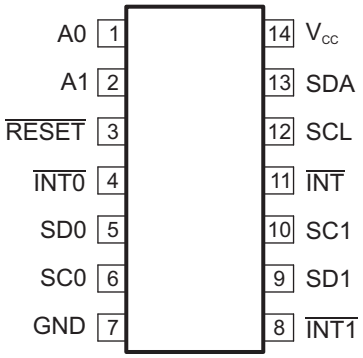
PCA9543A
TWO-CHANNEL I²C-BUS SWITCH WITH INTERRUPT LOGIC AND RESET

SCPS169–SEPTEMBER 2007

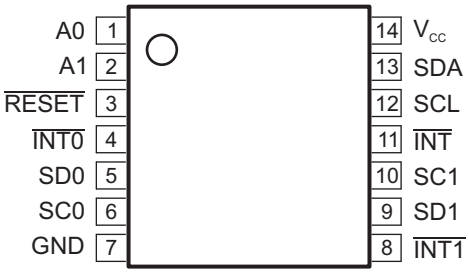
FEATURES

- 1-of-2 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Two Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Pins Allowing up to Four Devices on the I²C Bus
- Channel Selection Via I²C Bus, in Any Combination
- Power Up With All Switch Channels Deselected
- Low r_{on} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
- 5-V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD78
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The PCA9543A is a bidirectional translating switch controlled by the I²C bus. The SCL/SDA upstream pair fans out to two downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Two interrupt inputs ($\overline{INT0}$–$\overline{INT1}$), one for each of the downstream pairs, are provided. One interrupt output ($\overline{INT}$) acts as an AND of the two interrupt inputs.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 50	PCA9543AD	PCA9543A
		Reel of 2500	PCA9543ADR	
	TSSOP – PW	Tube of 90	PCA9543APW	PD543A
		Reel of 2000	PCA9543APWR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

An active-low reset ($\overline{\text{RESET}}$) input allows the PCA9543A to recover from a situation where one of the downstream I²C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage, which will be passed by the PCA9543A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pullup resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5-V tolerant.

TERMINAL FUNCTIONS

D AND PW PIN NUMBER	NAME	DESCRIPTION
1	A0	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} through a pullup resistor, if not used.
4	$\overline{\text{INT0}}$	Active-low interrupt input 0. Connect to V_{CC} through a pullup resistor.
5	SD0	Serial data 0. Connect to V_{CC} through a pullup resistor.
6	SC0	Serial clock 0. Connect to V_{CC} through a pullup resistor.
7	GND	Ground
8	$\overline{\text{INT1}}$	Active-low interrupt input 1. Connect to V_{CC} through a pullup resistor.
9	SD1	Serial data 1. Connect to V_{CC} through a pullup resistor.
10	SC1	Serial clock 1. Connect to V_{CC} through a pullup resistor.
11	$\overline{\text{INT}}$	Active-low interrupt output. Connect to V_{CC} through a pullup resistor.
12	SCL	Serial clock line. Connect to V_{CC} through a pullup resistor.
13	SDA	Serial data line. Connect to V_{CC} through a pullup resistor.
14	V_{CC}	Supply power

BLOCK DIAGRAM

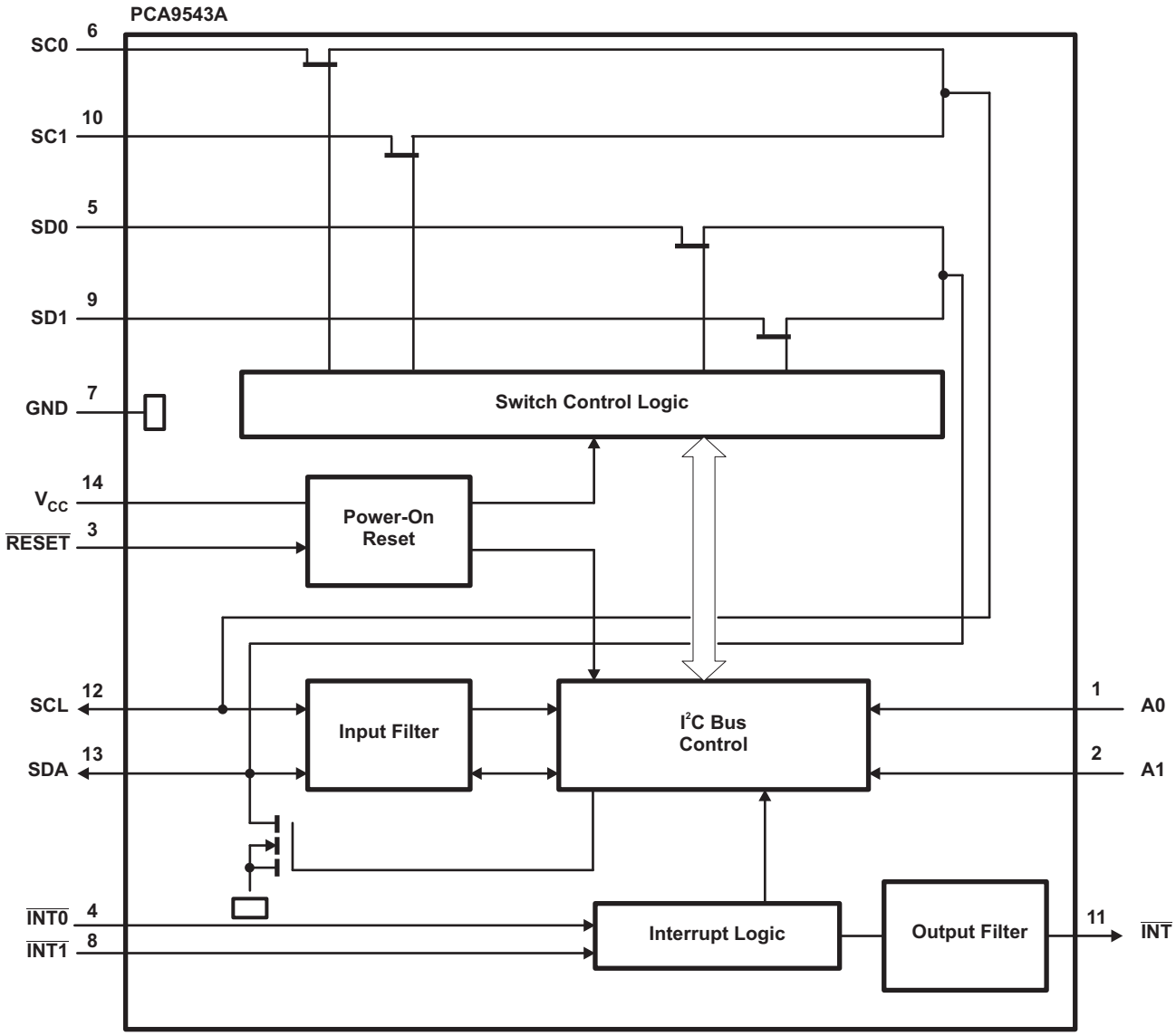


Figure 1. Block Diagram

Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the PCA9543A is shown in Figure 2. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins and they must be pulled high or low.

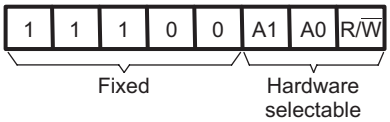


Figure 2. Slave Address PCA9543A

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

Control Register

Following the successful acknowledgement of the slave address, the bus master sends a byte to the PCA9543A, which is stored in the control register (see Figure 3). If multiple bytes are received by the PCA9543A, it saves the last byte received. This register can be written and read via the I²C bus.

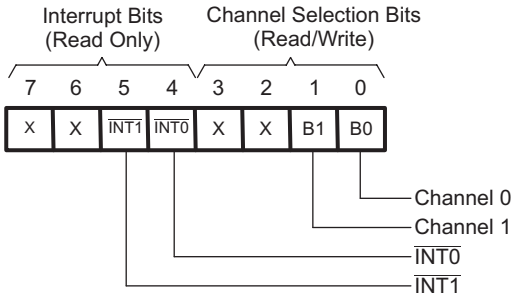


Figure 3. Control Register

Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the PCA9543A has been addressed, the control register is written. The two LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I²C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Channel 0 and channel 1 can be enabled at the same time. Care should be taken not to exceed the maximum bus capacitance.

Interrupt Handling

The PCA9543A provides two interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the PCA9543A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bit 4 and Bit 5 of the control register correspond to the $\overline{INT0}$ and $\overline{INT1}$ inputs of the PCA9543A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the PCA9543A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the PCA9543A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC} through a pullup resistor.

Table 2. Control Register Read (Interrupt)(1)

D7	D6	$\overline{INT1}$	$\overline{INT0}$	D3	D2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
0	0	0	0	0	0	0	0	No channel selected; power-up/reset default state

(1) Two interrupts can be active at the same time.

$\overline{RESET}$ Input

The $\overline{RESET}$ input can be used to recover the PCA9543A from a bus-fault condition. The registers and the I²C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. All channels also are deselected in this case. $\overline{RESET}$ must be connected to V_{CC} through a pullup resistor.

Power-On Reset

When power is applied to V_{CC}, an internal power-on reset holds the PCA9543A in a reset condition until V_{CC} has reached V_{POR}. At this point, the reset condition is released and the PCA9543A registers and I²C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

Voltage Translation

The pass-gate transistors of the PCA9543A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I²C bus to another.

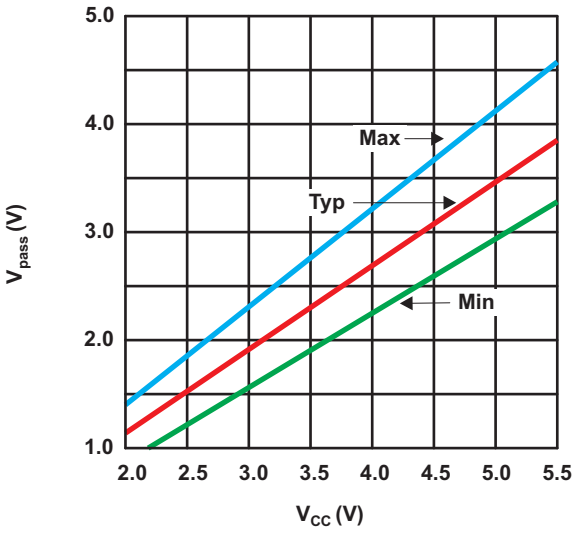


Figure 4. V_{pass} Voltage vs V_{CC}

Figure 4 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Electrical Characteristics section of this data sheet). In order for the PCA9543A to act as a voltage translator, the V_{pass} voltage should be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 4, $V_{pass(max)}$ is at 2.7 V when the PCA9543A supply voltage is 3.5 V or lower, so the PCA9543A supply voltage could be set to 3.3 V. Pullup resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 14).

I²C Interface

The I²C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time is interpreted as control signals (see Figure 5).

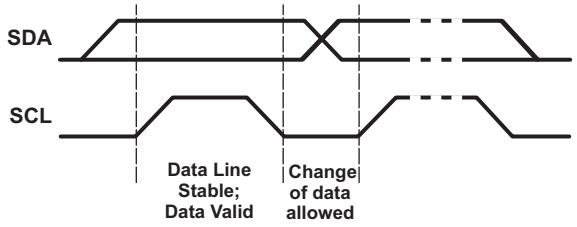


Figure 5. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 6).

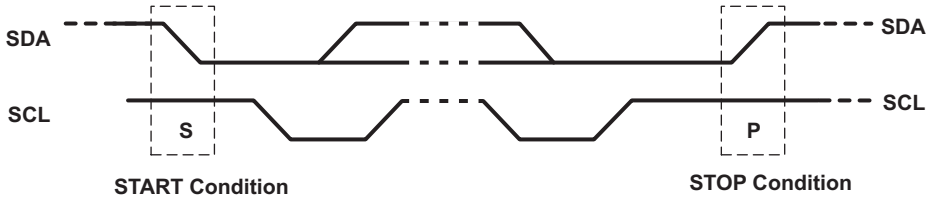


Figure 6. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices that are controlled by the master are the slaves (see Figure 7).

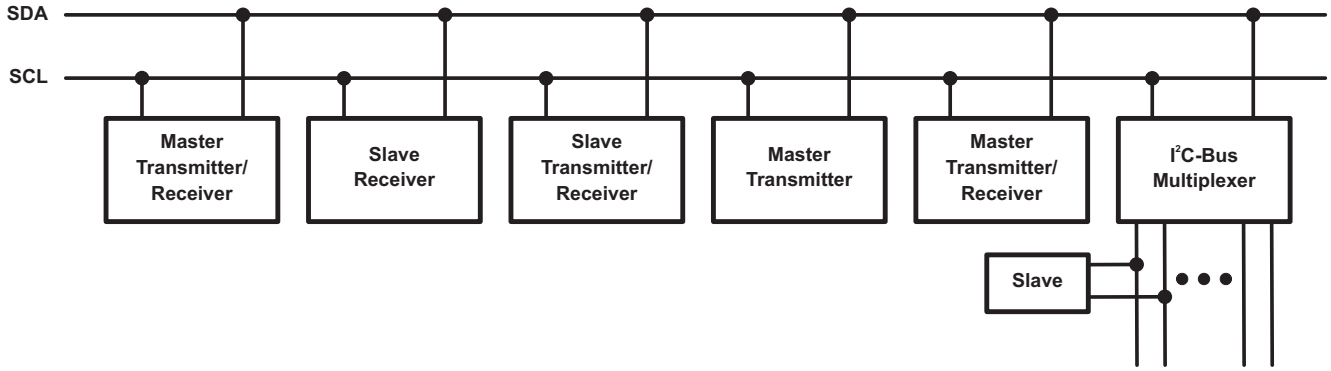


Figure 7. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 8). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

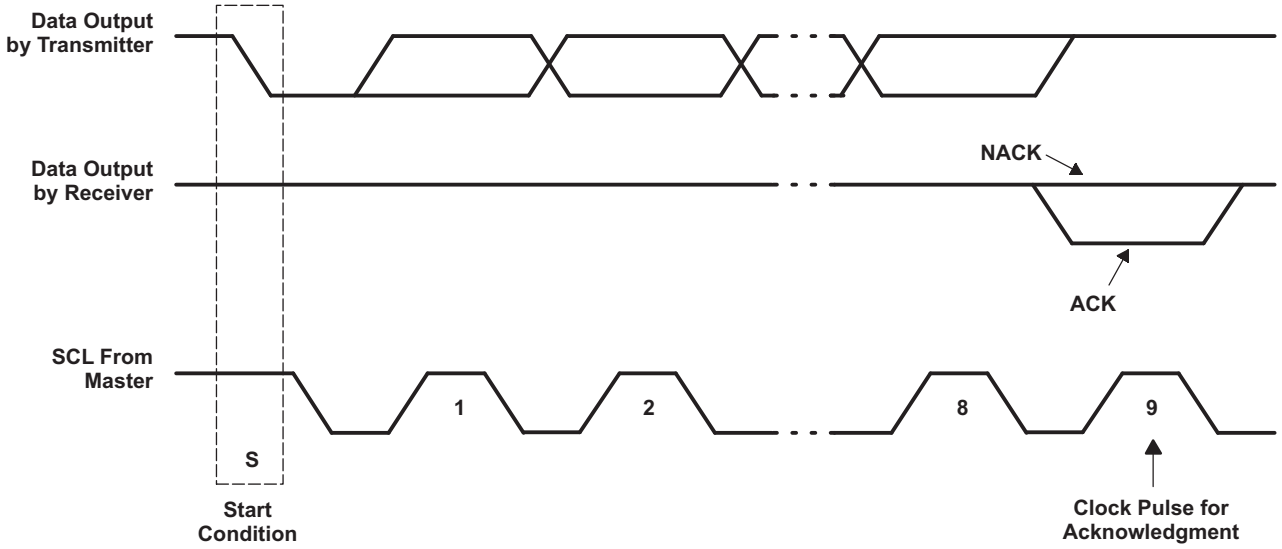


Figure 8. Acknowledgment on I²C Bus

Data is transmitted to the PCA9543A control register using the write mode shown in Figure 9.

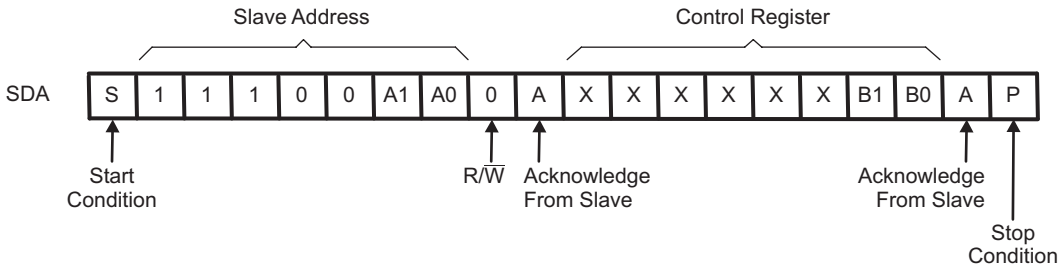


Figure 9. Write Control Register

Data is read from the PCA9543A control register using the read mode shown in Figure 10.

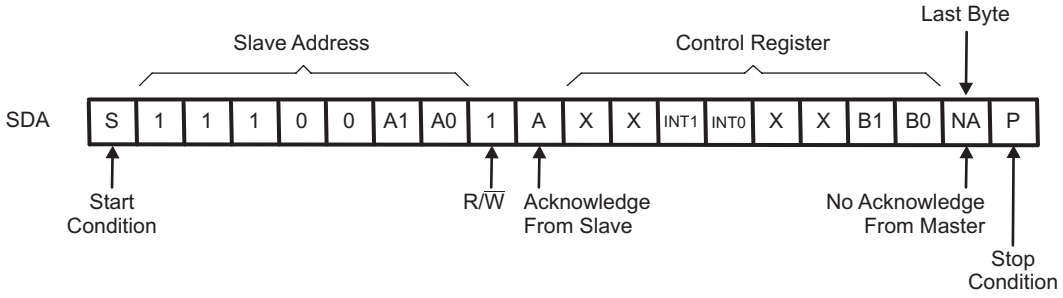


Figure 10. Read Control Register

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
I_I	Input current			±20	mA
I_O	Output current			±25	mA
	Continuous current through V_{CC}			±100	mA
	Continuous current through GND			±100	mA
θ_{JA}	Package thermal impedance(3)	D package		86	°C/W
		PW package		113	
P_{tot}	Total power dissipation			400	mW
T_{stg}	Storage temperature range		–60	150	°C
T_A	Operating free-air temperature range		–40	85	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA		$0.7 \times V_{CC}$	6	V
		A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$	V_{CC} = 2.3 V to 3.6 V	$0.7 \times V_{CC}$	V_{CC} + 0.5	
			V_{CC} = 3.6 V to 4.5 V	$0.7 \times V_{CC}$	V_{CC} + 0.5	
			V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA		–0.5	$0.3 \times V_{CC}$	V
		A1, A0, $\overline{INT1}$, $\overline{INT0}$, $\overline{RESET}$		–0.5	$0.3 \times V_{CC}$	
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{POR}	Power-on reset voltage		No load: $V_I = V_{CC}$ or GND(2)	V_{POR}		1.6	2.1	V
V_{pass}	Switch output voltage		$V_{SWin} = V_{CC}$, $I_{SWout} = -100$ µA	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.5		
				2.3 V to 2.7 V	1.1		2	
I_{OH}	$\overline{INT}$		$V_O = V_{CC}$	2.3 V to 5.5 V			100	µA
I_{OL}	SDA		V_{OL} = 0.4 V	2.3 V to 5.5 V	3	7		mA
			V_{OL} = 0.6 V		6	10		
	$\overline{INT}$		V_{OL} = 0.4 V		3			
I_I	SCL, SDA		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V	–1		1	µA
	SC1–SC0, SD1–SD0		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
				4.5 V to 5.5 V	–1		100	
	A1, A0		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
				4.5 V to 5.5 V	–1		50	
	$\overline{INT1}$–$\overline{INT0}$		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
				4.5 V to 5.5 V	–1		50	
	$\overline{RESET}$		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V	–1		1	
				4.5 V to 5.5 V	–1		50	
I_{CC}	Operating mode	f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		17	50	µA
				3.6 V		6	20	
				2.7 V		3	16	
	Standby mode	Low inputs	V_I = GND, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
		High inputs	$V_I = V_{CC}$, $I_O = 0$	5.5 V		0.3	1	
				3.6 V		0.1	1	
				2.7 V		0.1	1	
ΔI_{CC}	Supply-current change	$\overline{INT1}$–$\overline{INT0}$	One $\overline{INT1}$–$\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V		8	20	µA
			One $\overline{INT1}$–$\overline{INT0}$ input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	20	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND			8	20	
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND			8	20	
C_i	A1, A0		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V		4	5	pF
				4.5 V to 5.5 V		4	5	
	$\overline{INT1}$–$\overline{INT0}$		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V		4	6	
				4.5 V to 5.5 V		4	6	
	$\overline{RESET}$		$V_I = V_{CC}$ or GND	2.3 V to 3.6 V		4	5	
				4.5 V to 5.5 V		4	5	
	SCL		$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		9	12	

(1) For operation between published voltage ranges, refer to the worst-case parameter in both ranges.
(2) To reset the part, either $\overline{RESET}$ must be low or V_{CC} must be lowered to 0.2 V.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{io(OFF)}$ (3)	SDA	V_I = V_{CC} or GND, Switch OFF	2.3 V to 5.5 V		11	13	pF
	SC1–SC0, SD1–SD0				6	8	
r_{on}	Switch on-state resistance	V_O = 0.4 V, I_O = 15 mA	4.5 V to 5.5 V	4	9	20	Ω
			3 V to 3.6 V	5	11	25	
		V_O = 0.4 V, I_O = 10 mA	2.3 V to 2.7 V	7	16	50	

(3) $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 11)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0 (1)		0 (1)		µs
t_{icr}	I²C input rise time			1000	20 + 0.1C_b (2)	300	ns
t_{icf}	I²C input fall time			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low) (3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high) (3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 11)

Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 13)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{iv}	Interrupt valid time (2)		$\overline{INTn}$	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time (2)		$\overline{INTn}$	$\overline{INT}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pullup resistor and 100-pF load (see Figure 13)

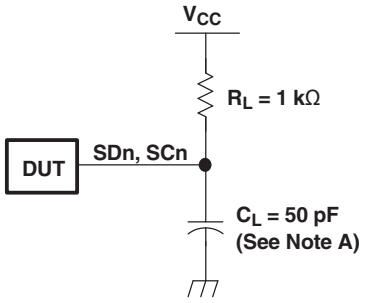
Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 13)

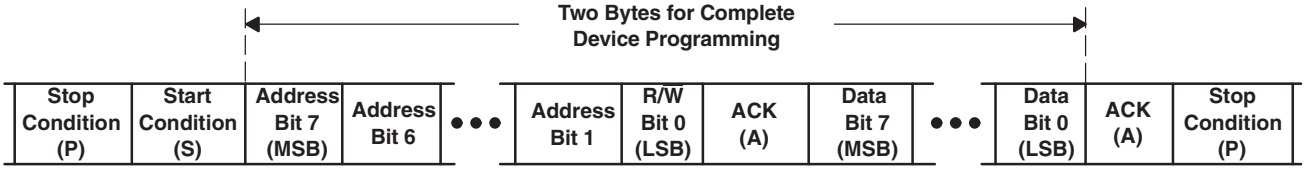
PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Required low-level pulse duration of $\overline{INTn}$ inputs (1)	1		µs
t_{PWRH}	Required high-level pulse duration of $\overline{INTn}$ inputs (1)	0.5		µs
t_{WL}	Pulse duration, $\overline{RESET}$ low	4		ns
t_{rst} (2)	$\overline{RESET}$ time (SDA clear)		500	ns
t_{REC}	Recovery time from $\overline{RESET}$ to start	0		ns

(1) The device has interrupt input rejection circuitry for pulses less than the listed minimum.
(2) t_{rst} is the propagation delay measured from the time the $\overline{RESET}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

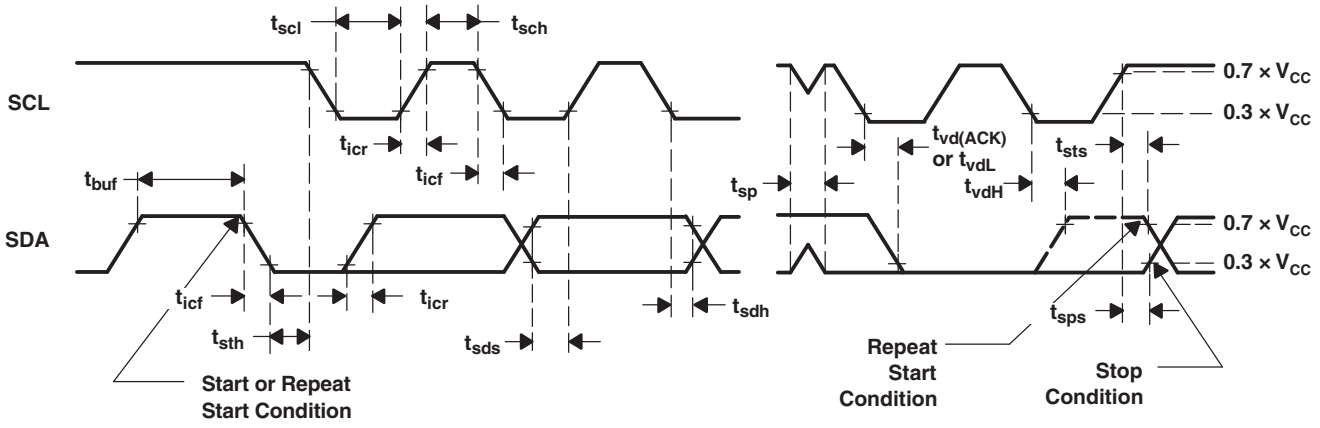
PARAMETER MEASUREMENT INFORMATION



I²C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I²C address + R/$\overline{W}$
2	Control register data



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 11. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

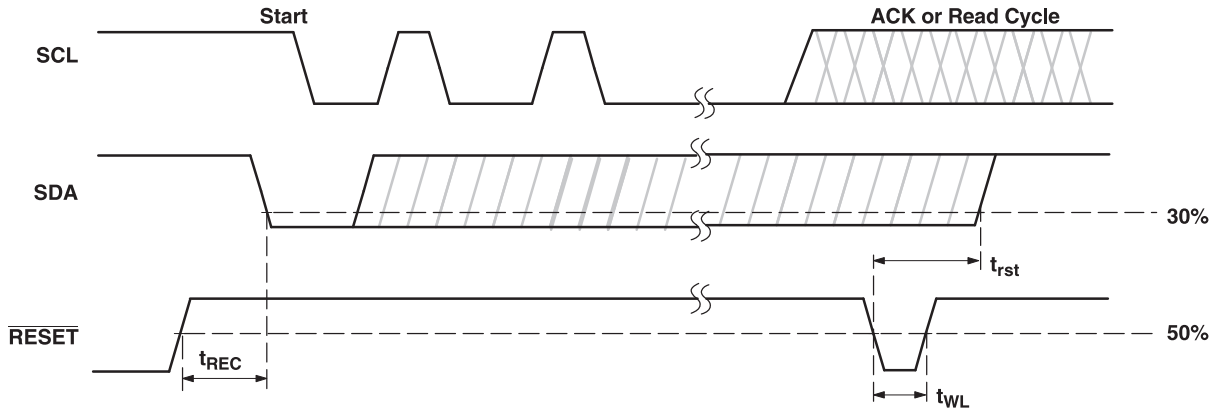
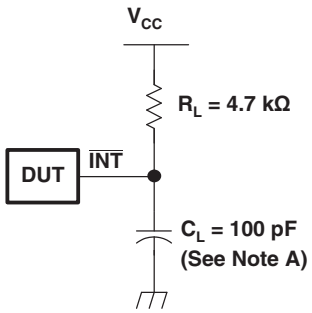
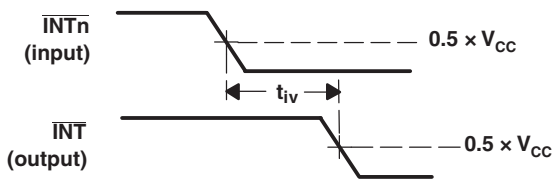


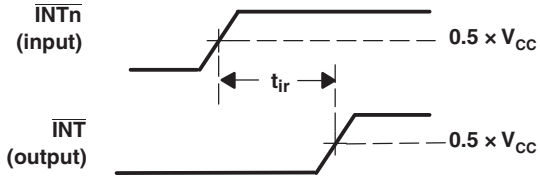
Figure 12. Reset Timing



INTERRUPT LOAD CONFIGURATION



VOLTAGE WAVEFORMS (t_{iv})



VOLTAGE WAVEFORMS (t_{ir})

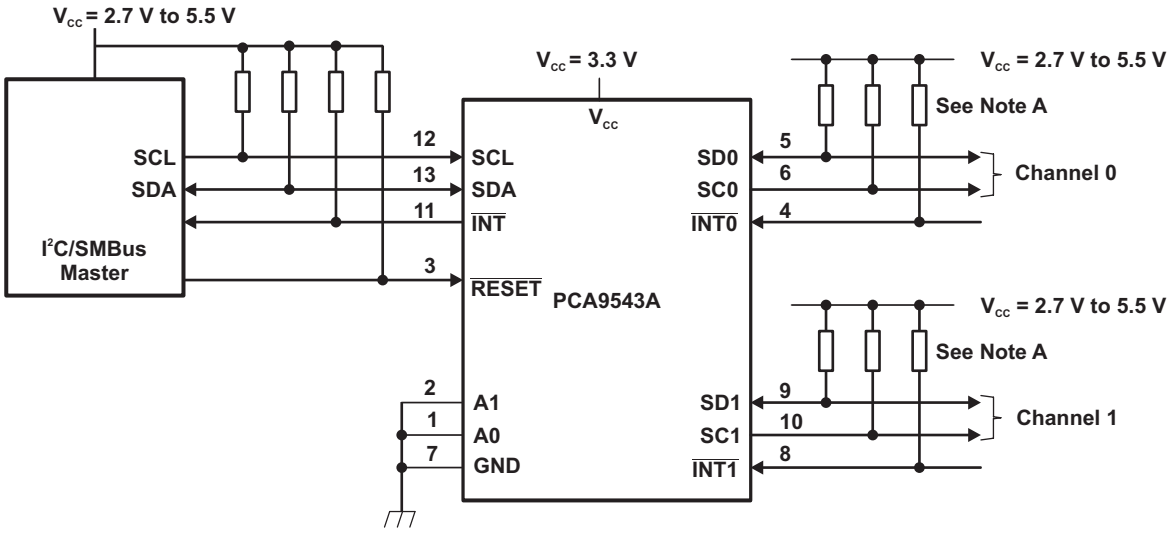
A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

Figure 13. Interrupt Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 14 shows an application in which the PCA9543A can be used.



NOTE: A. If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pullup resistor is required.
If the device generating the interrupt has a totem-pole output structure and cannot be 3-stated, a pullup resistor is not required.
The interrupt inputs should not be left floating.
B. Pin numbers shown are for the D and PW packages.

Figure 14. Typical Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
PCA9543AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9543APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

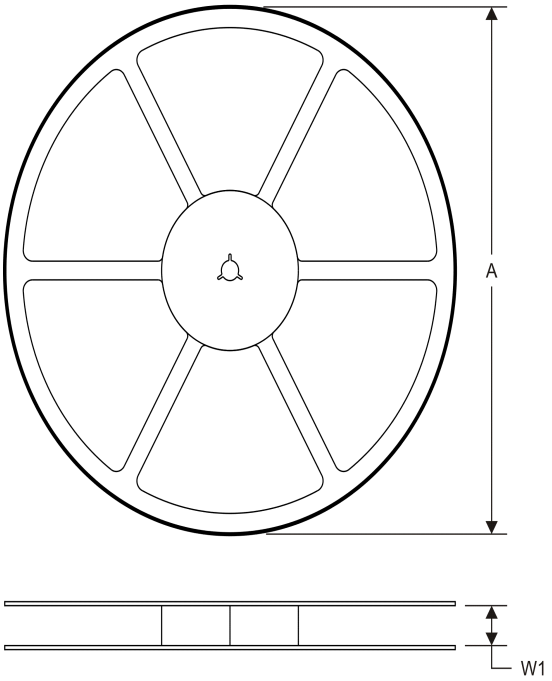
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

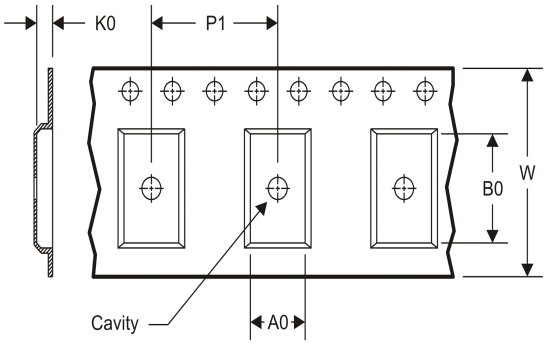
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



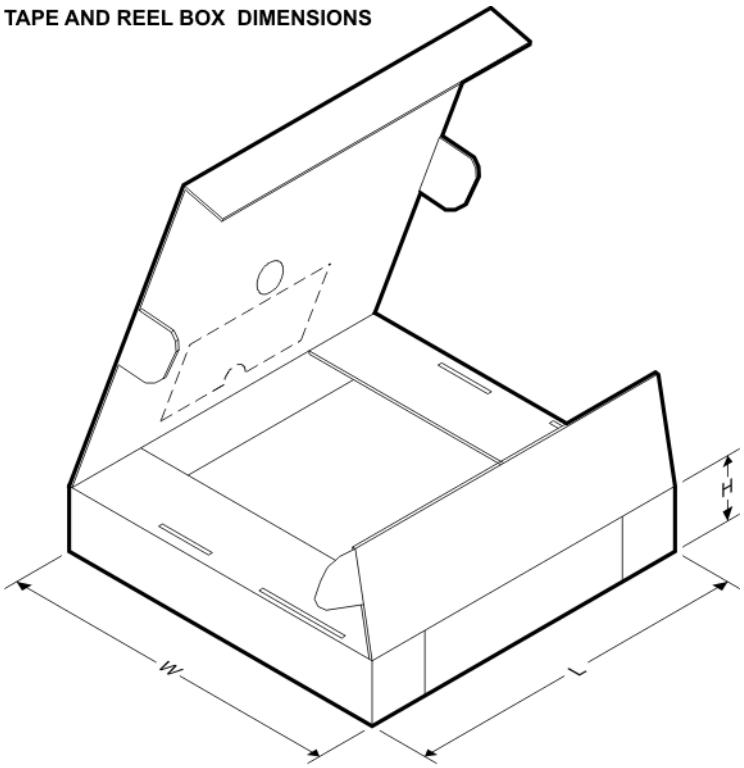
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9543APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

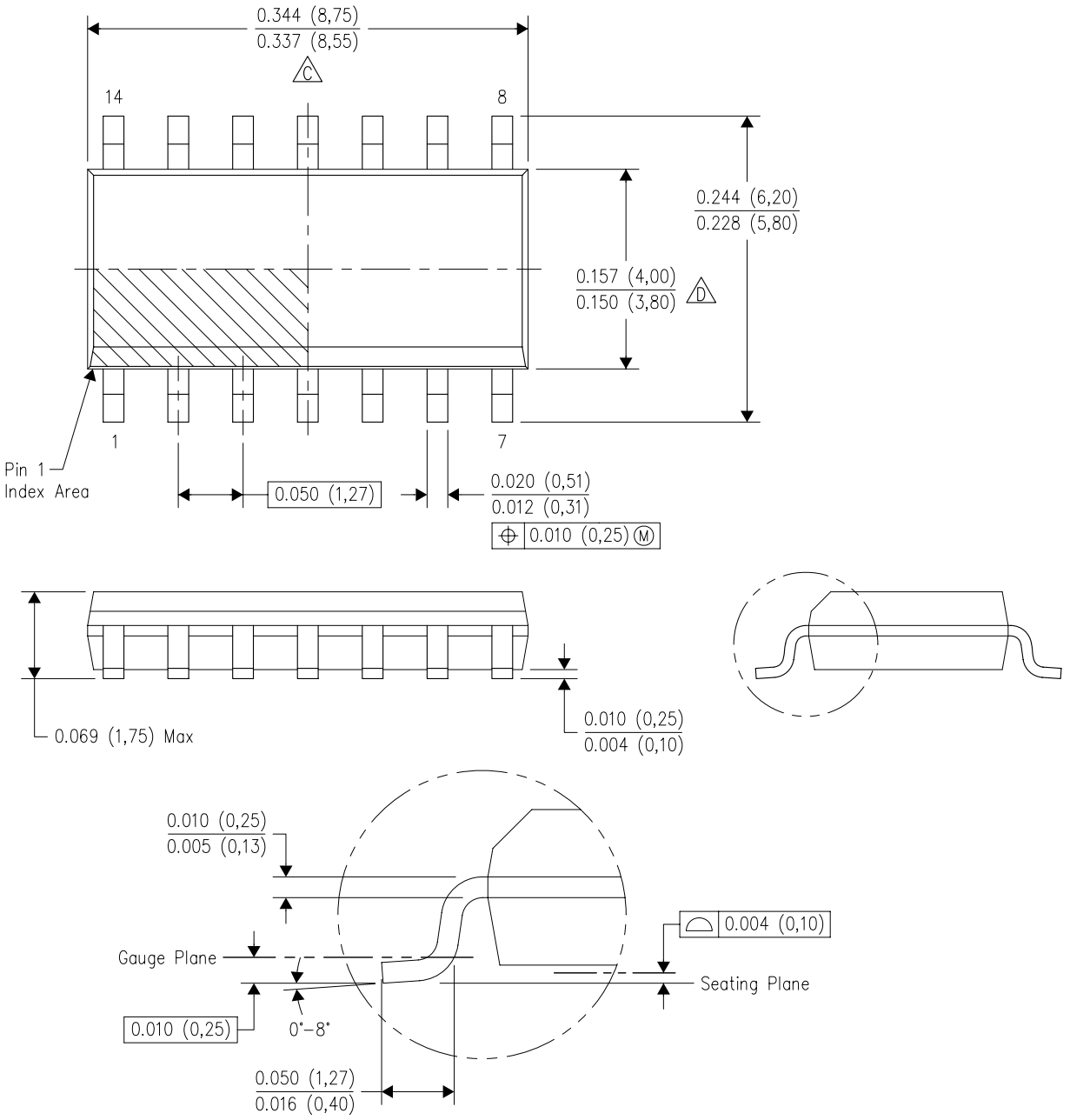
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9543APWR	TSSOP	PW	14	2000	367.0	367.0	35.0

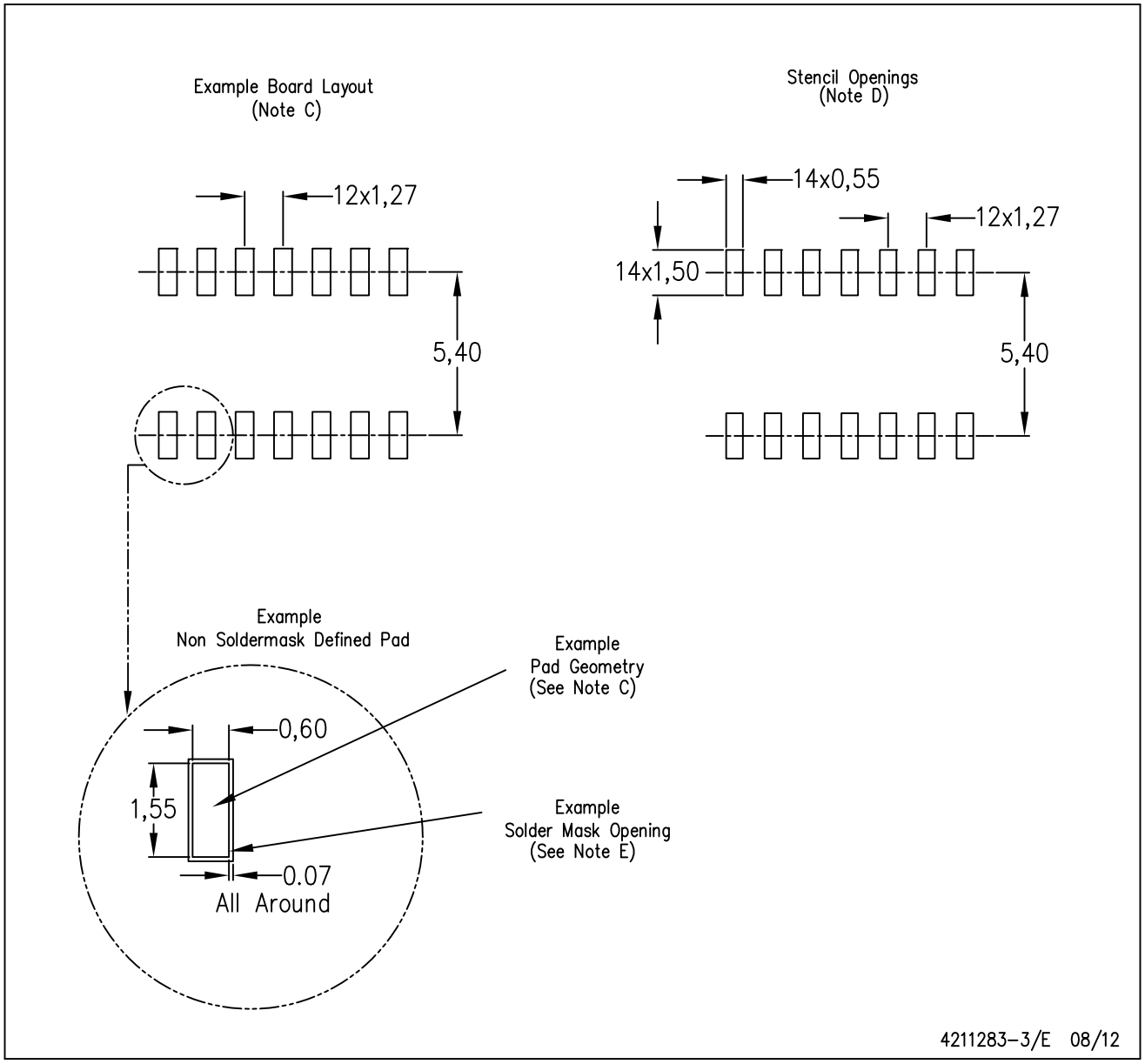
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

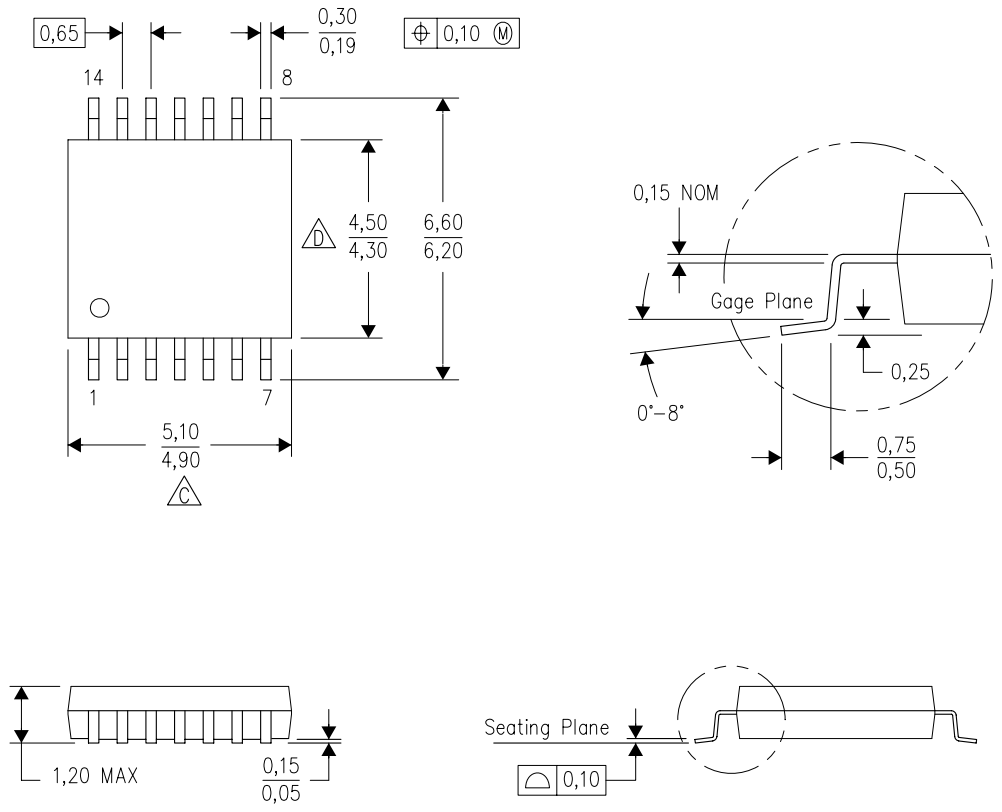
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

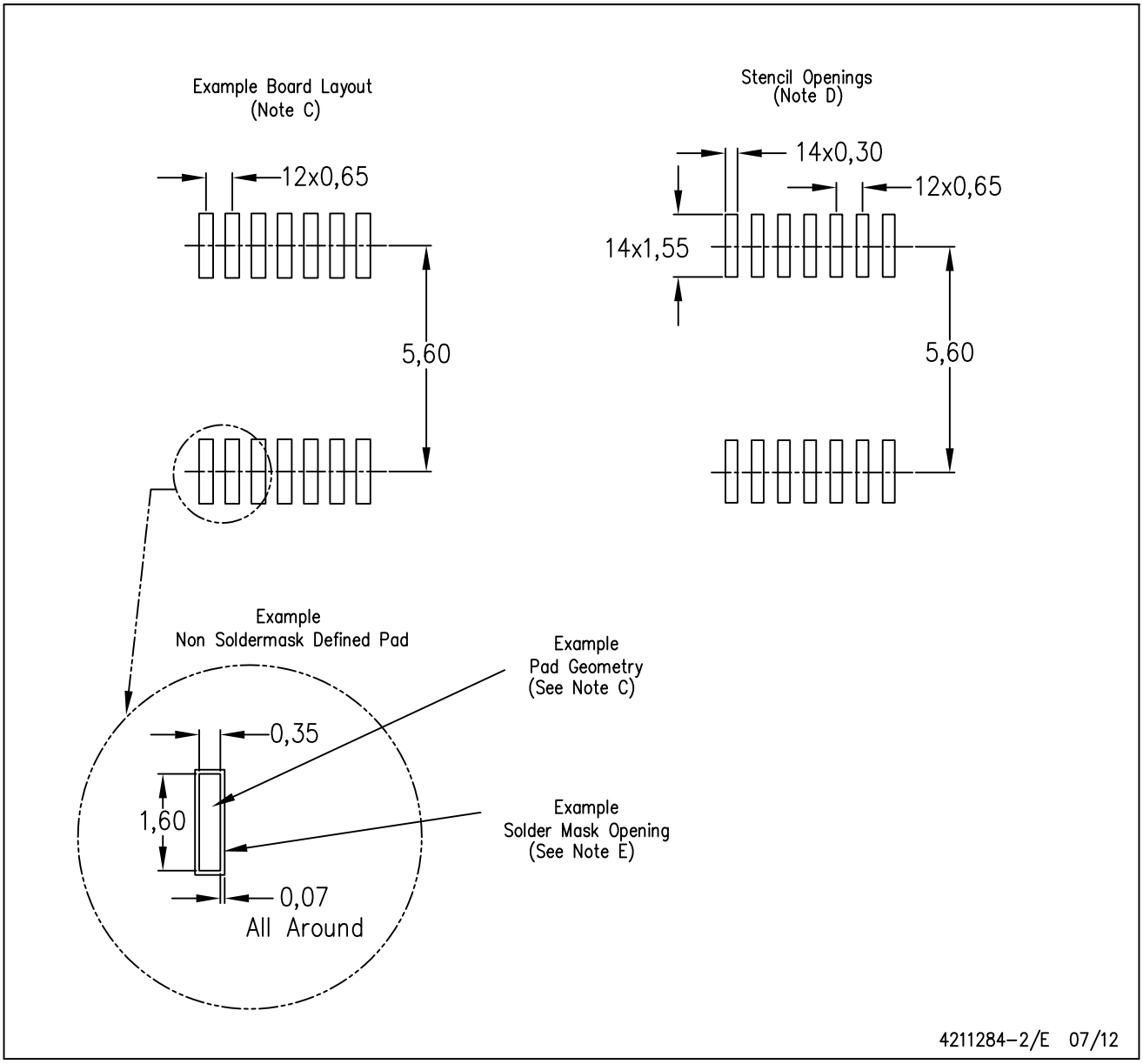
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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- Подбор аналогов;
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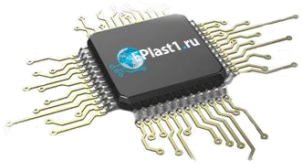

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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.