Octal bus switch

Rev. 5 — 9 April 2020

Product data sheet

1. General description

The CBT3245A provides eight bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3245A is organized as one 8-bit bus switches with one output enable (\overline{OE}) input. When \overline{OE} is LOW, the switch is on and port A is connected to the B port. When \overline{OE} is HIGH, each switch is disabled.

2. Features and benefits

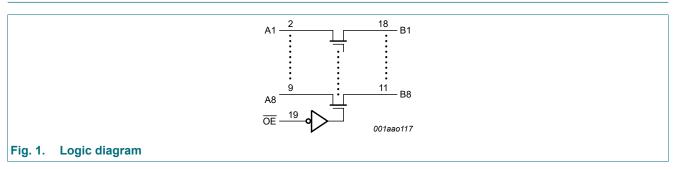
- 5 Ω switch connection between two ports
- · TTL-compatible control input levels
- Multiple package options
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115B exceeds 150 V
 - CDM JESD22-C101C exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package	Package									
	Temperature range	Name	Description	Version							
CBT3245AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1							
CBT3245APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1							
CBT3245ABQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1							

4. Functional diagram

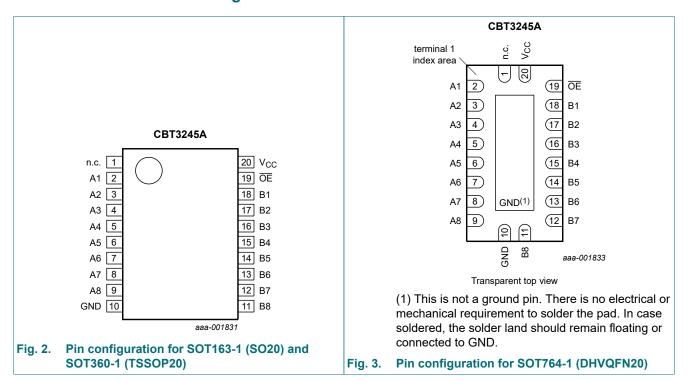




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5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Table 2. Fill description		
Symbol	Pin	Description
n.c.	1	not connected
A1 to A8	2, 3, 4, 5, 6, 7, 8, 9	data input/output (A port)
GND	10	ground (0 V)
B1 to B8	18, 17, 16, 15, 14, 13, 12, 11	data input/output (B port)
ŌE	19	output enable input (active LOW)
V _{CC}	20	positive supply voltage

6. Functional description

Table 3. Functional description

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
ŌE	An, Bn
L	An = Bn
Н	Z

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage	[1	-0.5	+7.0	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage	[1	-0.5	+7.0	V
Io	output current	V _O < 0 V	-	±128	mA
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
T _{amb}	ambient temperature	operating in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T _{amb} =	Unit		
				Min	Typ [1]	Max	
V_{IK}	input clamping voltage	V _{CC} = 4.5 V; I _I = -18 mA		-	-	-1.2	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V		-	-	±5	μΑ
I _{CC}	supply current	$V_{CC} = 5.5 \text{ V}; I_{O} = 0 \text{ mA}; V_{I} = V_{CC} \text{ or GND}$		-	1	3	μΑ
ΔI _{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	[2]	-	-	3.5	mA
C _I	input capacitance	control pins; V _I = 3 V or 0 V		-	3.2	-	pF
C _{io(off)}	off-state input/output capacitance	port off; $V_1 = 3 \text{ V or } 0 \text{ V}$; $\overline{OE} = V_{CC}$		-	6.6	-	pF
R _{ON}	ON resistance	V _{CC} = 4.5 V; V _I = 0 V; I _I = 64 mA	[3]	-	5	7	Ω
		V _{CC} = 4.5 V; V _I = 0 V; I _I = 30 mA	[3]	-	5	7	Ω
		V _{CC} = 4.5 V; V _I = 2.4 V; I _I = -15 mA	[3]	-	10	15	Ω

^{1]} All typical values are measured at V_{CC} = 5 V and T_{amb} = 25 °C.

CBT3245A

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

^[3] Measured by the voltage drop between the An and the Bn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) terminals.

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10. Dynamic characteristics

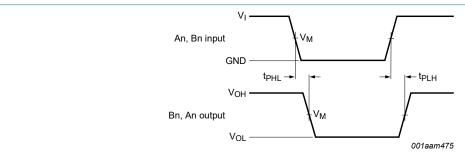
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	Conditions		T_{amb} = -40 °C to +85 °C		
				Min	Max		
t _{pd}	propagation delay	An, Bn to Bn, An; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$; see Fig. 4 [1]	[2]	-	0.25	ns	
t _{en}	enable time	$\overline{\text{OE}}$ to An or Bn; V_{CC} = 5.0 V ± 0.5 V; see Fig. 5	[3]	1.0	5.9	ns	
t _{dis}	disable time	OE to An or Bn; V _{CC} = 5.0 V ± 0.5 V; see Fig. 5	[4]	1.0	6.0	ns	

- [1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_{en} is the same as t_{PZL} and t_{PZH} .
- [4] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

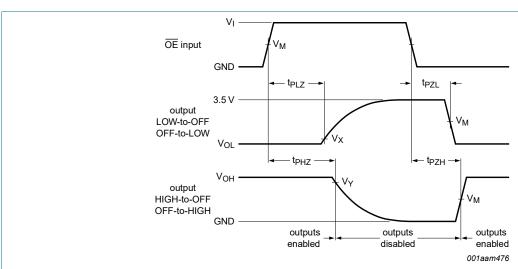
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in Table 8.

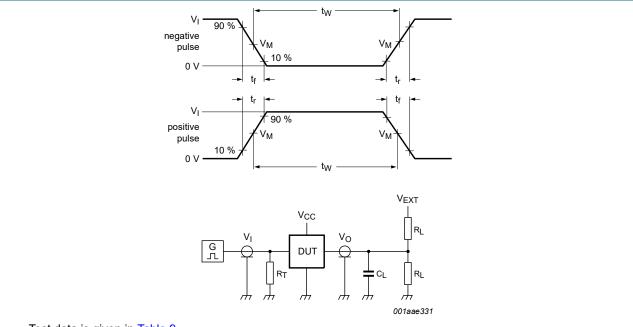
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

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Table 8. Measurement points

Supply voltage	Input		Output					
V _{CC}	V _I V _M		V _M	V _X	V _Y			
$V_{CC} = 5.0 V \pm 0.5 V$	GND to 3.0 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V			



Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz; $Z_o = 50 \Omega$.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig. 6. Test circuit for measuring switching times

Table 9. Test data

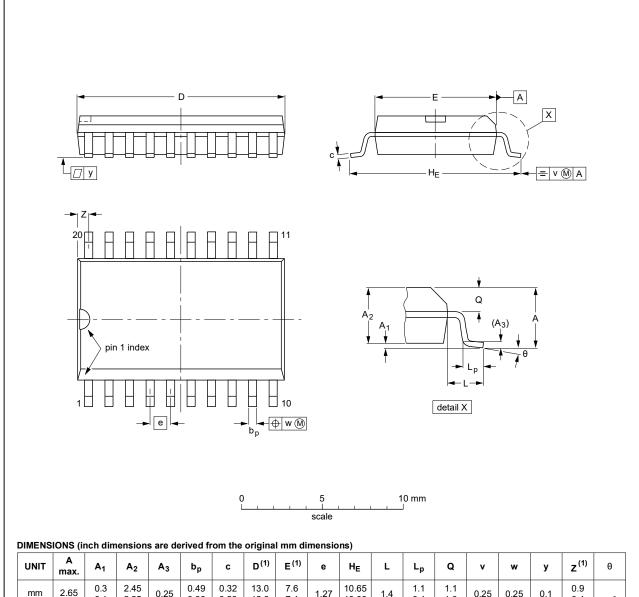
Supply voltage	Input		Load		V _{EXT}			
			CL	R_L	t _{PLH} , t _{PHL}	t_{PLZ},t_{PZL}	t _{PHZ} , t _{PZH}	
$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open	

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11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

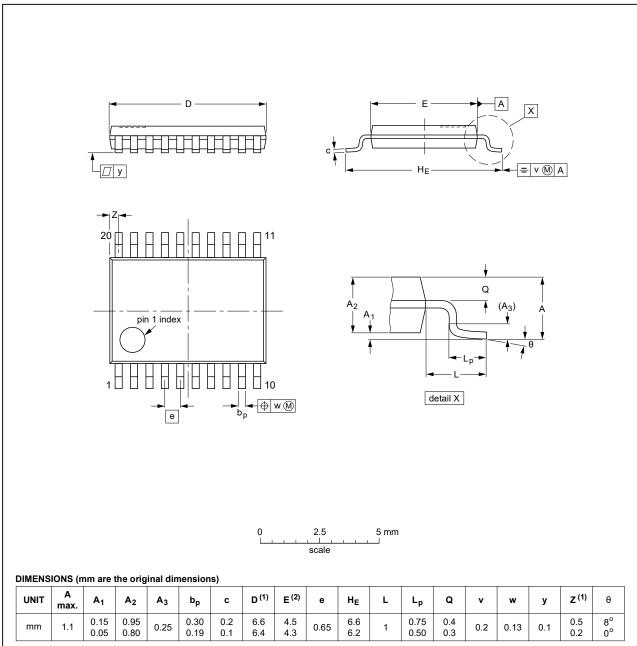
OUTLINE		REFER	RENCES	EUROPEAN ISSUE DATE			
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE		
SOT163-1	075E04	MS-013			99-12-27 03-02-19		

Fig. 7. Package outline SOT163-1 (SO20)

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT360-1		MO-153				99-12-27 03-02-19

Fig. 8. Package outline SOT360-1 (TSSOP20)

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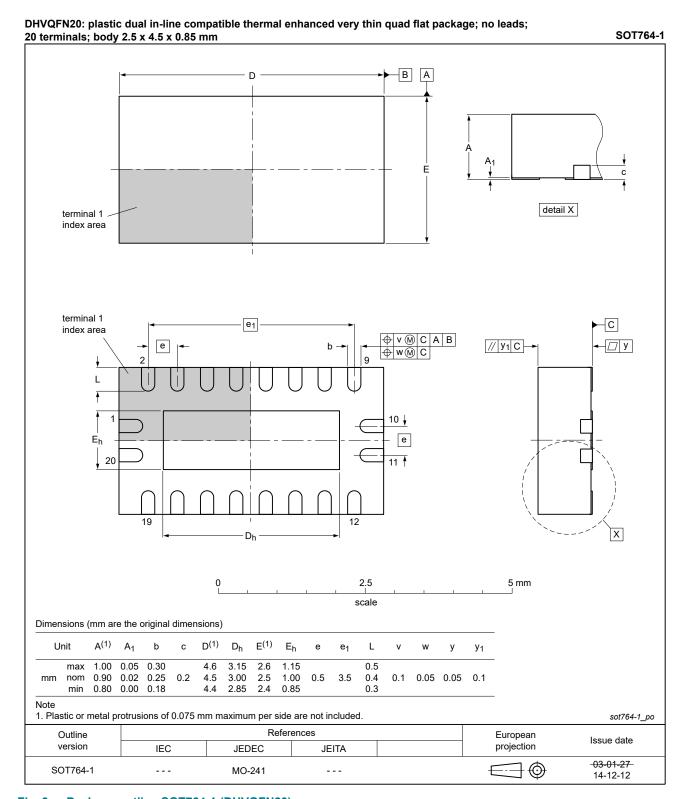


Fig. 9. Package outline SOT764-1 (DHVQFN20)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
DUT	Device Under Test
НВМ	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
CBT3245A v.5	20200409	Product data sheet	-	CBT3245A v.4		
Modifications:	Type numb	Type number CBT3245ADB (SOT339-1/SSOP20) removed.				
CBT3245A v.4	20190430	Product data sheet	-	CBT3245A v.3		
Modifications:	guidelines Legal texts Type numb	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number CBT3245ADS (SOT724-1/SSOP20) removed. Fig. 9: Package outline drawing SOT764-1 updated. 				
CBT3245A v.3	20120105	Product data sheet	-	CBT3245A v.2		
Modifications:	 The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Marking code removed from order information section. Description of C_I and C_{I/O} corrected (errata). 					
CBT3245A v.2	20020627	Product data sheet	-	CBT3245A v.1		
CBT3245A v.1	20020218	Product data sheet	-	-		

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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