

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

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H7N1002LD, H7N1002LS, H7N1002LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1131-0800

Rev.8.00

Nov 13, 2009

Features

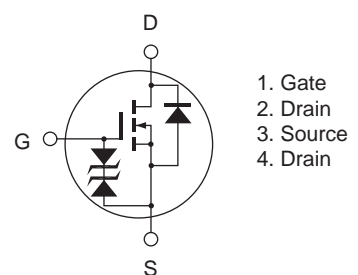
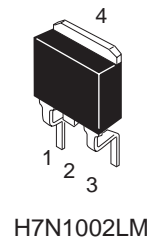
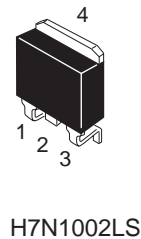
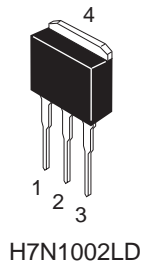
- Low on-resistance
 $R_{DS(on)} = 8 \text{ m}\Omega$ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))

: PRSS0004AE-B
: LDKPAK (S)-(1))

: PRSS0004AE-C
: LDKPAK (S)-(2))



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

| Item | Symbol | Value | Unit |
|---|----------------------------------|-------------|------------------|
| Drain to source voltage | V_{DSS} | 100 | V |
| Gate to source voltage | V_{GSS} | ± 20 | V |
| Drain current | I_D | 75 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note 1} | 300 | A |
| Body to drain diode reverse drain current | I_{DR} | 75 | A |
| Avalanche current | I_{AP} ^{Note 3} | 50 | A |
| Avalanche energy | E_{AR} ^{Note 3} | 166 | mJ |
| Channel dissipation | P_{ch} ^{Note 2} | 100 | W |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ\text{C}$
 3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

Electrical Characteristics

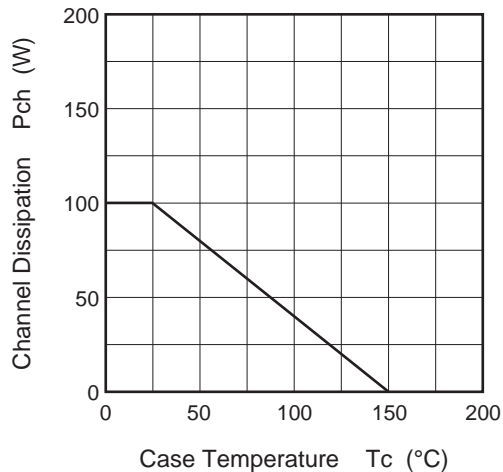
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|----------------|----------|------|----------|------------------|--|
| Drain to source breakdown voltage | $V_{(BR) DSS}$ | 100 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR) GSS}$ | ± 20 | — | — | V | $I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 10 | μA | $V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 10 | μA | $V_{DS} = 100 \text{ V}$, $V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 1.5 | — | 2.5 | V | $I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note 4} |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 8 | 10 | $\text{m}\Omega$ | $I_D = 37.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4} |
| | | — | 10 | 15 | $\text{m}\Omega$ | $I_D = 37.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 4} |
| Forward transfer admittance | $ y_{fs} $ | 57 | 95 | — | S | $I_D = 37.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4} |
| Input capacitance | C_{iss} | — | 9700 | — | pF | $V_{DS} = 10 \text{ V}$ |
| Output capacitance | C_{oss} | — | 740 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 330 | — | pF | $f = 1 \text{ MHz}$ |
| Total gate charge | Q_g | — | 155 | — | nC | $V_{DD} = 50 \text{ V}$ |
| Gate to source charge | Q_{gs} | — | 35 | — | nC | $V_{GS} = 10 \text{ V}$ |
| Gate to drain charge | Q_{gd} | — | 33 | — | nC | $I_D = 75 \text{ A}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 43 | — | ns | $V_{GS} = 10 \text{ V}$, $I_D = 37.5 \text{ A}$ |
| Rise time | t_r | — | 245 | — | ns | $R_L = 0.8 \text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | — | 130 | — | ns | $R_g = 4.7 \text{ }\Omega$ |
| Fall time | t_f | — | 25 | — | ns | |
| Body to drain diode forward voltage | V_{DF} | — | 0.93 | — | V | $I_F = 75 \text{ A}$, $V_{GS} = 0$ |
| Body to drain diode reverse recovery time | t_{rr} | — | 70 | — | ns | $I_F = 75 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$ |

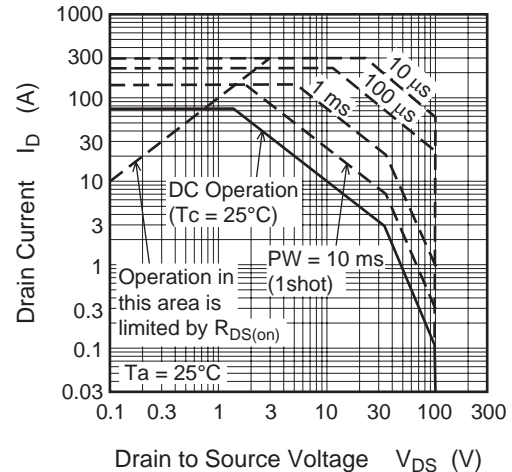
Note: 4. Pulse test

Main Characteristics

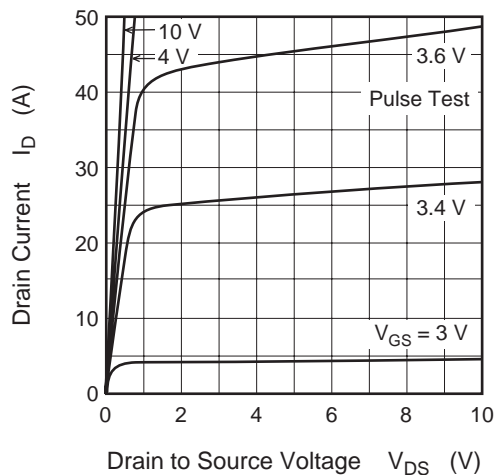
Power vs. Temperature Derating



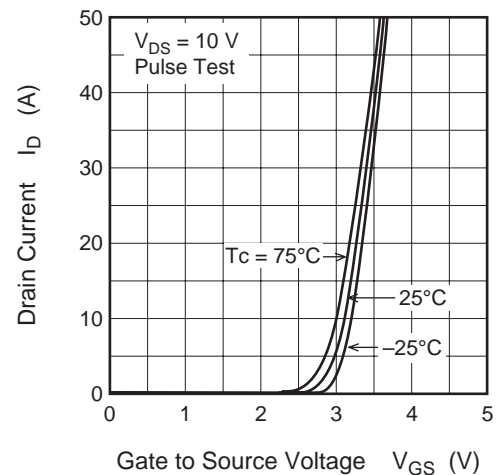
Maximum Safe Operation Area



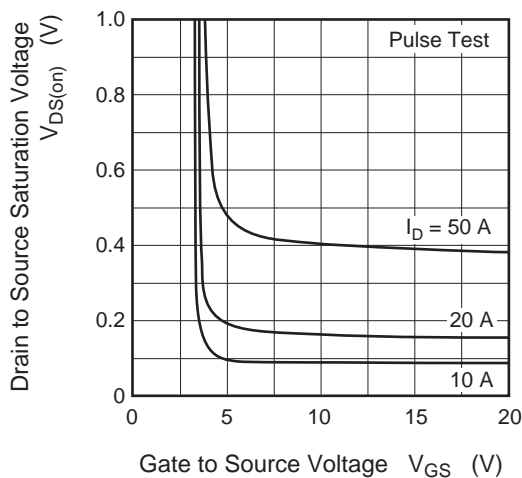
Typical Output Characteristics



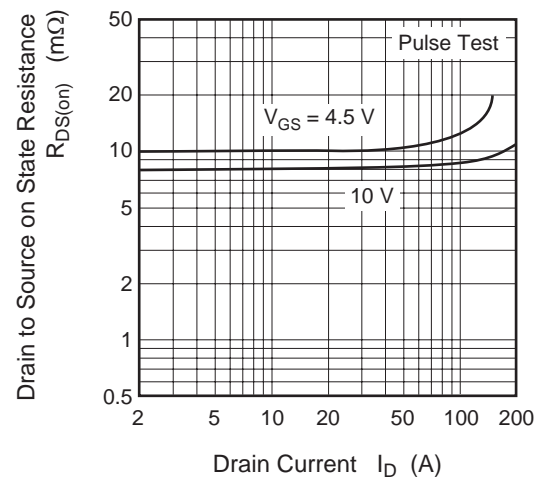
Typical Transfer Characteristics



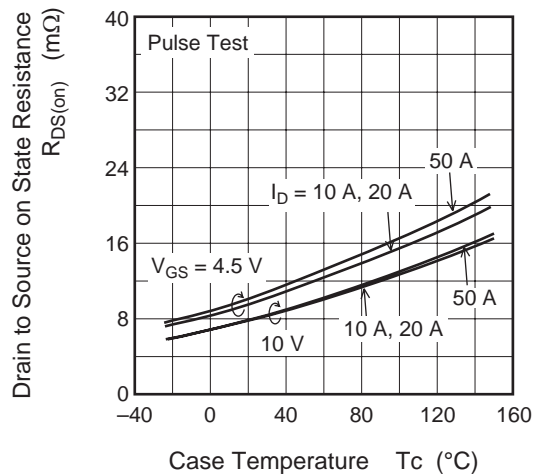
Drain to Source Saturation Voltage vs. Gate to Source Voltage



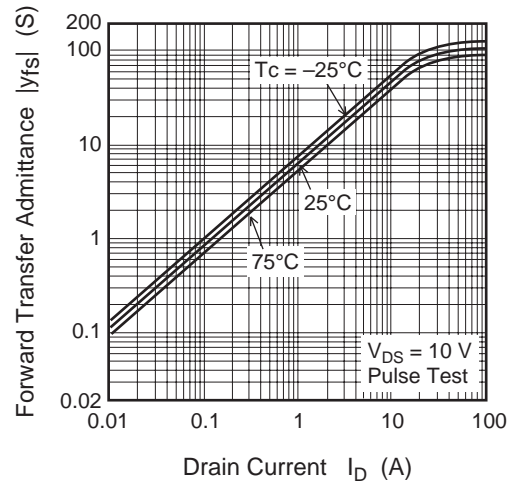
Static Drain to Source on State Resistance vs. Drain Current



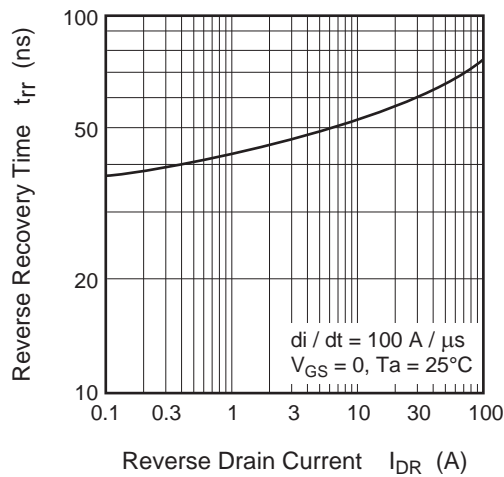
Static Drain to Source on State Resistance vs. Temperature



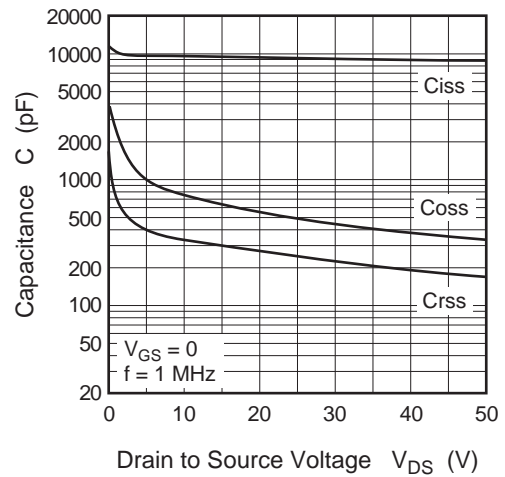
Forward Transfer Admittance vs. Drain Current



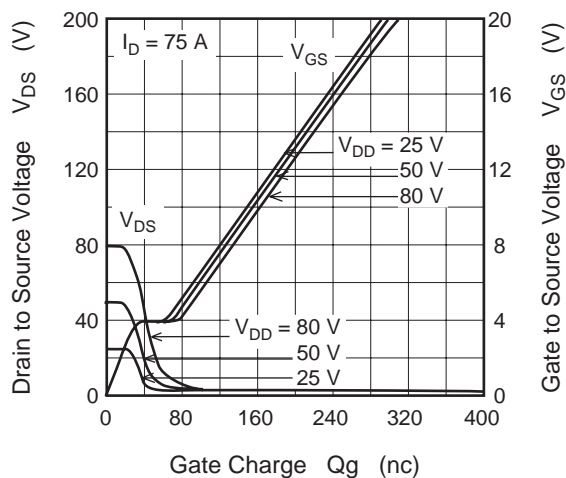
Body to Drain Diode Reverse Recovery Time



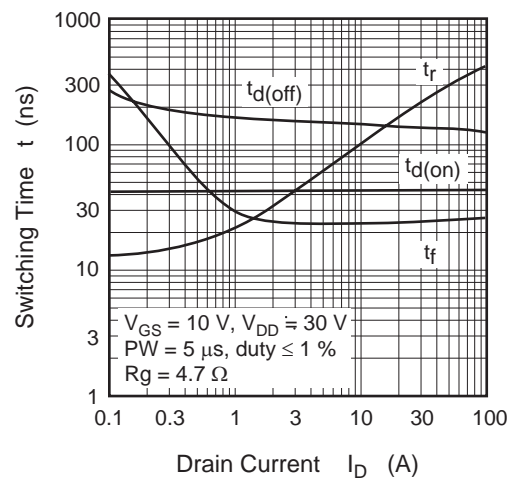
Typical Capacitance vs. Drain to Source Voltage

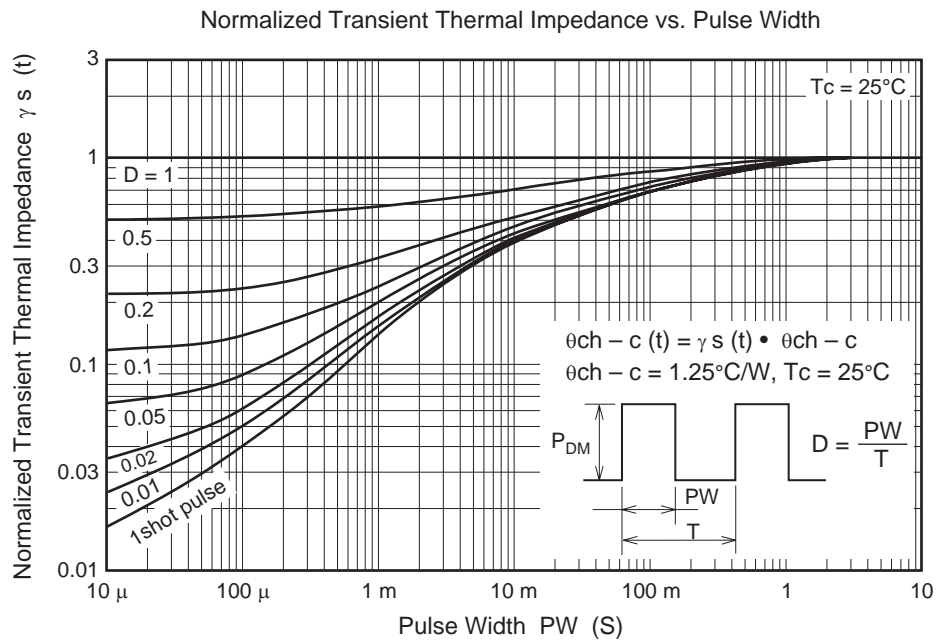
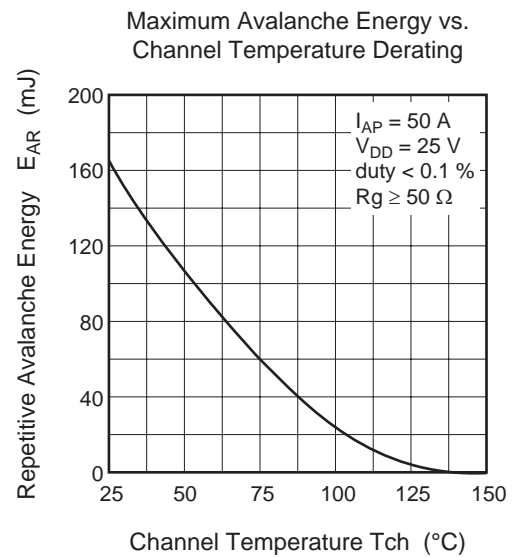
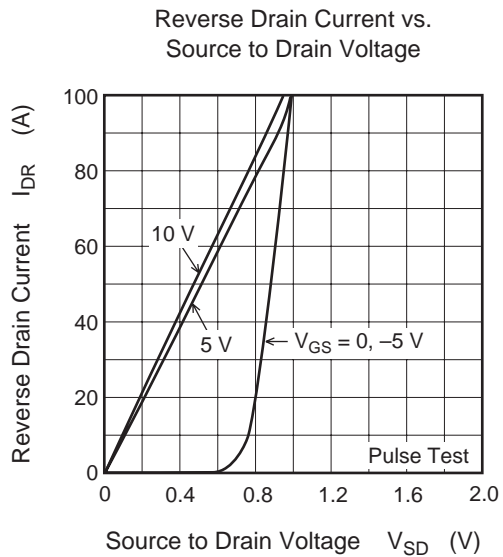


Dynamic Input Characteristics

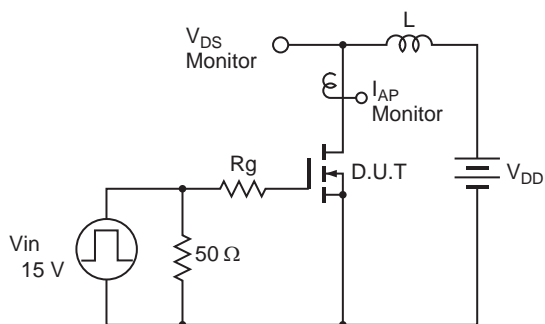


Switching Characteristics



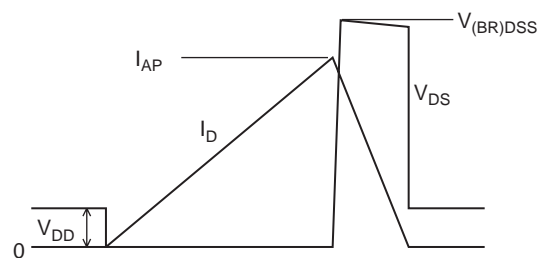


Avalanche Test Circuit

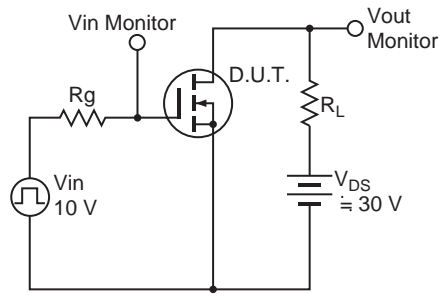


Avalanche Waveform

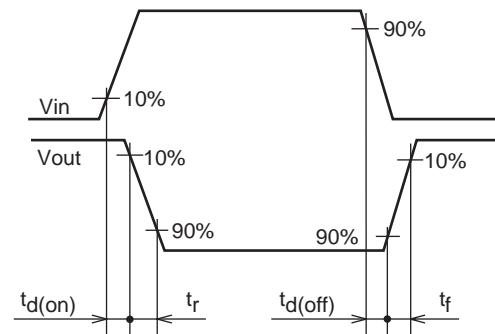
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



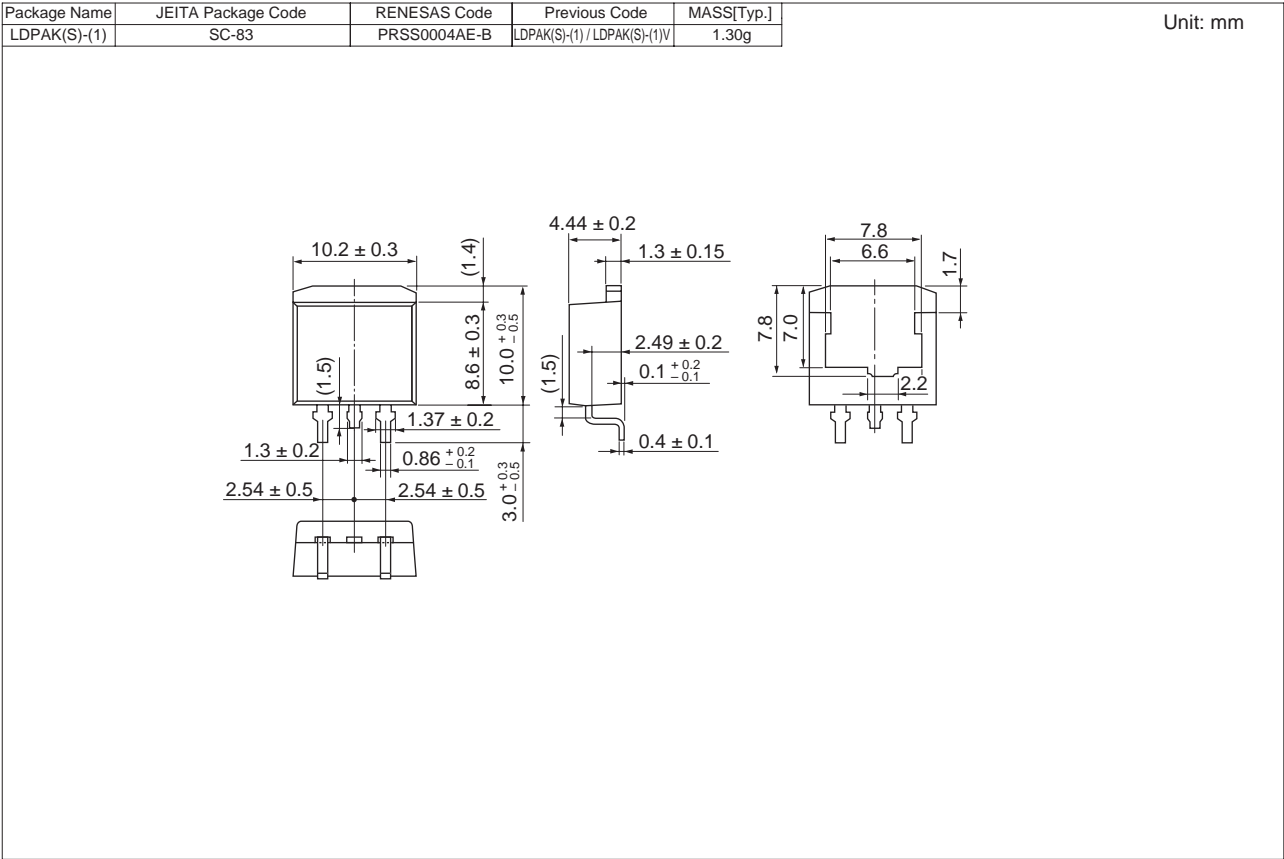
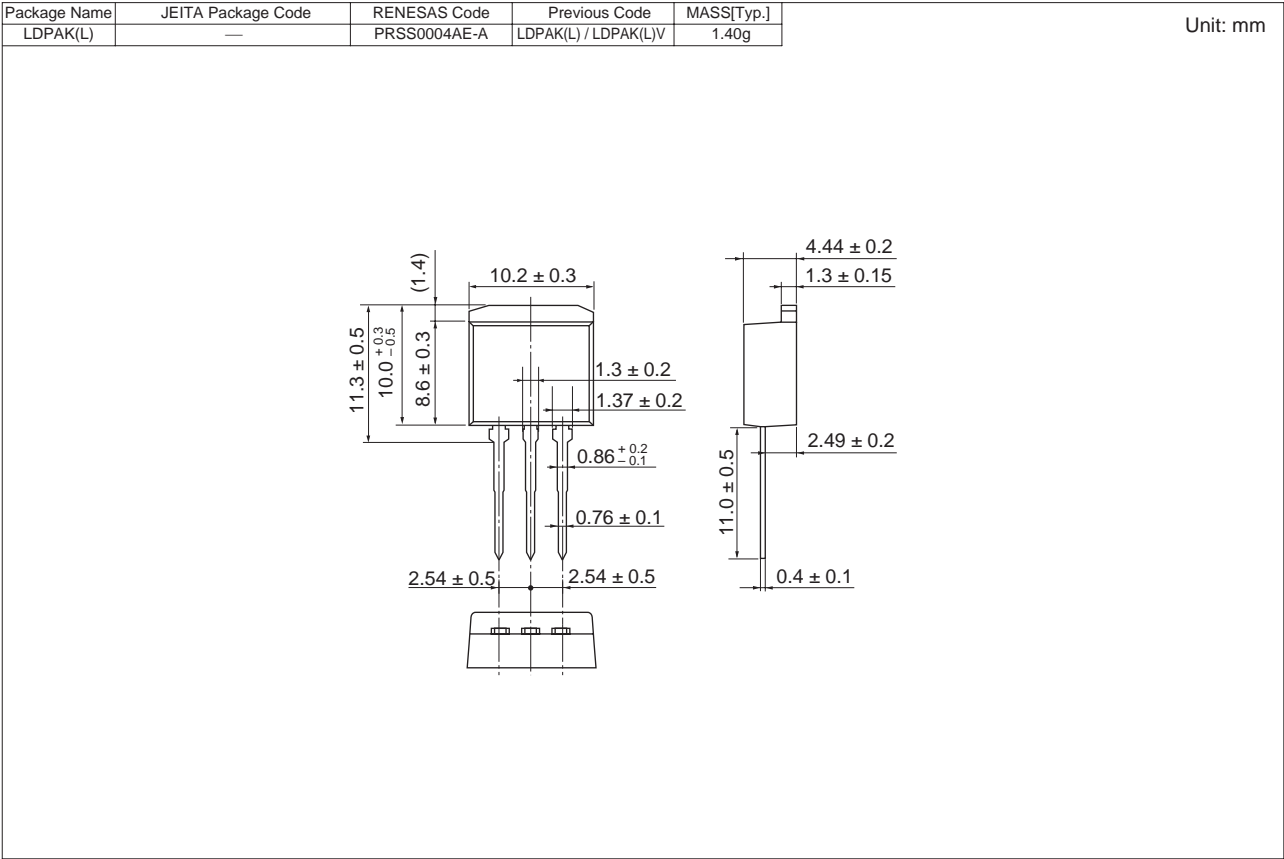
Switching Time Test Circuit



Waveform



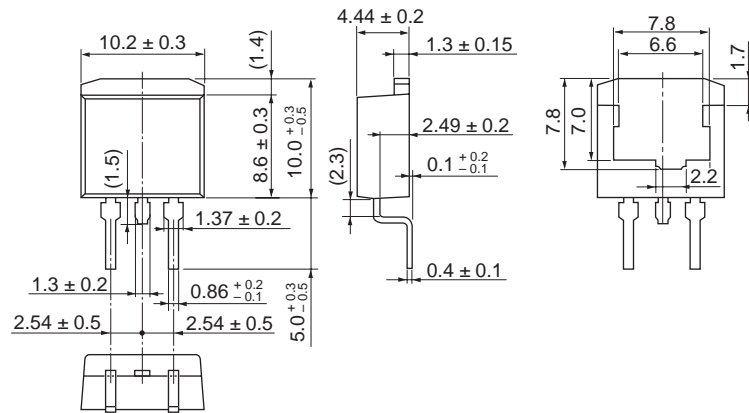
Package Dimensions



H7N1002LD, H7N1002LS, H7N1002LM

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|--------------|--------------------|--------------|------------------------------|------------|
| LDBAK(S)-(2) | — | PRSS0004AE-C | LDBAK(S)-(2) / LDBAK(S)-(2)V | 1.35g |

Unit: mm



Ordering Information

| Part Name | Quantity | Shipping Container |
|---------------|----------|-----------------------|
| H7N1002LD-E | 500 pcs | Box (Conductive Sack) |
| H7N1002LSTL-E | 1000 pcs | Taping |
| H7N1002LMTL-E | 1000 pcs | Taping |

Notes:

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