AAT3215
150mA CMOS High Performance LDO

PowerLinear™

General Description

The AAT3215 MicroPower™ low dropout (LDO) linear regulator is ideally suited for portable applications where low noise, extended battery life, and small size are critical. The AAT3215 has been specifically designed for very low output noise performance, fast transient response, and high power supply rejection ratio (PSRR), making it ideal for powering sensitive RF circuits.

Other features include low quiescent current, typically 95µA, and low dropout voltage which is typically less than 140mV at full output current. The device is output short-circuit protected and has a thermal shutdown circuit for additional protection under extreme conditions.

The AAT3215 also features a low-power shutdown mode for extended battery life. A reference bypass pin has been provided to improve PSRR performance and output noise by connecting an external capacitor from the AAT3215's reference output to ground.

The AAT3215 is available in a Pb-free, space-saving 5-pin SOT23 or 8-pin SC70JW package in ten factory-programmed voltages: 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.3V, or 3.6V.

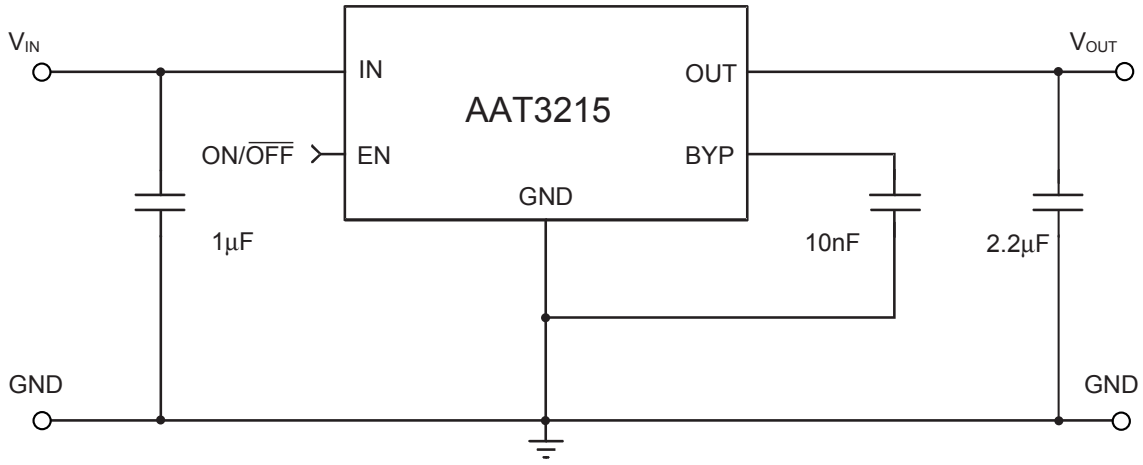
Features

- Low Dropout: 140mV at 150mA
- Guaranteed 150mA Output
- High Accuracy ±1.5%
- 95µA Quiescent Current
- High Power Supply Ripple Rejection
  - — 70dB at 1kHz
  - — 50dB at 10kHz
- Very Low Self Noise: 45µVrms
- Fast Line and Load Transient Response
- Short-Circuit Protection
- Over-Temperature Protection
- Uses Low Equivalent Series Resistance (ESR) Ceramic Capacitors
- Noise Reduction Bypass Capacitor
- Shutdown Mode for Longer Battery Life
- Low Temperature Coefficient
- Ten Factory-Programmed Output Voltages
- SOT23 5-Pin or SC70JW 8-Pin Package

Applications

- Bluetooth™ Headsets
- Cellular Phones
- Digital Cameras
- Notebook Computers
- Personal Portable Electronics
- Portable Communication Devices

Typical Application

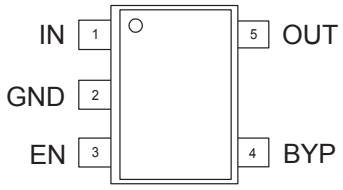


Pin Descriptions

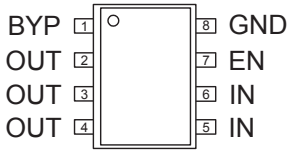
Pin #		Symbol	Function
SOT23-5	SC70JW-8		
1	5, 6	IN	Input voltage pin; should be decoupled with 1µF or greater capacitor.
2	8	GND	Ground connection pin.
3	7	EN	Enable pin. When pulled low, the PMOS pass transistor turns off and all internal circuitry enters low-power mode, consuming less than 1µA. This pin should not be left floating.
4	1	BYP	Bypass capacitor connection. To improve AC ripple rejection, connect a 10nF capacitor to GND. This will also provide a soft-start function.
5	2, 3, 4	OUT	Output pin; should be decoupled with 2.2µF capacitor.

Pin Configuration

SOT23-5
(Top View)



SC70JW-8
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C, unless otherwise noted.

Symbol	Description	Value	Units
V_{IN}	Input Voltage	6	V
$V_{ENIN(MAX)}$	Maximum EN to Input Voltage	0.3	V
I_{OUT}	DC Output Current	$P_D/(V_{IN}-V_O)$	mA
T_J	Operating Junction Temperature Range	-40 to 150	°C

Thermal Information[2]

Symbol	Description	Rating	Units
Θ_{JA}	Maximum Thermal Resistance (SOT23-5, SC70JW-8)	190	°C/W
P_D	Maximum Power Dissipation (SOT23-5, SC70JW-8)	526	mW

Recommended Operating Conditions

Symbol	Description	Rating	Units
V_{IN}	Input Voltage	(V_{OUT} + 0.3) to 5.5	V
T	Ambient Temperature Range	-40 to +85	°C

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on a demo board.

Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 1V, I_{OUT} = 1mA, C_{OUT} = 2.2µF, C_{IN} = 1µF, C_{BYP} = 10nF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

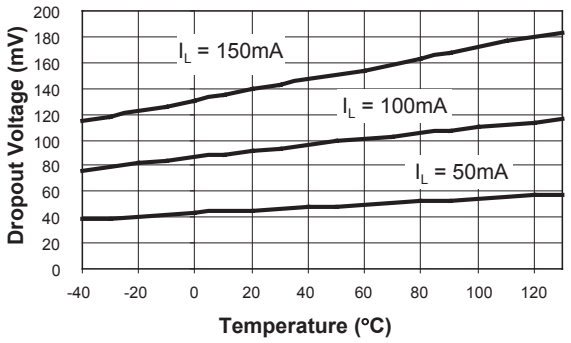
Symbol	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA to 150mA	T_A = 25°C	-1.5		1.5	%
			T_A = -40 to 85°C	-2.5		2.5	
I_{OUT}	Output Current	V_{OUT} > 1.2V		150			mA
V_{DO}	Dropout Voltage[1]	I_{OUT} = 150mA			140	250	mV
I_{SC}	Short-Circuit Current	V_{OUT} < 0.4V			600		mA
I_Q	Ground Current	V_{IN} = 5V, No Load, EN = V_{IN}			95	150	µA
I_{SD}	Shutdown Current	V_{IN} = 5V, EN = 0V				1	µA
$\Delta V_{OUT}/V_{OUT}*\Delta V_{IN}$	Line Regulation	V_{IN} = V_{OUT} + 1 to 5.5V				0.07	%/V
ΔV_{OUT}(line)	Dynamic Line Regulation	V_{IN} = V_{OUT} + 1V to V_{OUT} + 2V, I_{OUT} = 150mA, T_R/T_F = 2µs			1		mV
ΔV_{OUT}(load)	Dynamic Load Regulation	I_{OUT} = 1mA to 150mA, T_R < 5µs			30		mV
$V_{EN(L)}$	Enable Threshold Low					0.6	V
$V_{EN(H)}$	Enable Threshold High			1.5			V
I_{EN}	Leakage Current on Enable Pin	V_{EN} = 5V				1	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 10mA, C_{BYP} = 10nF	1kHz		70		dB
			10kHz		50		
			1MHz		47		
T_{SD}	Over-Temperature Shutdown Threshold				150		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis				10		°C
e_N	Output Noise				45		µVrms
T_C	Output Voltage Temperature Coefficient				22		ppm/°C

1. V_{DO} is defined as V_{IN} - V_{OUT} when V_{OUT} is 98% of nominal.

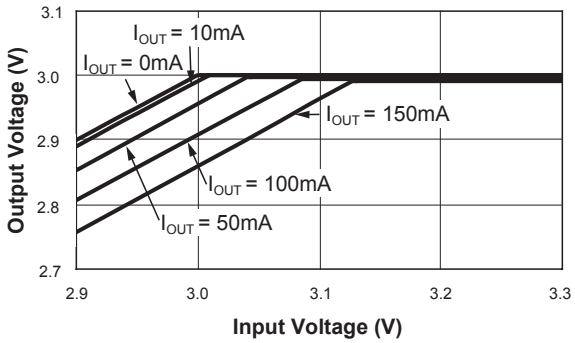
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

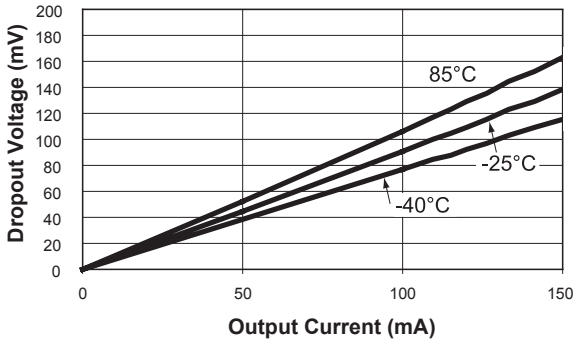
Dropout Voltage vs. Temperature



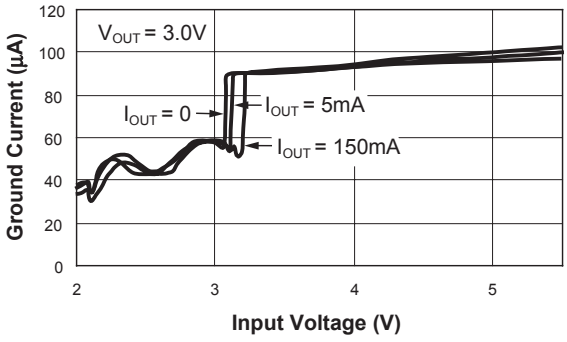
Dropout Characteristics



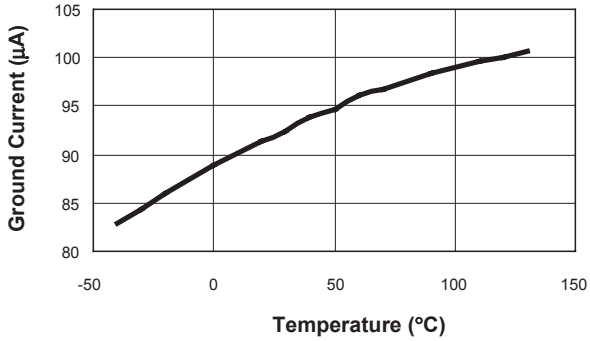
Dropout Voltage vs. Output Current



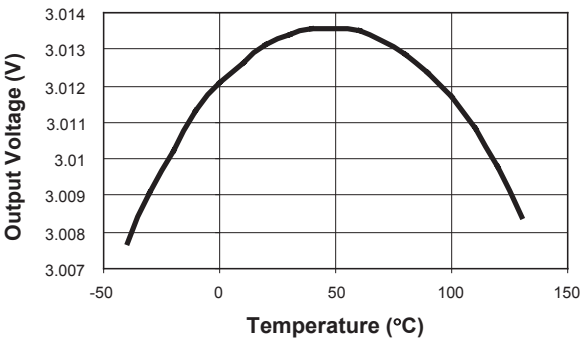
Ground Current vs. Input Voltage



Ground Current vs. Temperature
(V_{OUT} = 3.0V)



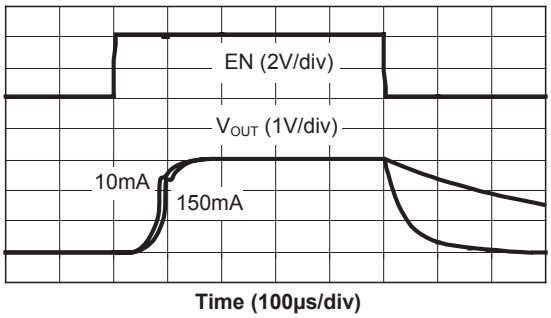
Output Voltage vs. Temperature



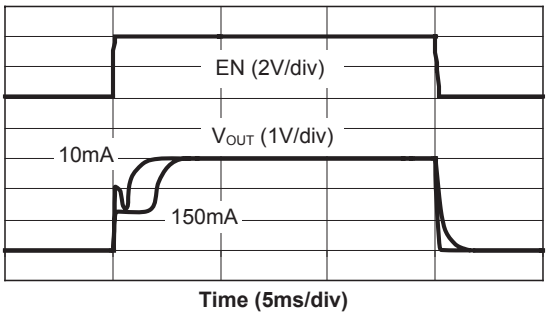
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

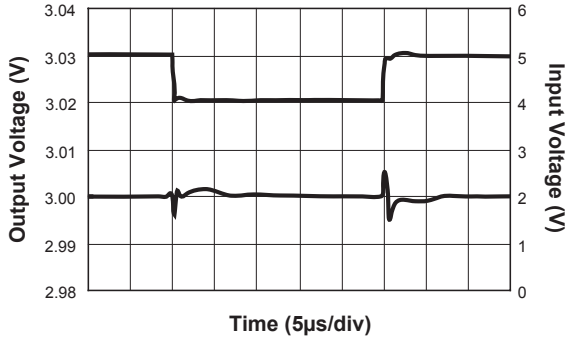
On/Off Transient Response
(No C_{BYP} Capacitor)



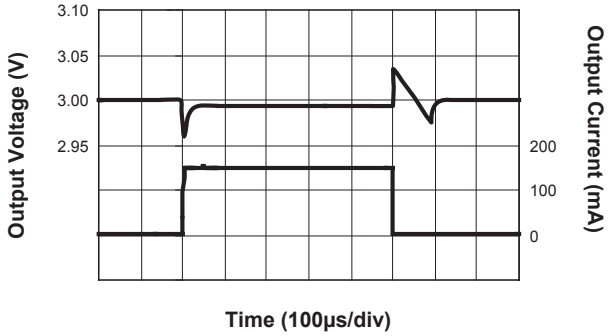
On/Off Transient Response
(C_{BYP} = 10nF)



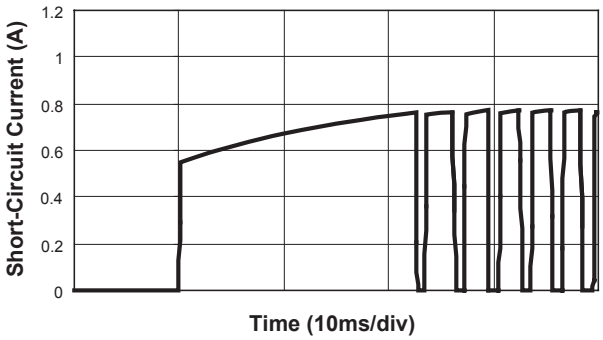
Line Transient Response



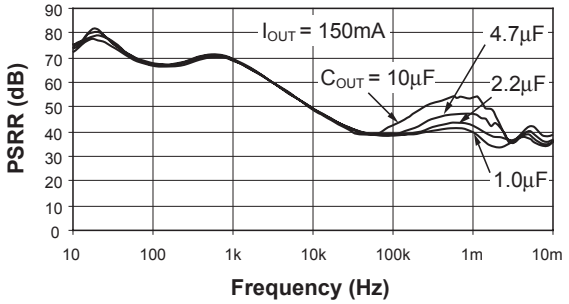
Load Transient Response



Short-Circuit Current



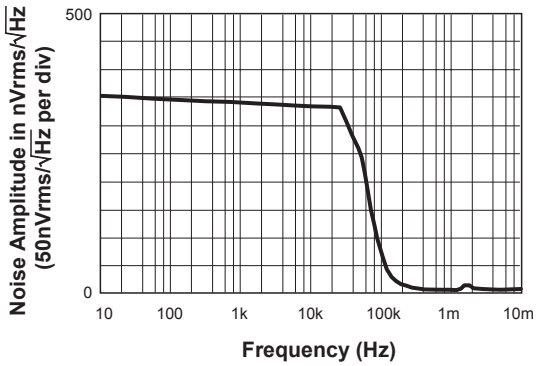
Power Supply Rejection Ratio vs. Frequency



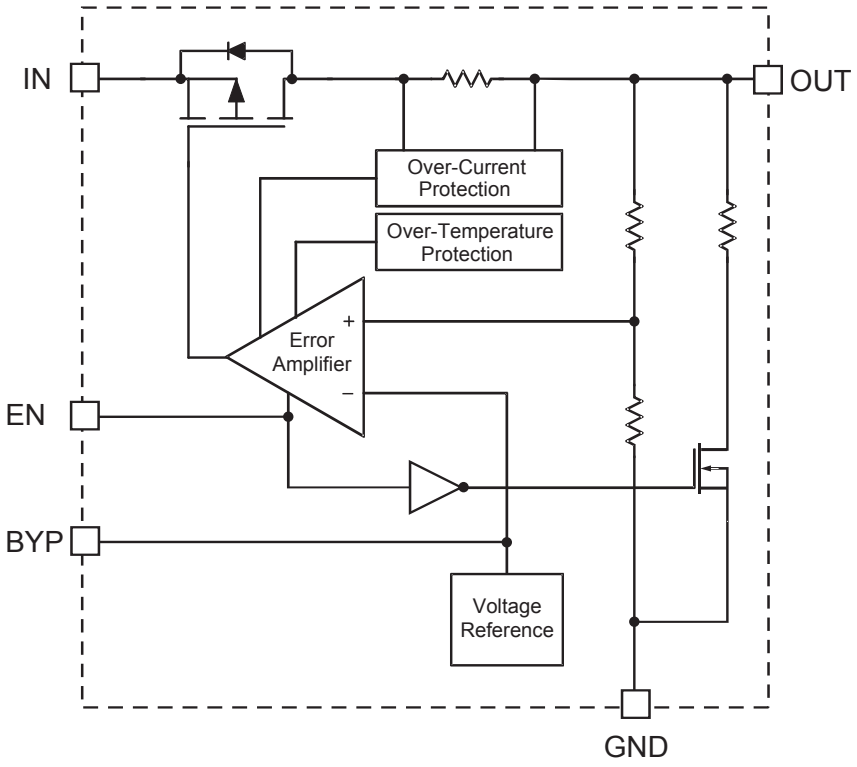
Typical Characteristics

Unless otherwise noted, V_{IN} = 5V, T_A = 25°C.

Output Self Noise



Functional Block Diagram



Functional Description

The AAT3215 is intended for LDO regulator applications where output current load requirements range from no load to 150mA.

The advanced circuit design of the AAT3215 provides excellent input-to-output isolation, which allows for good power supply ripple rejection characteristics. To optimize for very low output self noise performance, a bypass capacitor pin has been provided to decrease noise generated by the internal voltage reference. This bypass capacitor will also enhance PSRR behavior. The two combined characteristics of low noise and high PSRR make the AAT3215 a truly high performance LDO regulator especially well suited for circuit applications which are sensitive to their power source.

The LDO regulator output has been specifically optimized to function with low-cost, low-ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types.

The device enable circuit is provided to shut down the LDO regulator for power conservation in portable products. The enable circuit has an additional output capacitor discharge circuit to assure sharp application circuit turn-off upon device shutdown.

This LDO regulator has complete short-circuit and thermal protection. The integral combination of these two internal protection circuits gives the AAT3215 a comprehensive safety system during extreme adverse operating conditions. Device power dissipation is limited to the package type and thermal dissipation properties. Refer to the Thermal Considerations section of this datasheet for details on device operation at maximum output current loads.

Applications Information

To assure the maximum possible performance is obtained from the AAT3215, please refer to the following application recommendations.

Input Capacitor

Typically, a 1µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT3215 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device V_{IN} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 150mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins V_{OUT} and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance.

The AAT3215 has been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it will also work with higher ESR tantalum or aluminum electrolytic capacitors. However, for best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the AAT3215 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit.

In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

Bypass Capacitor and Low Noise Applications

A bypass capacitor pin is provided to enhance the very low noise characteristics of the AAT3215 LDO regulator. The bypass capacitor is not necessary for operation of the AAT3215. However, for best device performance, a small ceramic capacitor should be placed between the bypass pin (BYP) and the device ground pin (GND). The value of C_{BYP} may range from 470pF to 10nF. For lowest noise and best possible power supply ripple rejection performance, a 10nF capacitor should be used. To practically realize the highest power supply ripple rejection and lowest output noise performance, it is critical that the capacitor connection between the BYP pin and GND pin be direct and PCB traces should be as short as possible. Refer to the PCB Layout Recommendations section of this document for examples.

There is a relationship between the bypass capacitor value and the LDO regulator turn-on time. In applications where fast device turn-on time is desired, the value of C_{BYP} should be reduced.

In applications where low noise performance and/or ripple rejection are less of a concern, the bypass capacitor may be omitted. The fastest device turn-on time will be realized when no bypass capacitor is used.

DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance. For this reason, the use of a low leakage, high quality ceramic (NPO or C0G type) or film capacitor is highly recommended.

Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT3215. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lower cost, has a smaller PCB

footprint, and is non-polarized. Line and load transient response of the LDO regulator is improved by using low ESR ceramic capacitors. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

Equivalent Series Resistance: ESR is a very important characteristic to consider when selecting a capacitor. ESR is the internal series resistance associated with a capacitor that includes lead resistance, internal connections, size and area, material composition, and ambient temperature. Typically, capacitor ESR is measured in milliohms for ceramic capacitors and can range to more than several ohms for tantalum or aluminum electrolytic capacitors.

Ceramic Capacitor Materials: Ceramic capacitors less than 0.1µF are typically made from NPO or C0G materials. NPO and C0G materials generally have tight tolerance and are very stable over temperature. Larger capacitor values are usually composed of X7R, X5R, Z5U, or Y5V dielectric materials. Large ceramic capacitors (i.e., greater than 2.2µF) are often available in low-cost Y5V and Z5U dielectrics. These two material types are not recommended for use with LDO regulators since the capacitor tolerance can vary more than ±50% over the operating temperature range of the device. A 2.2µF Y5V capacitor could be reduced to 1µF over temperature; this could cause problems for circuit operation. X7R and X5R dielectrics are much more desirable. The temperature tolerance of X7R dielectric is better than ±15%.

Capacitor area is another contributor to ESR. Capacitors that are physically large in size will have a lower ESR when compared to a smaller sized capacitor of an equivalent material and capacitance value. These larger devices can improve circuit transient response when compared to an equal value capacitor in a smaller package size.

Consult capacitor vendor datasheets carefully when selecting capacitors for LDO regulators.

Enable Function

The AAT3215 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 2.0V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6 volts. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

When the LDO regulator is in shutdown mode, an internal 1.5kΩ resistor is connected between V_{OUT} and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

Short-Circuit Protection

The AAT3215 contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

Thermal Protection

The AAT3215 has an internal thermal protection circuit which will turn on when the device die temperature exceeds 150°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of overtemperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 150°C trip point.

The combination and interaction between the short-circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT3215 is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero.

Reverse Output-to-Input Voltage Conditions and Protection

Under normal operating conditions, a parasitic diode exists between the output and input of the LDO regulator. The input voltage should always remain greater than the output load voltage, main-

taining a reverse bias on the internal parasitic diode. Conditions where V_{OUT} might exceed V_{IN} should be avoided since this would forward bias the internal parasitic diode and allow excessive current flow into the V_{OUT} pin, possibly damaging the LDO regulator.

In applications where there is a possibility of V_{OUT} exceeding V_{IN} for brief amounts of time during normal operation, the use of a larger value C_{IN} capacitor is highly recommended. A larger value of C_{IN} with respect to C_{OUT} will effect a slower C_{IN} decay rate during shutdown, thus preventing V_{OUT} from exceeding V_{IN}. In applications where there is a greater danger of V_{OUT} exceeding V_{IN} for extended periods of time, it is recommended to place a Schottky diode across V_{IN} to V_{OUT} (connecting the cathode to V_{IN} and anode to V_{OUT}). The Schottky diode forward voltage should be less than 0.45V.

Thermal Considerations and High Output Current Applications

The AAT3215 is designed to deliver a continuous output load current of 150mA under normal operating conditions.

The limiting characteristic for the maximum output load current safe operating area is essentially package power dissipation and the internal preset thermal limit of the device. In order to obtain high operating currents, careful device layout and circuit operating conditions need to be taken into account.

The following discussions will assume the LDO regulator is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the Layout Considerations section of this datasheet.

At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT3215 are $T_{J(MAX)}$, the maximum junction temperature for the device which is 125°C, and Θ_{JA} = 190°C/W, the package thermal resistance. Typically, maximum conditions are calculated at the maximum operating temperature where T_A = 85°C, under normal ambient conditions T_A = 25°C. Given T_A = 85°C, the maximum package power dissipation is 211mW. At T_A = 25°C, the maximum package power dissipation is 526mW.

The maximum continuous output current for the AAT3215 is a function of the package power dissipation and the input-to-output voltage drop across the LDO regulator. Refer to the following simple equation:

$$I_{OUT(MAX)} < \frac{P_{D(MAX)}}{(V_{IN} - V_{OUT})}$$

For example, if V_{IN} = 5V, V_{OUT} = 3V, and T_A = 25°C, $I_{OUT(MAX)}$ < 264mA. If the output load current were to exceed 264mA or if the ambient temperature were to increase, the internal die temperature would increase. If the condition remained constant, the LDO regulator thermal protection circuit would activate.

To determine the maximum input voltage for a given load current, refer to the following equation. This calculation accounts for the total power dissipation of the LDO regulator, including that caused by ground current.

$$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \cdot I_{GND})$$

This formula can be solved for V_{IN} to determine the maximum input voltage.

$$V_{IN(MAX)} = \frac{P_{D(MAX)} + (V_{OUT} \cdot I_{OUT})}{I_{OUT} + I_{GND}}$$

The following is an example for an AAT3215 set for a 2.5 volt output:

V_{OUT} = 2.5V
I_{OUT} = 150mA
I_{GND} = 150µA

$$V_{IN(MAX)} = \frac{526mW + (2.5V \cdot 150mA)}{150mA + 150\mu A}$$

$V_{IN(MAX)}$ = 6.00V

From the discussion above, $P_{D(MAX)}$ was determined to equal 526mW at T_A = 25°C.

Thus, the AAT3215 can sustain a constant 2.5V output at a 150mA load current as long as V_{IN} is ≤ 6.00V at an ambient temperature of 25°C. 6.0V is the absolute maximum voltage where an AAT3215 would never be operated, thus at 25°C, the device would not have any thermal concerns or operational $V_{IN(MAX)}$ limits.

This situation can be different at 85°C. The following is an example for an AAT3215 set for a 2.5V output at 85°C:

V_{OUT} = 2.5V
I_{OUT} = 150mA
I_{GND} = 150µA

$$V_{IN(MAX)} = \frac{211mW + (2.5V \cdot 150mA)}{150mA + 150\mu A}$$

$V_{IN(MAX)}$ = 3.90V

From the discussion above, $P_{D(MAX)}$ was determined to equal 211mW at T_A = 85°C.

Higher input-to-output voltage differentials can be obtained with the AAT3215, while maintaining device functions within the thermal safe operating area. To accomplish this, the device thermal resistance must be reduced by increasing the heat sink area or by operating the LDO regulator in a duty-cycled mode.

For example, an application requires V_{IN} = 4.2V while V_{OUT} = 2.5V at a 150mA load and T_A = 85°C. V_{IN} is greater than 3.90V, which is the maximum safe continuous input level for V_{OUT} = 2.5V at 150mA for T_A = 85°C. To maintain this high input voltage and output current level, the LDO regulator must be operated in a duty-cycled mode. Refer to the following calculation for duty-cycle operation:

I_{GND} = 150µA
I_{OUT} = 150mA
V_{IN} = 4.2V

V_{OUT} = 2.5V

$$\%DC = 100 \frac{P_{D(MAX)}}{(V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \cdot I_{GND})}$$

$$\%DC = 100 \frac{211mW}{(4.2V - 2.5V)150mA + (4.2V \cdot 150\mu A)}$$

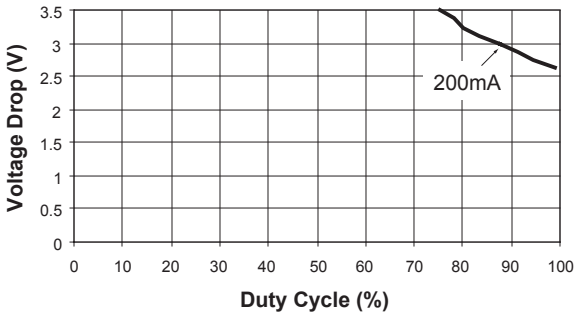
%DC = 85.54%

$P_{D(MAX)}$ was assumed to be 211mW.

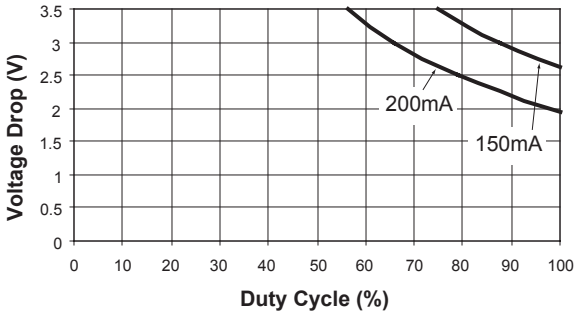
For a 150mA output current and a 2.7V drop across the AAT3215 at an ambient temperature of 85°C, the maximum on-time duty cycle for the device would be 85.54%.

The following family of curves show the safe operating area for duty-cycled operation from ambient room temperature to the maximum operating level.

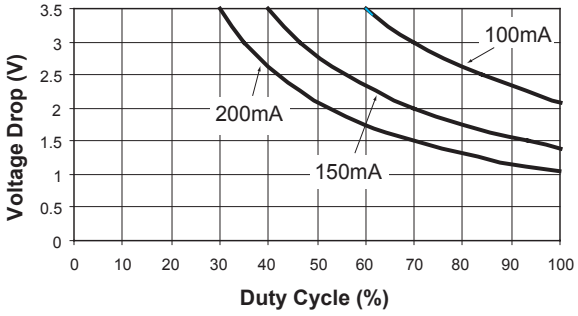
Device Duty Cycle vs. V_{DROP}
(V_{OUT} = 2.5V @ 25°C)



Device Duty Cycle vs. V_{DROP}
(V_{OUT} = 2.5V @ 50°C)



Device Duty Cycle vs. V_{DROP}
(V_{OUT} = 2.5V @ 85°C)



High Peak Output Current Applications

Some applications require the LDO regulator to operate at continuous nominal level with short duration, high-current peaks. The duty cycles for both output current levels must be taken into account. To do so, first calculate the power dissipation at the nominal continuous level, then factor in the additional power dissipation due to the short duration, high-current peaks.

For example, a 2.5V system using a AAT3215IGV-2.5-T1 operates at a continuous 100mA load current level and has short 150mA current peaks. The current peak occurs for 378µs out of a 4.61ms period. It will be assumed the input voltage is 4.2V.

First, the current duty cycle in percent must be calculated:

% Peak Duty Cycle: X/100 = 378µs/4.61ms
% Peak Duty Cycle = 8.2%

The LDO regulator will be under the 100mA load for 91.8% of the 4.61ms period and have 150mA peaks occurring for 8.2% of the time. Next, the continuous nominal power dissipation for the 100mA load should be determined then multiplied by the duty cycle to conclude the actual power dissipation over time.

$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \cdot I_{GND})$
$P_{D(100mA)} = (4.2V - 2.5V)100mA + (4.2V \cdot 150\mu A)$
$P_{D(100mA)} = 170.6mW$

$P_{D(91.8\%D/C)} = \%DC \cdot P_{D(100mA)}$
$P_{D(91.8\%D/C)} = 0.918 \cdot 170.6mW$
$P_{D(91.8\%D/C)} = 156.6mW$

The power dissipation for 100mA load occurring for 91.8% of the duty cycle will be 156.6mW. Now the power dissipation for the remaining 8.2% of the duty cycle at the 150mA load can be calculated:

$P_{D(MAX)} = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN} \cdot I_{GND})$
$P_{D(150mA)} = (4.2V - 2.5V)150mA + (4.2V \cdot 150mA)$
$P_{D(150mA)} = 255.6mW$

$P_{D(8.2\%D/C)} = \%DC \cdot P_{D(150mA)}$
$P_{D(8.2\%D/C)} = 0.082 \cdot 255.6mW$
$P_{D(8.2\%D/C)} = 21mW$

The power dissipation for 150mA load occurring for 8.2% of the duty cycle will be 21mW. Finally, the two power dissipation levels can summed to determine the total true power dissipation under the varied load.

$P_{D(total)} = P_{D(100mA)} + P_{D(150mA)}$
$P_{D(total)} = 156.6mW + 21mW$
$P_{D(total)} = 177.6mW$

The maximum power dissipation for the AAT3215 operating at an ambient temperature of 85°C is 211mW. The device in this example will have a total power dissipation of 177.6mW. This is well within the thermal limits for safe operation of the device.

Printed Circuit Board Layout Recommendations

In order to obtain the maximum performance from the AAT3215 LDO regulator, careful consideration should be given to the printed circuit board (PCB) layout. If grounding connections are not properly made, power supply ripple rejection, low output self noise, and transient response can be compromised.

Figure 1 shows a common LDO regulator layout scheme. The LDO regulator, external capacitors (C_{IN}, C_{OUT}, and C_{BYP}), and the load circuit are all connected to a common ground plane. This type of layout will work in simple applications where good power supply ripple rejection and low self noise are not a design concern. For high performance applications, this method is not recommended.

The problem with the layout in Figure 1 is the bypass capacitor and output capacitor share the same ground path to the LDO regulator ground pin, along with the high current return path from the load back to the power supply. The bypass capacitor node is connected directly to the LDO regulator internal reference, making this node very sensitive to noise or ripple. The internal reference output is fed into the error amplifier, thus any noise or ripple from the bypass capacitor will be subsequently amplified by the gain of the error amplifier. This effect can increase noise seen on the LDO regulator output, as well as reduce the maximum possible power supply ripple rejection. There is PCB trace impedance between the bypass capacitor connection to ground and the LDO regulator ground connection. When the high load current returns through this path, a small ripple voltage is created, feeding into the C_{BYP} loop.

Figure 2 shows the preferred method for the bypass and output capacitor connections. For low output noise and highest possible power supply ripple rejection performance, it is critical to connect the bypass and output capacitor directly to the LDO regulator ground pin. This method will eliminate any load noise or ripple current feedback through the LDO regulator.

Evaluation Board Layout

The AAT3215 evaluation layout follows the recommend printed circuit board layout procedures and can be used as an example for good application layouts (see Figures 3, 4, and 5).

Note: Board layout shown is not to scale.

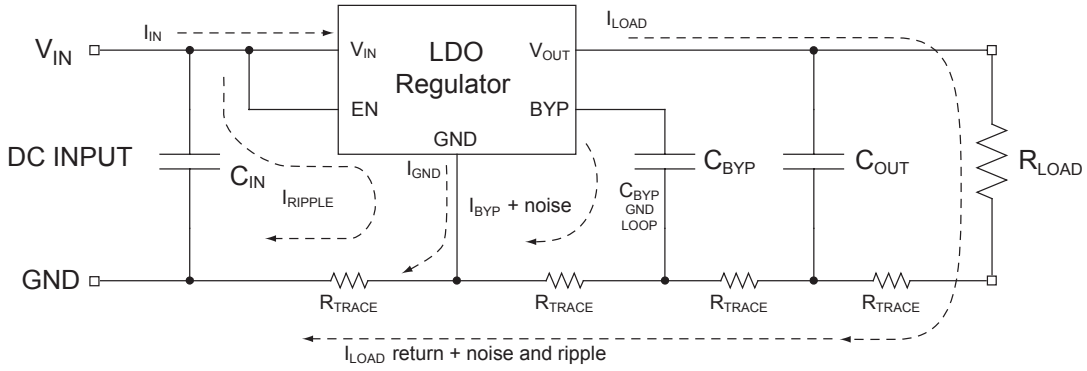


Figure 1: Common LDO Regulator Layout with C_{BYP} Ripple Feedback Loop.

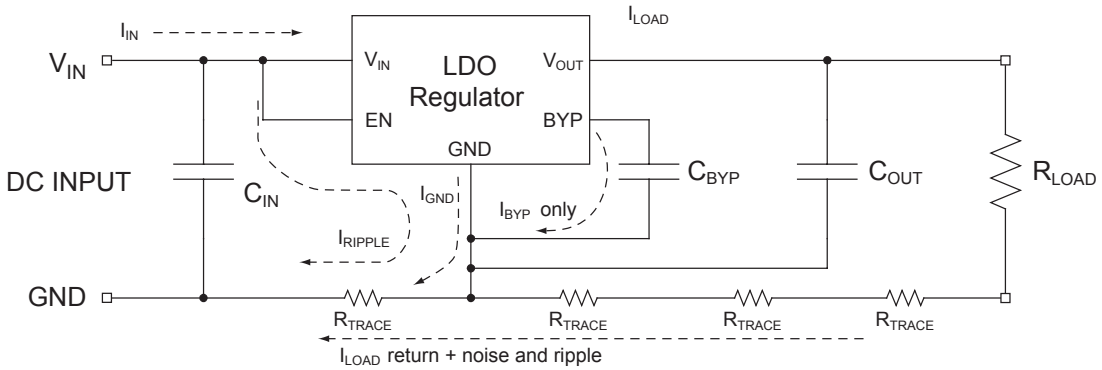


Figure 2: Recommended LDO Regulator Layout.

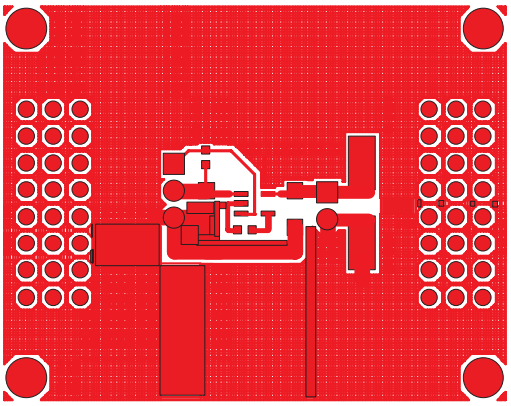


Figure 3: Evaluation Board
Component Side Layout.

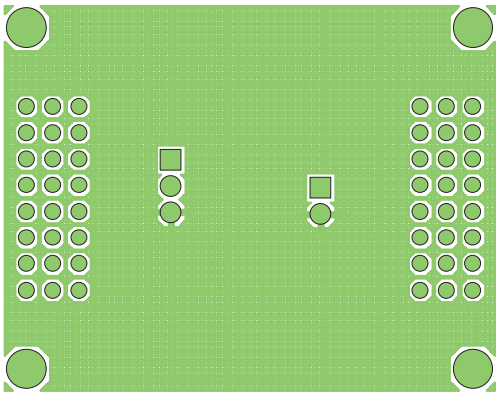


Figure 4: Evaluation Board
Solder Side Layout.

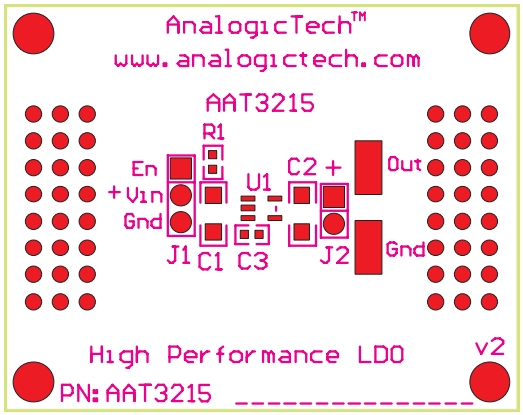


Figure 5: Evaluation Board
Top Side Silk Screen Layout /
Assembly Drawing.

Ordering Information

Output Voltage	Package	Marking[1]	Part Number (Tape and Reel)[2]
2.5V	SOT23-5	BQXYY	**AAT3215IGV-2.5-T1**
2.6V	SOT23-5	GKXYY	**AAT3215IGV-2.6-T1**
2.7V	SOT23-5	CHXYY	**AAT3215IGV-2.7-T1**
2.8V	SOT23-5	BSXYY	**AAT3215IGV-2.8-T1**
2.85V	SOT23-5	CIXYY	**AAT3215IGV-2.85-T1**
2.9V	SOT23-5	DVXYY	**AAT3215IGV-2.9-T1**
3.0V	SOT23-5	BTXYY	**AAT3215IGV-3.0-T1**
3.1V	SOT23-5	GJXYY	**AAT3215IGV-3.1-T1**
3.3V	SOT23-5	BUXYY	**AAT3215IGV-3.3-T1**
3.6V	SOT23-5	DVXYY	**AAT3215IGV-3.6-T1**
2.5V	SC70JW-8	BQXYY	**AAT3215IJS-2.5-T1**
2.6V	SC70JW-8	GKXYY	**AAT3215IJS-2.6-T1**
2.7V	SC70JW-8	CHXYY	**AAT3215IJS-2.7-T1**
2.8V	SC70JW-8	BSXYY	**AAT3215IJS-2.8-T1**
2.85V	SC70JW-8	CIXYY	**AAT3215IJS-2.85-T1**
2.9V	SC70JW-8	DVXYY	**AAT3215IJS-2.9-T1**
3.0V	SC70JW-8	BTXYY	**AAT3215IJS-3.0-T1**
3.3V	SC70JW-8	BUXYY	**AAT3215IJS-3.3-T1**

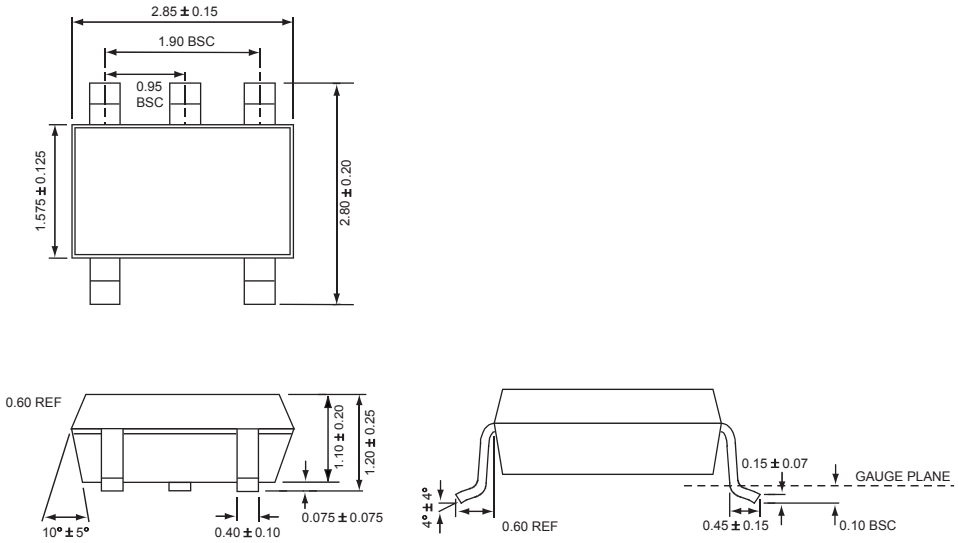


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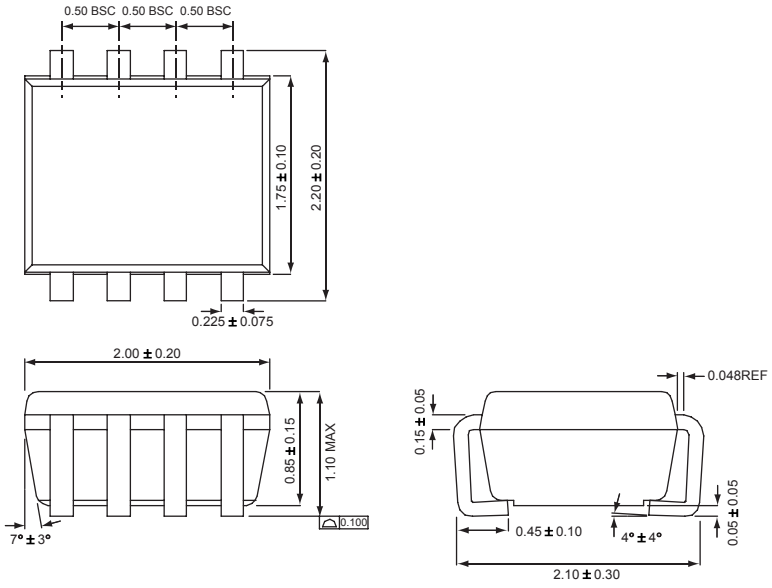
1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

Package Information

SOT23-5



SC70JW-8



All dimensions in millimeters.

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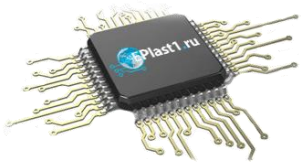
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