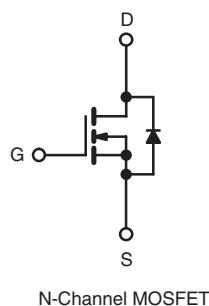
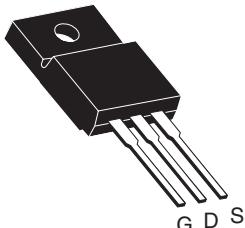


Power MOSFET

PRODUCT SUMMARY		
V _{DS} (V)	200	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.18
Q _g (Max.) (nC)	70	
Q _{gs} (nC)	13	
Q _{gd} (nC)	39	
Configuration	Single	

TO-220 FULLPAK


ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI640GPbF SiHFI640G-E3
SnPb	IRFI640G SiHFI640G

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	200	
Gate-Source Voltage	V _{GS}	± 20	V
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D
		T _C = 100 °C	
Pulsed Drain Current ^a	I _{DM}	39	A
Linear Derating Factor		0.32	W/°C
Single Pulse Avalanche Energy ^b	E _{AS}	430	mJ
Repetitive Avalanche Current ^a	I _{AR}	9.8	A
Repetitive Avalanche Energy ^a	E _{AR}	4.0	mJ
Maximum Power Dissipation	P _D	40	W
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 6.7 mH, R_G = 25 Ω, I_{AS} = 9.8 A (see fig. 12).

c. I_{SD} ≤ 18 A, dI/dt ≤ 150 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.

d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply


RoHS*
COMPLIANT

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS $T_J = 25^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25°C , $I_D = 1 \text{ mA}$		-	0.29	-	$^{\circ}\text{C}/\text{C}$
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	25	μA
		$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$	$I_D = 5.9 \text{ A}^b$	-	-	0.18	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50 \text{ V}$	$I_D = 5.9 \text{ A}^b$	5.2	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1.0 \text{ MHz}$, see fig. 5		-	1300	-	pF
Output Capacitance	C_{oss}			-	400	-	
Reverse Transfer Capacitance	C_{rss}			-	130	-	
Drain to Sink Capacitance	C	$f = 1.0 \text{ MHz}$		-	12	-	
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 18 \text{ A}$, $V_{DS} = 160 \text{ V}$, see fig. 6 and 13 ^b	-	-	70	nC
Gate-Source Charge	Q_{gs}			-	-	13	
Gate-Drain Charge	Q_{gd}			-	-	39	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}$, $I_D = 18 \text{ A}$, $R_G = 9.1 \Omega$, $R_D = 5.4 \Omega$, see fig. 10 ^b		-	14	-	ns
Rise Time	t_r			-	51	-	
Turn-Off Delay Time	$t_{d(off)}$			-	45	-	
Fall Time	t_f			-	36	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.8	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	39	
Body Diode Voltage	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_S = 9.8 \text{ A}$, $V_{GS} = 0 \text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_F = 18 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}^b$		-	300	610	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.4	7.1	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width $\leq 300 \mu\text{s}$; duty cycle ≤ 2

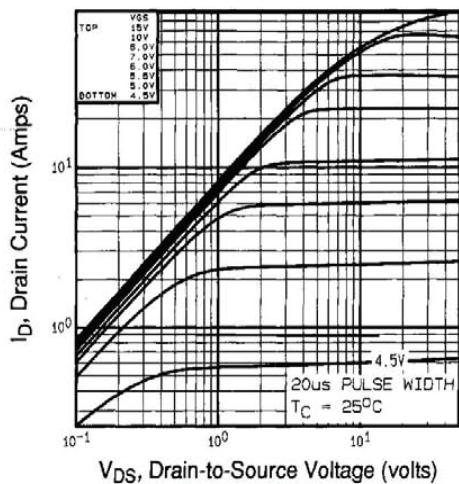
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

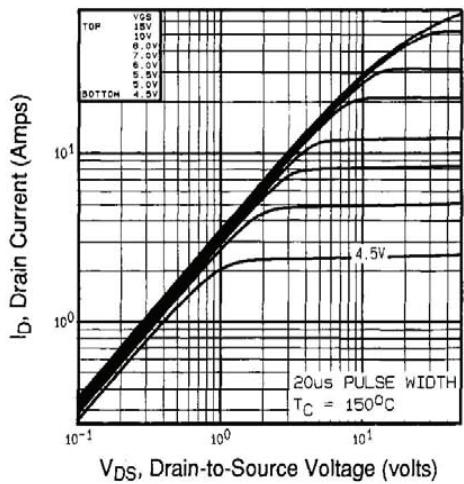
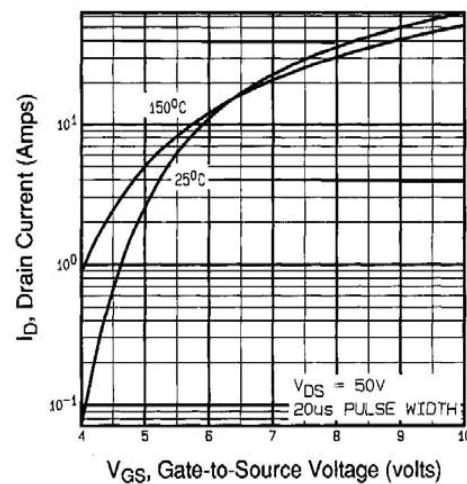
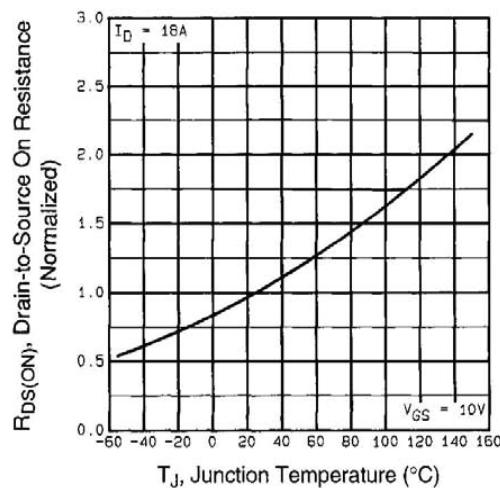


Fig. 2 - Typical Output Characteristics, $T_C = 150^\circ\text{C}$



IRFI640G, SiHFI640G

Vishay Siliconix

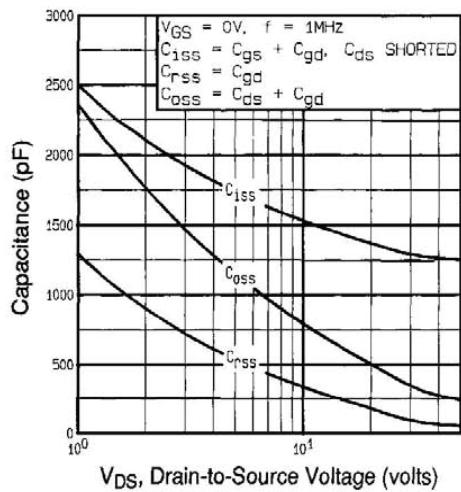


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

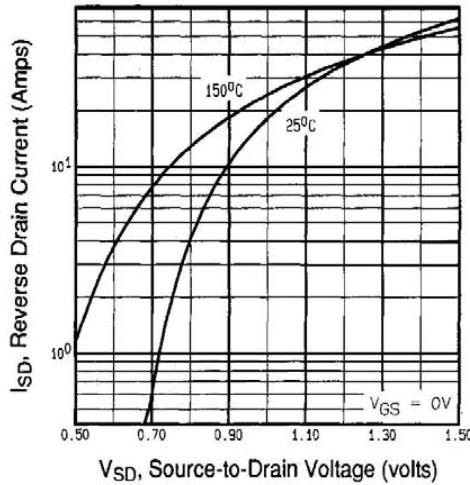


Fig. 7 - Typical Source-Drain Diode Forward Voltage

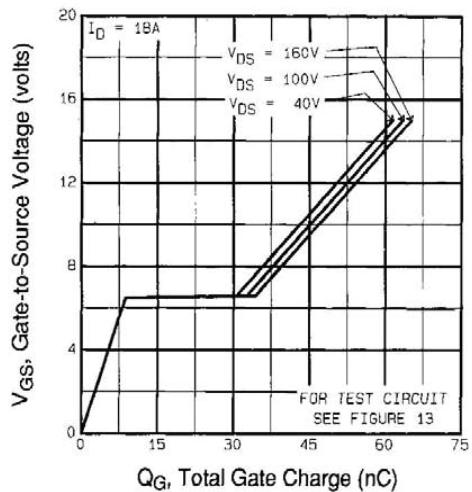


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

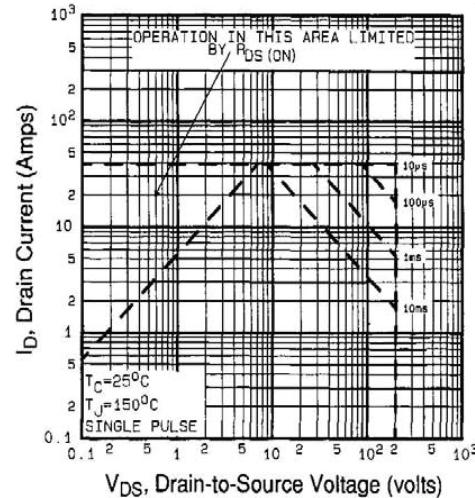


Fig. 8 - Maximum Safe Operating Area

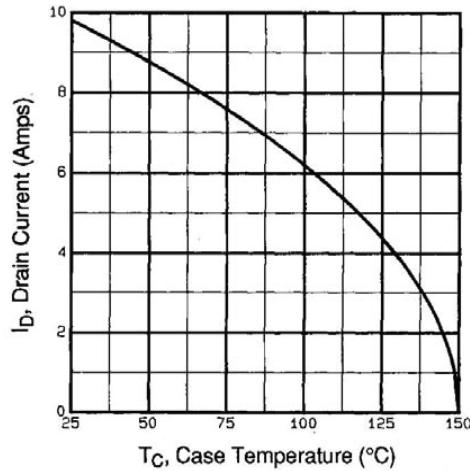


Fig. 9 - Maximum Drain Current vs. Case Temperature

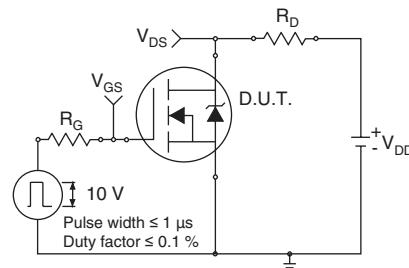


Fig. 10a - Switching Time Test Circuit

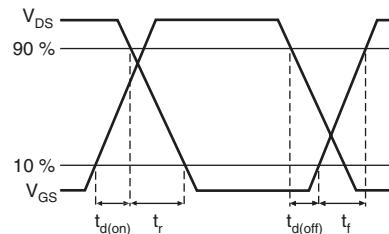


Fig. 10b - Switching Time Waveforms

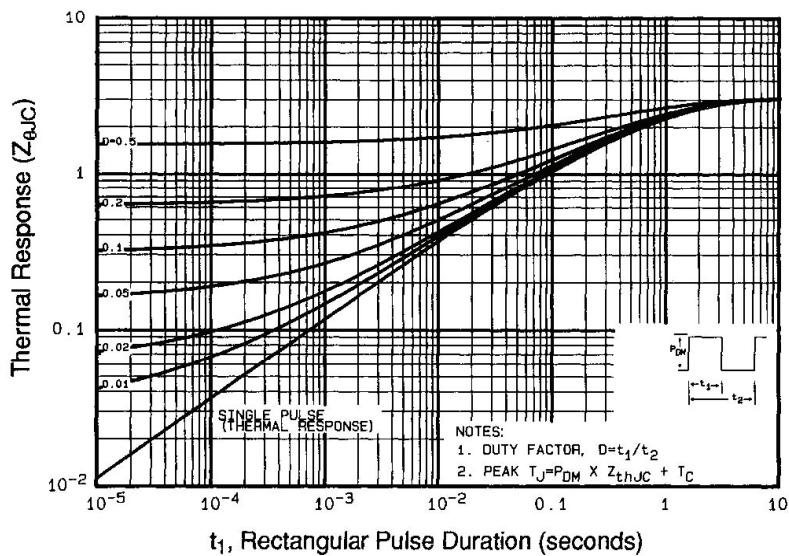


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

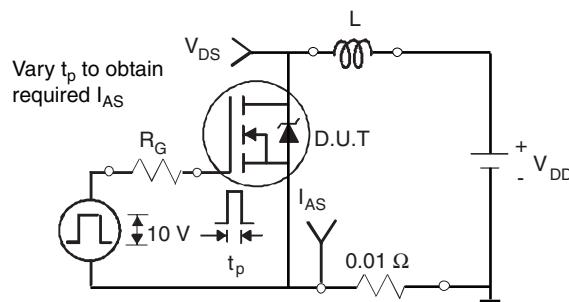


Fig. 12a - Unclamped Inductive Test Circuit

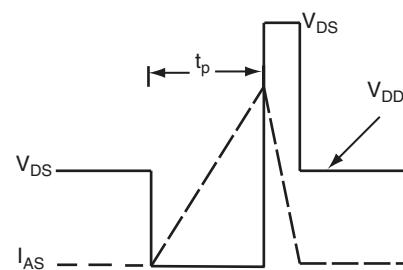


Fig. 12b - Unclamped Inductive Waveforms

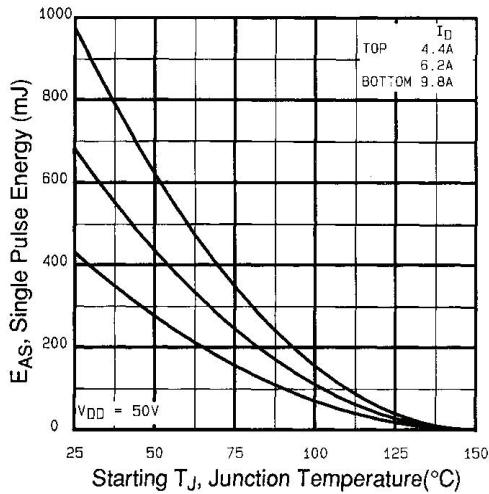


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

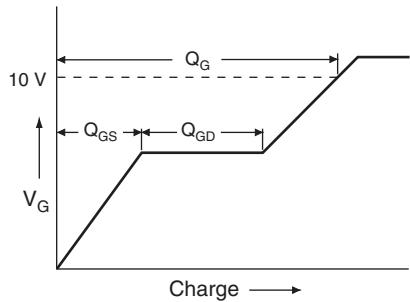


Fig. 13a - Basic Gate Charge Waveform

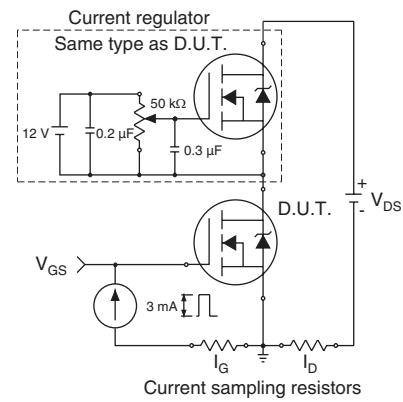
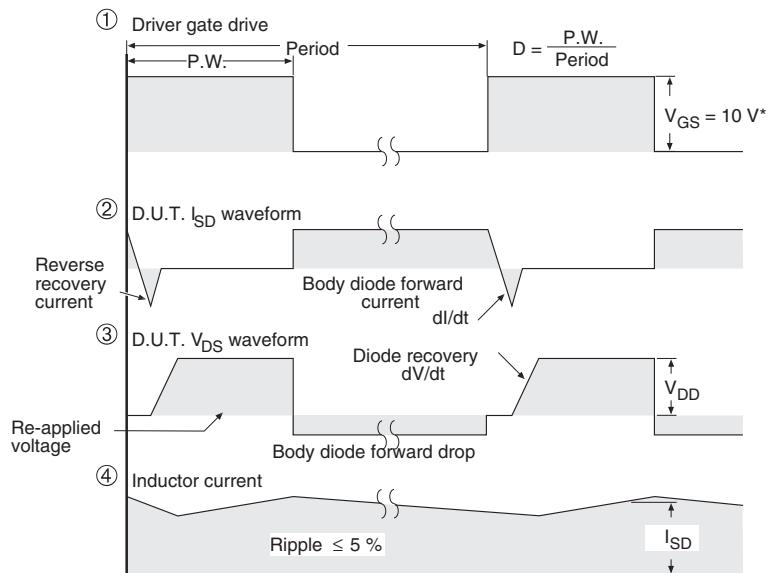
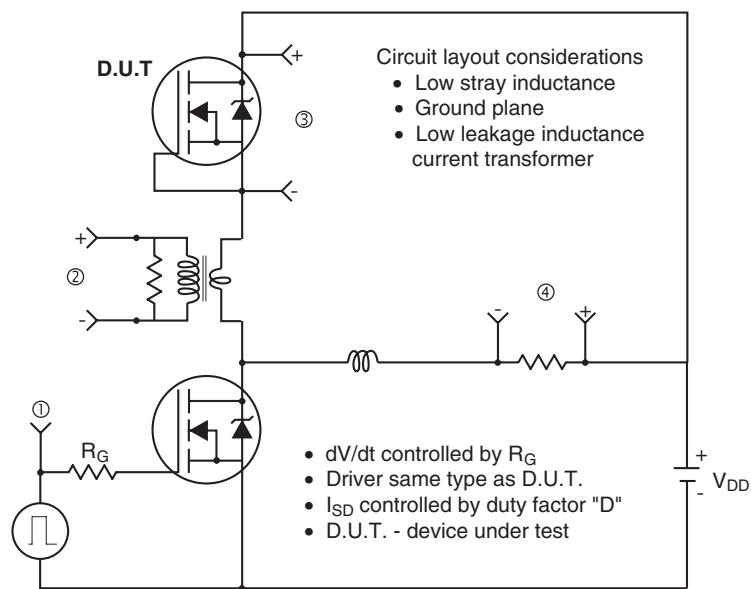


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 \text{ V}$ for logic level devices

Fig. 14 - For N-Channel



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- Техническая поддержка проекта, помошь в подборе аналогов, поставка прототипов;
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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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