

# ESD5205

## Transient Voltage Suppressors

### Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD5205 transient voltage suppressor is designed to protect high speed data lines from ESD. Low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

#### Features

- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- This is a Pb-Free Device

#### Typical Applications

- $\mu$ SD Connector

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation, 8 x 20 $\mu\text{s}$	$P_{PK}$	18	W
Operating Junction Temperature Range	$T_J$	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	$T_L$	260	$^\circ\text{C}$
IEC 61000-4-2 Contact (ESD)	ESD	$\pm 15$	kV
IEC 61000-4-2 Air (ESD)	ESD	$\pm 15$	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



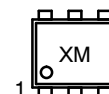
ON Semiconductor®

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#### MARKING DIAGRAM

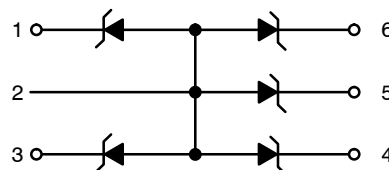


SOT-963  
CASE 527AD



X = Specific Device Code  
M = Month Code

#### PIN CONFIGURATION AND SCHEMATIC



#### ORDERING INFORMATION

Device	Package	Shipping
ESD5205P6T6G	SOT-963 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V <sub>RWM</sub>	I/O Pin to GND			5.0	V
Breakdown Voltage	V <sub>BR</sub>	I <sub>T</sub> = 1 mA, I/O Pin to GND	5.5			V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 5 V, I/O Pin to GND			1.0	μA
Clamping Voltage (Note 1)	V <sub>C</sub>	I <sub>PP</sub> = 1 A, I/O Pin to GND (8 x 20 μs pulse) I <sub>PP</sub> = 2 A, I/O Pin to GND (8 x 20 μs pulse)			9 10	V
Clamping Voltage (Note 2)	V <sub>C</sub>	IEC61000-4-2, ±8 KV Contact	See Figures 1 and 2			V
Clamping Voltage TLP (Note 3)	V <sub>C</sub>	I <sub>PP</sub> = 8 A I <sub>PP</sub> = 16 A I <sub>PP</sub> = -8 A I <sub>PP</sub> = -16 A		11.4 15.6 -4.5 -8.1		
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V, f = 1 MHz between I/O Pins and GND			9.0	pF

1. Surge current waveform per Figure 5.
2. For test procedure see Figures 3 and 4 and application note AND8307/D.
3. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 100 ns, t<sub>r</sub> = 4 ns, averaging window; t<sub>1</sub> = 30 ns to t<sub>2</sub> = 60 ns.

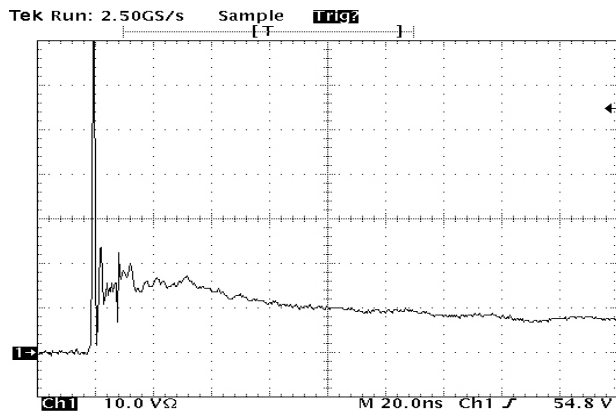


Figure 1. IEC61000-4-2 +8 KV Contact ESD Clamping Voltage

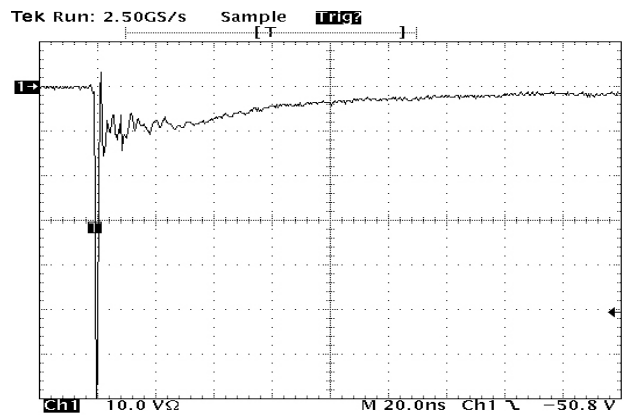


Figure 2. IEC61000-4-2 -8 KV Contact Clamping Voltage

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

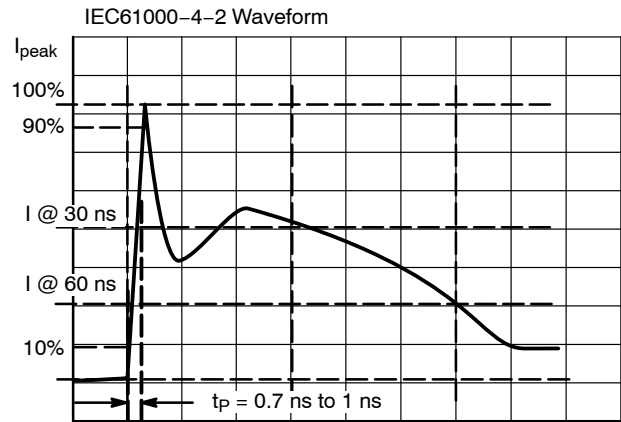


Figure 3. IEC61000-4-2 Spec

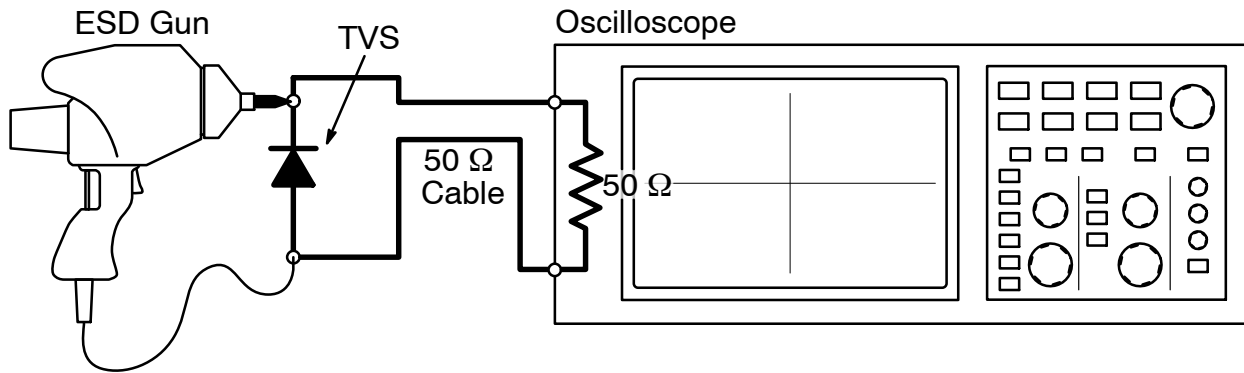


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note  
AND8308/D – Interpretation of Datasheet Parameters  
for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

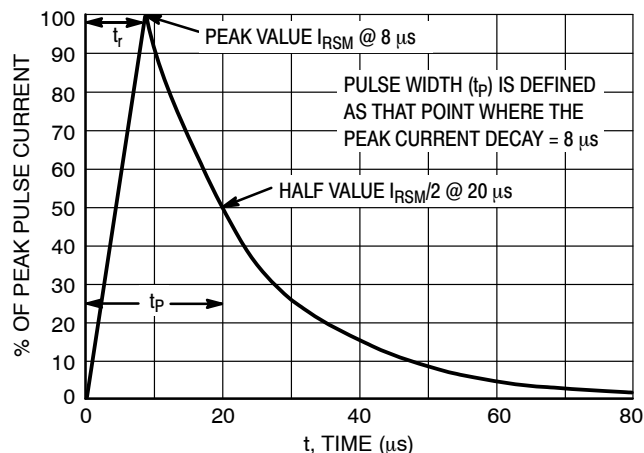
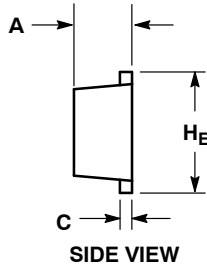
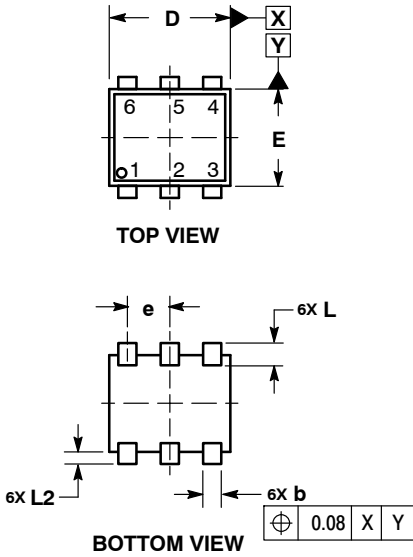


Figure 5. 8 X 20  $\mu$ s Pulse Waveform

# ESD5205

## PACKAGE DIMENSIONS

### SOT-963 CASE 527AD ISSUE E

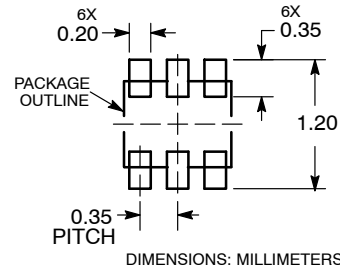


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H <sub>E</sub>	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

### RECOMMENDED MOUNTING FOOTPRINT



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