

## Specification

### Quad Small Form-factor Pluggable Plus

### QSFP+ Product



**TQS-Q1LH8-X11xx**

**Distance**

| Part Number     | Description                           |
|-----------------|---------------------------------------|
| TQS-Q1LH8-X1101 | 40Gbps QSFP+ Active Optical Cable 1m  |
| TQS-Q1LH8-X1103 | 40Gbps QSFP+ Active Optical Cable 3m  |
| TQS-Q1LH8-X1105 | 40Gbps QSFP+ Active Optical Cable 5m  |
| TQS-Q1LH8-X1107 | 40Gbps QSFP+ Active Optical Cable 7m  |
| TQS-Q1LH8-X1110 | 40Gbps QSFP+ Active Optical Cable 10m |
| TQS-Q1LH8-X1120 | 40Gbps QSFP+ Active Optical Cable 20m |

| Model Name      | Voltage | Category  | Device type | Interface | LOS    | Temperature |
|-----------------|---------|-----------|-------------|-----------|--------|-------------|
| TQS-Q1LH8-X11xx | 3.3V    | With DDMI | VCSEL/PIN   | CML/CML   | LVTTTL | 0°C ~ +70°C |

## Description

Formerica OptoElectronics Inc. Quad Small Form-factor Pluggable (QSFP) product is a new high speed pluggable I/O interface products. This interconnecting system offers 4 channels and maximum bandwidth of 40Gbps which are based on the proprietary technique Silicon Optical Bench (SiOB). This module provides high performance and excellent efficiency in the optical communication.

## Features

- Compliant with 40G Ethernet IEEE 802.3ae 40GBASE-SR4 standards
- QSFP footprint (Quad small form-factor, pluggable)
- Supports 40 Gbps data rate links of up to 100 m
- Compliant with QDR/DDR Infiniband data rates
- Hot pluggable electrical interface
- RoHS Compliant

## Applications

- 40GBASE-SR4 Ethernet links
- Infiniband QDR and DDR interconnects
- Client-side 40G Telecom connections

## Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

| Parameter                        | Symbol    | Min  | Typical | Max     | Unit | Note |
|----------------------------------|-----------|------|---------|---------|------|------|
| Storage Temperature              | Ts        | 0    |         | 70      | °C   | 1    |
| Relative Humidity                | RH        | 5    |         | 85      | %    | 2    |
| Data Input Voltage- Single Ended |           | -0.5 |         | Vcc+0.5 |      |      |
| Center Wavelength                | $\lambda$ | 840  |         | 860     | nm   |      |

### Notes:

1. Limited by the fiber cable jacket, not the active ends.
2. Non-condensing.

## Recommended Operatin Conditions

| Parameter                                  | Symbol | Min   | Typical           | Max     | Unit | Note |
|--|--------|-------|-------------------|---------|------|------|
| Case Temperature                           | Top    | 0     | 40                | 70      | °C   |      |
| 3.3 V Power Supply Voltage                 | Vcc    | 3.135 | 3.3               | 3.465   | V    |      |
| Signal Rate per Channel                    |        | 2.5   |                   | 10.3125 | GB/s | 1    |
| Control* Input Voltage High                | Vih    | 2     |                   | Vcc+0.3 | V    |      |
| Control* Input Voltage Low                 | Vil    | -0.3  |                   | 0.8     | V    |      |
| Two Wire Serial (TWS) Interface Clock Rate |        |       | 100               |         | kHz  |      |
| Power Supply Noise                         |        |       |                   | 50      | mV   | 2    |
| Receiver Differential Data Output Load     |        |       | 100               |         | Ohms |      |
| Standard Cable Lengths                     |        | 3     |                   | 100     | m    |      |
| Bit Error Ratio                            |        |       | 10 <sup>-12</sup> |         |      | 3    |

### Notes:

1. Lane speed up to 12.5-Gbps is available upon customer requests.
2. Power supply noise is defined as peak-to-peak noise amplitude over 1K to 15 MHz frequency range at host supply side by the recommended power supply filter for module. See Section 10 for the recommended power supply filter.
3. Bit-Error-Rate (BER) is tested with PRBS 2<sup>31</sup>-1 pattern.

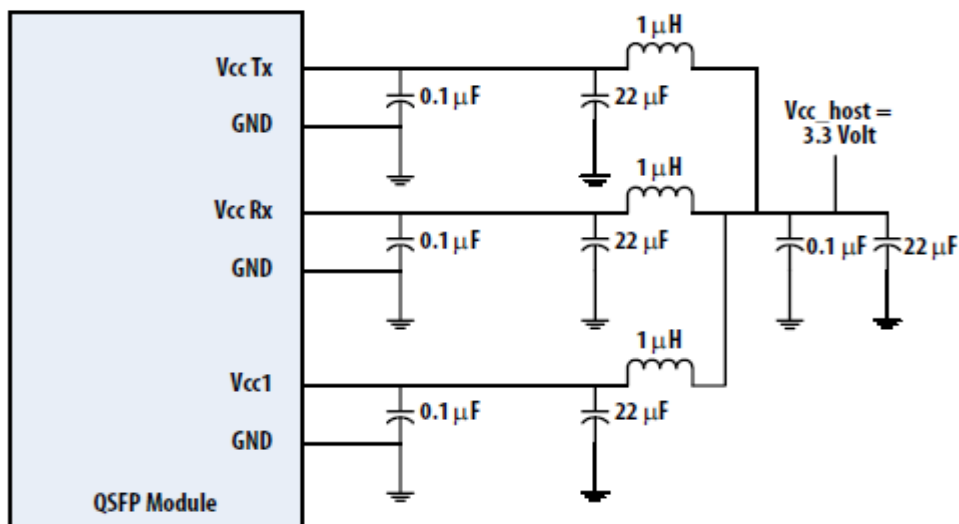
## Electrical Characteristics

| Parameter   | Symbol          | Min | Typical | Max        | Unit | Note       |
|---|-----------------|-----|---------|------------|------|------------|
| <b>Transceiver</b>                                  |                 |     |         |            |      |            |
| Power Consumption                                   |                 |     |         | 1.5        | W    |            |
| Supply Current                                      |                 |     |         | 420        | mA   |            |
| Initialization Time                                 | tpwr init       |     |         | 2000       | ms   | 1          |
| <b>Receiver</b>                                     |                 |     |         |            |      |            |
| Data Output Differential Peak-to-Peak Voltage Swing | $\Delta VDO$ pp | 200 |         | 900        | mVpp |            |
| Output Total Jitter                                 |                 |     |         | 62         | ps   |            |
| BER   |                 |     |         | $10^{-12}$ |      | PRBS3<br>1 |

### Notes:

1. "Initialization Time" is the time from when the supply voltages reach and remain above the minimum "Recommended Operating Conditions" to the time when the module enables TWS access. The module at that point is fully functional.

## Recommended Host Board POWER Supply Circuit



### QSFP+ Module Pad Assignments and Descriptions



| Pin | Logic       | Symbol  | Description                         | Plug Sequence | Notes |
|-----|-------------|---------|-------------------------------------|---------------|-------|
| 1   |             | GND     | Ground                              | 1             | 1     |
| 2   | CML-I       | Tx2n    | Transmitter Inverted Data Input     | 3             |       |
| 3   | CML-I       | Tx2p    | Transmitter Non-Inverted Data Input | 3             |       |
| 4   |             | GND     | Ground                              | 1             | 1     |
| 5   | CML-I       | Tx4n    | Transmitter Inverted Data Input     | 3             |       |
| 6   | CML-I       | Tx4p    | Transmitter Non-Inverted Data Input | 3             |       |
| 7   |             | GND     | Ground                              | 1             | 1     |
| 8   | LVTTL-I     | ModSelL | Module Select                       | 3             |       |
| 9   | LVTTL-I     | ResetL  | Module Reset                        | 3             |       |
| 10  |             | Vcc Rx  | +3.3V Power Supply Receiver         | 2             | 2     |
| 11  | LVC MOS-I/O | SCL     | 2-wire serial interface clock       | 3             |       |
| 12  | LVC MOS-I/O | SDA     | 2-wire serial interface data        | 3             |       |
| 13  |             | GND     | Ground                              | 1             | 2     |
| 14  | CML-O       | Rx3p    | Receiver Non-Inverted Data Output   | 3             |       |
| 15  | CML-O       | Rx3n    | Receiver Inverted Data Output       | 3             |       |
| 16  |             | GND     | Ground                              | 1             | 1     |

|    |         |         |                                     |   |   |
|----|---------|---------|-------------------------------------|---|---|
| 17 | CML-O   | Rx1p    | Receiver Non-Inverted Data Output   | 3 |   |
| 18 | CML-O   | Rx1n    | Receiver Inverted Data Output       | 3 |   |
| 19 |         | GND     | Ground                              | 1 | 1 |
| 20 |         | GND     | Ground                              | 1 | 1 |
| 21 | CML-O   | Rx2n    | Receiver Inverted Data Output       | 3 |   |
| 22 | CML-O   | Rx2p    | Receiver Non-Inverted Data Output   | 3 |   |
| 23 |         | GND     | Ground                              | 1 | 1 |
| 24 | CML-O   | Rx4n    | Receiver Inverted Data Output       | 3 |   |
| 25 | CML-O   | Rx4p    | Receiver Non-Inverted Data Output   | 3 |   |
| 26 |         | GND     | Ground                              | 1 | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present                      | 3 |   |
| 28 | LVTTL-O | IntL    | Interrupt                           | 3 |   |
| 29 |         | Vcc Tx  | +3.3V Power supply transmitter      | 2 | 2 |
| 30 |         | Vcc1    | +3.3V Power supply                  | 2 | 2 |
| 31 | LVTTL-I | LPMode  | Low Power Mode                      | 3 |   |
| 32 |         | GND     | Ground                              | 1 | 1 |
| 33 | CML-I   | Tx3p    | Transmitter Non-Inverted Data Input | 3 |   |
| 34 | CML-I   | Tx3n    | Transmitter Inverted Data Input     | 3 |   |
| 35 |         | GND     | Ground                              | 1 | 1 |
| 36 | CML-I   | Tx1p    | Transmitter Non-Inverted Data Input | 3 |   |
| 37 | CML-I   | Tx1n    | Transmitter Inverted Data Input     | 3 |   |
| 38 |         | GND     | Ground                              | 1 | 1 |

**Note :**

1. **GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.**
2. **Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Host board power supply circuit. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500 mA.**

## Memory Map



## Module Outline

Unit: mm



## ESD

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.





### Contact Information

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