

## 2-Output LVPECL Fibre Channel (FC) and Ethernet Clock Generator

### Features

- Two differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies:
  - Ethernet: 50MHz, 100MHz, 150MHz, 156.25MHz, 200MHz
  - Fibre Channel: 53.125MHz, 106.25MHz, 159.375MHz, 187.5MHz, 212.5MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (12kHz – 20MHz): 0.28ps (typical)
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz – 20MHz): 0.32ps (typical)
- RMS phase jitter @ 156.25MHz, using a 26.041667MHz crystal (12kHz – 20MHz): 0.30ps (typical)
- Full 3.3V or 2.5V supply modes
- Industrial operating temperature
- Available in lead-free package: 20-TSSOP

### Description

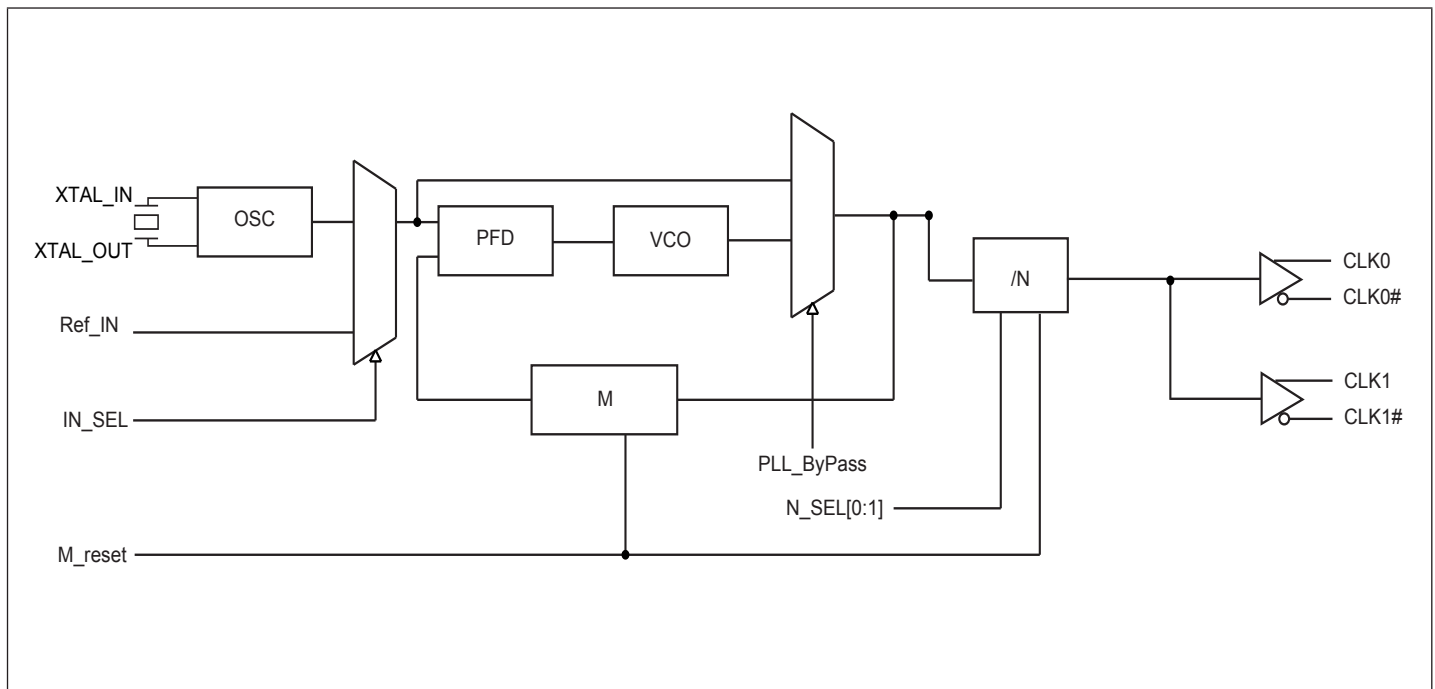
The PI6LC48P02 is a 2-output LVPECL synthesizer optimized to generate Fibre Channel, Ethernet and storage reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 26.5625MHz crystal, the most popular Fibre Channel (FC) frequencies can be generated based on the settings of 2 frequency select pins. Using 25MHz Xtal, most Ethernet frequencies including 100MHz can be generated, while using 26.041667MHz Xtal, 156.25MHz can be generated for Networking applications.

The PI6LC48P02 uses Pericom's proprietary low phase noise PLL technology to achieve ultra low phase jitter, it is ideal for Networking, data center, and storage systems.

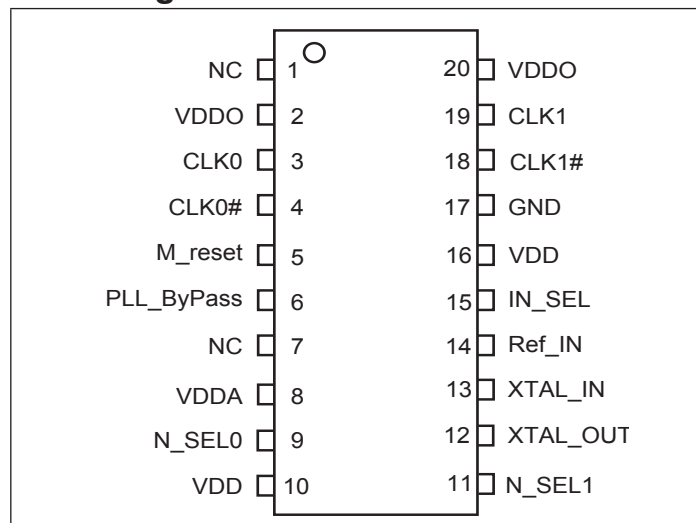
### Applications

- Networking and Data Center Server systems
- Fibre Channel (FC) and Storage systems

### Block Diagram



## Pin Configuration



## Pinout Table

| Pin No. | Pin Name       | I/O Type |           | Description   |
|---------|----------------|----------|-----------|---|
| 1, 7    | NC             |          |           | No connection   |
| 2, 20   | VDDO           | Power    | -         | Output Power Supply   |
| 3, 4    | CLK0, CLK0#    | Output   | -         | LVPECL Output clock 0   |
| 5       | M_reset        | Input    | Pull-down | Master reset. "1", CLK0/CLK1 go to "low", CLK0#/CLK1# go to "high"; "0" outputs are enabled |
| 6       | PLL_ByPass     | Input    | Pull-down | PLL bypass select. "0" PLL is enabled, "1" PLL is bypassed                                  |
| 8       | VDDA           | Power    | -         | Analog Power Supply   |
| 9, 11   | N_SEL0, N_SEL1 | Input    | Pull-down | Output frequency select   |
| 10, 16  | VDD            | Power    | -         | Core Power Supply   |
| 12, 13  | XOUT, XIN      | Crystal  | -         | Crystal input and output  |
| 14      | Ref_IN         | Input    | Pull-down | CMOS reference clock input  |
| 15      | IN_SEL         | Input    | Pull-down | "0" selects Crystal, "1" selects reference input  |
| 17      | GND            | Ground   | -         | Ground  |
| 18, 19  | CLK1#, CLK1    | Output   | -         | LVPECL Output clock 1   |

### Output Frequency Selection Table

| Xtal Frequency (MHz) | N_SEL1 N_SEL0 | Output Frequency (MHz) |
|----------------------|---------------|------------------------|
| 25                   | 0 0           | 200                    |
|                      | 0 1           | 150                    |
|                      | 1 0           | 100                    |
|                      | 1 1           | 50                     |
| 26.5625              | 0 0           | 212.5                  |
|                      | 0 1           | 159.375                |
|                      | 1 0           | 106.25                 |
|                      | 1 1           | 53.125                 |
| 23.4375              | 0 0           | 187.5                  |
| 26.041667            | 0 1           | 156.25                 |

### Typical Crystal Requirement

| Parameter                          | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-------------|---------|---------|----------|
| Mode of Oscillation                | Fundamental |         |         |          |
| Frequency                          | 23.33       |         | 28.33   | MHz      |
| Equivalent Series Resistance (ESR) |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |             |         | 7       | pF       |
| Drive Level                        |             |         | 1       | mW       |

### Recommended Crystal Specification

Pericom recommends:

- a) FL2650003, SMD 3.2x2.5(4P), 26.5625MHz, CL=18pF, +/-25ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>
- b) FY2650002, SMD 5x3.2(4P), 26.5625MHz, CL=18pF, +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25MHz, CL=18pF, +/-20ppm, <http://www.pericom.com/pdf/datasheets/se/FL.pdf>
- d) FY2500091, SMD 5x3.2(4P), 25MHz, CL=18pF, +/-30ppm, [http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)

For other crystal options, please contact Pericom sales.

**Maximum Ratings** (Over operating free-air temperature range)

|   |                 |
|---|-----------------|
| Storage Temperature.....                    | -65°C to +155°C |
| Ambient Temperature with Power Applied..... | -40°C to +85°C  |
| Supply Voltage .....                        | -0.5 to +3.7V   |
| ESD Protection (HBM) .....                  | 2000V           |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics**

**Power Supply DC Characterisitcs, (T<sub>A</sub> = -40°C to 85°C)**

| Symbol   | Parameter             | Condition | Min   | Typ | Max   | Units |
|--|-----------------------|-----------|-------|-----|-------|-------|
| V <sub>DD</sub> ,<br>V <sub>DDA</sub> , V <sub>DDO</sub> | Supply Voltage        |           | 2.97  | 3.3 | 3.63  | V     |
| V <sub>DD</sub> ,<br>V <sub>DDA</sub> , V <sub>DDO</sub> | Supply Voltage        |           | 2.375 | 2.5 | 2.625 | V     |
| I <sub>GND</sub>   | Power Supply Current  |           |       |     | 110   | mA    |
| I <sub>DDA</sub>   | Analog Supply Current |           |       |     | 30    | mA    |

**I<sub>V</sub>CMOS/LVTTL DC Characterisitcs, (T<sub>A</sub> = -40°C to 85°C)**

| Symbol          | Parameter          | Condition   | Min  | Typ | Max                   | Units |
|-----------------|--------------------|---|------|-----|-----------------------|-------|
| V <sub>IH</sub> | Input High Voltage | V <sub>DD</sub> = 3.3 V +/- 10%   | 2    |     | V <sub>DD</sub> + 0.3 | V     |
|                 |                    | V <sub>DD</sub> = 2.5 V +/- 5%  | 1.7  |     | V <sub>DD</sub> + 0.3 | V     |
| V <sub>IL</sub> | Input Low Voltage  | V <sub>DD</sub> = 3.3 V +/- 10%   | -0.3 |     | 0.8                   | V     |
|                 |                    | V <sub>DD</sub> = 2.5 V +/- 5%  | -0.3 |     | 0.7                   | V     |
| I <sub>IH</sub> | Input High Current | M_reset, PLL_ByPass, N_SEL[0:1],<br>IN_SEL, Ref_IN<br>V <sub>DD</sub> = V <sub>IN</sub> = 3.63V     |      |     | 150                   | µA    |
| I <sub>IL</sub> | Input Low Current  | M_reset, PLL_ByPass, N_SEL[0:1],<br>IN_SEL, Ref_IN<br>V <sub>DD</sub> = 3.63V, V <sub>IN</sub> = 0V | -5   |     |                       | µA    |

**Pin Characterisitcs**

| Symbol                 | Parameter          | Condition | Min | Typ | Max | Units |
|------------------------|--------------------|-----------|-----|-----|-----|-------|
| C <sub>IN</sub>        | Input Capacitance  |           |     | 4   |     | pF    |
| R <sub>PULLDOWNN</sub> | Pull down resistor |           |     | 51  |     | kΩ    |

**LVPECL DC Characteristics, ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ )**

| Symbol          | Parameter                          | Condition              | Min | Typ | Max | Units |
|-----------------|------------------------------------|------------------------|-----|-----|-----|-------|
| V <sub>OH</sub> | Output High Voltage <sup>(1)</sup> | V <sub>DD</sub> = 3.3V | 1.9 |     | 2.4 | V     |
|                 |                                    | V <sub>DD</sub> = 2.5V | 1.1 |     | 1.6 |       |
| V <sub>OL</sub> | Output Low Voltage <sup>(1)</sup>  | V <sub>DD</sub> = 3.3V | 1.2 |     | 1.6 | V     |
|                 |                                    | V <sub>DD</sub> = 2.5V | 0.4 |     | 0.8 |       |

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

**AC Electrical Characteristics, ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ )**

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

| Symbol                       | Parameter                                 | Condition                        | Min.   | Typ. | Max    | Units |
|------------------------------|---|----------------------------------|--------|------|--------|-------|
| f <sub>OUT</sub>             | Output Frequency                          | N_SEL[1:0] = 00                  | 186.67 |      | 226.67 | MHz   |
|                              |   | N_SEL[1:0] = 01                  | 140    |      | 170    | MHz   |
|                              |   | N_SEL[1:0] = 10                  | 93.33  |      | 113    | MHz   |
|                              |   | N_SEL[1:0] = 11                  | 46.67  |      | 56.67  | MHz   |
| t <sub>sk(0)</sub>           | Output Skew <sup>(1,3)</sup>              | Outputs at the same same loading |        | 30   |        | ps    |
| t <sub>jit(0)</sub>          | RMS Phase Jitter, (Random) <sup>(2)</sup> | 212.5MHz, (637kHz - 10MHz)       |        | 0.17 |        | ps    |
|                              |   | 212.5MHz, (12kHz - 20MHz)        |        | 0.28 |        | ps    |
|                              |   | 200MHz, (1.875MHz - 20MHz)       |        | 0.10 |        | ps    |
|                              |   | 200MHz, (12kHz - 20MHz)          |        | 0.29 |        | ps    |
|                              |   | 156.25MHz, (1.875MHz - 20MHz)    |        | 0.15 |        | ps    |
|                              |   | 156.25MHz, (12kHz - 20MHz)       |        | 0.30 |        | ps    |
|                              |   | 159.375MHz, (637kHz - 10MHz)     |        | 0.20 |        | ps    |
|                              |   | 159.375MHz, (12kHz - 20MHz)      |        | 0.30 |        | ps    |
|                              |   | 150MHz, (1.875MHz - 20MHz)       |        | 0.15 |        | ps    |
|                              |   | 150MHz, (12kHz - 20MHz)          |        | 0.31 |        | ps    |
|                              |   | 106.25MHz, (637kHz - 10MHz)      |        | 0.20 |        | ps    |
|                              |   | 106.25MHz, (12kHz - 20MHz)       |        | 0.32 |        | ps    |
|                              |   | 100MHz, (1.875MHz - 20MHz)       |        | 0.18 |        | ps    |
|                              |   | 100MHz, (12kHz - 20MHz)          |        | 0.32 |        | ps    |
|                              |   | 53.125MHz, (637kHz - 10MHz)      |        | 0.25 |        | ps    |
|                              |   | 53.125MHz, (12kHz - 20MHz)       |        | 0.42 |        | ps    |
|                              |   | 50MHz, (1.875MHz - 10MHz)        |        | 0.36 |        | ps    |
|                              |   | 50MHz, (12kHz - 20MHz)           |        | 0.60 |        | ps    |
| 187.5MHz, (1.875MHz - 10MHz) |   | 0.11                             |        | ps   |        |       |
| 187.5MHz, (12kHz - 20MHz)    |   | 0.28                             |        | ps   |        |       |

### AC Electrical Characteristics, (T<sub>A</sub> = -40°C to 85°C) Cont.

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

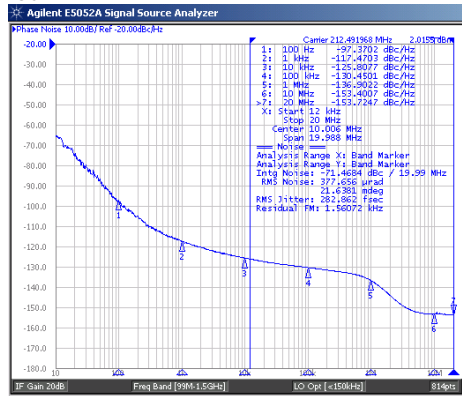
| Symbol                          | Parameter             | Condition  | Min. | Typ. | Max | Units |
|---------------------------------|-----------------------|------------|------|------|-----|-------|
| t <sub>R</sub> / t <sub>F</sub> | Output Rise/Fall Time | 20% to 80% |      |      | 400 | ps    |
| O <sub>DC</sub>                 | Output Duty Cycle     |            | 48   |      | 52  | %     |

**Note:**

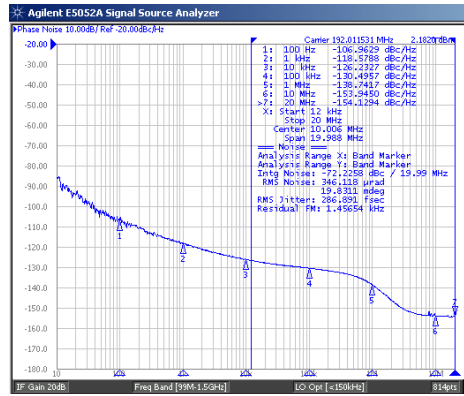
1. Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
2. Please refer to the Phase Noise Plots.
3. This parameter is defined in accordance with JEDEC Standard 65.

### Phase Noise Plots

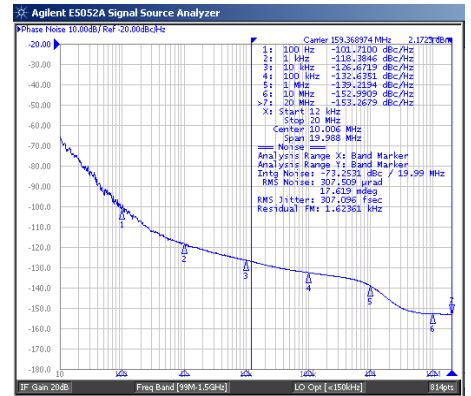
f<sub>OUT</sub> = 212.5MHz



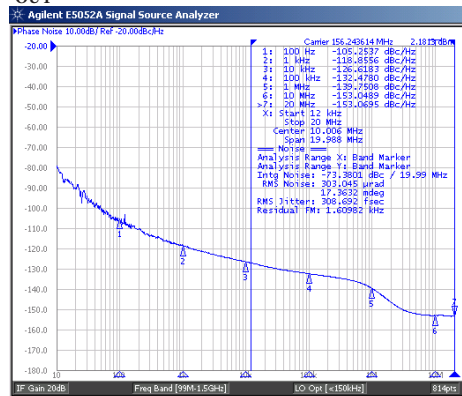
f<sub>OUT</sub> = 187.5MHz



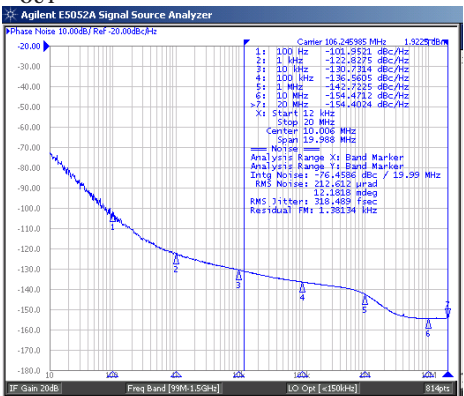
f<sub>OUT</sub> = 159.375MHz



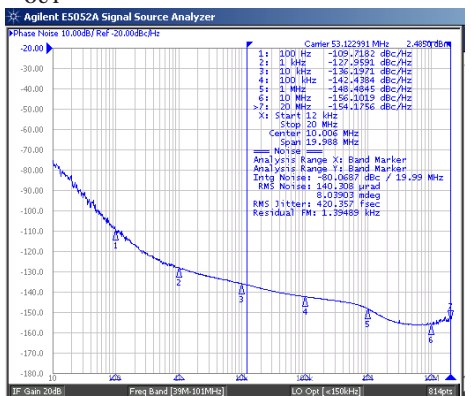
f<sub>OUT</sub> = 156.25MHz



f<sub>OUT</sub> = 106.25MHz

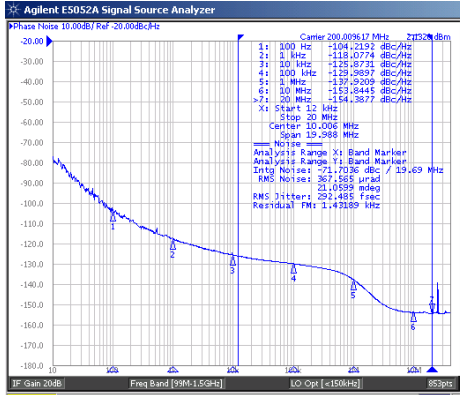


f<sub>OUT</sub> = 53.125MHz

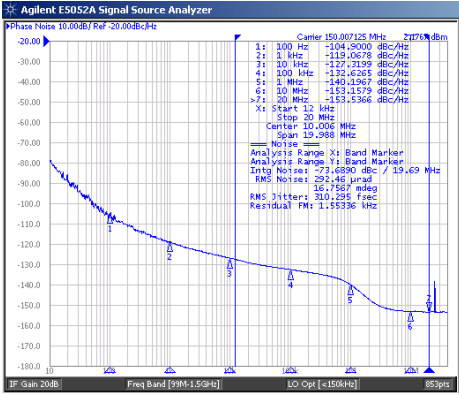


**Phase Noise Plots**

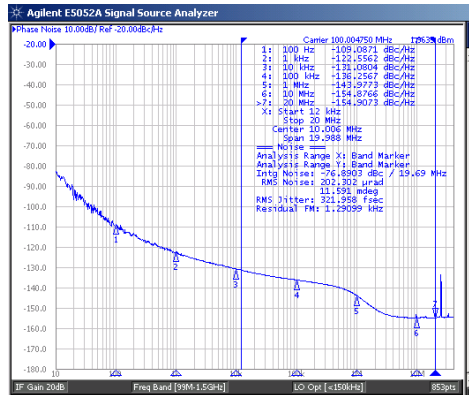
$f_{OUT} = 200\text{MHz}$



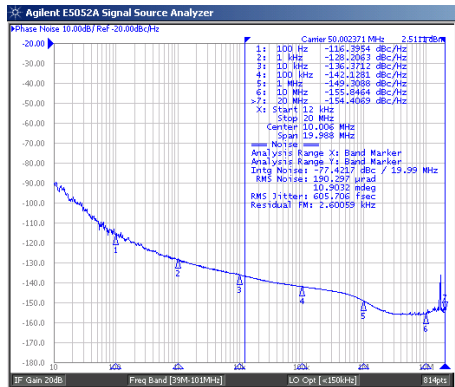
$f_{OUT} = 150\text{MHz}$



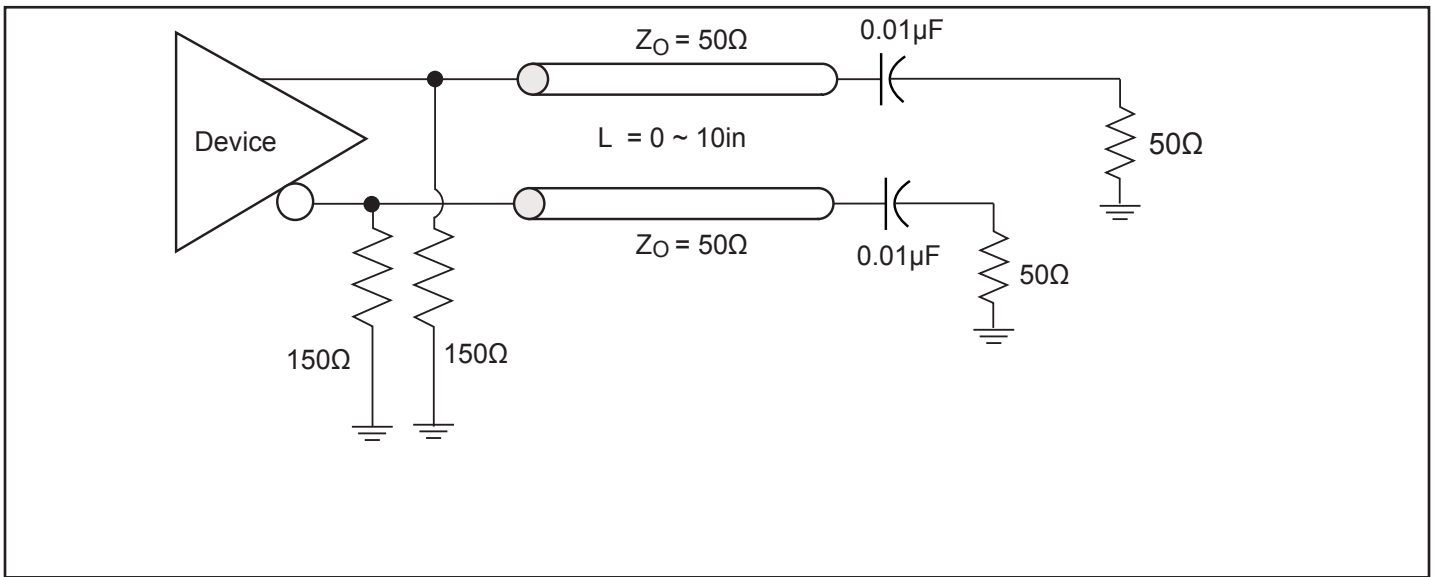
$f_{OUT} = 100\text{MHz}$



$f_{OUT} = 50\text{MHz}$

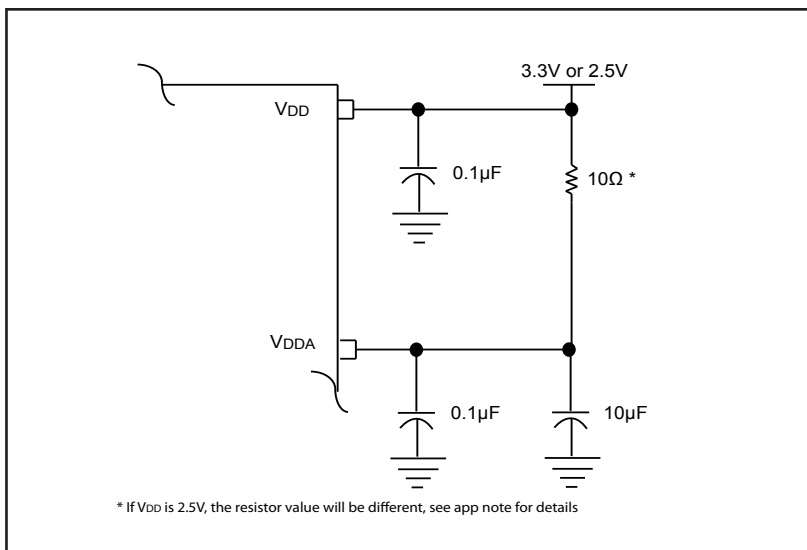


**LVPECL Test Circuit**



**Power Supply Filtering Techniques**

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and 0.1μF bypass capacitors should be used for each pin. Figure below illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional 10Ω resistor along with a 10μF bypass capacitor be connected to the  $V_{DDA}$  pin.





## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. A 1kΩ resistor can be tied from XTAL\_IN to ground for additional protection.

#### Ref\_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref\_IN to ground can provide additional protection.

#### LVC MOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.

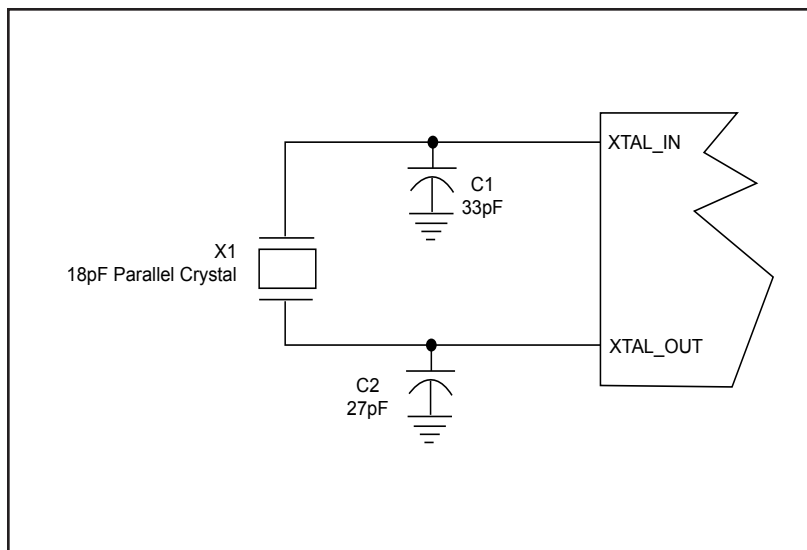
### Outputs:

#### LVPECL Outputs:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

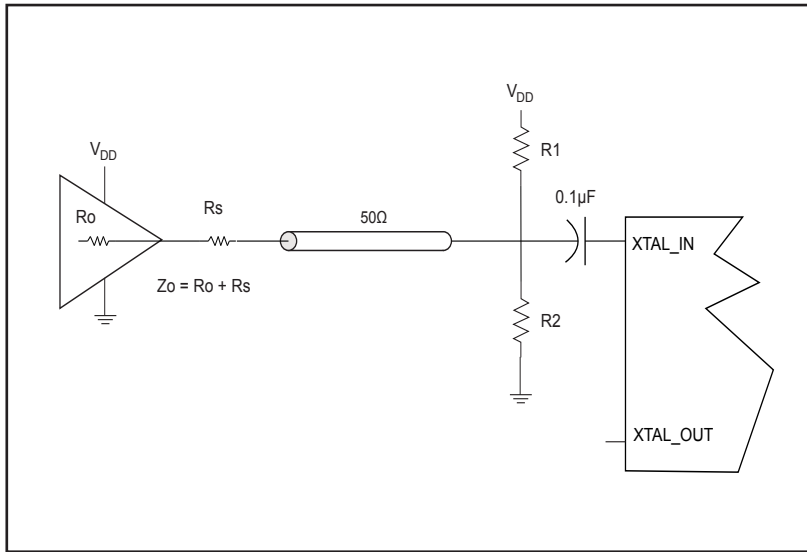
## Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



**LVCMOS to XTAL Interface**

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Thermal Information**

| Symbol        | Description                            |           |
|---------------|--|-----------|
| $\Theta_{JA}$ | Junction-to-ambient thermal resistance | 84.0 °C/W |
| $\Theta_{JC}$ | Junction-to-case thermal resistance    | 17.0 °C/W |

**Packaging Mechanical: 20-Contact TSSOP (L)**

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS  | MIN.     | NOM. | MAX. |
|----------|----------|------|------|
| A        | —        | —    | 1.20 |
| A1       | 0.05     | —    | 0.15 |
| A2       | 0.80     | —    | 1.05 |
| b        | 0.19     | —    | 0.30 |
| C        | 0.09     | —    | 0.20 |
| D        | 6.40     | 6.50 | 6.60 |
| E1       | 4.30     | 4.40 | 4.50 |
| E        | 6.40 BSC |      |      |
| e        | 0.65 BSC |      |      |
| L1       | 1.00 REF |      |      |
| L        | 0.45     | 0.60 | 0.75 |
| S        | 0.20     | —    | —    |
| $\theta$ | 0°       | —    | 8°   |

**Notes:**

- Refer JEDEC MO-153F/AC
- Controlling dimensions in millimeters
- Package outline exclusive of mold flash and metal burr

DATE: 05/03/12

|  |             |
|--|-------------|
| DESCRIPTION: 20-pin, 173mil Wide TSSOP |             |
| PACKAGE CODE: L                        |             |
| DOCUMENT CONTROL #: PD-1311            | REVISION: F |

12-0373

**Ordering Information**

| Ordering Code  | Packaging Type | Package Description                        | Operating Temperature |
|----------------|----------------|--|-----------------------|
| PI6LC48P02LIE  | L              | Pb-free & Green, 20-pin TSSOP              | Industrial            |
| PI6LC48P02LIEX | L              | Pb-free & Green, 20-pin TSSOP, Tape & Reel | Industrial            |

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

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[PI6LC48H02LIEEX](#) [PI6LC48L0201LIEEX](#) [PI6LC48P25104LE](#) [PI6LC48P25104LIEEX](#) [PI6LC48P25104LEX](#)  
[PT7C4512WEX](#) [PT7C4512WE](#) [PI6LC48P0301AZHIE](#) [PI6LC48P0401LIEEX](#) [PI6LC48P0301AZHIEX](#)  
[PI6LC48P0301AZHEX](#) [PI6LC48P0301AZHE](#) [PI6LC48H04LIEEX](#) [PI6LC48P0405LIEEX](#) [PI6LC48C51LIE](#)  
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[PI6LC48P04LIE](#) [PI6LC48P04LIEEX](#) [PI6LC48S25AZBBIE](#) [PI6LC48S25AZBBIEX](#) [PI6LC4831BZBIE](#) [PI6LC4831BZBIEX](#)  
[PI6C3622-1LE](#) [PI6C49053AIE](#) [PI6C49053AIEEX](#) [PI6C3622LEX](#) [PI6LC48S25ZBBIE](#) [PI6LC48S25ZBBIEX](#)



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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