

NC7WZ04

TinyLogic® UHS Dual Inverter

Features

- Ultra-High Speed: t_{PD} 2.3ns (Typical) into 50pF at 5V V_{CC}
- High Output Drive: $\pm 24mA$ at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches Performance of LCX when Operated at 3.3V V_{CC}
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5V to 3V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SC70 6-Lead Package

Description

The NC7WZ04 is a dual inverter from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Related Resources

- [MS-503 — Family Characteristics TinyLogic® HS/HST and UHS Series](#)

Ordering Information

Part Number	Top Mark	 Eco Status	Package	Packing Method
NC7WZ04P6X	Z04	RoHS	6-Lead SC70, EIAJ SC88 1.25mm Wide	3000 Units on Tape & Reel
NC7WZ04L6X	A7	RoHS	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7WZ04FHX	A7	Green	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

 For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Connection Diagrams

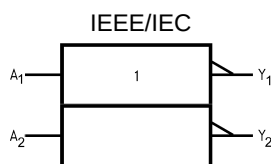


Figure 1. Logic Symbol

Pin Configurations

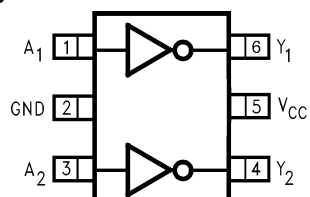


Figure 2. SC70 (Top View)

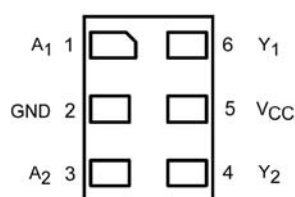


Figure 3. MicroPak (Top Through View)

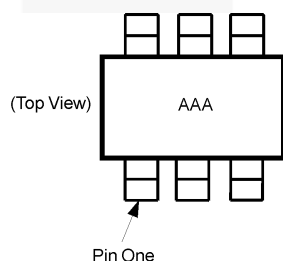


Figure 4. Pin 1 Orientation

Notes:

1. AAA represents product code top mark (see *Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Pin Definitions

Pin # SC70	Pin # MicroPak	Name	Description
1	1	A	Input
2	2	GND	Ground
3	3	A	Input
4	4	Y	Output
5	5	V _{CC}	Supply Voltage
6	6	Y	Output

Function Table

Y = /A

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	$V_{IN} < -0V$		-50	mA
I_{OK}	DC Output Diode Current	$V_{OUT} < 0V$		-50	mA
I_{OUT}	DC Output Source / Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SC70-6		180	mW
		MicroPak-6		130	
		MicroPak2-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8V, 2.5V ±0.2V	0	20	ns/V
		V_{CC} at 3.3V ± 0.3V	0	10	
		V_{CC} at 5.0V ± 0.5V	0	5	
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance	SC70-6		350	°C/W
		MicroPak-6		500	
		MicroPak2-6		560	

Note:

- Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.75V _{CC}			0.75V _{CC}		V
		2.30 to 5.50		0.70V _{CC}			0.70V _{CC}		
V _{IL}	LOW Level Input Voltage	1.65 to 1.95				0.25V _{CC}		0.25V _{CC}	V
		2.30 to 5.50				0.30V _{CC}		0.30V _{CC}	
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} =V _{IL} , I _{OH} =-100μA	1.55	1.65		1.55		V
		1.80		1.70	1.80		1.70		
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I _{OH} =-4mA	1.29	1.52		1.29		
		2.30	I _{OH} =-8mA	1.90	2.14		1.90		
		3.00	I _{OH} =-16mA	2.40	2.75		2.40		
		3.00	I _{OH} =-24mA	2.30	2.62		2.30		
		4.50	I _{OH} =-32mA	3.80	4.13		3.80		
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} =V _{IH} , I _{OL} =100μA		0.10	0.10		0.10	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I _{OL} =4mA		0.80	0.24		0.24	
		2.30	I _{OL} =8mA		0.10	0.30		0.30	
		3.00	I _{OL} =16mA		0.16	0.40		0.40	
		3.00	I _{OL} =24mA		0.24	0.55		0.55	
		4.50	I _{OL} =32mA		0.25	0.55		0.55	
I _{IN}	Input Leakage Current	0 to 5.5	0 ≤ V _{IN} ≤ 5.5V			±1		±1.0	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5V			1		10	μA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5V, GND			1		10	μA

AC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =−40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{PLH} , t _{PHL}	Propagation Delay	1.65	C _L =15pF, R _L =1MΩ	1.8	5.3	9.2	1.8	11.0	ns	Figure 5 Figure 6
		1.80		1.8	4.4	7.6	1.8	8.4		
		2.50 ± 0.20		1.2	3.0	5.1	1.2	5.6		
		3.30 ± 0.30		0.8	2.2	3.4	0.8	3.8		
		5.00 ± 0.50		0.5	1.8	2.8	0.5	3.1		
		3.30 ± 0.30	C _L =50pF, R _L =500Ω	1.2	2.9	4.5	1.2	5.0		
		5.00 ± 0.50		0.8	2.3	3.6	0.8	4.0		
C _{IN}	Input Capacitance	0.00			2.5				pF	
C _{PD}	Power Dissipation Capacitance ⁽⁵⁾	3.30			9				pF	Figure 7
		5.00			11					

Note:

5. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CCStatic}).

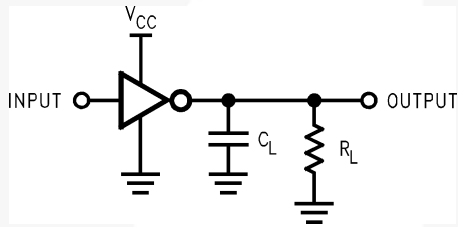


Figure 5. AC Test Circuit

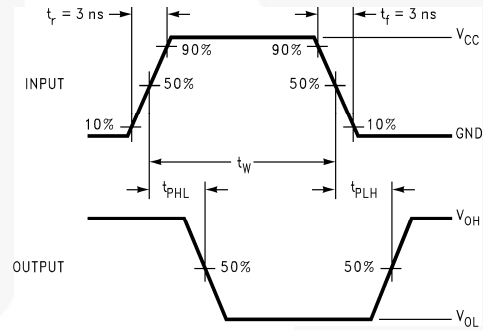


Figure 6. AC Waveforms

Notes:

6. C_L includes load and stray capacitance.
7. Input PRR = 1.0MHz, t_w = 500ns.

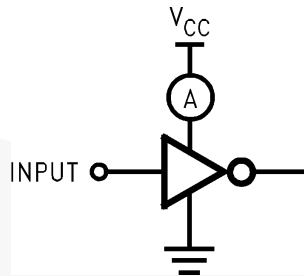
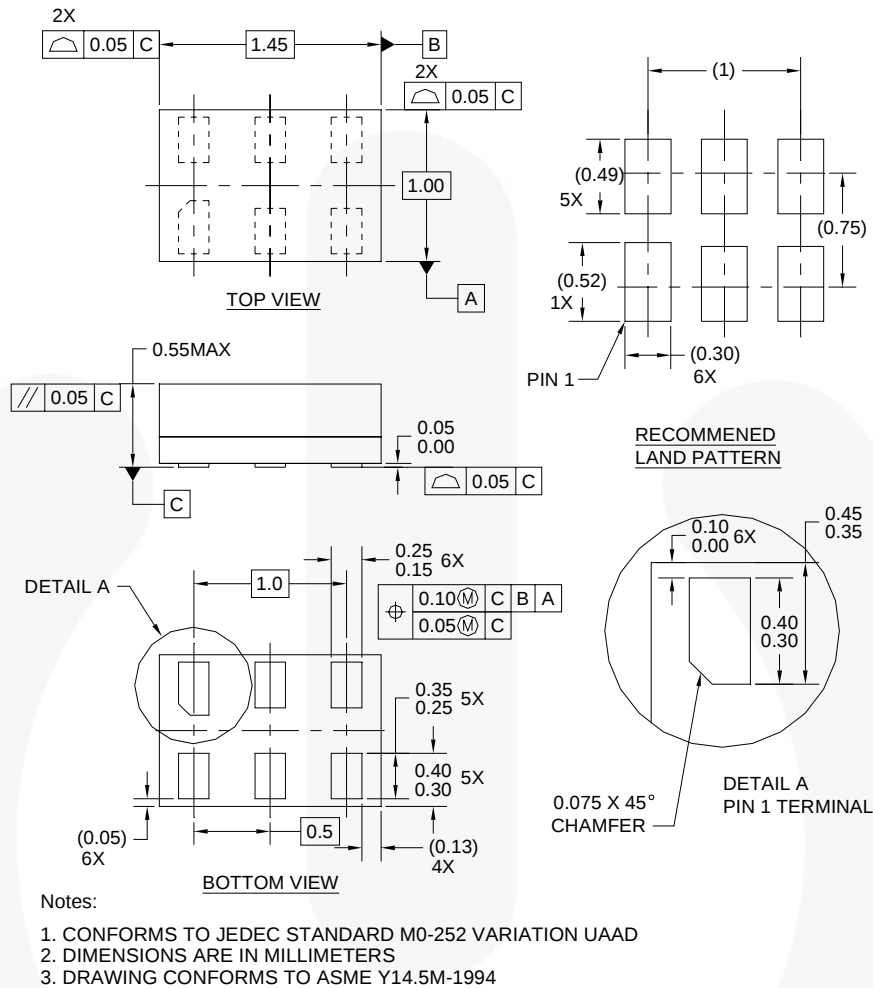


Figure 7. I_{CCD} Test Circuit

Note:

8. Input=AC Waveform; t_r=t_f=1.8ns.
9. PRR=Variable; Duty Cycle=50%.

Physical Dimensions



MAC06AREVC

Figure 9. 6-Lead, MicroPak™, 1.0mm Wide

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Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

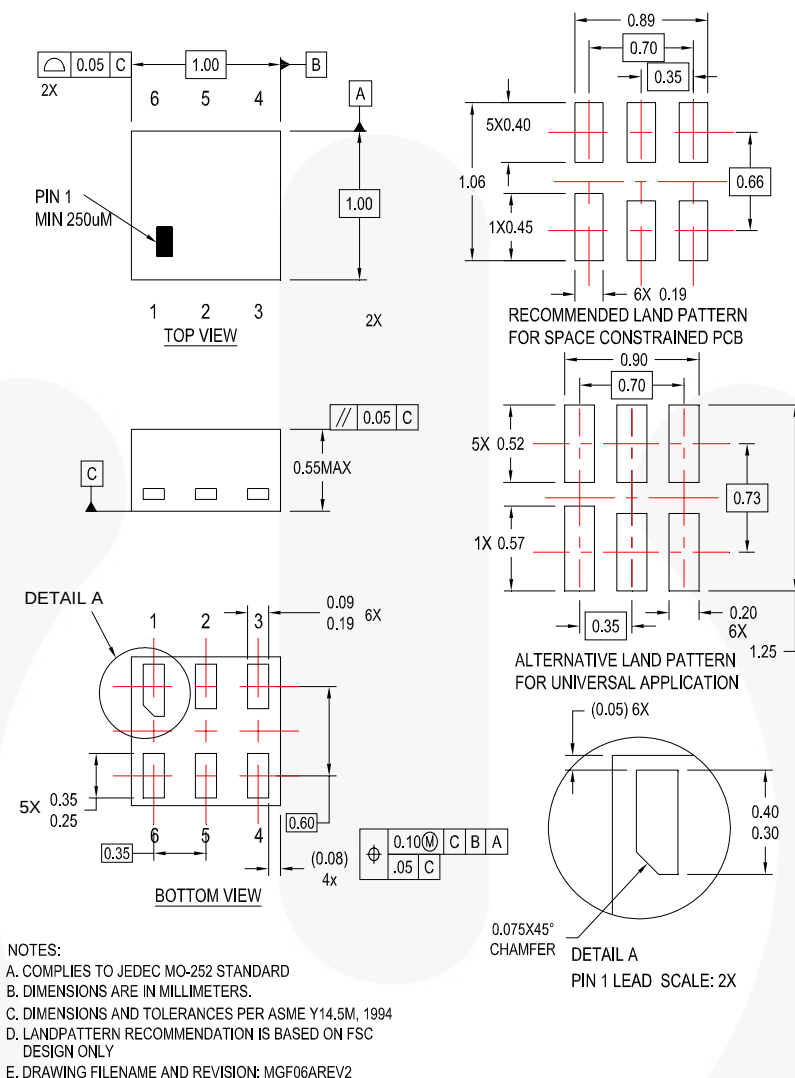


Figure 10. 6-Lead, MicroPak2, 1x1mm Body, .35mm Pitch

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:

http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. 146



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