Ordering number : ENA2304

LC87F0G08A

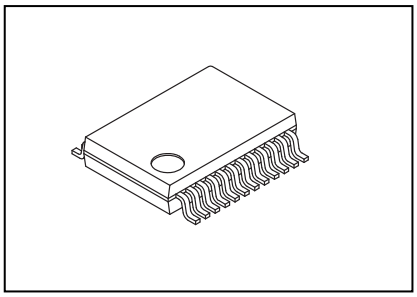
ON Semiconductor®

http://onsemi.com

CMOS LSI

8-bit 1-chip Microcontroller

8K-byte Flash ROM / 256-byte RAM / 24-pin



SSOP24(225mil)

Features

- a 10 × /20 × amplifier
- a 8/10-bit High-speed PWM(150kHz)
- a Reference Voltage Generator Circuit(2V/4V) for an AD converter
- a Temperature sensor
- an internal reset circuit
- a 7-channel AD converter with 12-/8-bit resolution selector
- Internal oscillation circuits (30kHz/1MHz/8MHz)

Performance

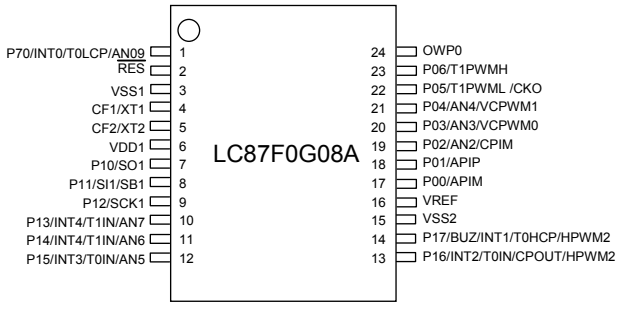
- 83.3ns (12.0MHz) V_{DD}=2.7V to 5.5V Ta= –40°C to + 85°C
- 125ns (8.0MHz) V_{DD}=2.0V to 5.5V Ta= –40°C to + 85°C
- 250ns (4.0MHz) V_{DD}=1.8V to 5.5V Ta= –40°C to + 85°C

Function Descriptions

- Ports
  - I/O ports : 18
  - Reference voltage outputs : 1 (VREF)
  - Power supply pins : 3 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$)
- Timers (3ch)
  - Timer 0 : 16-bit timer/counter with a capture register.
  - Timer 1 : 16-bit timer/counter that supports PWM/toggle outputs
  - a Base timer serving as a realtime clock
- SIO (1ch)
  - SIO1 : 8-bit asynchronous/synchronous serial interface
- Comparator
- Watchdog Timer
- Frequency tunable 12-bit PWM × 2ch
- System Clock Divider Function
- CF Oscillation Circuit, X'tal Oscillation Circuit
- 15 sources, 10 vectors interrupts
- On-chip Debugger Function

Application

- Shaver, Battery charge control



Pin Assignment (Top view)

* This product is licensed from Silicon Storage Technology, Inc. (USA).

ORDERING INFORMATION

See detailed ordering and shipping information on page 31 of this data sheet.

Semiconductor Components Industries, LLC, 2014

Function Details

■Flash ROM
- Capable of on-board programming with a wide range of supply voltages : 2.2 to 5.5V
- Block-erasable in 128 byte units
- Writes data in 2-byte units
- 8192 × 8 bits

■RAM
- 256 × 9 bits

■Bus Cycle Time
- 83.3ns (12MHz, V_{DD}=2.7V to 5.5V, Ta=–40°C to 85°C)
- 125ns (8MHz, V_{DD}=2.0V to 5.5V, Ta=–40°C to 85°C)
- 250ns (4MHz, V_{DD}=1.8V to 5.5V, Ta=–40°C to 85°C)

Note : The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 250ns (12MHz, V_{DD}=2.7V to 5.5V, Ta=–40°C to 85°C)
- 375ns (8MHz, V_{DD}=2.0V to 5.5V, Ta=–40°C to 85°C)
- 750ns (4MHz, V_{DD}=1,8V to 5.5V, Ta=–40°C to 85°C)

■Potrs
- Normal withstand voltage I/O ports whose I/O direction can be designated in 1-bit units 18($\overline{P0n}$, P1n, P70, CF1, CF2)
- Reset pins 1($\overline{RES}$)
- Power supply pins 3($V_{SS}1$, $V_{SS}2$,$V_{DD}1$)
- Reference voltage outputs 1(VREF)
- Dedicated debugger port 1(OWP0)

■Timers
- Timer 0 : 16-bit timer/counter with 2 capture registers.
  - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels
  - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)
  - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)
  - Mode 3 : 16-bit counter (with two 16-bit capture registers)
- Timer 1 : 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2 : 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from lower-order 8 bits)
  - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle outputs) (lower-order 8 bits may be used as a PWM output)
- Base timer
  (1) The clock is selectable from the subclock (32.768kHz crystal oscillation), the low speed RC, system clock, and timer 0 prescaler output.
  (2) with an 8-bit programmable prescaler
  (3) Interrupts programmable in 5 different time schemes

■SIO
- SIO1 : 8-bit asynchronous/synchronous serial interface
  Mode 0 : Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1 : Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■AD Converter:
- AD converter input port with 10 × /20 × amplifier (1channel)
- AD converter input port (7channel)
  12-/8-bit resolution selectable AD converter
- Selectable reference voltage source for an AD converter
  (Selectable from V_{DD} , Internal Reference Voltage Generator Circuit(VREF) .)

■Internal Reference Voltage Generator Circuit(VREF)
- Generates 2.0V/4.0V for AD converter.

■Comparator
Comparator input pin (1 channel)
Comparator output pin (1 channel)
Comparator output set high when (comparator input level) < 1.22V
Comparator output set low when (comparator input level) > 1.22V

■Clock Output Function
- Generates clocks with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillation clock that is selected as the system clock.

■Watchdog Timer
- Generates an internal reset on an overflow occurring in the timer running on the low-speed RC oscillator clock (approx. 30kHz) or subclock.
- Operating mode at standby is selectable from 3 modes
  (continue counting/suspend operation/suspend counting with the count value retained)

■Interrupts

- 15 sources, 10 vectors
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/BT
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	HPWM2
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	P0/VCPWM

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: Up to 128levels (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- Internal oscillation circuits
  1) Low-speed RC oscillation circuit: For system clock (approx.30kHz)
  2) Medium-speed RC oscillation circuit: For system clock (1MHz)
  3) Hi-speed RC oscillation circuit1: For system clock (8MHz)
  4) Hi-speed RC oscillation circuit2: For High speed PWM (40MHz)

■System Clock Divider Function

- Can run on low consumption current.
- Minimum instruction cycle selectable from 375ns, 750ns, 1.5µs, 3.0µs, 6.0µs, 12.0µs, 24.0µs, 48.0µs, and 96.0µs (at 8MHz main clock)

■Internal Reset Circuit

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level is 1.67V.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level can be selected from 7 levels (1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V and 4.28V), through option configuration.

■Standby Function

● HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
1) Oscillation is not halted automatically.
2) There are three ways of resetting the HALT mode.
(1) Setting the reset pin to the low level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt generated

● HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
1) The CF, RC and crystal oscillators automatically stop operation.
Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
2) There are four ways of resetting the HOLD mode:
(1) Setting the reset pin to the lower level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt source established at one of the INT0, INT1, INT2 and INT4 pins
* INT0 and INT1 can be used in the level sense mode only.
(4) Having an interrupt source established at port 0.

● X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer. (when X'tal oscillation or low-speed RC oscillation is selected).
1) The CF, low-speed, and medium-speed RC oscillators automatically stop operation.
Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
Note: If the base timer is run with low-speed RC oscillation selected as the base timer input clock source and the X'tal HOLD mode is entered, the low-speed RC oscillator retains the state that is established when the X'tal HOLD mode is entered.
2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
3) There are five ways of resetting the X'tal HOLD mode.
(1) Setting the reset pin to the low level
(2) Having the watchdog timer or LVD function generate a reset
(3) Having an interrupt source established at one of the INT0, INT1, INT2, and INT4 pins
* INT0 and INT1 can be used in the level sense mode only.
(4) Having an interrupt source established at port 0
(5) Having an interrupt source established in the base timer circuit

■VCPWM: Frequency tunable 12-bit PWM × 2ch

■High speed PWM (HPWM2)
8-/10- bits PWM ×1ch
1) The PWM clock is selectable from system clock and Hi-speed RC2 (40MHz)
2) The PWM type is selectable from 8 bits(Normal mode) and 10 bits(additive puls mode).

■Temperature sensor
• Senseor voltage can be comapred by the AD converter.

■On-chip Debugger Function
• Supports software debugging with the IC mounted on the target board.
• Provides 1 channel of on-chip debugger pin.
OWP0

■Data Security Function
• Protects the program data stored in flash memory from unauthorized read or copy.
Note: This data security function does not necessarily provide absolute data security.

■Package Form
• SSOP24 (225mil): Lead-free and halogen-free type

■Development Tools

- On-chip debugger: TCB87 Type C (1-wire interface cable) + LC87F0G08A

■Programming Boards

Package	Programming boards
SSOP24(225mil)	W87F0GS

■Flash Programmer

Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9709C	Rev 03.28 or later	87F008SU
Flash Support Group, Inc. (FSG) + Our company (Note 1)	Onboard Single/Gang Programmer	AF9101/AF9103(Main unit) (FSG models) + SIB87 Type C(Inter Face Driver) (Our company model)	(Note 2)	-
Our company	Single/Gang Programmer	SKK Type B / SKK Type C	Application Version 1.08 or later Chip Data Version 2.46 or later	LC87F0G08
	Onboard Single/Gang Programmer	SKK-DBG Type C		

For information about AF-Series :
Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

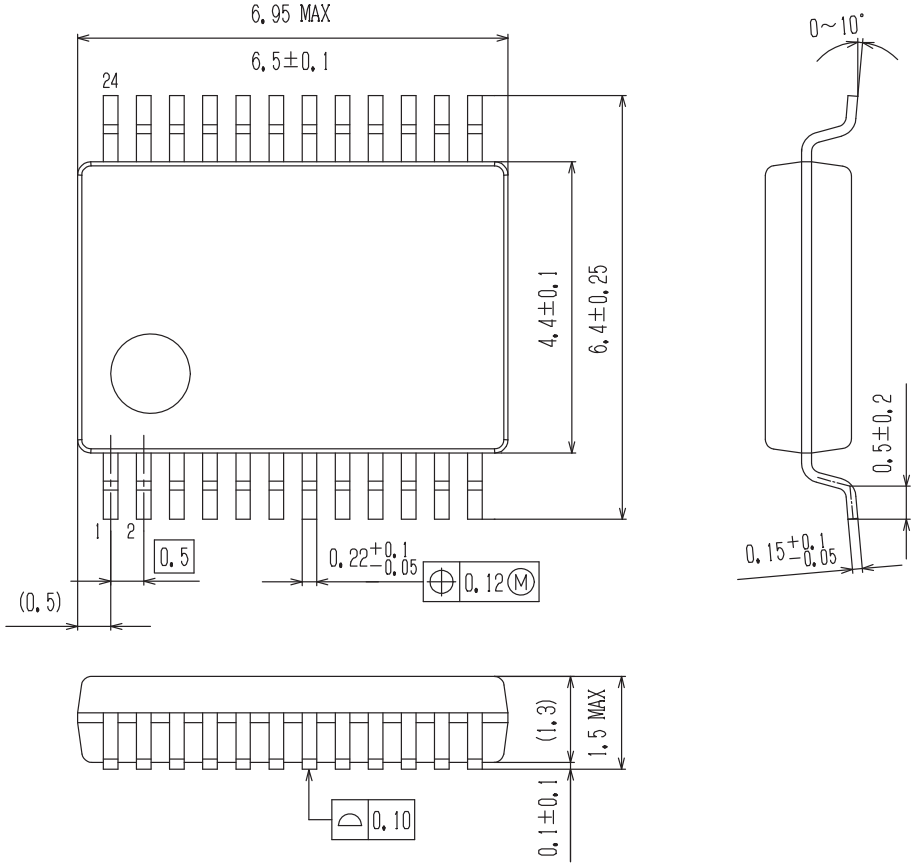
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87 Type C) together can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or Our company for the information.

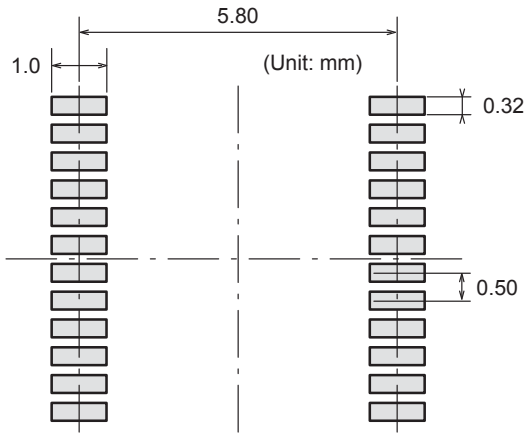
Package Dimensions

unit : mm

SSOP24 (225mil)
CASE 565AR
ISSUE A



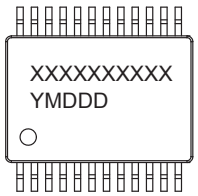
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

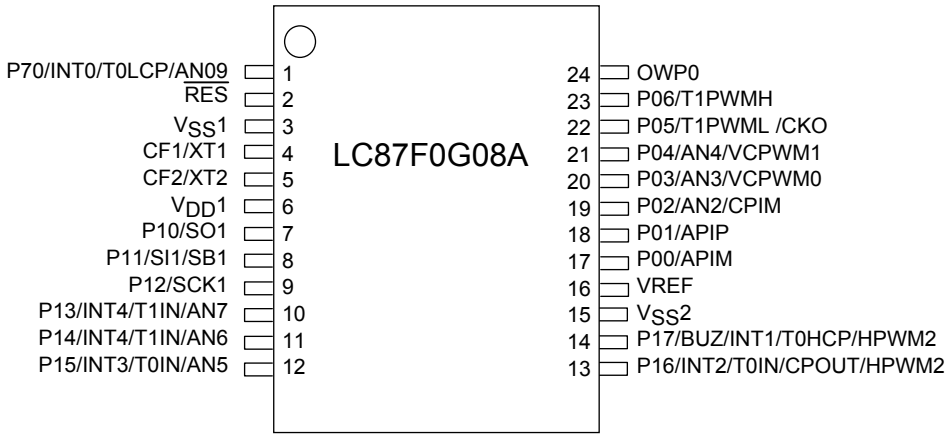
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

Pin Assignment

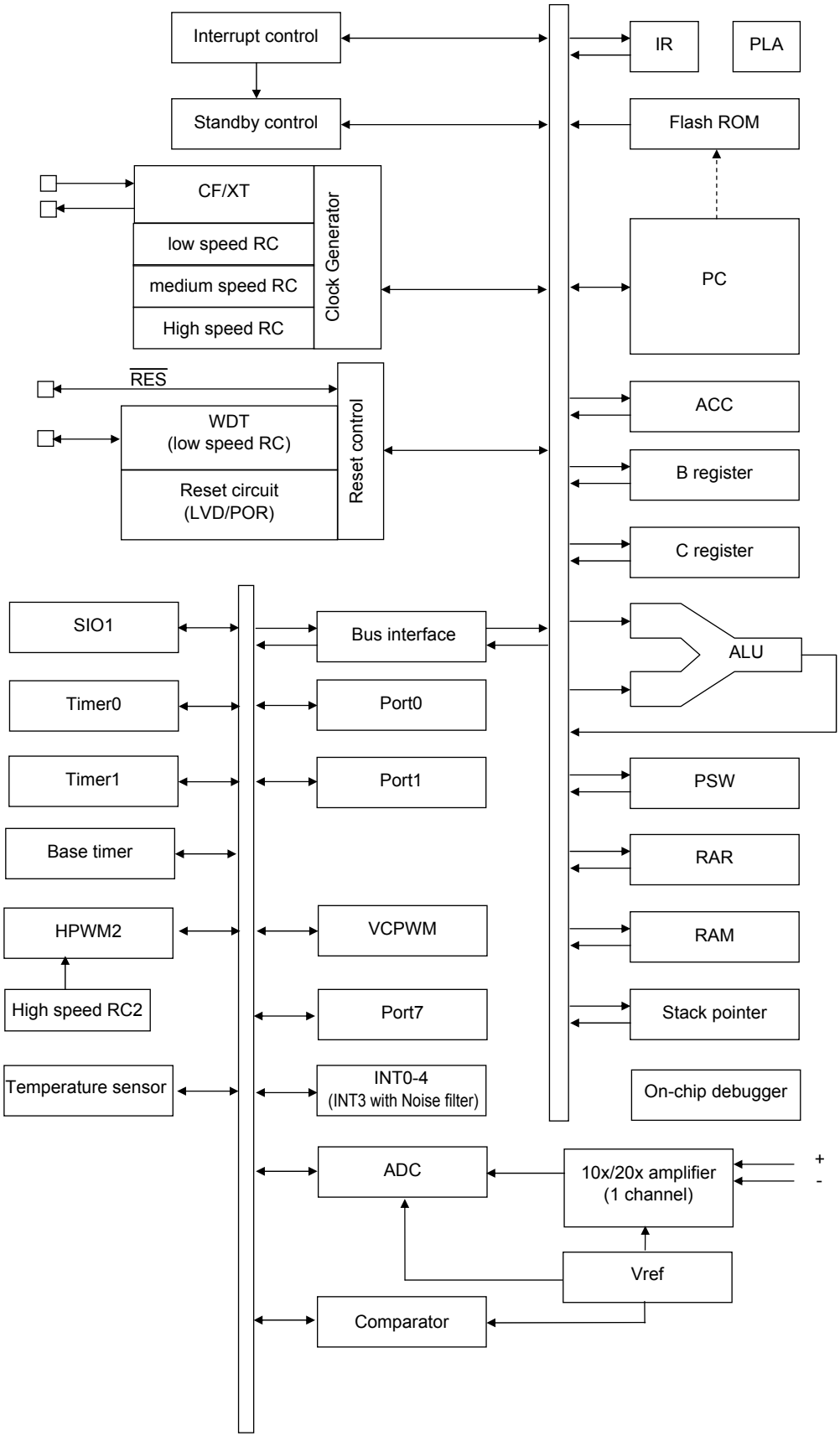


SSOP24(225mil) "Lead-/Halogen-free Type"

SSOP24	NAME
1	P70/INT0/T0LCP/AN09
2	$\overline{RES}$
3	$V_{SS}1$
4	CF1/XT1
5	CF2/XT2
6	$V_{DD}1$
7	P10/SO1
8	P11/SI1/SB1
9	P12/SCK1
10	P13/INT4/T1IN/AN7
11	P14/INT4/T1IN/AN6
12	P15/INT3/T0IN/AN5

SSOP24	NAME
13	P16/INT2/T0IN/CPOUT/HPWM2
14	P17/BUZ/INT1/T0HCP/HPWM2
15	$V_{SS}2$
16	VREF
17	P00/APIM
18	P01/APIP
19	P02/AN2/CPIM
20	P03/AN3/VCPWM0
21	P04/AN4/VCPWM1
22	P05/T1PWML/CKO
23	P06/T1PWMH
24	OWP0

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>$V_{SS}2$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>VREF</td><td>I/O</td><td>Reference voltage output(2.0V/4.0V) or External input</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>On-chip debugger pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P06</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.

• Pin functions
P00 (AN0), P01 (AN1): AD converter input port with 10x/20x operational amplifier
P02: AD converter input port (AN2) / Comparator input (CPIM)
P03: AD converter input port (AN3) / VCPWM0 output
P04: AD converter input port (AN4) / VCPWM1 output
P05: Timer 1 PWML output / System clock output
P06: Timer 1 PWMH output
P07: On-chip debugger pin (OWP0)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P15</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.

• Pin functions
P10: SIO1 data output
P11: SIO1 data input/bus input/output
P12: SIO1 clock input/output
P13: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/ timer 0H capture input/ AD converter input port (AN7)
P14: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/ timer 0H capture input/ AD converter input port (AN6)
P15: INT3 input(with noise filter)/timer 0 event input/timer 0H capture input/ AD converter input port (AN5)
P16: INT2 input/HOLD release input/timer 0 event input/ timer 0L capture input/HPWM2 output
P17: beeper output/INT1 input/HOLD release input/timer 0H capture input/HPWM2 output

Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable
• Pull-up resistors can be turned on and off.

• Pin functions
P70 : INT0 input/HOLD release input/timer 0L capture input/AD converter input port (AN9)

Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>External reset input/internal reset output pin</td><td>Yes
Internal pullup
ON/OFF</td></tr>
<tr><td>CF1/XT1</td><td>I/O</td><td>• Ceramic oscillator/32.768kHz crystal oscillator input pin

• Pin functions
• 1-bit I/O port
• I/O specifiable
(only Nch-open drain)</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic oscillator/32.768kHz crystal oscillator output pin

• Pin functions
• 1-bit I/O port
• I/O specifiable</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>On-chip debugger pin</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P06	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
CF1/XT1	-	No	Nch-open drain when general I/O port is selected.	No
CF2/XT2	-	No	CMOS / Nch-open drain when general I/O port is selected.(programmable)	No
P70	-	No	Nch-open drain	Programmable

User Option Table

Option Name	Option Type	Flash Version	Option Selected in Units of	Option Selection
Port output form	P00 to P06	enable	1 bit	CMOS
				Nch-open drain
	P10 to P17	enable	1 bit	CMOS
				Nch-open drain
Program start address	-	enable	-	00000h or 01E00h When protected area 1) is selected
				00000h When either of protected area 2), 3) or 4) is selected
Protected area (Note1)	-	enable	-	1) 1800h-1FFFh
				2) 0000h-1DFFh,1F00h-1FFFh
				3) 0000h-1CFFh,1F00h-1FFFh
				4) 0000h-1AFFh,1F00h-1FFFh
Reset pin	Internal pullup ON/OFF	enable	-	ON
				OFF
Low-voltage detection reset function	Detect function	enable	-	Enable: Use
				Disable: Not Used
	Detect level	enable	-	7-level
Power-on reset function	Power-On reset level	enable	-	1-level

Note1: onboard programming inhbited address

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P70	Open	Output low
CF1/XT1	Open	General I/O port output low
CF2/XT2	Open	General I/O port output low
OWP0	Pulled low with a 100kΩ resistor	-

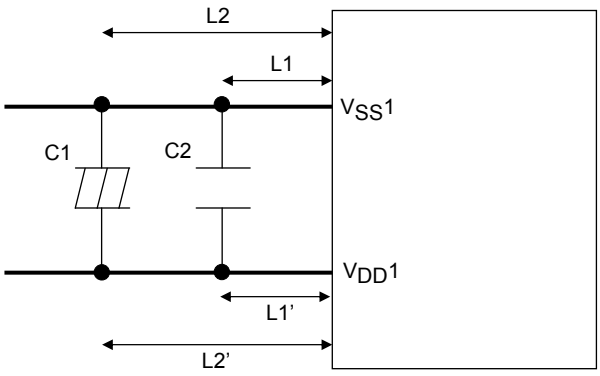
On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "Rd87 On-chip Debugger Installation Manual"

Power Pin Treatment Recommendations ($V_{DD}1$, $V_{SS}1$)

Connect bypass capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.
  The capacitance of C2 should be approximately 0.1μF.



Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		$V_{DD}MAX$	$V_{DD}1$			-0.3	to	+6.5	V
Input/output voltage		VIO	Port0,1 Port7 CF1,CF2, $\overline{RES}$			-0.3	to	V_{DD}+0.3	V
High level output current	Peak output current	IOPH(1)	Port0 Port1 CF2	• When CMOS output type is selected • Per 1 applicable pin		-10			mA
	Average output current (Note 1-1)	IOMH(1)	Port0 Port1 CF2	• When CMOS output type is selected • Per 1 applicable pin		-7.5			
	Total output current	ΣIOAH(1)	Port0,1, CF2	Total current of all applicable pins		-30			
Low level output current	Peak output current	IOPL(1)	Port0	• Per 1 applicable pin				20	
		IOPL(2)	Port1	• Per 1 applicable pin				20	
		IOPL(3)	Port7,CF1,CF2	• Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	Port0	• Per 1 applicable pin				15	
		IOML(2)	Port1	• Per 1 applicable pin				15	
		IOML(3)	Port7,CF1,CF2	• Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Port0,1,7, CF1,CF2	Total current of all applicable pins				80	
Allowable power Dissipation		Pdmax(1)	SSOP24(225mil)	Ta=-40 to + 85°C Package with thermal resistance board (Note 1-2)				260	mW
Operating ambient Temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	VDD(1)	VDD1	0.245μs ≤ tCYC ≤ 200μs		2.7		5.5	V
	VDD(2)		0.367μs ≤ tCYC ≤ 200μs		2.0		5.5	
	VDD(3)		0.735μs ≤ tCYC ≤ 200μs		1.8		5.5	
Memory sustaining supply voltage	VHD	VDD1	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	VIH(1)	Port 0,1 P70		1.8 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	VIH(4)	CF1,CF2, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	VIL(1)	Port 0,1 P70		4.0 to 5.5	V_{SS}		$0.1V_{DD}+0.4$	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	VIL(4)	CF1,CF2, $\overline{RES}$		1.8 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	μs
				2.0 to 5.5	0.367		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50 ± 5%	2.7 to 5.5	0.1		12	MHz
				2.2 to 5.5	0.1		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1,CF2	When 12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		MHz
	FmCF(2)	CF1,CF2	When 8MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		8		
	FmCF(3)	CF1,CF2	When 4MHz ceramic oscillation See Fig. 1.	1.8 to 5.5		4		
	FmFRC(1)		Internal high-speed RC oscillation Ta=-10°C to +85°C (Note 2-4)	1.8 to 5.5	7.76	8.0	8.24	
	FmFRC(2)		Internal high-speed RC oscillation Ta=-40°C to +85°C (Note 2-4)	1.8 to 5.5	7.60	8.0	8.40	
	FmRC		Internal medium-speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation (Note 2-5)	1.8 to 5.5	27	30	33	kHz
	FsX'tal	XT1,XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		kHz
	FmPWMRC		Internal high-speed RC oscillation for HPWM2	2.7 to 5.5	38	40	42	MHz
Oscillation Stabilization Time	tmsCF	CF1,CF2	• When oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" . • See Fig. 3.	See Table 1				μs
	tmsFRC (Note 2-4)			1.8 to 5.5			100	
	tmsPWMRC			1.8 to 5.5			100	
	tmsRC			1.8 to 5.5		0		
	tmsSRC (Note2-5)			1.8 to 5.5			1	ms
	tmsX'tal	XT1,XT2		See Table 2				

Note 2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: An oscillation stabilization time of 100μs or longer must be provided before switching the system clock source after the state of the high-speed RC oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" .

Note 2-5: An oscillation stabilization time of 1ms or longer must be provided before switching the system clock source after the state of the low-speed RC oscillation circuit is switched from "oscillation stopped" to "oscillation enabled" .

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Port 0,1, Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5			1	μA
	$I_{IH}(2)$	CF1	$V_{IN}=V_{DD}$	1.8 to 5.5			15	
Low level input current	$I_{IL}(1)$	Port 0,1, Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	-1			
	$I_{IL}(2)$	CF1	$V_{IN}=V_{SS}$	1.8 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Port 0,1, CF2	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.2mA	1.8 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Port 0,1, P70,CF1,CF2	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.0mA	1.8 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Port 0,1, P70	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			1.8 to 4.5	18	50	230	
	Rpu(3)	$\overline{RES}$		1.8 to 5.5	300	400	500	
Hysteresis voltage	VHYS(1)	Port 0,1, P70 $\overline{RES}$		2.7 to 5.5		$0.1V_{DD}$		V
				1.8 to 5.5		$0.07V_{DD}$		
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	1.8 to 5.5		10		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SIO1 Serial I/O Characteristics (Note 4-1)

Parameter			Symbol	Pin/ Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK1(P12)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK1(P12)	• CMOS output type selected • See Fig. 5.	1.8 to 5.5	2			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SI1(P11), SB1(P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Output delay time		tdDO(1)	SO1(P10), SB1(P11)	• Specified with respect to falling edge of SIOCLK • Specified as the time up to the beginning of output change in open drain output mode. • See Fig. 5.	1.8 to 5.5			(1/3)tCYC +0.08	

Note 4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P16), INT4(P13, P14)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	1.8 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P15) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	256			
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	1.8 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P14) AN7(P13) AN9(P70) (Note 6-3)		1.8 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	1.8 to 5.5			±16	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 6-2)	2.7 to 5.5	32		115	µs
				2.2 to 5.5	134		215	
				1.8 to 5.5	400		430	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}		V_{DD}	V
	VAIN(2)		When internal VREF=4V is selected. VREF≤V_{DD}	4.3 to 5.5	V_{SS}		VREF	
			When internal VREF=2V is selected VREF≤V_{DD}	2.3 to 3.6	V_{SS}		VREF	
Analog port input current	IAINH		VAIN=V_{DD}	1.8 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	1.8 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P14) AN7(P13) AN9(P70) (Note 6-3)		1.8 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	1.8 to 5.5			±1.5	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 6-2)	2.7 to 5.5	20		90	µs
				2.2 to 5.5	80		135	
				1.8 to 5.5	245		265	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}		V_{DD}	V
	VAIN(2)		When internal VREF=4V is selected. VREF≤V_{DD}	4.3 to 5.5	V_{SS}		VREF	
			When internal VREF=2V is selected. VREF≤V_{DD}	2.3 to 3.6	V_{SS}		VREF	
Analog port input current	IAINH		VAIN=V_{DD}	1.8 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	1.8 to 5.5	-1			

<Conversion time calculation method>

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)× (1/3)×tCYC

<Recommended Operating Conditions>

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-8MHz	2.7V to 5.5V	1/1	375ns	1/8	52.25μs	32.25μs
	2.2V to 5.5V	1/1	375ns	1/32	208.25μs	128.25μs
CF-4MHz	2.7V to 5.5V	1/1	750ns	1/8	104.5μs	64.5μs
	2.2V to 5.5V	1/1	750ns	1/16	208.5μs	128.5μs
	1.8V to 5.5V	1/1	750ns	1/32	416.5μs	256.5μs

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion executed in the 12-bit AD conversion mode after a system reset
- The first AD conversion executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode

Note 6-3: See section 8, "10×/20× amplifier characteristics", for analog channel 0 (10×/20× amplifier output).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Reference Voltage Generator Circuit (VREF) Characteristics

at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
VREF=2V voltage accuracy	VREF2VO	VREF (Note 7-2)		1.8 to 2.0	V_{DD}-0.1		V_{DD}	V
				2.0 to 5.5	1.90		2.02	
				2.3 to 5.5	1.98		2.02	
VREF=4V voltage accuracy	VREF4VO			1.8 to 4.0	V_{DD}-0.1		V_{DD}	
				4.0 to 5.5	3.90		4.04	
				4.3 to 5.5	3.96		4.04	
VREFoutput current	VREFIO			1.8 to 5.5	V_{SS}		0.5	mA
Operation stabilization time (Note 7-1)	tVREFW			1.8 to 5.5			5	ms

Note 7-1: Refers to the interval between the time VR12ON and VR24ON are set to 1 and the time operation gets stabilized.

Note 7-2: An external 4.7μF capacitor must be connected to the VREF pin to stabilize the VREF voltage.

10x/20x Amplifier Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		V_{DD}[V]	Specification min	typ	max	unit
20x Amplifier gain	APGAIN20 See Fig7	P00/APIM P01/APIP	• Ta=-40 to +85°C 1)APDIR=0 & GAIN20=1. • P01=0V,P00≤0V or P00=0V,P01≥0V 2)APDIR=1 & GAIN20=1. • P01=0V,P00≥0V or P00=0V,P01≤0V		4.3 to 5.0		20		
20x Amplifier offset	VAPIO20					200		600	mV
20x Amplifier input voltage range	VAPIM20-1	P00/APIM	1)	P01/APIP=0V		-0.17		0	V
	VAPIP20-1	P01/APIP		P00/APIM=0V		0		0.17	
	VAPIM20-2	P00/APIM	2)	P01/APIP=0V		0		0.17	V
	VAPIP20-2	P01/APIP		P00/APIM=0V		-0.17		0	
10x Amplifier gain	APGAIN10 See Fig7	P00/APIM P01/APIP	• Ta=-40 to +85°C 3)APDIR=0 & GAIN20=0. • P01=0V,P00≤0V or P00=0V,P01≥0V 4)APDIR=1 & GAIN20=0. • P01=0V,P00≥0V or P00=0V,P01≤0V				10		
10x Amplifier offset	VAPIO10					100		300	mV
10x Amplifier input voltage range	VAPIM10-3	P00/APIM	3)	P01/APIP=0V		-0.24		0	V
	VAPIP10-3	P01/APIP		P00/APIM=0V		0		0.24	
	VAPIM10-4	P00/APIM	4)	P01/APIP=0V		0		0.24	V
	VAPIP10-4	P01/APIP		P00/APIM=0V		-0.24		0	
Amplifier input port input current	IAPINL	P00/APIM	$P00/APIM=V_{SS}-0.2V$			-1			μA
	IAPINH	P01/APIP	$P01/APIP=V_{DD}$					1	
Operation stabilization time (Note 8-1)	tAPW							20	μs

Note 8-1: Refers to the interval between the time APON is set to 1 and the time operation gets stabilized.

<Amplifier input vaoltage calculation method:See Fig7>

VAPFUL = (VREFAD - VAPIO) / APGAIN

(VREFAD can be selected from internal-VREF4V, internal-VREF2V and V_{DD}.)

Note: VAPFUL must not exceed VAPIP or VAPIM.

Comparator Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Comparator threshold voltage (Note 9-1)	VCMVT	P02/CPIM		2.5 to 5.5	1.12	1.22	1.32	V
Input voltage range	VCMIN			2.5 to 5.5	V_{SS}		V_{DD}	V
Offset voltage	VOFF		• Within input voltage range	2.5 to 5.5		±10	±30	mV
Response time	tRT		• Within input voltage range • Input amplitude =100mV • Overdrive=50mV	2.5 to 5.5		200	600	ns
Operation stabilization time (Note 9-2)	tCMW			2.5 to 5.5			1.0	μs

Note 9-1: Comparator output=High level when (P02/CPIM voltage) < VCMVT
Comparator output=Low level when (P02/CPIM voltage) > (VCMVT +VOFF)

Note 9-2: Refers to the interval between the time CPON is set to 1 and the time operation gets stabilized.

Temperature Sensor Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

<4-diode mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Output voltage	VOTMP4(1)		Ta=-40°C	5.0	3.23	3.25	3.27	V
	VOTMP4(2)		Ta=+25°C	5.0	2.75	2.77	2.80	
	VOTMP4(3)		Ta=+85°C	5.0	2.28	2.31	2.34	
sensitivity	Vsen4		Ta=-40 to +85°C	3.5 to 5.5	-7.63	-7.54	-7.45	mV/°C
Absolute accuracy (Note 10-1) (Note 10-2)	ETTMP4	Vref=4[V]	Ta=(60±10) °C (Note 10-3)	3.5 to 5.5		±2.5	±5	°C
			Ta=-40 to +85°C	3.5 to 5.5		±5	±10	

<2-diode mode>

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Output voltage	VOTMP2(1)		Ta=-40°C	3.3	1.61	1.63	1.64	V
	VOTMP2(2)		Ta=+25°C	3.3	1.37	1.39	1.40	
	VOTMP2(3)		Ta=+85°C	3.3	1.14	1.16	1.17	
sensitivity	Vsen2		Ta=-40 to +85°C	2.0 to 5.5	-3.81	-3.77	-3.72	mV/°C
Absolute accuracy (Note 10-1) (Note 10-2)	ETTMP2	Vref=2[V]	Ta=(60±10) °C (Note 10-4)	2.0 to 5.5		±2.5	±5	°C
			Ta=-40 to +85°C	2.0 to 5.5		±5	±10	

Note 10-1: There are cases when the absolute accuracy specification value is exceeded when a large current flows through the ports.

Note 10-2: Including error of AD Converter.

Note 10-3: When using the Temperature sensor 60°C 2-diodes reference register D2TL/ D2TH.

Note 10-4: When using the Temperature sensor 60°C 4-diodes reference register D4TL/ D4TH.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions	Specification			
			Option Selected Voltage	min	typ	max	unit
POR release voltage	PORRL		Option selected (Note 11-1)	1.67V	1.10		1.79	V
Detection voltage unpredictable area	POUKS		See Fig. 8. (Note 11-2)			0.7	0.95	
Power supply rise time	PORIS		Power startup time from VDD=0V to 1.6V				100	ms

Note 11-1: The POR release voltage can be selected when the low-voltage detection feature is deselected.
Note 11-2: There is an unpredictable area before the transistor starts to turn on.

Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions	Specification				
				Option Selected Voltage	min	typ	max	unit
LVD reset voltage (Note 12-2)	LVDET		Option selected See Fig. 9. (Note 12-1) (Note 12-3)	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.93	
				3.79V	3.69	3.79	3.92	
				4.28V	4.18	4.28	4.41	
LVD voltage hysteresis	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unpredictable area	LVUKS		See Fig. 9. (Note 12-4)			0.7	0.95	V
Minimum low voltage detection width (response sensitivity)	TLVDW		LVDET-0.5V See Fig. 10.		0.2			ms

Note 12-1: The LVD reset voltage can be selected from 7 levels when the low-voltage detection feature is selected.
Note 12-2: The hysteresis voltage is not included in the LVD reset voltage specification value.
Note 12-3: There are cases when the LVD reset voltage specification value is exceeded when a greater change in the output level or large current is applied to the port.
Note 12-4: There is an unpredictable area before the transistor starts to turn on.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin / Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 13-1) (Note 13-2)	IDDOP(1)	$V_{DD}1$	• FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5		3.8	5.2	mA
				2.2 to 3.6		2.2	2.9	
	IDDOP(2)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		2.1	3.5	
				1.8 to 3.6		1.1	1.7	
	IDDOP(3)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		0.23	0.39	
				1.8 to 3.6		0.13	0.19	
	IDDOP(4)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5		2.7	3.6	
				1.8 to 3.6		1.7	2.3	
	IDDOP(5)		• External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		10	42	μA
				1.8 to 3.6		6	21	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		46	101	
				1.8 to 3.6		16	40	

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin / Remarks	Conditions	V_{DD}[V]	Specification min	Typ	max	unit
HALT mode consumption current (Note 13-1) (Note 13-2)	IDDHALT(1)	V_{DD}1	HALT mode • FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5		2.0	3.2	mA
				2.2 to 3.6		1.0	1.6	
	IDDHALT(2)		HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		1.2	2.4	
				1.8 to 3.6		0.5	1.0	
	IDDHALT(3)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		0.12	0.25	
				1.8 to 3.6		0.06	0.11	
	IDDHALT(4)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5		1.1	1.7	
				1.8 to 3.6		0.7	1.0	
	IDDHALT(5)		HALT mode • External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5		3.8	37	μA
				1.8 to 3.6		2.4	17	
	IDDHALT(6)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5		42	97	
				1.8 to 3.6		13	38	
HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(1)	V_{DD}1	HOLD mode	1.8 to 5.5		0.023	33.2	μA
				1.8 to 3.6		0.012	14.2	
	IDDHOLD(2)		HOLD mode • LVD option selected	1.8 to 5.5		1.09	26.9	
				1.8 to 3.6		0.86	11.8	
Timer HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(3)	V_{DD}1	Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	1.8 to 5.5		39	94	
				1.8 to 3.6		12	36	
	IDDHOLD(4)		Timer HOLD mode • FmSRC=30kHz internal low-speed RC oscillation mode	1.8 to 5.5		0.63	34	
				1.8 to 3.6		0.53	15	

Note 13-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

Note 13-2: Unless otherwise specified, the consumption current for the LVD circuit is not included.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	μs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator
■MURATA Manufacturing Co., Ltd.

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
12MHz	SMD	CSTCE12M0G52-R0	(10)	(10)	Open	680	2.6 to 5.5	0.02	0.3	C1 and C2 integrated type
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1k	2.1 to 5.5	0.02	0.3	
4MHz	SMD	CSTCR4M00G53-R0	(15)	(15)	Open	1.5k	1.8 to 5.5	0.03	0.45	

Characteristics of a Sample Subsystem Clock Oscillation Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit that Uses a Crystal Oscillator
■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
32.768kHz	SMD	MC-306	9	9	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value = 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 3):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is released.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

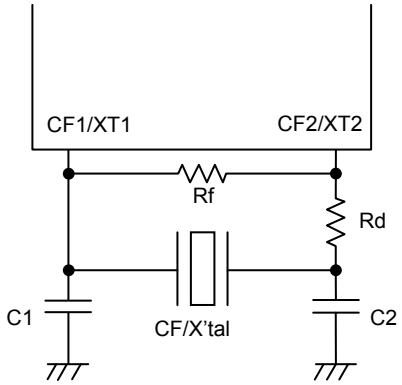


Figure 1 CF/XT Oscillator Circuit

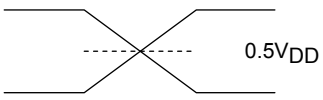
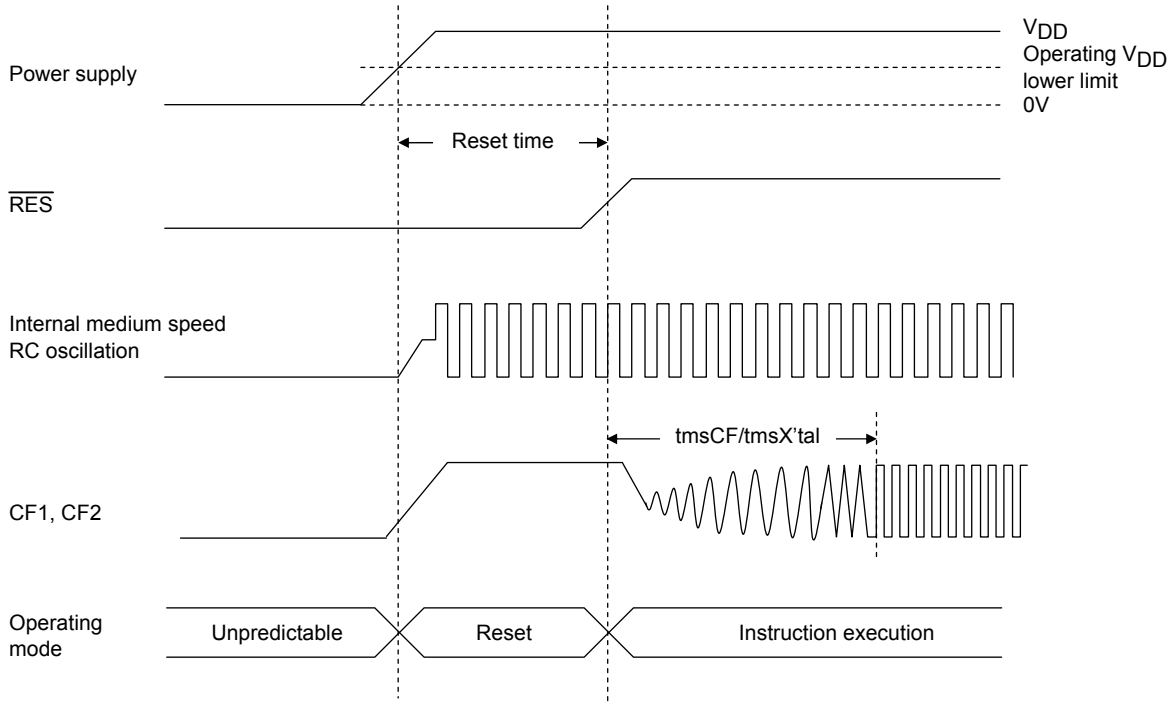
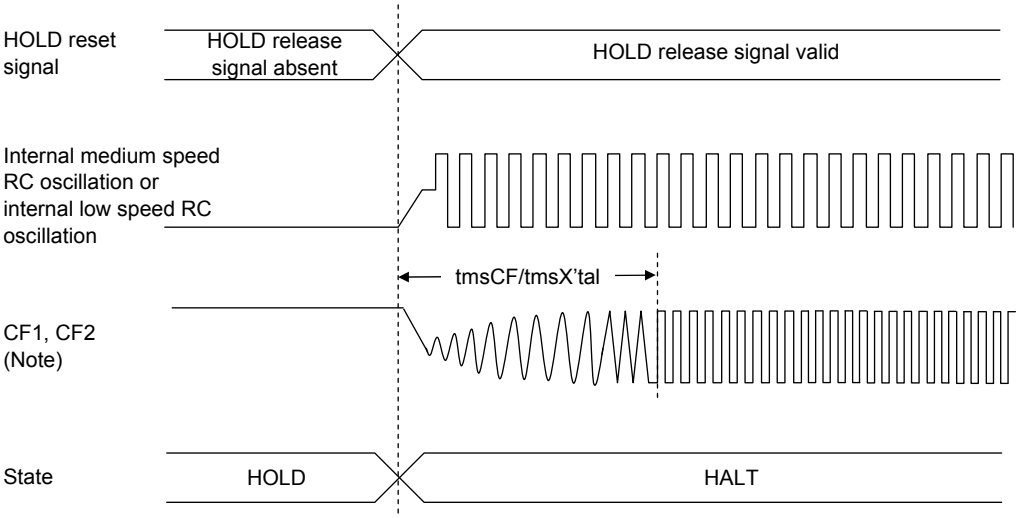


Figure 2 AC Timing Measurement Point



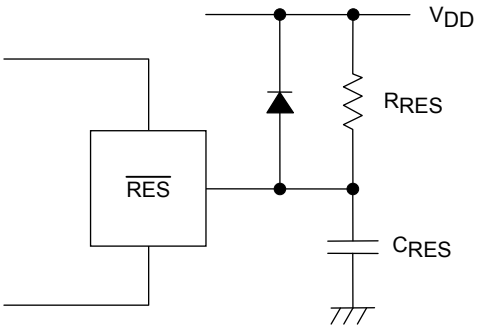
Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Note: When an external oscillation circuit is selected.

Figure 3 Oscillation Stabilization Time



Note:
The external circuit for reset may vary depending on the usage of POR and LVD. See “Reset Function” in the user's manual.

Figure 4 Sample Reset Circuit

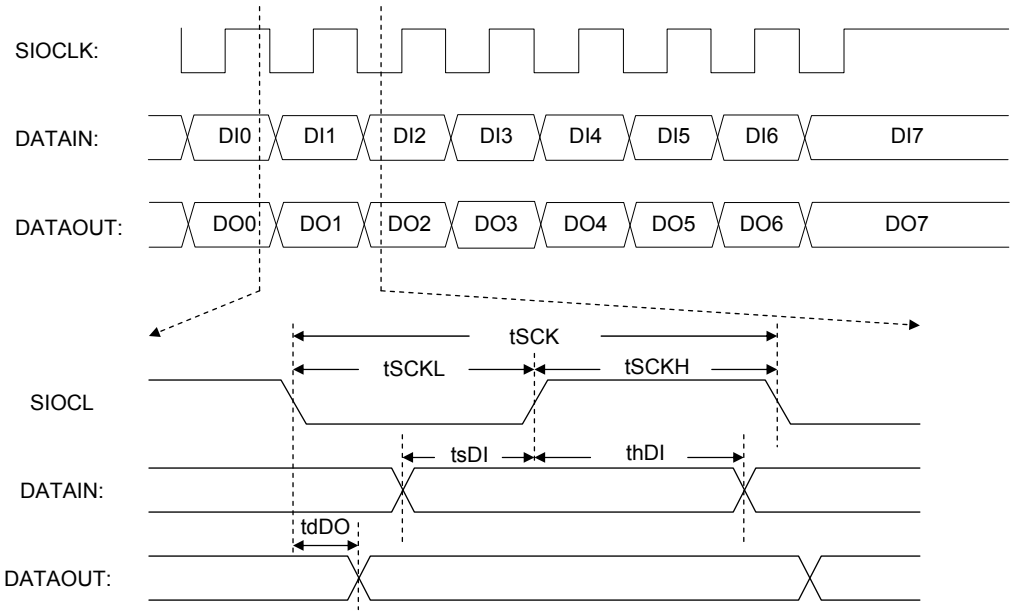


Figure 5 Serial I/O Waveform

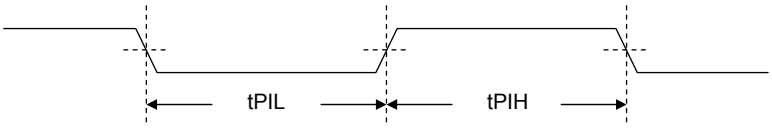


Figure 6 Pulse Input Timing Signal Waveform

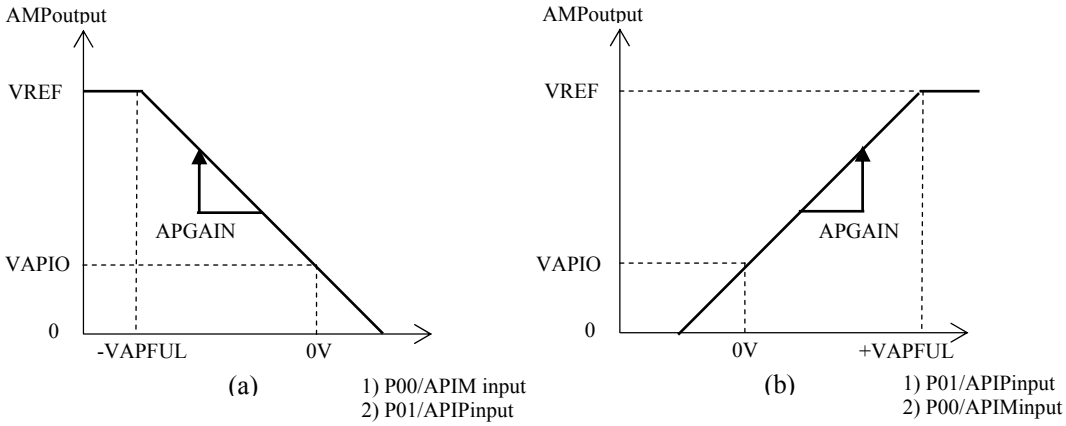


Figure 7 10×/20× Amplifier Characteristics

(a) 1) When P01/APIP is 0V, P00/APIM ≤ 0V.
2) When P00/APIM is 0V, P01/APIP ≤ 0V.

(b) 1) When P00/APIM is 0V, P01/APIP ≥ 0V.
2) When P01/APIP is 0V, P00/APIM ≥ 0V.

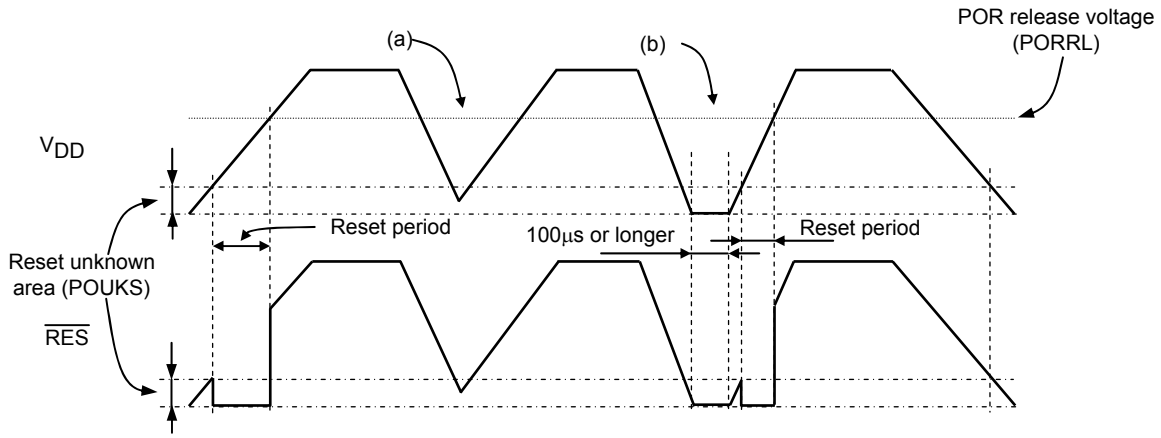


Figure 8 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- The POR function generates a reset only when the power voltage goes up from the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit as shown below.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

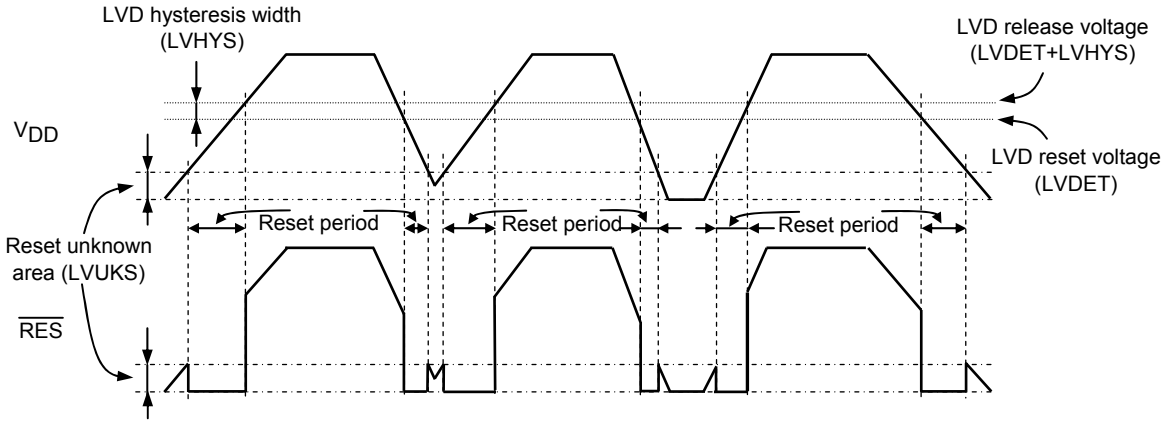


Figure 9 Example of POR + LVD Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

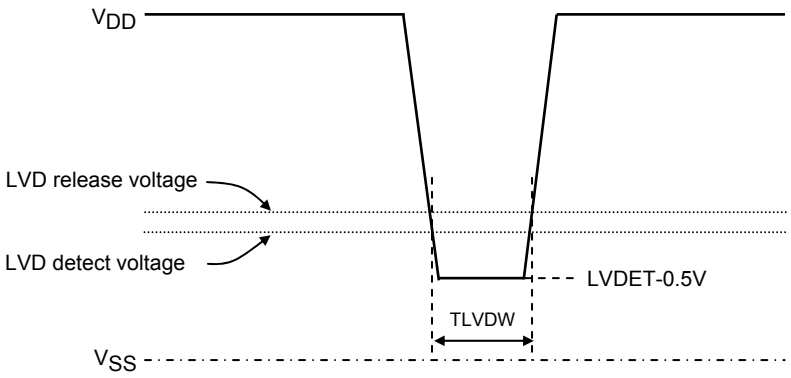


Figure 10 Minimum Low Voltage Detection Width (Example of Voltage Sag/Fluctuation Waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F0G08AUJA-AH	SSOP24(225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LC87F0G08AUJA-FH	SSOP24(225mil) (Pb-Free / Halogen Free)	2000 / Tape & Reel
LC87F0G08AUJA-ZH	SSOP24(225mil) (Pb-Free / Halogen Free)	1400 / Fan-Fold

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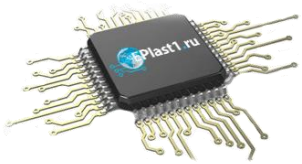

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