LSM330DLC

iNEMO inertial module: 3D accelerometer and 3D gyroscope

Datasheet — production data

Features

- Analog supply voltage: 2.4 V to 3.6 V
- Digital supply voltage IOs: 1.8 V
- Low power mode
- Power-down mode
- 3 independent acceleration channels and 3 angular rate channels
- ±2 *g*/±4 *g*/±8 *g*/±16 *g* dynamically selectable full scale
- ±250/±500/±2000 dps dynamically selectable full scale
- SPI/I^2C serial interface (16-bit data output)
- Programmable interrupt generator for free-fall and motion detection
- ECOPACK® RoHS and “Green” compliant

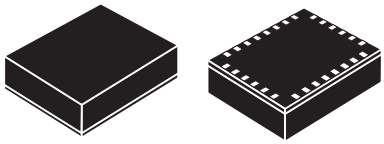
Application

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM330DLC is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers.



LGA-28L (4x5x1.1 mm)

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330DLC has dynamically user-selectable full scale acceleration range of ±2 *g*/±4 *g*/±8 *g*/±16 *g* and angular rate of ±250/±500/±2000 deg/sec.

The accelerometer and gyroscope sensors can be either activated or separately put in Low power/Power-down mode for applications optimized for power saving.

The LSM330DLC is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM330DLC	-40 to +85	LGA-28L (4x5x1.1 mm)	Tray
LSM330DLCTR	-40 to +85		Tape and reel

This is information on a product in full production. www.st.com

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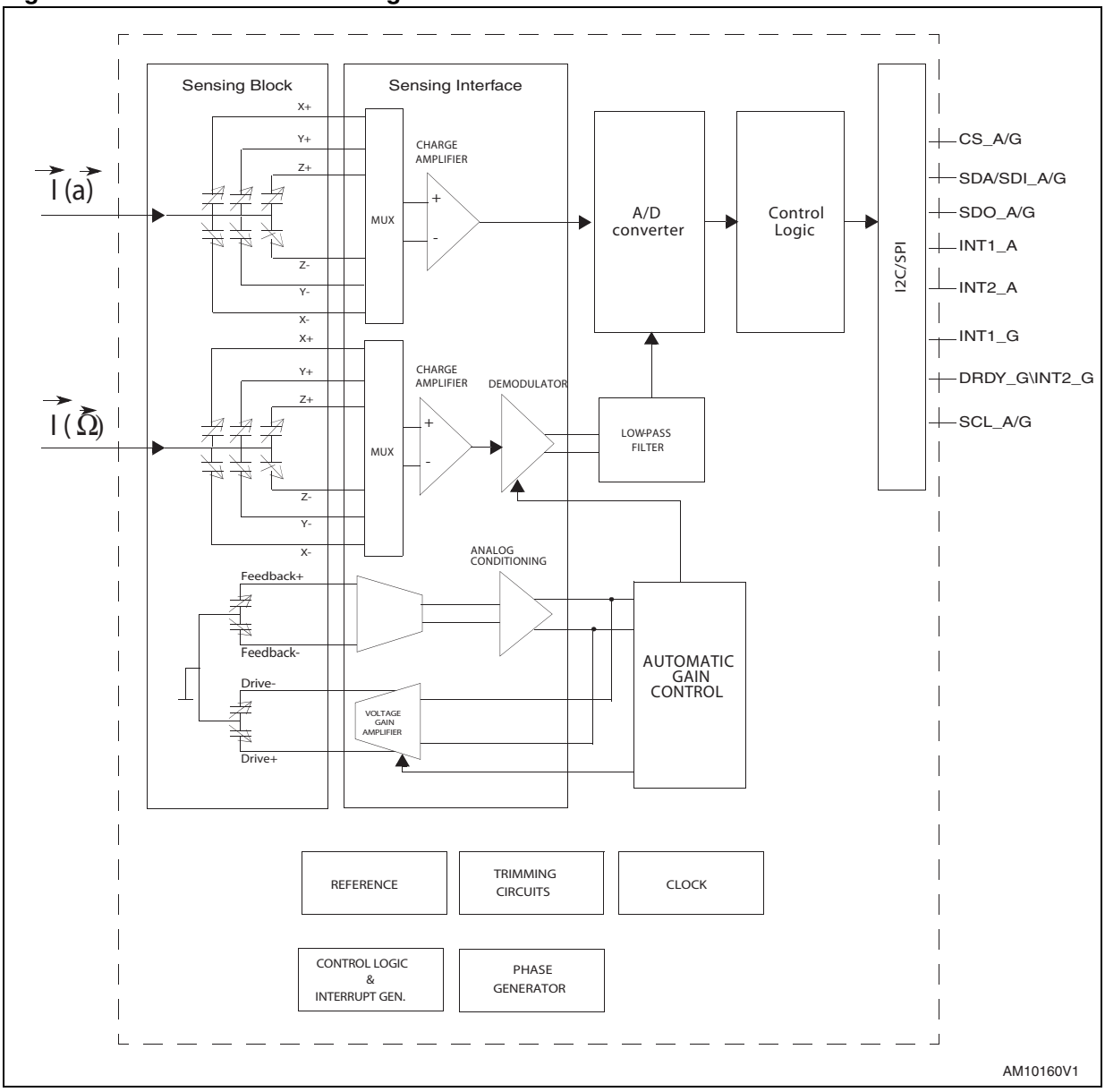
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. LSM330DLC block diagram



1.2 Pin description

Figure 2. Pin connection

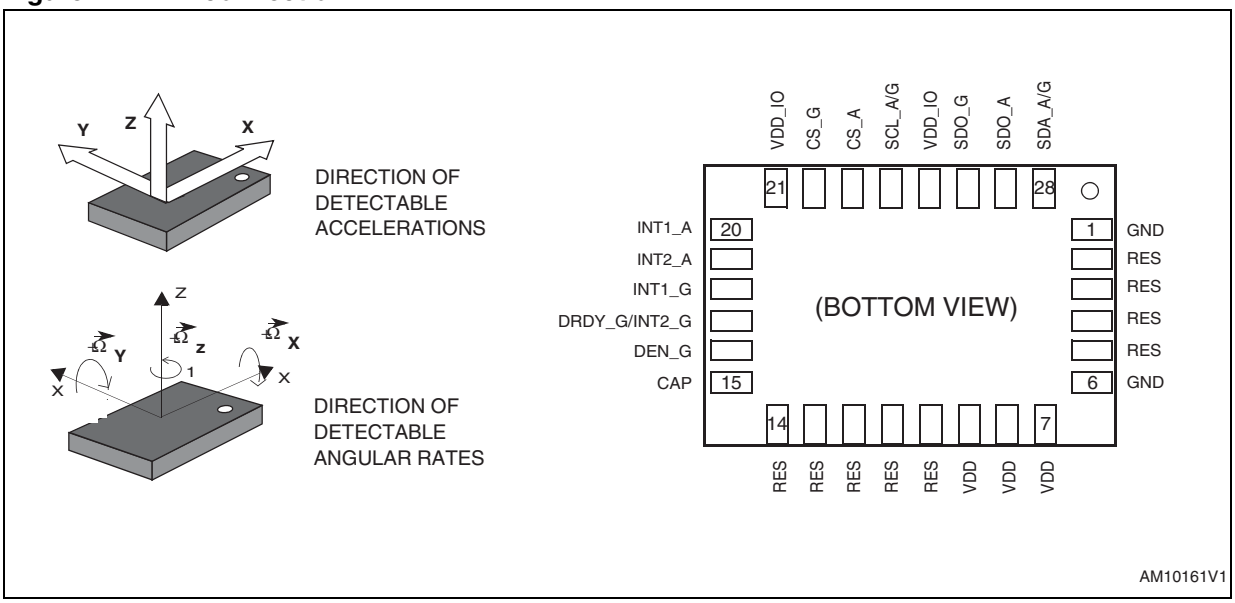


Table 2. Pin description

Pin#	Name	Function
1	GND	0 V supply
2	Res	Reserved. Connect to GND
3	Res	Reserved. Connect to GND
4	Res	Reserved. Connect to GND
5	Res	Reserved. Connect to GND
6	GND	0 V supply
7	Vdd	Power supply
8	Vdd	Power supply
9	Vdd	Power supply
10	Res	Reserved. Connect to Vdd
11	Res	Reserved. Connect to Vdd
12	Res	Reserved. Connect to Vdd
13	Res	Reserved. Connect to Vdd
14	Res	Reserved. Connect to Vdd
15	Cap	Connect to GND with ceramic capacitor, 10 nF (+/-10%), 25 V
16	DEN_G	Gyroscope data enable
17	DRDY_G/ INT2_G	Gyroscope data ready/interrupt signal 2
18	INT1_G	Gyroscope interrupt signal

Table 2. Pin description (continued)

Pin#	Name	Function
19	INT2_A	Accelerometer interrupt signal
20	INT1_A	Accelerometer interrupt signal
21	Vdd_IO	Power supply for IO pins
22	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
23	CS_A	Accelerometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
24	SCL_A/G	I^2C serial clock (SCL)/SPI serial port clock (SPC)
25	Vdd_IO	Power supply for IO pins
26	SDO_G	Gyroscope: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
27	SDO_A	Accelerometer: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
28	SDA_A/G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]	User-selectable		±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range[3]	User-selectable		±250		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	FS = ±2 *g*		1		m*g*/digit
		FS = ±4 *g*		2		
		FS = ±8 *g*		4		
		FS = ±16 *g*		12		
G_So	Angular rate sensitivity	FS = ±250 dps		8.75		mdps/ digit
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_So	Linear acceleration sensitivity change vs. temperature	FS = ±2 *g*		±0.05		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[3]	FS bit set to 00		±60		m*g*
G_TyOff	Angular rate typical zero-rate level[4]	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max delta from 25 °C		±0.5		m*g*/°C
G_TCOff	Zero-rate level change vs. temperature			±0.05		dps/°C
An	Acceleration noise density	FS = ±2 g, Normal mode *Table 9*, ODR bit set to 1001 *Table 19*		220		µg/√Hz

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

Table 3. Mechanical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Rn	Rate noise density	FS = ±250 dps, BW = 50 Hz		0.03		dps/√Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.

2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd+0.1	V
LA_Idd	Accelerometer current consumption in Normal mode	ODR = 50 Hz		11		µA
		ODR = 1 Hz		2		
LA_IddLowP	Accelerometer current consumption in Low power mode	ODR = 50 Hz		6		µA
LA_IddPdn	Accelerometer current consumption in Power-down mode			0.5		µA
G_Idd	Gyroscope current consumption in Normal mode			6.1		mA
G_IddLowP	Gyroscope supply current in Sleep mode(2)			2		mA
G_IddPdn	Gyroscope current consumption in Power-down mode			5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to Power-down mode.

2.3 Temperature sensor characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [b]

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

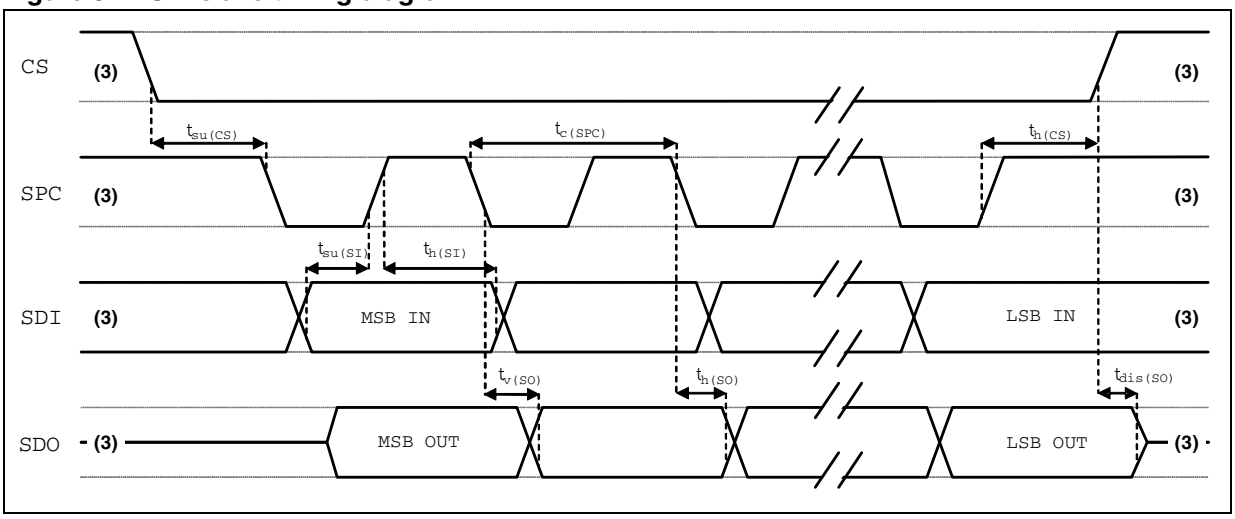
Subject to general operating conditions for Vdd and T_{OP}

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	6		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	9		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results. Not tested in production.

Figure 3. SPI slave timing diagram(c)(d)



3. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

c. The SDO output line features an internal pull-up.

d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter IC control interface

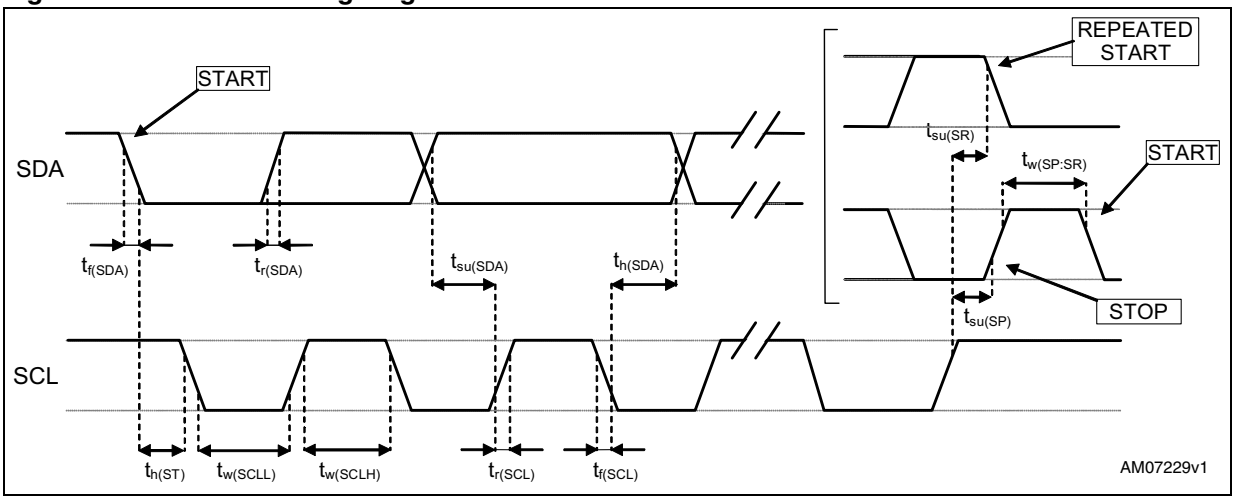
Subject to general operating conditions for Vdd and T_{OP}

Table 7. I²C slave timing values

Symbol	Parameter(1)	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	KHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. SCL (SCL_A/G pin), SDA (SDA_A/G pin)
2. Cb = total capacitance of one bus line, in pF

Figure 4. I²C slave timing diagram(e)



e. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings(1)

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL_A/G, SDA_A/G, SDO_A, SDO_G, CS_A, CS_G, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

1. Supply voltage on any pin should never exceed 4.8 V.



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.



This is an ESD sensitive device, improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

Linear acceleration sensitivity can be determined e.g. by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

Angular Rate Sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and also very little over time.

3.2 Zero-*g* level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X axis and Y axes, whereas the Z axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and over time.

4 Functionality

The LSM330DLC is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope.

The device includes specific sensing elements and two IC interfaces capable to measuring both the acceleration and angular rate applied to the module and to provide a signal to external applications through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330DLC may also be configured to generate an inertial *wakeup* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes.

4.1 Normal mode, Low power mode

The LSM330DLC provides two different operating modes: *Normal mode* and *Low power mode*. Normal mode guarantees high resolution, while Low power mode further reduces current consumption.

The table below summarizes how to select the operating mode and the corresponding characteristics.

Table 9. Operating mode selection

Operating mode	CTRL_REG1[3] (LPen bit)	CTRL_REG4[3] (HR bit)	BW [Hz]	Turn-on time [ms]
Low power mode (8-bit)	1	0	ODR/2	1
Normal mode (12-bit)	0	1	ODR/9	7/ODR(kHz)

4.1.1 Self-test

Self-test allows the checking of sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0’. When the self-test bit is programmed to ‘1’ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.1.2 6D/4D orientation detection

The LSM330DLC includes 6D/4D orientation detection. In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, Z axis position detection is disabled.

4.1.3 "Sleep-to-wake" and "Return to sleep"

The LSM330DLC can be programmed to automatically switch to Low power mode upon recognition of a determined event. Once the event condition is over, the device returns to the preset Normal mode.

To enable this function, the desired threshold value must be stored in the *Act_THS register*, while the duration value is written in the *Act_DUR register*.

When the internally high-pass filtered acceleration becomes lower than the threshold value on all the three axes, the device automatically switches to Low power mode (10Hz ODR). During this condition, the ODRx bits and LPen bit in the *CTRL_REG1_G register* and the HR bit in the *CTRL_REG3_G register* are not considered.

When the acceleration goes back over the threshold (on at least one axis), the system restores the operating mode and ODRs as per the *CTRL_REG1_G register* and *CTRL_REG3_G register* settings.

4.2 Linear acceleration digital main blocks

4.2.1 FIFO

The LSM330DLC embeds 32 slots of data FIFO for each of the three output channels: X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL_REG_A register*. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1_A/INT2_A pin (configured through the *FIFO_CTRL_REG_A register*).

4.2.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.3 FIFO mode

In FIFO mode, data from the X, Y and Z channels are stored into the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in the *FIFO_CTRL_REG_A register* in order to be raised when the FIFO is filled to the level specified into the FIFO_WTMK_LEVEL bits of the *FIFO_CTRL_REG_A register*. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO stops collecting data from the input channels.

4.2.4 Stream mode

In Stream mode, data from X, Y and Z measurement are stored into the FIFO. A watermark interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO discards the older data as the new data arrives.

4.2.5 Stream-to-FIFO mode

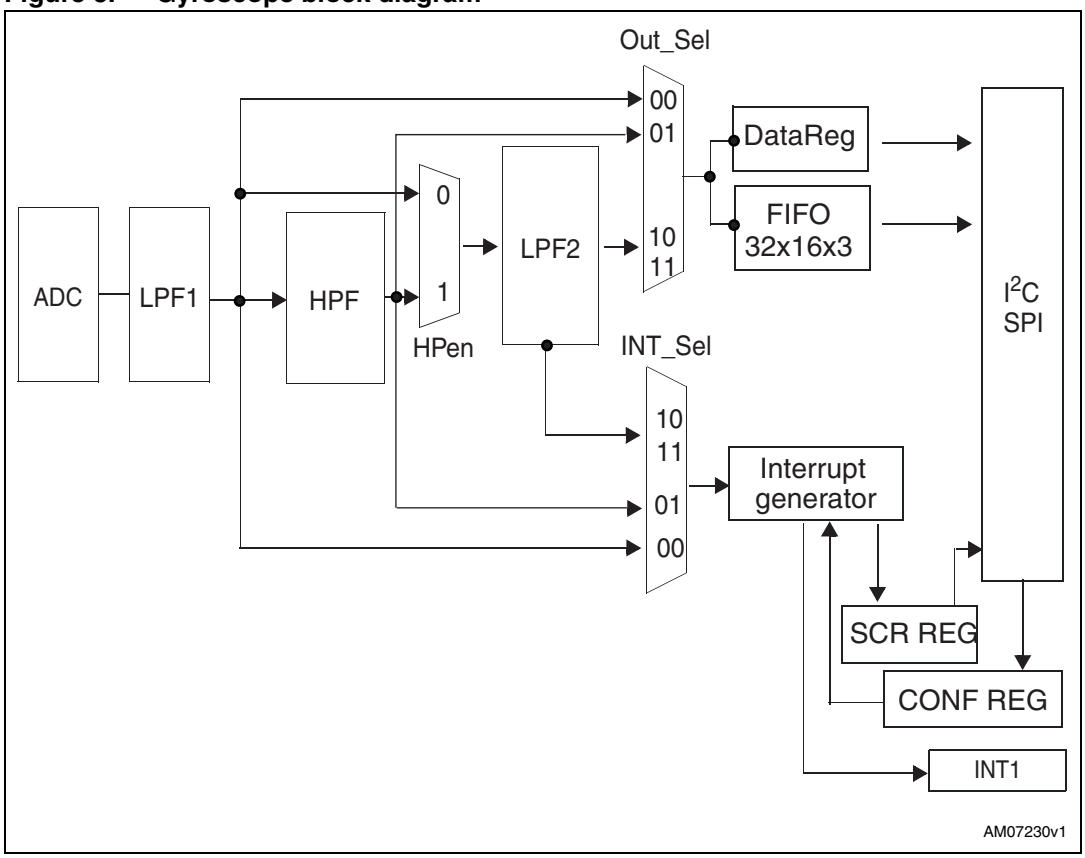
In Stream-to-FIFO mode, data from X, Y and Z measurement is stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in the *FIFO_CTRL_REG_A register*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of the *FIFO_CTRL_REG_A register*. The FIFO continues filling until it is full (32 slots of 8 -bit data for X, Y and Z). When full, the FIFO discards the older data as the data new arrives. Once trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.6 Retrieve data from FIFO

FIFO data is read through *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* and *OUT_Z_L _A, OUT_Z_H_A*. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* or *OUT_Z_L _A, OUT_Z_H_A* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* and *OUT_Z_L _A, OUT_Z_H_A* registers and both single read and read_burst operations can be used.

4.3 Gyroscope digital main blocks

Figure 5. Gyroscope block diagram



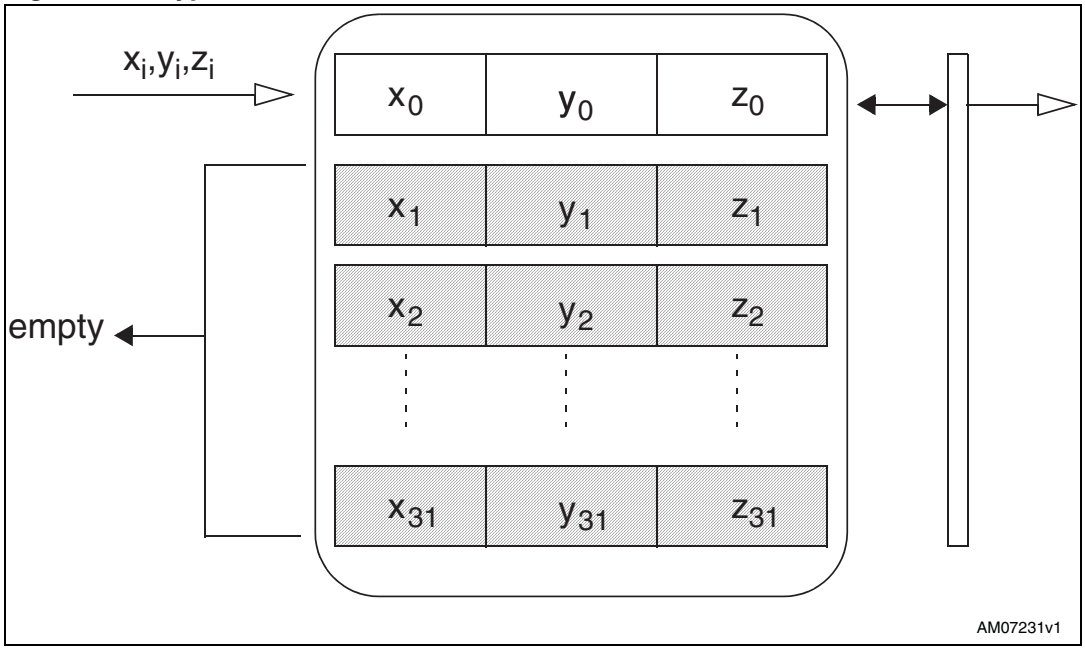
4.4 FIFO

The LSM330DLC embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL_REG_G register*. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through the *CTRL_REG3_G register* and event detection information is available in the *FIFO_SRC_REG_G register*. Watermark level can be configured to WTM4:0 in the *FIFO_CTRL_REG_G register*.

4.4.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 6* below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available the old data is overwritten.

Figure 6. Bypass mode

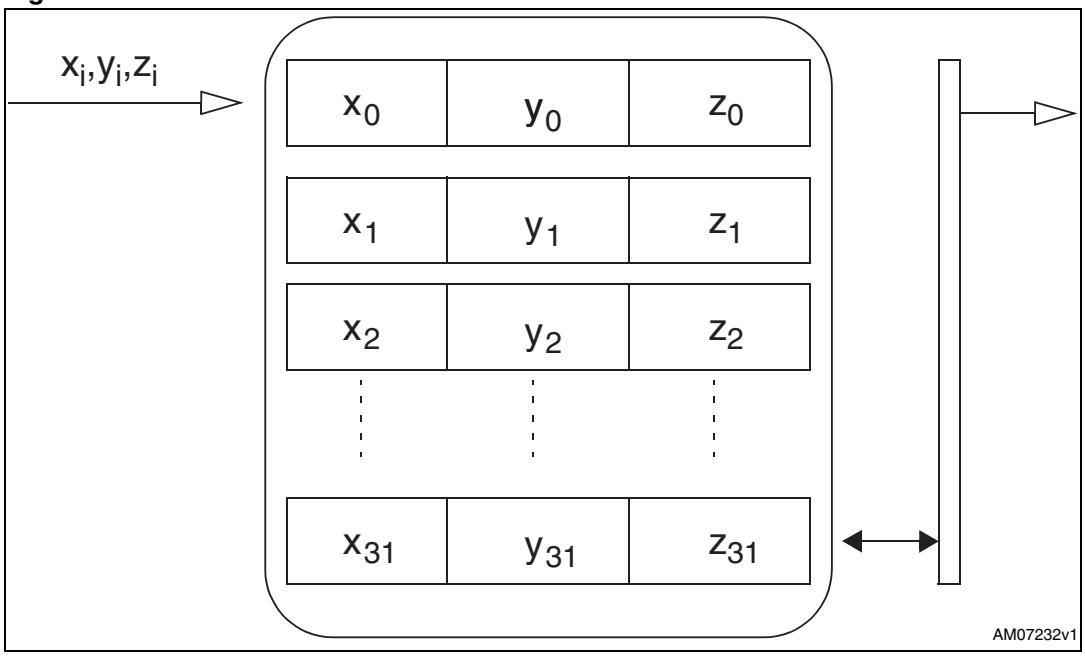


4.4.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in the *CTRL_REG3_G register*) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of the *FIFO_CTRL_REG_G register*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the *FIFO_CTRL_REG_G register* must be written back to Bypass mode.

FIFO mode is represented in *Figure 7: FIFO mode*.

Figure 7. FIFO mode

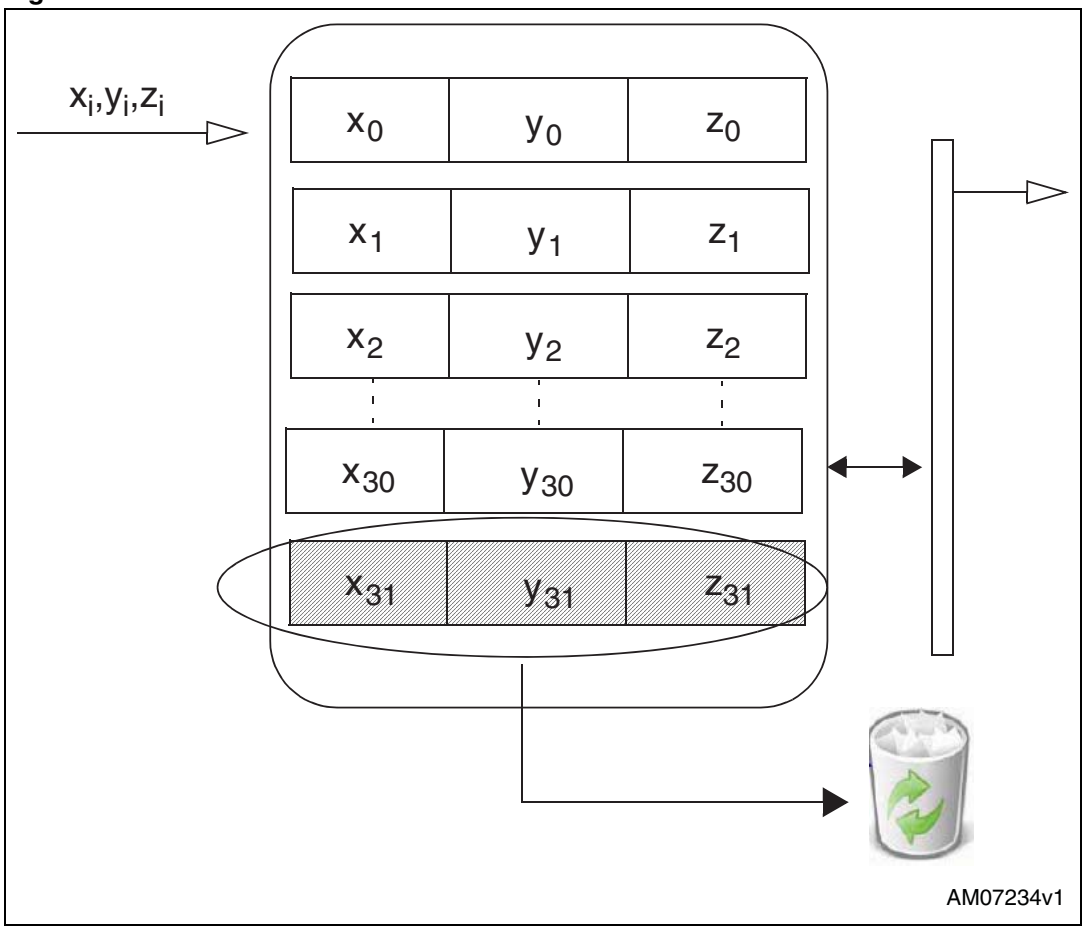


4.4.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through the *CTRL_REG3_G register*.

Stream mode is represented in *Figure 8: Stream mode*.

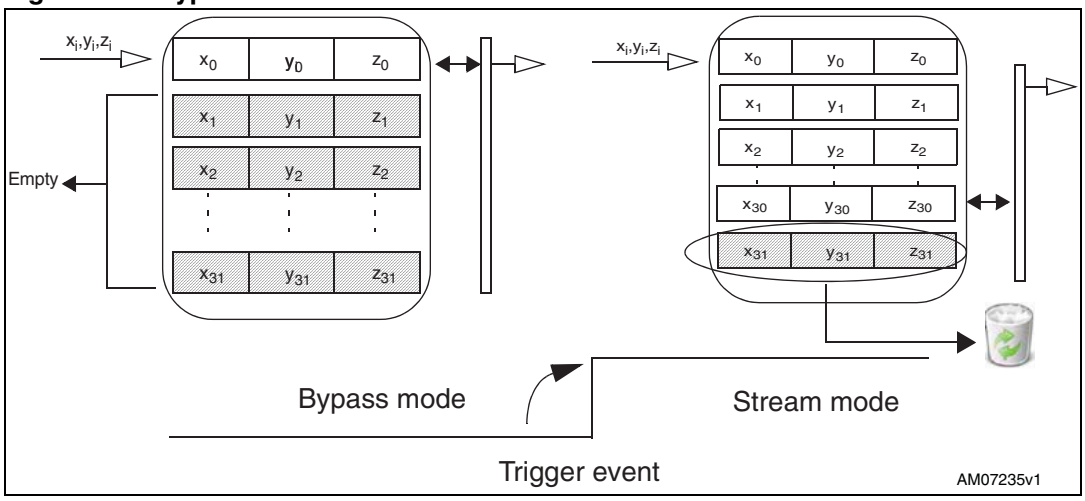
Figure 8. Stream mode



4.4.4 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *INT1_CFG_G register* events) the FIFO starts operating in Stream mode. Refer to *Figure 9* below.

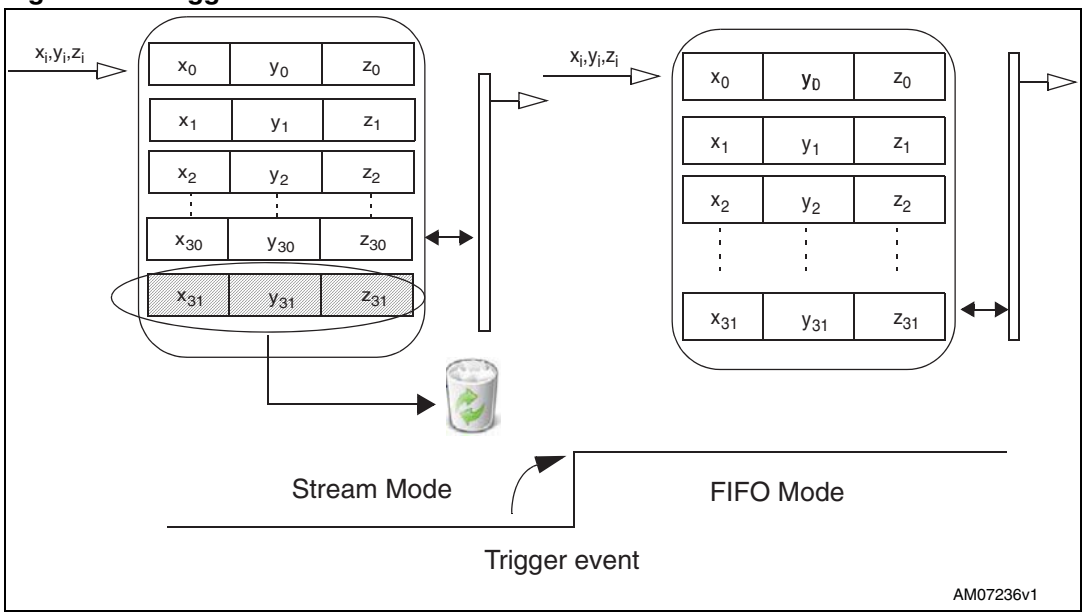
Figure 9. Bypass-to-stream mode



4.4.5 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2_WTM bit in *CTRL_REG3_G register* to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of the *FIFO_CTRL_REG_G register*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to *INT1_CFG_G register* events), the FIFO starts operating in FIFO mode. Refer to *Figure 10: Trigger stream mode*.

Figure 10. Trigger stream mode



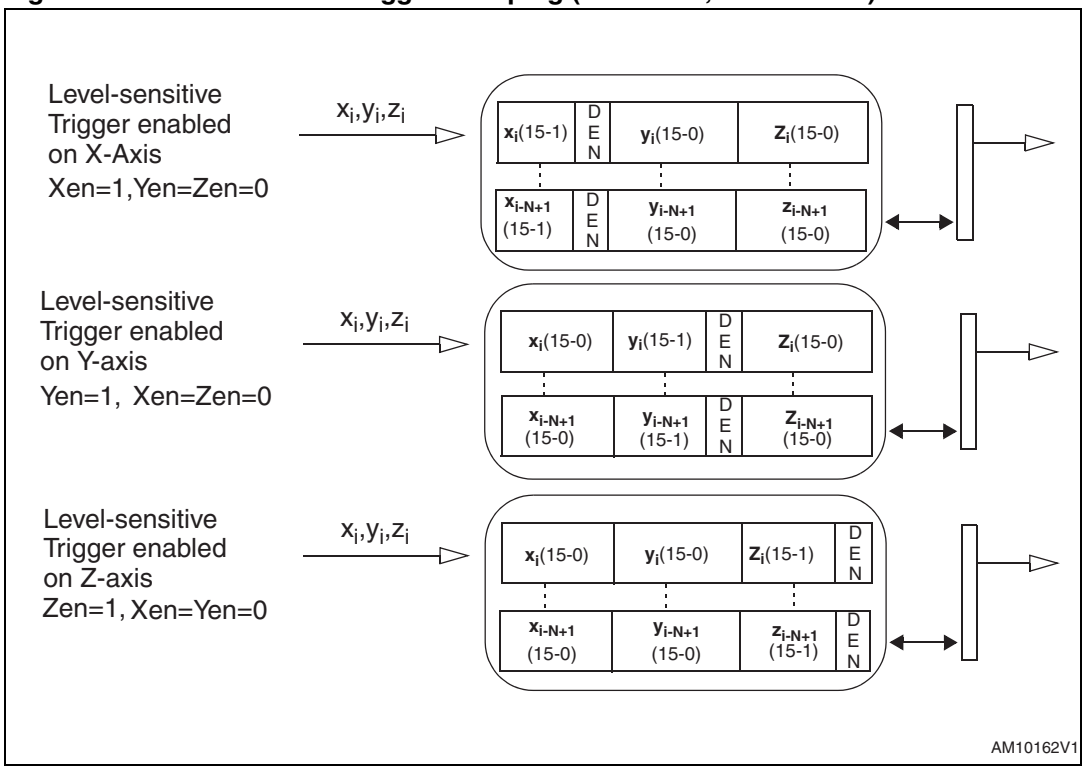
4.4.6 Retrieve data from FIFO

FIFO data is read through *OUT_X_L_G, OUT_X_H_G*, *OUT_Y_L_G, OUT_Y_H_G* and *OUT_Z_L_G, OUT_Z_H_G*. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the *OUT_X_L_G, OUT_X_H_G*, *OUT_Y_L_G, OUT_Y_H_G* or *OUT_Z_L_G, OUT_Z_H_G* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data are placed in the *OUT_X_L_G, OUT_X_H_G*, *OUT_Y_L_G, OUT_Y_H_G* and *OUT_Z_L_G, OUT_Z_H_G* registers and both single read and read_burst (X,Y & Z with autoincremental address) operations can be used. When data included in OUT_Z_H_G is read, the system again starts to read information from addr OUT_X_L _G.

4.5 Level-sensitive / Edge-sensitive data enable

The LSM330DLC allows external trigger level recognition through the enabling of the EXTRen and LVLen bits in the *CTRL_REG2_G register*. Two different modes can be used: Level-sensitive or Edge-sensitive trigger.

Figure 11. Level-sensitive trigger stamping (LVLen = 1; EXTRen = 0)



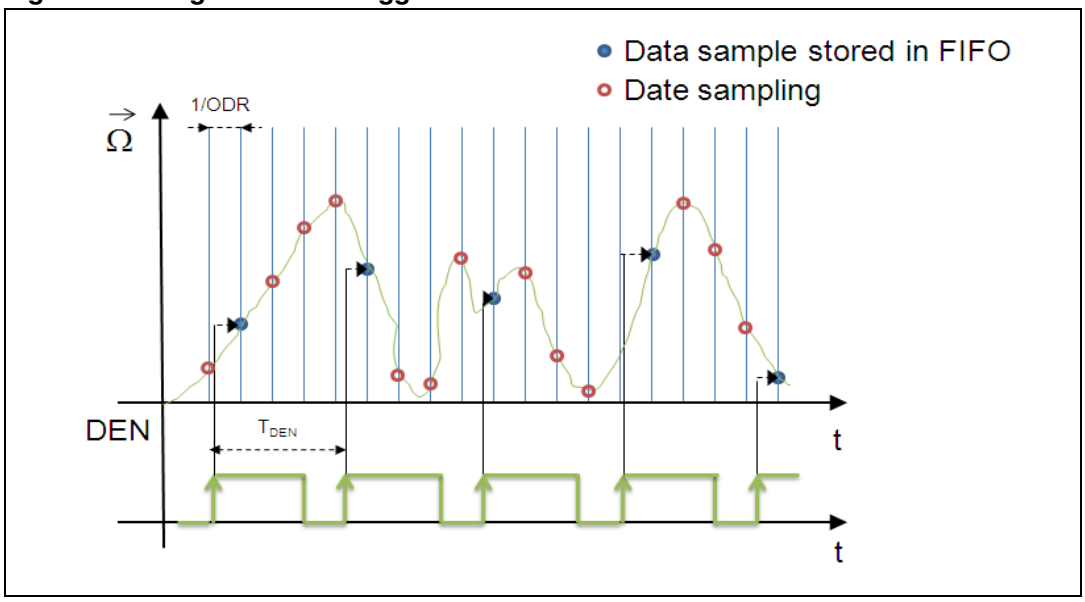
4.5.1 Level-sensitive trigger stamping

Once enabled, DEN level replaces the LSb of the X, Y or Z axes, configurable through the Xen, Yen, Zen bits in the *CTRL_REG1_G register*. Data is stored in the FIFO with the internally-selected ODR.

4.5.2 Edge-sensitive trigger

Once enabled by setting EXTRen = 1, FIFO is filled with the pitch, roll and yaw data on the rising edge of the DEN input signal. When selected ODR is 800 Hz, the maximum DEN sample frequency is $f_{DEN} = 1/T_{DEN} = 400$ Hz.

Figure 12. Edge-sensitive trigger

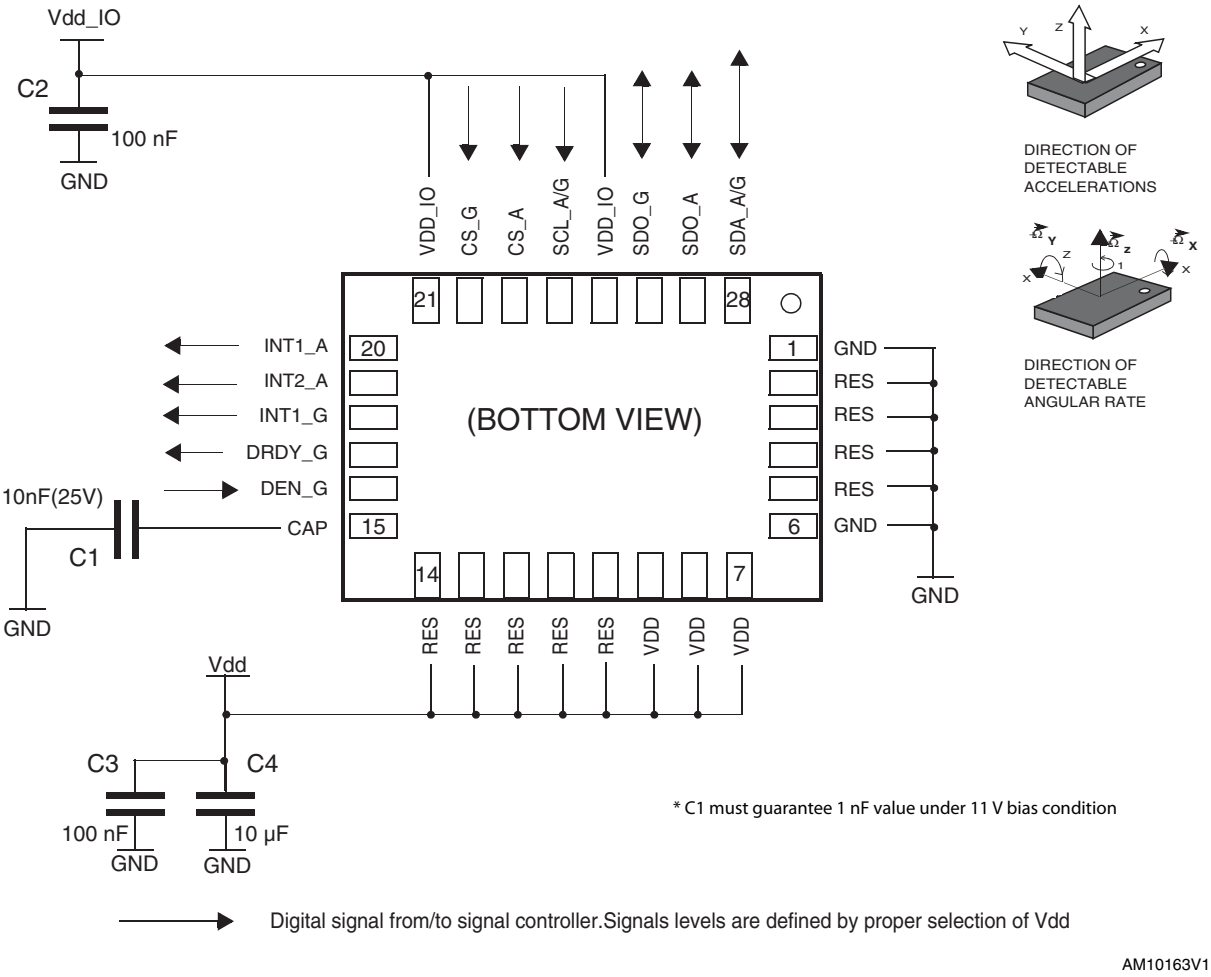


4.6 Factory calibration

The IC interface is factory calibrated for sensitivity and zero level. The trimming values are stored in the device in non volatile memory. Any time the device is turned on, the trimming parameters are downloaded to the registers to be used during normal operation. This allows use of the device without further calibration.

5 Application hints

Figure 13. LSM330DLC electrical connection



5.1 External capacitors

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C2, C3=100 *nF* ceramic, C4=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice).

All voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to *Figure 13*).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I^{2}C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I^{2}C interface.

5.2 Soldering information

The LGA package is compliant with ECOPACK®, RoHS and “Green” standards. It is qualified for soldering heat resistance according to JEDEC J-STD-020D.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

6 Digital interfaces

The registers embedded in the LSM330DLC may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS_A	Linear acceleration SPI enable Linear acceleration I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
CS_G	Angular rate SPI enable Angular rate I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL_A/G	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA_A/G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO_A SDO_G	I^2C least significant bit of the device address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LSM330DLC I^2C is a bus slave. The I^2C is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial DAta line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits, and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM330DLC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST), a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) will be automatically increased to allow multiple data read/write.

Table 12. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 13. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 14. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state.

Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pin (SDO_A / SDO_G) can be used to modify the least significant bit of the device address. If the SA0 pad is connected to voltage supply, the LSb is '1' (ex. address 0011001b), otherwise if the SA0 pad is connected to ground, the LSb value is '0' (ex address 0011000b).

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 16* and *17* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration address: the default (factory) 7-bit slave address is 001100xb.

Table 16. Linear acceleration SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO_A pin	R/W	SAD+R/W
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

Angular rate sensor: the default (factory) 7-bit slave address is 110101xb.

Table 17. Angular rate SAD+Read/Write patterns

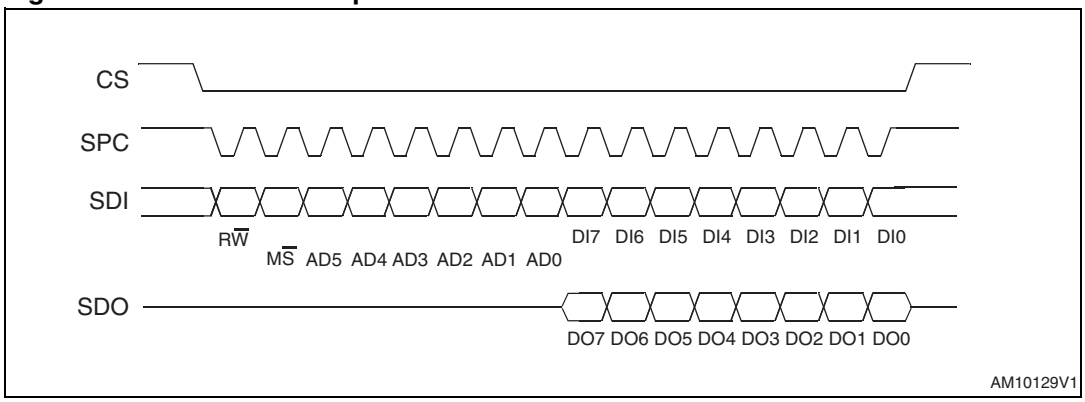
Command	SAD[6:1]	SAD[0] = SDO_G pin	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

6.2 SPI bus interface

The LSM330DLC SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO** (SPC, SDI, SD0 are common).

Figure 14. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple-byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS**, while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that will be written to the device (MSb first).

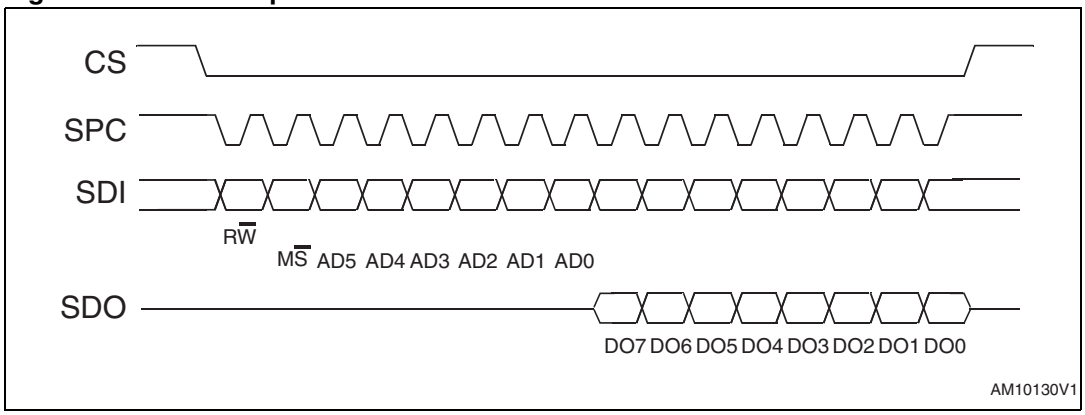
bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is '0', the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 15. SPI read protocol



The SPI read command is performed with 16 clock pulses. A multiple-byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

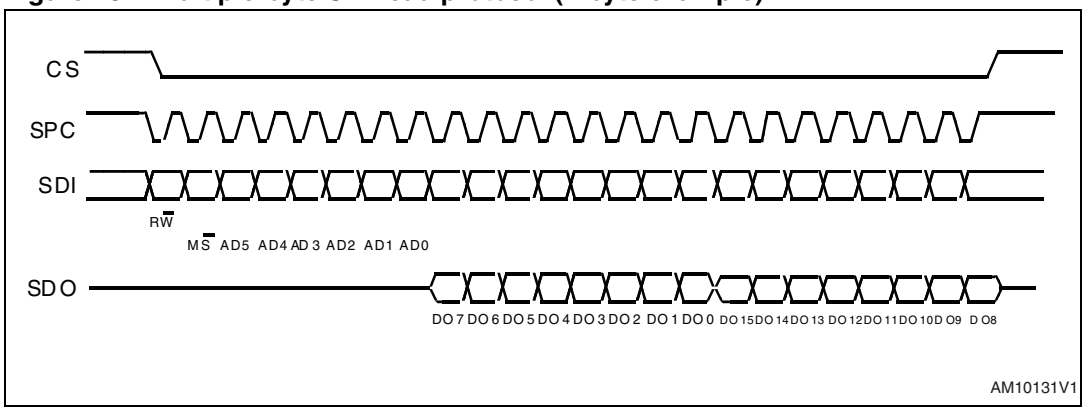
bit 1: MS bit. When 0, do not increment address; when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

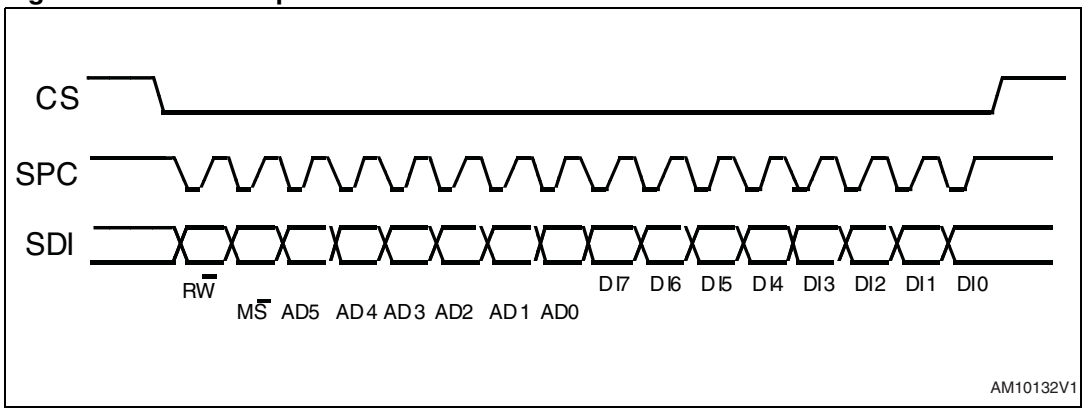
bit 16-... : data DO(...-8). Further data in multiple-byte reading.

Figure 16. Multiple-byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 17. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple-byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

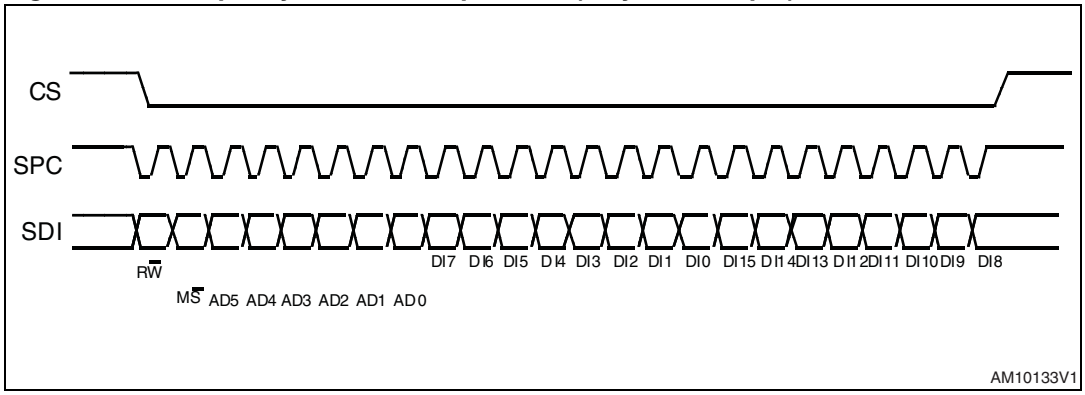
bit 1: MS bit. When 0, do not increment address; when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that will be written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple-byte writing.

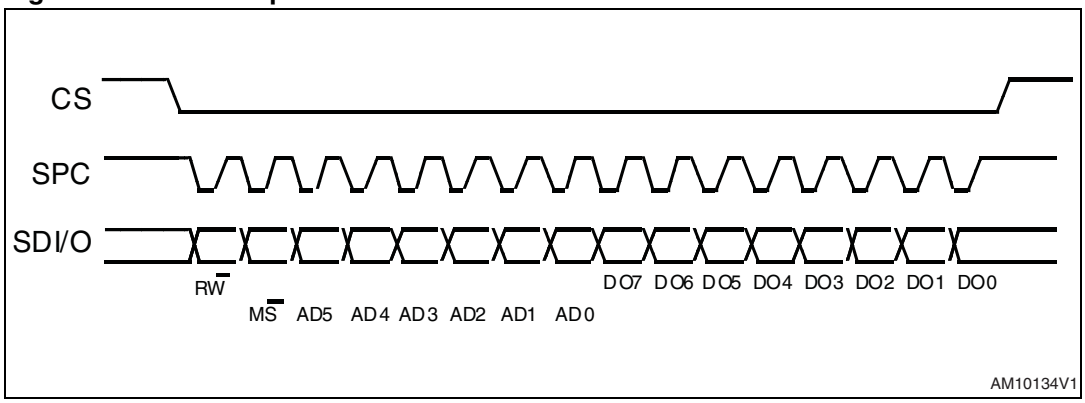
Figure 18. Multiple bytes SPI write protocol (2 bytes example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bit to ‘1’ (SPI serial interface mode selection) in the *CTRL_REG4_G register*.

Figure 19. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

7 Register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and their related addresses:

Table 18. Register address map

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
Reserved (do not modify)	*Table 16*		00 - 1F			Reserved
CTRL_REG1_A	*Table 16*	rw	20	010 0000	00000111	
CTRL_REG2_A	*Table 16*	rw	21	010 0001	00000000	
CTRL_REG3_A	*Table 16*	rw	22	010 0010	00000000	
CTRL_REG4_A	*Table 16*	rw	23	010 0011	00000000	
CTRL_REG5_A	*Table 16*	rw	24	010 0100	00000000	
CTRL_REG6_A	*Table 16*	rw	25	010 0101	00000000	
REFERENCE_A	*Table 16*	rw	26	010 0110	00000000	
STATUS_REG_A	*Table 16*	r	27	010 0111	00000000	
OUT_X_L_A	*Table 16*	r	28	010 1000	output	
OUT_X_H_A	*Table 16*	r	29	010 1001	output	
OUT_Y_L_A	*Table 16*	r	2A	010 1010	output	
OUT_Y_H_A	*Table 16*	r	2B	010 1011	output	
OUT_Z_L_A	*Table 16*	r	2C	010 1100	output	
OUT_Z_H_A	*Table 16*	r	2D	010 1101	output	
FIFO_CTRL_REG	*Table 16*	rw	2E	010 1110	00000000	
FIFO_SRC_REG	*Table 16*	r	2F	010 1111		
INT1_CFG_A	*Table 16*	rw	30	011 0000	00000000	
INT1_SOURCE_A	*Table 16*	r	31	011 0001	00000000	
INT1_THS_A	*Table 16*	rw	32	011 0010	00000000	
INT1_DURATION_A	*Table 16*	rw	33	011 0011	00000000	
INT2_CFG_A	*Table 16*	rw	34	011 0100	00000000	
INT2_SOURCE_A	*Table 16*	r	35	011 0101	00000000	
INT2_THS_A	*Table 16*	rw	36	011 0110	00000000	
INT2_DURATION_A	*Table 16*	rw	37	011 0111	00000000	
CLICK_CFG_A	*Table 16*	rw	38	011 1000	00000000	
CLICK_SRC_A	*Table 16*	rw	39	011 1001	00000000	
CLICK_THS_A	*Table 16*	rw	3A	011 1010	00000000	
TIME_LIMIT_A	*Table 16*	rw	3B	011 1011	00000000	

Table 18. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
TIME_LATENCY_A	Table 16	rw	3C	011 1100	00000000	
TIME_WINDOW_A	Table 16	rw	3D	011 1101	00000000	
Act_THS	Table 16	rw	3E	011 1110	00000000	
Act_DUR	Table 16	rw	3F	011 1111	00000000	
Reserved	Table 17	-	00-1E	-	-	Reserved
WHO_AM_I_G	Table 17	rw	0F	0001111	11010100	
Reserved	Table 17	rw	10-1F	-	-	
CTRL_REG1_G	Table 17	rw	20	010 0000	00000111	
CTRL_REG2_G	Table 17	rw	21	010 0001	00000000	
CTRL_REG3_G	Table 17	rw	22	010 0010	00000000	
CTRL_REG4_G	Table 17	rw	23	010 0011	00000000	
CTRL_REG5_G	Table 17	r	24	010 0100	00000000	
REFERENCE_G	Table 17	r	25	010 0101	00000000	
OUT_TEMP_G	Table 17	r	26	010 0110	output	
STATUS_REG_G	Table 17	r	27	010 0111	output	
OUT_X_L_G	Table 17	r	28	010 1000	output	
OUT_X_H_G	Table 17	r	29	010 1001	output	
OUT_Y_L_G	Table 17	r	2A	010 1010	output	
OUT_Y_H_G	Table 17	r	2B	010 1011	output	
OUT_Z_L_G	Table 17	rw	2C	010 1100	output	
OUT_Z_H_G	Table 17	r	2D	010 1101	output	
FIFO_CTRL_REG_G	Table 17	rw	2E	010 1110	00000000	
FIFO_SRC_REG_G	Table 17	r	2F	010 1111	output	
INT1_CFG_G	Table 17	rw	30	011 0001	output	
INT1_SRC_G	Table 17	rw	31	011 0001	output	
INT1_TSH_XH_G	Table 17	rw	32	011 0010	00000000	
INT1_TSH_XL_G	Table 17	rw	33	011 0011	00000000	
INT1_TSH_YH_G	Table 17	rw	34	011 0100	00000000	
INT1_TSH_YL_G	Table 17	rw	35	011 0101	00000000	
INT1_TSH_ZH_G	Table 17	rw	36	011 0110	00000000	
INT1_TSH_ZL_G	Table 17	rw	37	011 0111	00000000	
INT1_DURATION_G	Table 17	rw	38	011 1000	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register descriptions

The device contains a set of registers which are used to control its behavior and to retrieve acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

8.1 CTRL_REG1_A (20h)

Table 19. CTRL_REG1_A register

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

Table 20. CTRL_REG1_A description

ODR3-0	Data rate selection. Default value: 0 (0000: Power-down; Others: refer to *Table 21*, “Data rate configuration”)
LPen	Low power mode enable. Default value: 0 (0: Normal mode, 1: Low power mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

ODR<3:0> is used to set the power mode and ODR selection. *Table 21* below provides all the frequencies resulting from the ODR<3:0> combinations.

Table 21. Data rate configuration

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	Normal / Low power mode (1 Hz)
0	0	1	0	Normal / Low power mode (10 Hz)
0	0	1	1	Normal / Low power mode (25 Hz)
0	1	0	0	Normal / Low power mode (50 Hz)
0	1	0	1	Normal / Low power mode (100 Hz)
0	1	1	0	Normal / Low power mode (200 Hz)
0	1	1	1	Normal / Low power mode (400 Hz)
1	0	0	0	Low power mode (1.620 kHz)
1	0	0	1	Normal (1.344 kHz) / Low power mode (5.376 kHz)

8.2 CTRL_REG2_A (21h)

Table 22. CTRL_REG2_A register

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

Table 23. CTRL_REG2_A description

HPM1 -HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 24*, “High pass filter mode configuration”
HPCF2 - HPCF1	High-pass filter cut-off frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
HPCLICK	High-pass filter enabled for CLICK function. (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for AOI function on interrupt 2, (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for AOI function on interrupt 1, (0: filter bypassed; 1: filter enabled)

Table 24. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

8.3 CTRL_REG3_A (22h)

Table 25. CTRL_REG3_A register

I1_CLICK	I1_AOI1	0(1)	I1_DRDY1	I1_DRDY2	I1_WTM	I1_OVERRUN	--

1. This bit has to be set ‘0’ for correct operation

Table 26. CTRL_REG3_A description

I1_CLICK	CLICK interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)
I1_AOI1	AOI1 interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)

Table 26. CTRL_REG3_A description (continued)

I1_DRDY1	DRDY1 interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)
I1_DRDY2	DRDY2 interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)
I1_WTM	FIFO watermark interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)
I1_OVERRUN	FIFO Overrun interrupt on INT1_A. Default value 0. (0: Disable; 1: Enable)

8.4 CTRL_REG4_A (23h)

Table 27. CTRL_REG4_A register

0(1)	BLE	FS1	FS0	HR	0(1)	0(1)	SIM

1. This bit must be set to '0' for correct operation.

Table 28. CTRL_REG4_A description

BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full Scale selection. default value: 00 (00: +/- 2G; 01: +/- 4G; 10: +/- 8G; 11: +/- 16G)
HR	High resolution output mode: Default value: 0 (0: High resolution disable; 1: High resolution enable)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

8.5 CTRL_REG5_A (24h)

Table 29. CTRL_REG5_A register

BOOT	FIFO_EN	--	--	LIR_INT1	D4D_INT1	0(1)	0(1)

1. This bit must be set to '0' for correct operation.

Table 30. CTRL_REG5_A description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)

Table 30. CTRL_REG5_A description (continued)

LIR_INT1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
D4D_INT1	4D enable: 4D detection is enabled on INT1 when 6D bit on INT1_CFG is set to 1.

8.6 CTRL_REG6_A (25h)

Table 31. CTRL_REG6_A register

I2_CLICKen	I2_INT1	0(1)	BOOT_I2	0(1)	--	H_LACTIVE	--

1. This bit must be set to '0' for correct operation.

Table 32. CTRL_REG6 description

I2_CLICKen	Click interrupt on INT2_A. Default value 0.
I2_INT1	Interrupt 1 function enabled on INT2_A. Default 0.
BOOT_I2	Boot on INT2_A.
H_LACTIVE	0: interrupt active high; 1: interrupt active low.

8.7 REFERENCE/DATACAPTURE_A (26h)

Table 33. REFERENCE_A register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 34. REFERENCE register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

8.8 STATUS_REG_A (27h)

Table 35. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 36. STATUS_REG_A register description

ZYXOR	X, Y and Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)

Table 36. STATUS_REG_A register description (continued)

YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y and Z axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)

8.9 OUT_X_L_A, OUT_X_H_A

X-axis acceleration data. The value is expressed in two's complement.

8.10 OUT_Y_L_A, OUT_Y_H_A

Y-axis acceleration data. The value is expressed in two's complement.

8.11 OUT_Z_L _A, OUT_Z_H_A

Z-axis acceleration data. The value is expressed in two's complement.

8.12 FIFO_CTRL_REG_A (2Eh)

Table 37. FIFO_CTRL_REG_A register

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

Table 38. FIFO_CTRL_REG_A register description

FM1-FM0	FIFO mode selection. Default value: 00 (see *Table 39: FIFO mode configuration*)
TR	Trigger selection. Default value: 0 0: Trigger event linked to trigger signal on INT1_A 1: Trigger event linked to trigger signal on INT2_A
FTH4:0	Default value: 0

Table 39. FIFO mode configuration

FM1	FM0	FIFO mode
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Trigger mode

8.13 FIFO_SRC_REG_A (2Fh)

Table 40. FIFO_SRC_REG_A register

WTM	OVRN_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 41. FIFO_SRC_REG_A description

WTM	WTM bit is set high when FIFO content exceeds watermark level
OVRN_FIFO	OVRN bit is set high when FIFO buffer is full, this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is reset when the first sample set has been read
EMPTY	EMPTY flag is set high when all FIFO samples have been read and FIFO is empty
FSS4-0	FSS[4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time that one sample set is retrieved from FIFO

8.14 INT1_CFG_A (30h)

Table 42. INT1_CFG_A register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 43. INT1_CFG_A description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 44: Interrupt mode*, “Interrupt mode”
6D	6 direction detection function enabled. Default value: 0. Refer to *Table 44: Interrupt mode*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)

Table 43. INT1_CFG_A description (continued)

YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

The content of this register is loaded at boot.

A write operation at this address is possible only after system boot.

.

Table 44. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from “unknown zone” to “known zone”. The interrupt signal remains for an ODR duration.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a “known zone”. The interrupt signal remains until orientation is within the zone.

8.15 INT1_SRC_A (31h)

Table 45. INT1_SRC_A register

0(1)	IA	ZH	ZL	YH	YL	XH	XL

1. This bit must be set to ‘0’ for correct operation.

Table 46. INT1_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)

Table 46. INT1_SRC_A description (continued)

YH	Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt 1 source register. Read only register.

Reading at this address clears INT1_SRC_A IA bit (and the interrupt signal on INT 1 pin) and allows the refreshing of the data in the *INT1_SRC_A register* if the latched option was chosen.

8.16 INT1_THS_A (32h)

Table 47. INT1_THS_A register

0(1)	THS6	THS5	THS4	THS3	THS2	THS1	THS0

1. This bit has to be set '0' for correct operation.

Table 48. INT1_THS_A description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.17 INT1_DURATION_A (33h)

Table 49. INT1_DURATION_Aregister

0(1)	D6	D5	D4	D3	D2	D1	D0

1. This bit must be set '0' for correct operation.

Table 50. INT1_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.18 CLICK_CFG _A (38h)

Table 51. CLICK_CFG_A register

--	--	ZD	ZS	YD	YS	XD	XS

Table 52. CLICK_CFG_A description

ZD	Enable interrupt double CLICK on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single CLICK on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double CLICK on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single CLICK on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double CLICK on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single CLICK on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.19 CLICK_SRC_A (39h)

Table 53. CLICK_SRC_A register

--	IA	DCLICK	SCLICK	Sign	Z	Y	X

Table 54. CLICK_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DCLICK	Double CLICK-CLICK enable. Default value: 0 (0:double CLICK-CLICK detection disable, 1: double CLICK-CLICK detection enable)
SCLICK	Single CLICK-CLICK enable. Default value: 0 (0:Single CLICK-CLICK detection disable, 1: single CLICK-CLICK detection enable)
Sign	CLICK-CLICK Sign. 0: positive detection, 1: negative detection
Z	Z CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Z High event has occurred)

Table 54. CLICK_SRC_A description

Y	Y CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
X	X CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: X High event has occurred)

8.20 CLICK_THS_A (3Ah)

Table 55. CLICK_THS_A register

--	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 56. CLICK_SRC_A description

Ths6-Ths0	CLICK-CLICK threshold. Default value: 000 0000

8.21 TIME_LIMIT_A (3Bh)

Table 57. TIME_LIMIT_A register

--	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 58. TIME_LIMIT_A description

TLI7-TLI0	CLICK-CLICK Time limit. Default value: 000 0000

8.22 TIME_LATENCY_A (3Ch)

Table 59. TIME_LATENCY_A register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 60. TIME_LATENCY_A description

TLA7-TLA0	CLICK-CLICK time latency. Default value: 000 0000

8.23 TIME WINDOW_A (3Dh)

Table 61. TIME_WINDOW_A register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 62. TIME_WINDOW_A description

TW7-TW0	CLICK-CLICK time window

8.24 Act_THS (3Eh)

Table 63. Act_THS register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 64. Act_THS description

Acth[6-0]	Sleep-to-Wake, Return to Sleep activation threshold 1LSb = 16m*g*

8.25 Act_DUR (3Fh)

Table 65. Act_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 66. Act_DUR description

ActD[7-0]	Sleep-to-Wake, Return to Sleep duration DUR = (Act_DUR + 1)*8/ODR

8.26 WHO_AM_I_G (0Fh)

Table 67. WHO_AM_I_G register

1	1	0	1	0	1	0	0

Device identification register.

8.27 CTRL_REG1_G (20h)

Table 68. CTRL_REG1_G register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 69. CTRL_REG1_G description

DR1-DR0	Output data rate selection. Refer to *Table 70*
BW1-BW0	Bandwidth selection. Refer to *Table 70*

Table 69. CTRL_REG1_G description

PD	Power-down mode enable. Default value: 0 (0: Power-down mode, 1: Normal mode or Sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used to set ODR selection. **BW <1:0>** is used to set bandwidth selection.

Table 70 below provides all the frequencies resulting from the DR / BW bit combinations.

Table 70. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-off
00	00	95	12.5
00	01	95	25
00	10	95	25
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

The combination of **PD, Zen, Yen, Xen** is used to set the device in different modes (Power-down / Normal / Sleep mode) according to the following table:

Table 71. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-

Table 71. Power mode selection configuration

Sleep	1	0	0	0
Normal	1	-	-	-

8.28 CTRL_REG2_G (21h)

Table 72. CTRL_REG2_G register

EXTRen	LVLen	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

Table 73. CTRL_REG2_G description

EXTRen	Edge-sensitive trigger Enable: Default value: 0 (0: external trigger disabled; 1: External trigger enabled)
LVLen	Level-sensitive trigger Enable: Default value: 0 (0: level sensitive trigger disabled; 1: level sensitive trigger enabled)
HPM1- HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 74*
HPCF3- HPCF0	High-pass filter cut-off frequency selection Refer to *Table 75*

Table 74. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 75. High-pass filter cut-off frequency configuration [Hz]

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45

Table 75. High-pass filter cut-off frequency configuration [Hz] (continued)

1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

8.29 CTRL_REG3_G (22h)

Table 76. CTRL_REG3_G register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 77. CTRL_REG3_G description

I1_Int1	Interrupt enable on INT1_G pin. Default value 0. (0: Disable; 1: Enable)
I1_Boot	Boot status available on INT1_G. Default value 0. (0: Disable; 1: Enable)
H_Lactive	Interrupt active configuration on INT1_G. Default value 0. (0: High; 1:Low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: Push-pull; 1: Open drain)
I2_DRDY	Date ready on DRDY_G/INT2_G. Default value 0. (0: Disable; 1: Enable)
I2_WTM	FIFO watermark interrupt on DRDY_G/INT2_G. Default value: 0. (0: Disable; 1: Enable)
I2_ORun	FIFO overrun interrupt on DRDY_G/INT2_G Default value: 0. (0: Disable; 1: Enable)
I2_Empty	FIFO empty interrupt on DRDY_G/INT2_G. Default value: 0. (0: Disable; 1: Enable)

8.30 CTRL_REG4_G (23h)

Table 78. CTRL_REG4_G register

BDU	BLE	FS1	FS0	-	0	0	SIM

Table 79. CTRL_REG4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	3-wire SPI Serial interface read mode enable. Default value: 0 (0: 3-wire Read mode disabled; 1: 3-wire read enabled).

8.31 CTRL_REG5_G (24h)

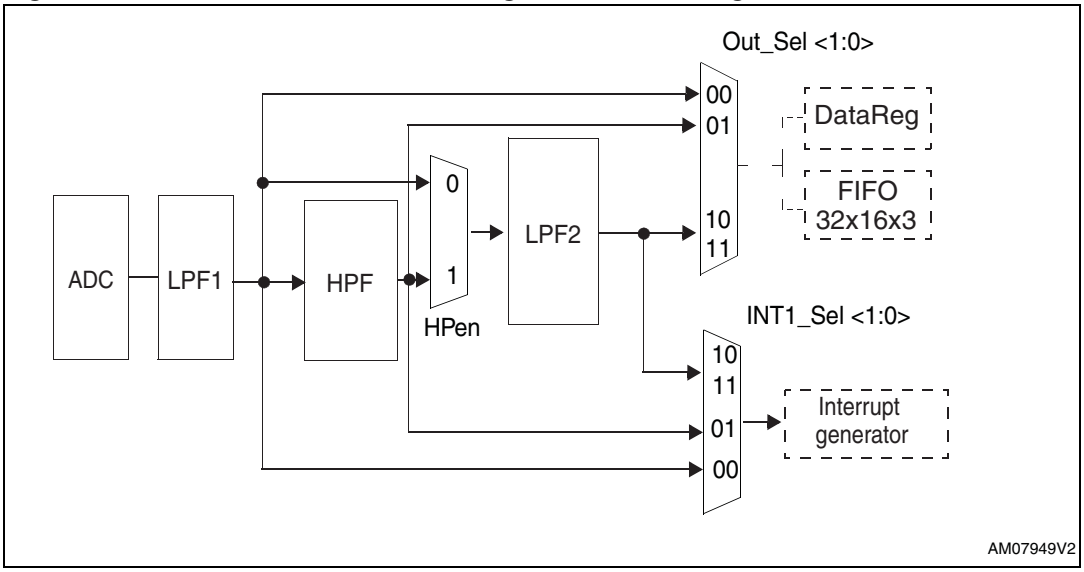
Table 80. CTRL_REG5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 81. CTRL_REG5_G description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
HPen	High-pass filter Enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, see *Figure 20*)
INT1_Sel1- INT1_Sel0	INT1 selection configuration. Default value: 0 (see *Figure 20*)
Out_Sel1- Out_Sel1	Out selection configuration. Default value: 0 (see *Figure 20*)

Figure 20. INT1_Sel and Out_Sel configuration block diagram



8.32 REFERENCE_G (25h)

Table 82. REFERENCE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 83. REFERENCE_G register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

8.33 OUT_TEMP_G (26h)

Table 84. OUT_TEMP_G register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 85. OUT_TEMP_G register description

Temp7-Temp0	Temperature data (1LSb/deg - 8-bit resolution). The value is expressed as two's complement.

8.34 STATUS_REG_G (27h)

Table 86. STATUS_REG_G register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 87. STATUS_REG description

ZYXOR	X, Y, Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.35 OUT_X_L_G, OUT_X_H_G

X-axis angular rate data. The value is expressed as two's complement.

8.36 OUT_Y_L_G, OUT_Y_H_G

Y-axis angular rate data. The value is expressed as two's complement.

8.37 OUT_Z_L_G, OUT_Z_H_G

Z-axis angular rate data. The value is expressed as two's complement.

8.38 FIFO_CTRL_REG_G (2Eh)

Table 88. FIFO_CTRL_REG_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 89. FIFO_CTRL_REG_G description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 90*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 90. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-stream mode

8.39 FIFO_SRC_REG_G (2Fh)

Table 91. FIFO_SRC_REG_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 92. FIFO_SRC_REG_G description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

8.40 INT1_CFG_G (30h)

Table 93. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 94. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch Interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC_G reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

Configuration register for interrupt source.

8.41 INT1_SRC_G (31h)

Table 95. INT1_SRC_G register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 96. INT1_SRC_G description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)

Table 96. INT1_SRC_G description

ZL	Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt source register. Read only register.

Reading at this address clears the INT1_SRC_G IA bit (and eventually the interrupt signal on the INT1_G pin) and allows the refreshing of data in the *INT1_SRC_G register* if the latched option was chosen.

8.42 INT1_THS_XH_G (32h)

Table 97. INT1_THS_XH_G register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 98. INT1_THS_XH_G description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000

8.43 INT1_THS_XL_G (33h)

Table 99. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 100. INT1_THS_XL_G description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

8.44 INT1_THS_YH _G (34h)

Table 101. INT1_THS_YH_G register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 102. INT1_THS_YH_G description

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000

8.45 INT1_THS_YL_G (35h)

Table 103. INT1_THS_YL_G register

THSR7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 104. INT1_THS_YL_G description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

8.46 INT1_THS_ZH_G (36h)

Table 105. INT1_THS_ZH_G register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 106. INT1_THS_ZH_G description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000

8.47 INT1_THS_ZL_G (37h)

Table 107. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 108. INT1_THS_ZL_G description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

8.48 INT1_DURATION_G (38h)

Table 109. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 110. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

WAIT bit has the following meaning:

Wait ='0': the interrupt falls immediately if signal crosses the selected threshold

Wait ='1': if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 21. Wait disabled

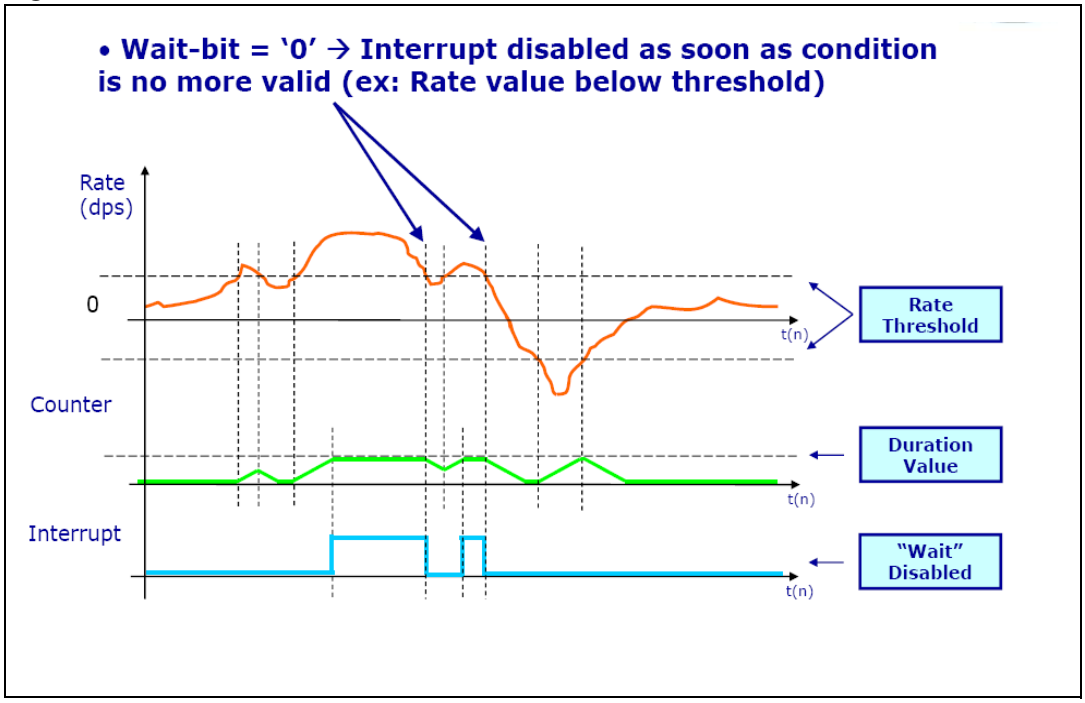
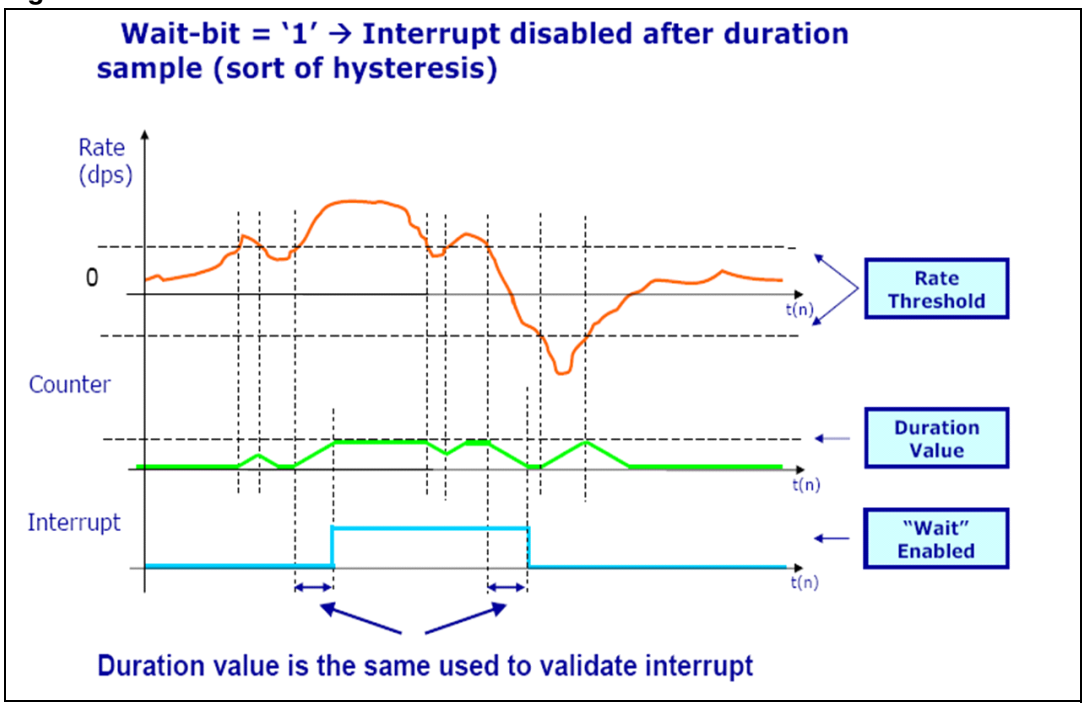


Figure 22. Wait enabled



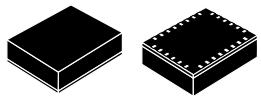
9 Package information

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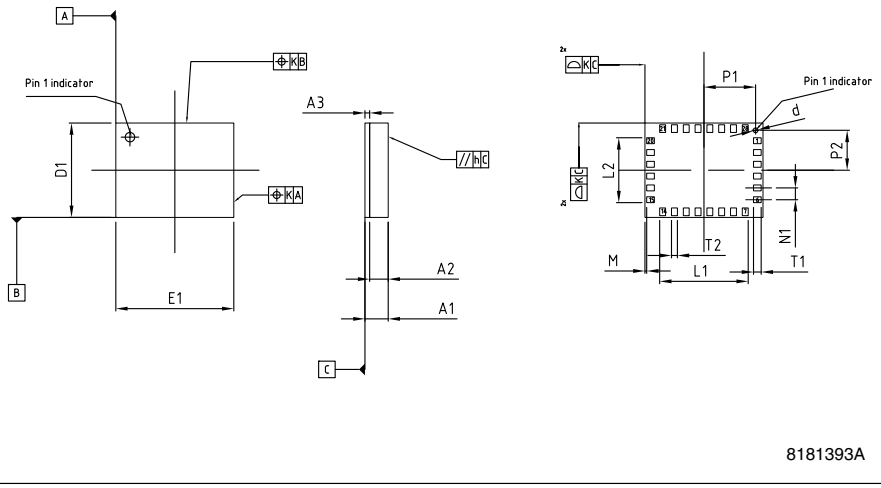
Figure 23. LGA-28 (4x5x1.1 mm): mechanical data and package dimensions

Dimensions			
Ref.	mm		
	Min.	Typ.	Max.
A1			1.1
A2		0.855	
A3		0.200	
D1	3.850	4.000	4.150
E1	4.850	5.000	5.150
L1		3.75	
L2		2.75	
N1		0.500	
M		0.075	
P1		2.200	
P2		1.700	
T1	0.265	0.325	0.385
T2	0.19	0.250	0.310
d		0.200	
k		0.050	
h		0.100	

Outline and mechanical data



LGA-28 (4x5x1.1mm)
Land Grid Array Package



10 Revision history

Table 111. Document revision history

Date	Revision	Changes
02-Sep-2011	1	Initial release.
17-Sep-2012	2	Updated *Table 3: Mechanical characteristics*: Zero-rate level change vs. temperature. Document status promoted from preliminary data to datasheet.

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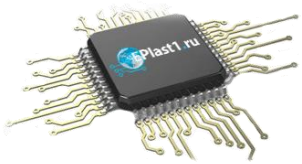
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