Low Cost Analog Multiplier

Enhanced Product

AD633-EP

FEATURES

4-quadrant multiplication
Low cost, 8-lead SOIC package
Complete—no external components required
Laser-trimmed accuracy and stability
Total error within 2% of full scale
Differential high impedance X and Y inputs
High impedance unity-gain summing input
Laser-trimmed 10 V scaling reference

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Multiplication, division, squaring
Modulation/demodulation, phase detection
Voltage-controlled amplifiers/attenuators/filters

FUNCTIONAL BLOCK DIAGRAM

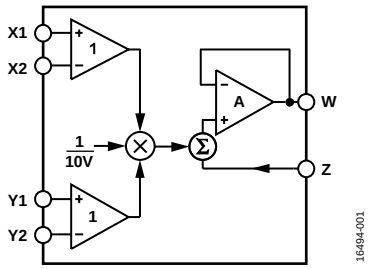

Figure 1.

GENERAL DESCRIPTION

The AD633-EP is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs, and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener.

The AD633-EP is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y input is typically less than 0.1% and noise referred to the output is typically less than 100 µV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/µs slew rate, and the ability to drive capacitive loads make the AD633-EP useful in a wide variety of applications where simplicity and cost are key concerns.

The versatility of the AD633-EP is not compromised by its simplicity. The Z input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications. For further information, see the Multiplier Application Guide.

The AD633-EP is available in an 8-lead SOIC package. It is specified to operate over the −55°C to +125°C military temperature range.

Additional application and technical information can be found in the AD633 data sheet.

PRODUCT HIGHLIGHTS

1. The AD633-EP is a complete four-quadrant multiplier offered in a low cost 8-lead SOIC package. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633-EP.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

Rev. B Document Feedback
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REVISION HISTORY

6/2018—Rev. A to Rev. B

Changes to Figure 3 ... 5

1/2018—Rev. 0 to Rev. A

Changes to Thermal Resistance Section, Table 3, and Figure 2 ... 4
Changes to Endnote 1, Table 3 ... 4
Added Endnote 2, Table 3 ... 4

12/2017—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±15 V, $R_L \geq 2$ kΩ.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
TRANSFER FUNCTION			$W = \frac{(X1 - X2)(Y1 - Y2)}{10\ \text{V}} + Z$		
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	±2	% full scale
T_{MIN} to T_{MAX}			±3		% full scale
Scale Voltage Error	SF = 10.00 V nominal		±0.25%		% full scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% full scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	±1	% full scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	±0.4	% full scale
X Feedthrough	Y nulled, X = ±10 V		±0.3	±1	% full scale
Y Feedthrough	X nulled, Y = ±10 V		±0.1	±0.4	% full scale
Output Offset Voltage[1]			±5	±50	mV
DYNAMICS					
Small Signal Bandwidth	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/µs
Settling Time to 1%	ΔV_O = 20 V		2		µs
OUTPUT NOISE					
Spectral Density			0.8		µV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		µV rms
OUTPUT					
Output Voltage Swing		±11			V
Short Circuit Current	R_L = 0 Ω		30	40	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	±10			V
	Common mode	±10			V
Offset Voltage (X, Y)			±5	±30	mV
CMRR (X, Y)	V_{CM} = ±10 V, f = 50 Hz	60	80		dB
Bias Current (X, Y, Z)			0.8	2.0	µA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		±8		±18	V
Supply Current	Quiescent		4	6	mA

[1] Allow approximately 0.5 ms for settling following power on.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	See Figure 2
Input Voltages[1]	±18 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	260°C
ESD Rating	1000 V

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3.

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
R-8	123.9	42.8	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD51.
[2] Test Condition 2: Thermal impedance simulate values are based on JEDEC 1S0P thermal test board. See JEDEC JESD51.

POWER DERATING CURVE

Figure 2 shows the maximum power dissipation vs. the ambient temperature.

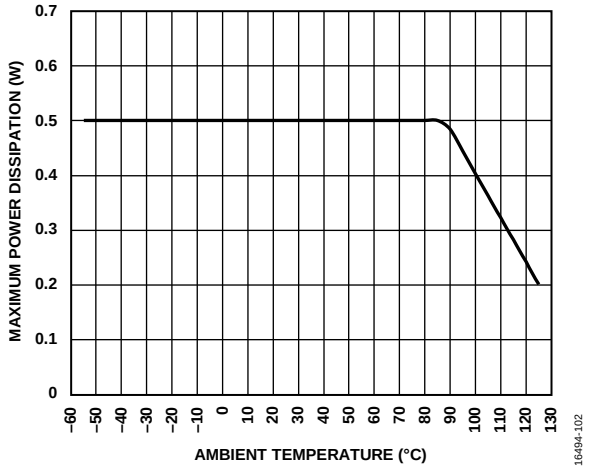


Figure 2. Maximum Power Dissipation vs. Ambient Temperature (T_A)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

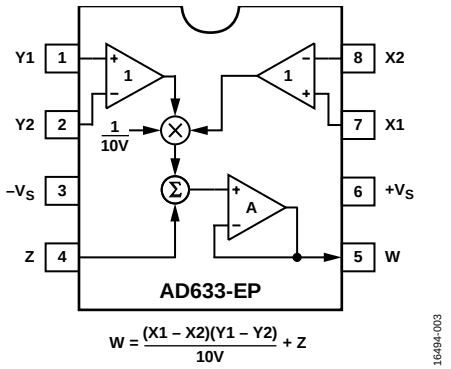


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Y Multiplicand Noninverting Input
2	Y2	Y Multiplicand Inverting Input
3	$-V_S$	Negative Supply Rail
4	Z	Summing Input
5	W	Product Output
6	$+V_S$	Positive Supply Rail
7	X1	X Multiplicand Noninverting Input
8	X2	X Multiplicand Inverting Input

TYPICAL PERFORMANCE CHARACTERISTICS

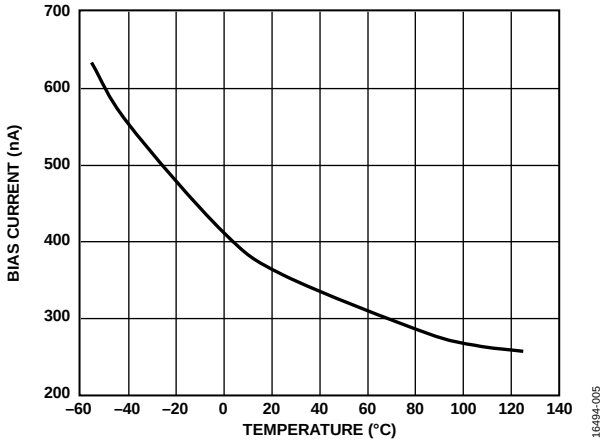
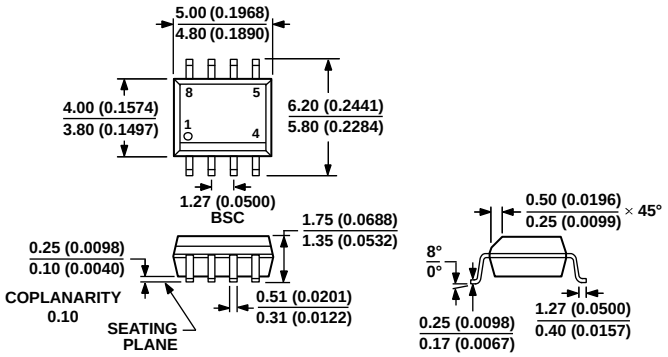


Figure 4. Input Bias Current vs. Temperature (X, Y, or Z Inputs)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 5. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD633TRZ-EP	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD633TRZ-EP-R7	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

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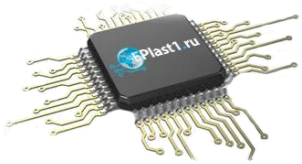

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