

56858

Data Sheet

Technical Data

56800E

16-bit Digital Signal Controllers

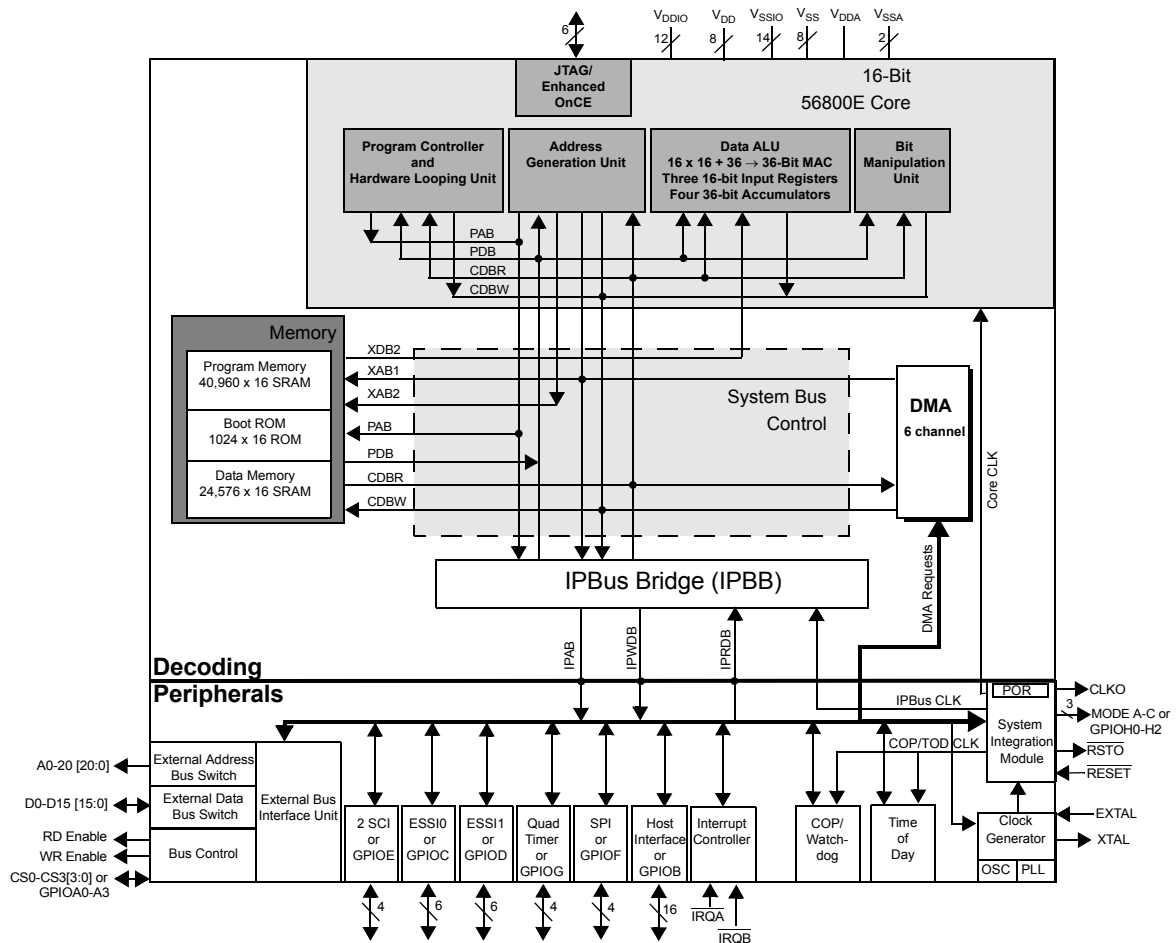
DSP56858
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DSP56858 General Description

- 120 MIPS at 120MHz
- 40K x 16-bit Program SRAM
- 24K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M data memory
- Chip Select Logic for glue-less interface to ROM and SRAM
- Six (6) independent channels of DMA
- Two (2) Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of-Day (TOD)
- 144 LQFP and 144 MAPBGA packages
- Up to 47 GPIO



56858 Block Diagram

Part 1 Overview

1.1 56858 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16×16 -bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C-Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
 - $40K \times 16$ -bit Program RAM
 - $24K \times 16$ -bit Data RAM
 - $1K \times 16$ -bit Boot ROM
- Off-Chip Memory Expansion (EMI)
 - Access up to 2M words of program or 8M data memory (using chip selects)
 - Chip Select Logic for glue-less interface to ROM and SRAM

1.1.3 56858 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer*
- Two Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Two (2) Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging

- Six (6) independent channels of DMA
- 8-bit Parallel Host Interface*
- Time-of-Day (TOD)
- Up to 47 GPIO

* Each peripheral I/O can be used alternately as a GPIO if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 56858 Description

The 56858 is a member of the 56800E core-based family of controllers. This device combines the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution. The low cost, flexibility, and compact program code make this device well-suited for many applications. The 56858 includes peripherals that are especially useful for teledatacom devices; Internet appliances; portable devices; TAD; voice recognition; hands-free devices; and general purpose applications.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

The 56858 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56858 also provides two external dedicated interrupt lines, and up to 47 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56858 controller includes 40K words of Program RAM, 24K words of Data RAM and 1K of Boot RAM. It also supports program execution from external memory.

This controller also provides a full set of standard programmable peripherals that include an 8-bit Parallel Host Interface, two Enhanced Synchronous Serial Interfaces (ESSI), one Serial Peripheral Interface (SPI), two Serial Communications Interfaces (SCI), and one Quad Timer. The Host Interface, Quad Timer, SSI, SPI, SCI I/O and four chip selects can be used as General Purpose Input/Outputs when its primary function is not required.

1.3 State of the Art Development Environment

- Processor ExpertTM (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in [Table 1-1](#) are required for a complete description of and proper design with the 56858. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at www.freescale.com.

Table 1-1 56858 Chip Documentation

Topic	Description	Order Number
56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit core processor and the instruction set	56800ERM
DSP56858 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56858	DSP5685xUM
56858 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56858
DSP56858 Errata	Details any chip issues that might be present	DSP56858E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

OVERBAR This is used to indicate a signal that is active when pulled low. For example, the RESET pin is active when low.

“asserted” A high true (active high) signal is high or a low true (active low) signal is low.

“deasserted” A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage ¹
	<u>PIN</u>	True	Asserted	V_{IL}/V_{OL}
	<u>PIN</u>	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56858 are organized into functional groups, as shown in [Table 2-1](#) and as illustrated in [Figure 2-1](#). In [Table 3-1](#) each table row describes the package pin and the signal or signals present.

Table 2-1 56858 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD} , V_{DDIO} , or V_{DDA})	(8, 12, 1) ¹
Ground (V_{SS} , V_{SSIO} , or V_{SSA})	(8, 14, 2) ¹
PLL and Clock	3
External Bus Signals	39
External Chip Select*	4
Interrupt and Program Control	7 ²
Host Interface (HI)*	16 ³
Enhanced Synchronous Serial Interface (ESSI0) Port*	6
Enhanced Synchronous Serial Interface (ESSI1) Port*	6
Serial Communications Interface (SCI0) Ports*	2
Serial Communications Interface (SCI1) Ports*	2
Serial Peripheral Interface (SPI) Port*	4
Quad Timer Module Port*	4
JTAG/On-Chip Emulation (OnCE)	6

*Alternately, GPIO pins

1. $V_{DD} = V_{DD\text{ CORE}}$, $V_{SS} = V_{SS\text{ CORE}}$, $V_{DDIO} = V_{DD\text{ IO}}$, $V_{SSIO} = V_{SS\text{ IO}}$, $V_{DDA} = V_{DD\text{ ANA}}$, $V_{SSA} = V_{SS\text{ ANA}}$

2. MODA, MODB and MODC can be used as GPIO after the bootstrap process has completed.

3. The following Host Interface signals are multiplexed: HRWB to $\overline{\text{HRD}}$, HDS to $\overline{\text{HWR}}$, HREQ to $\overline{\text{HTRQ}}$ and $\overline{\text{HACK}}$ to HRRQ.

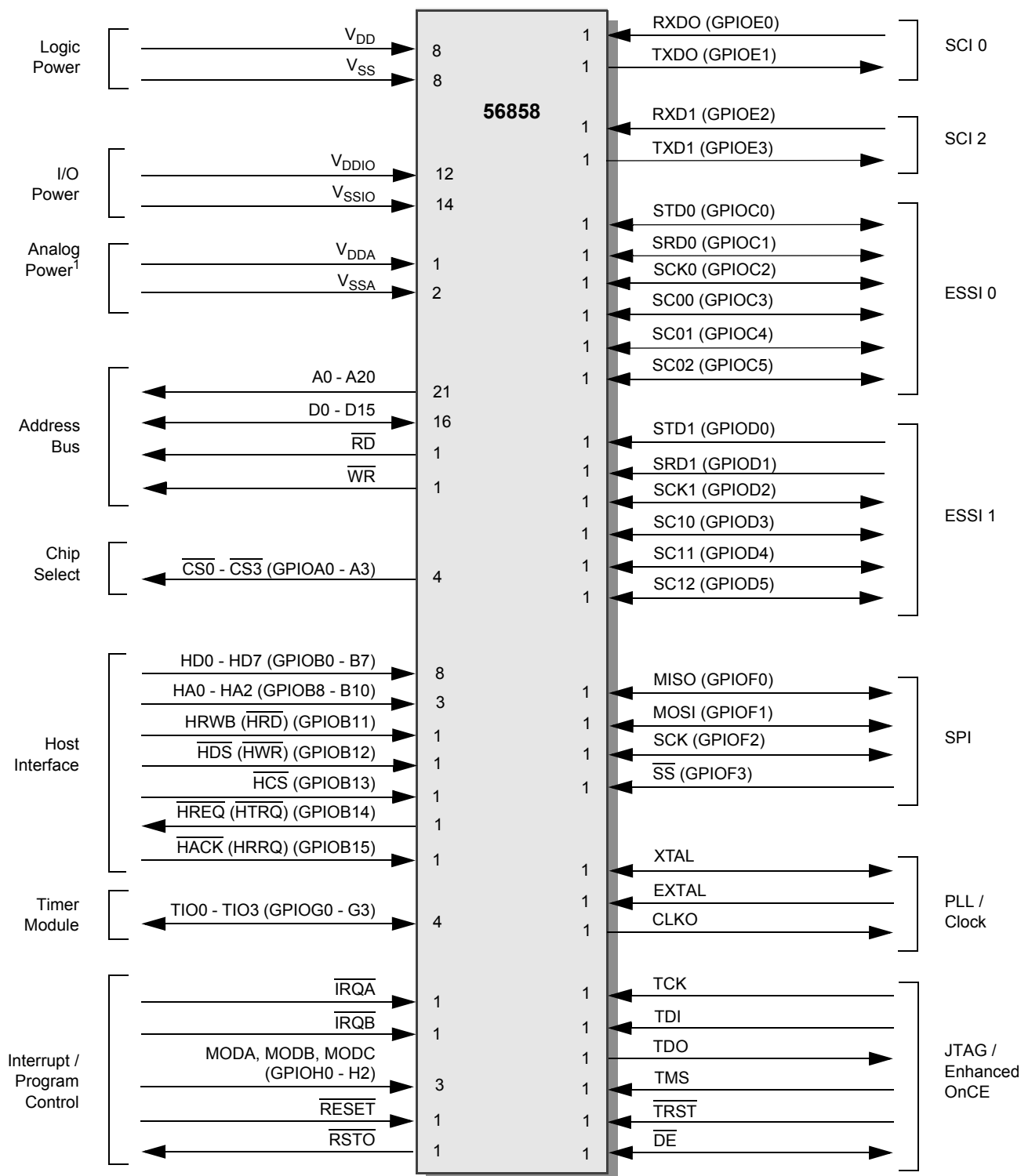


Figure 2-1 56858 Signals Identified by Functional Group²

1. Specifically for PLL, OSC, and POR.

2. Alternate pin functions are shown in parentheses. Pin direction/type is represented as the preferred functionality. GPIO may provide bidirectional use of any pin.

Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. MODE A, MODE B and MODE C pins have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Output(Z) means an output in a High-Z condition.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V _{DD}	E1	14	V _{DD}	Logic Power (V_{DD}) —These pins provide power to the internal structures of the chip, and should all be attached to V _{DD} .
V _{DD}	M6	36		
V _{DD}	F12	52		
V _{DD}	A9	72		
V _{DD}	M2	87		
V _{DD}	J12	88		
V _{DD}	E12	109		
V _{DD}	A12	125		
V _{SS}	G1	15	V _{SS}	Logic Power–Ground (V_{SS}) —These pins provide grounding for the internal structures of the chip and should all be attached to V _{SS} .
V _{SS}	L6	16		
V _{SS}	D12	53		
V _{SS}	A7	54		
V _{SS}	F1	71		
V _{SS}	M7	89		
V _{SS}	K12	126		
V _{SS}	A8	127		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
V _{DDIO}	B1	5	V _{DDIO}	I/O Power (V_{DDIO}) —These pins provide power for all I/O and ESD structures of the chip and should all be attached to V _{DDIO} (3.3V).
V _{DDIO}	H1	6		
V _{DDIO}	M3	20		
V _{DDIO}	M8	45		
V _{DDIO}	M11	61		
V _{DDIO}	H12	67		
V _{DDIO}	C12	68		
V _{DDIO}	A11	80		
V _{DDIO}	A5	105		
V _{DDIO}	A3	113		
V _{DDIO}	C1	129		
V _{DDIO}	M10	139		
V _{SSIO}	D1	7	V _{SSIO}	I/O Power–Ground (V_{SSIO}) —These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to V _{SS} .
V _{SSIO}	J1	21		
V _{SSIO}	M5	46		
V _{SSIO}	M9	47		
V _{SSIO}	L12	62		
V _{SSIO}	G12	69		
V _{SSIO}	B12	70		
V _{SSIO}	A10	82		
V _{SSIO}	A4	106		
V _{SSIO}	A1	115		
V _{SSIO}	A2	128		
V _{SSIO}	M4	130		
V _{SSIO}	M12	140		
V _{SSIO}	A6	141		
V _{DDA}	K1	24	V _{DDA}	Analog Power (V_{DDA}) —These pins supply an analog power source.
V _{SSA}	M1	25	V _{SSA}	Analog Ground (V_{SSA}) —This pin supplies an analog ground.
V _{SSA}	L1	26		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
A0	E5	10	Output(Z)	Address Bus (A0-A20) —These signals specify a word address for external program or data memory access.
A1	E4	11		
A2	E3	12		
A3	E2	13		
A4	J2	29		
A5	H3	30		
A6	G4	31		
A7	H4	32		
A8	G5	48		
A9	L5	49		
A10	J6	50		
A11	K6	51		
A12	J8	63		
A13	K8	64		
A14	L9	65		
A15	K9	66		
A16	K10	75		
A17	K11	76		
A18	J9	77		
A19	J10	78		
A20	J11	79		

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
D0	H7	81	Input/ Output(Z)	Data Bus (D0-D15) —These pins provide the bidirectional data for external program or data memory accesses.
D1	G7	94		
D2	F9	95		
D3	F10	96		
D4	F11	97		
D5	E10	98		
D6	D7	120		
D7	B7	121		
D8	E7	122		
D9	F8	123		
D10	F7	124		
D11	D5	137		
D12	B4	138		
D13	C4	142		
D14	F6	143		
D15	B3	144		
$\overline{RD}$	D3	8	Output	Read Enable ($\overline{RD}$) — is asserted during external memory read cycles. This signal is pulled high during reset.
$\overline{WR}$	D4	9	Output	Write Enable ($\overline{WR}$) —is asserted during external memory write cycles. This signal is pulled high during reset.
$\overline{CS0}$ GPIOA0	H8	83	Output Input/Output	External Chip Select ($\overline{CS0}$) —This pin is used as a dedicated GPIO. Port A GPIO (0) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS1}$ GPIOA1	H9	84	Output Input/Output	External Chip Select ($\overline{CS1}$) —This pin is used as a dedicated GPIO. Port A GPIO (1) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS2}$ GPIOA2	H11	85	Output Input/Output	External Chip Select ($\overline{CS2}$) —This pin is used as a dedicated GPIO. Port A GPIO (2) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS3}$ GPIOA3	H10	86	Output Input/Output	External Chip Select ($\overline{CS3}$) —This pin is used as a dedicated GPIO. Port A GPIO (3) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
HD0	J3	33	Input	Host Address (HD0) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB0			Input/Output	Port B GPIO (0) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD1	K2	34	Input	Host Address (HD1) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB1			Input/Output	Port B GPIO (1) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD2	L2	35	Input	Host Address (HD2) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB2			Input/Output	Port B GPIO (2) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD3	J4	40	Input	Host Address (HD3) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB3			Input/Output	Port B GPIO (3) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD4	L4	41	Input	Host Address (HD4) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB4			Input/Output	Port B GPIO (4) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD5	J5	42	Input	Host Address (HD5) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB5			Input/Output	Port B GPIO (5) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
HD6	K5	43	Input	Host Address (HD6) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB6			Input/Output	Port B GPIO (6) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HD7	H5	44	Input	Host Address (HD7) —This input provides data selection for HI registers. This pin is disconnected internally during reset.
GPIOB7			Input/Output	Port B GPIO (7) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
HA0	G10	90	Input	Host Address (HA0) —These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB8			Input/Output	Port B GPIO (8) —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA1	G11	91	Input	Host Address (HA0) —These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB9			Input/Output	Port B GPIO (9) —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HA2	G9	92	Input	Host Address (HA0) —These inputs provide the address selection for HI registers. These pins are disconnected internally during reset.
GPIOB10			Input/Output	Port B GPIO (10) —These pins are General Purpose I/O (GPIO) pins when not configured for host port usage.
HRWB	G8	93	Input	Host Read/Write (HRWB) —When the HI08 is programmed to interface to a single-data-strobe <u>host</u> bus and the HI function is selected, this signal is the Read/Write input. These pins are disconnected internally during reset.
$\overline{\text{HRD}}$			Input	Host Read Data ($\overline{\text{HRD}}$) —This signal is the Read Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB11			Input/Output	Port B GPIO (11) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HDS}}$	C8	116	Input	Host Data Strobe ($\overline{\text{HDS}}$) —When the HI08 is programmed to interface to a single-data-strobe host bus and the HI function is selected, this input enables a data transfer on the HI when $\overline{\text{HCS}}$ is asserted. These pins are disconnected internally during reset.
$\overline{\text{HWR}}$			Input	Host Write Enable ($\overline{\text{HWR}}$) —This signal is the Write Data input when the HI08 is programmed to interface to a double-data-strobe host bus and the HI function is selected.
GPIOB12			Input/Output	Port B GPIO (12) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HCS}}$	D8	117	Input	Host Chip Select ($\overline{\text{HCS}}$) —This input is the chip select input for the Host Interface. These pins are disconnected internally during reset.
GPIOB13			Input/Output	Port B GPIO (13) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{\text{HREQ}}$	B8	118	Open Drain Output	Host Request ($\overline{\text{HREQ}}$) —When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this open drain output is <u>used by</u> the HI to request service from the host processor. The $\overline{\text{HREQ}}$ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. These pins are disconnected internally during reset.
$\overline{\text{HTRQ}}$			Open Drain Output	Transmit Host Request ($\overline{\text{HTRQ}}$) —This signal is the Transmit Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB14			Input/Output	Port B GPIO (14) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HACK}}$	C7	119	Input	Host Acknowledge ($\overline{\text{HACK}}$) —When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally during reset.
HRRQ			Open Drain Output	Receive Host Request (HRRQ) —This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB15			Input/Output	Port B GPIO (15) —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
TIO0	B9	114	Input/Output	Timer Input/Outputs (TIO0) —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG0			Input/Output	Port G GPIOG0 —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO1	C9	112	Input/Output	Timer Input/Outputs (TIO1) —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG1			Input/Output	Port G GPIO (1) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO2	D9	111	Input/Output	Timer Input/Outputs (TIO2) —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG2			Input/Output	Port G GPIO (2) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO3	B10	110	Input/Output	Timer Input/Outputs (TIO3) —This pin can be independently configured to be either a timer input source or an output flag.
GPIOG3			Input/Output	Port G GPIO (3) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
$\overline{\text{IRQA}}$	G2	22	Input	External Interrupt Request A and B —The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
$\overline{\text{IRQB}}$	F5	23		
MODE A	F4	17	Input	Mode Select (MODE A) —During the bootstrap process MODE A selects one of the eight bootstrap modes.
GPIOH0			Input/Output	Port H GPIO (0) —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MODE B	F3	18	Input	Mode Select (MODE B) —During the bootstrap process MODE A selects one of the eight bootstrap modes.
GPIOH1			Input/Output	Port H GPIO (1) —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
MODE C	F2	19	Input	Mode Select (MODE C) —During the bootstrap process MODE A selects one of the eight bootstrap modes.
GPIOH2			Input/Output	Port H GPIO (2) —This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.
$\overline{\text{RESET}}$	K4	39	Input	Reset ($\overline{\text{RESET}}$)—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODE A, MODE B, and MODE C pins. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
$\overline{\text{RSTO}}$	K3	38	Output	Reset Output ($\overline{\text{RSTO}}$) —This output is asserted on any reset condition (external reset, low voltage, software, or COP).
RXD0	L10	73	Input	Serial Receive Data 0 (RXD0) —This input receives byte-oriented serial data and transfers it to the SCI 0 receive shift register.
GPIOE0			Input/Output	Port E GPIO (0) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
TXD0	L11	74	Output(Z)	Serial Transmit Data 0 (TXD0) —This signal transmits data from the SCI 0 transmit data register.
GPIOE1			Input/Output	Port E GPIO (1) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
RXD1	B11	107	Input	Serial Receive Data 1 (RXD1) —This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register.
GPIOE2			Input/Output	Port E GPIO (2) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
TXD1	C10	108	Output(Z)	Serial Transmit Data 1 (TXD1) —This signal transmits data from the SCI 1 transmit data register.
GPIOE3			Input/Output	Port E GPIO (3) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
STD0	B6	131	Output	ESSI Transmit Data (STD0) —This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOC0			Input/Output	Port C GPIO (0) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD0	C6	132	Input	ESSI Receive Data (SRD0) —This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOC1			Input/Output	Port C GPIO (1) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK0	C5	133	Input/Output	ESSI Serial Clock (SCK0) —This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOC2			Input/Output	Port C GPIO (2) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC00	D6	134	Input/Output	ESSI Serial Control Pin 0 (SC00) —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOC3			Input/Output	Port C GPIO (3) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC01	B5	135	Input/Output	ESSI Serial Control Pin 1 (SC01) —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOC4			Input/Output	Port C GPIO (4) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC02	E6	136	Input/Output	ESSI Serial Control Pin 2 (SC02) —This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input or Output	Port C GPIO (5) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
STD1	E8	99	Output	ESSI Transmit Data (STD1) —This output pin transmits serial data from the ESSI Transmitter Shift Register.
GPIOD0			Input/Output	Port D GPIO (0) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SRD1	E11	100	Input	ESSI Receive Data (SRD1) —This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
GPIOD1			Input/Output	Port D GPIO (1) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SCK1	E9	101	Input/Output	ESSI Serial Clock (SCK1) —This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
GPIOD2			Input/Output	Port D GPIO (2) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC10	D10	102	Input/Output	ESSI Serial Control Pin 0 (SC10) —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
GPIOD3			Input/Output	Port D GPIO (3) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC11	D11	103	Input/Output	ESSI Serial Control Pin 1 (SC11) —The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
GPIOD4			Input/Output	Port D GPIO (4) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
SC12	C11	104	Input/Output	ESSI Serial Control Pin 2 (SC12) —This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
GPIOC5			Input/Output	Port D GPIO (5) —This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MISO	B2	1	Input/Output	SPI Master In/Slave Out (MISO) —This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's Wired-OR mode (WOM) bit when this pin is configured for SPI operation.
GPIOF0			Input/Output	Port F GPIO (0) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
MOSI	C3	2	Input/ Output (Z)	SPI Master Out/Slave In (MOSI) —This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation.
GPIOF1			Input/Output	Port F GPIO (1) —This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin.
SCK	C2	3	Input/Output	SPI Serial Clock (SCK) —This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the $\overline{SS}$ pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device.
GPIOF2			Input/Output	Port F GPIO (2) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
$\overline{SS}$	D2	4	Input	SPI Slave Select ($\overline{SS}$) —This input pin selects a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high.
GPIOF3			Input/Output	Port F GPIO (3) —This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
XTAL	H2	27	Input/Output	Crystal Oscillator Output (XTAL) —This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.
EXTAL	G3	28	Input	External Crystal Oscillator Input (EXTAL) —This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See Section 4.5.2
CLKO	L3	37	Output	Clock Output (CLKO) —This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
TCK	L8	60	Input	Test Clock Input (TCK) —This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TDI	K7	58	Input	Test Data Input (TDI) —This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	G6	57	Output(Z)	Test Data Output (TDO) —This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
TMS	J7	59	Input	Test Mode Select Input (TMS) —This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. Note: Always tie the TMS pin to V _{DD} through a 2.2K resistor.
$\overline{\text{TRST}}$	L7	56	Input	Test Reset ($\overline{\text{TRST}}$) —As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$. Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the device. Note: For normal operation, connect $\overline{\text{TRST}}$ directly to V _{SS} . If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V _{SS} through a 1K resistor.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{DE}}$	H6	55	Input/Output	Debug Event ($\overline{\text{DE}}$) —This is an open-drain, bidirectional, active low signal. As an input, it is a means of entering debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered debug mode. This pin is connected internally to a weak pull-up resistor.

Part 4 Specifications

4.1 General Characteristics

The 56858 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of $3.3\text{V} \pm 10\%$ during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in [Table 4-1](#) are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56858 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}^1	$V_{SS} - 0.3$	$V_{SS} + 2.0$	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}^2 V_{DDIO}^2	$V_{SSIO} - 0.3$ $V_{SSA} - 0.3$	$V_{SSIO} + 4.0$ $V_{DDA} + 4.0$	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	$V_{SSIO} - 0.3$ $V_{SSA} - 0.3$	$V_{SSIO} + 5.5$ $V_{DDA} + 0.3$	V
Current drain per pin excluding V_{DD} , GND	I	—	8	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}

2. V_{DDIO} and V_{DDA} must not differ by more than 0.5V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency ¹	f_{pll}	—	240	MHz
Operating Frequency ²	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz

Table 4-2 Recommended Operating Conditions (Continued)

Characteristic	Symbol	Min	Max	Unit
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.

2. Master clock is derived from on of the following four sources:

$f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXTAL

$f_{clk} = f_{pll}$ when PLL is selected

$f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected

$f_{clk} = f_{extal}$ when the source clock is the direct clock to EXTAL and PLL is not selected

Table 4-3 Thermal Characteristics¹

Characteristic	Symbol	Value		Unit
		144-pin LQFP	144 MAPBGA	
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	42.9	36.1	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined		W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$		W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / R\theta_{JA}^2$		W

1. See [Section 6.1](#) for more detail.

2. T_J = Junction Temperature
 T_A = Ambient Temperature

4.2 DC Electrical Characteristics

Table 4-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{pF}$, $f_{op} = 120\text{MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	$V_{DDA} - 0.8$	V_{DDA}	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V

Table 4-4 DC Electrical Characteristics (Continued)Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Input current low (pullups disabled)	I_{IL}	-1	—	1	μA
Input current high (pullups disabled)	I_{IH}	-1	—	1	μA
Output tri-state current low	I_{OZL}	-10	—	10	μA
Output tri-state current high	I_{OZH}	-10	—	10	μA
Output High Voltage	V_{OH}	$V_{DDIO} - 0.7$	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current (Core logic, memories, peripherals)	I_{DD}^4				
Run ¹		—	70	110	mA
Deep Stop ²		—	0.05	10	mA
Light Stop ³		—	5	14	mA
V_{DDIO} supply current (I/O circuitry)	I_{DDIO}				
Run ⁵		—	40	50	mA
Deep Stop ²			0	1.5	mA
V_{DDA} supply current (analog circuitry)	I_{DDA}				
Deep Stop ²		—	60	120	μA
Low Voltage Interrupt ⁶	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset ⁷	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source ($f_{osc} = 4\text{ MHz}$) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

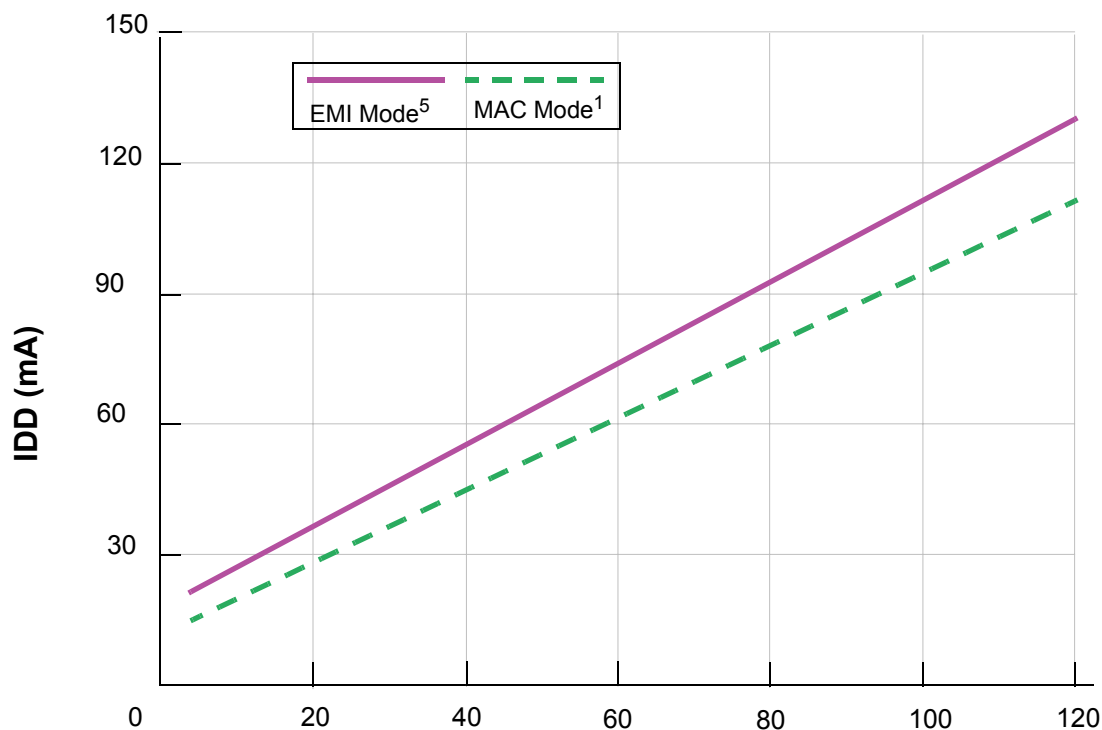
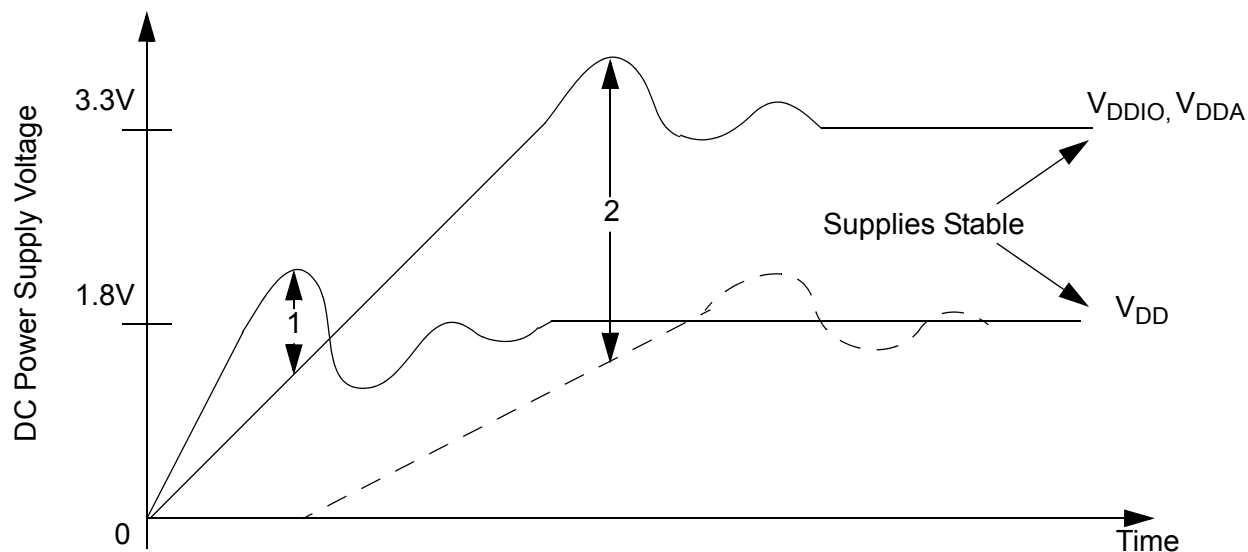


Figure 4-1 Maximum Run $I_{DDTOTAL}$ vs. Frequency (see Notes 1. and 5. in Table 4-4)

4.3 Supply Voltage Sequencing and Separation Cautions

Figure 4-2 shows two situations to avoid in sequencing the V_{DD} and V_{DDIO} , V_{DDA} supplies.



Note: 1. V_{DD} rising before V_{DDIO} , V_{DDA}
 2. V_{DDIO} , V_{DDA} rising much faster than V_{DD}

Figure 4-2 Supply Voltage Sequencing and Separation Cautions

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (1.8V) from the voltage generated by the 3.3V V_{DDIO} supply, see **Figure 4-3**. This keeps V_{DD} from rising faster than V_{DDIO} .

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in **Figure 4-3**. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 2.1, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:

$$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 2.1V)$$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

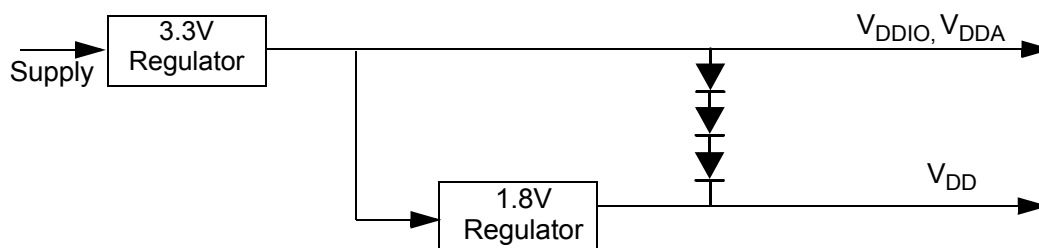


Figure 4-3 Example Circuit to Control Supply Sequencing

4.4 AC Electrical Characteristics

Timing waveforms in **Section 4.3** are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in **Section 4.2**. In **Figure 4-4** the levels of V_{IH} and V_{IL} for an input signal are shown.

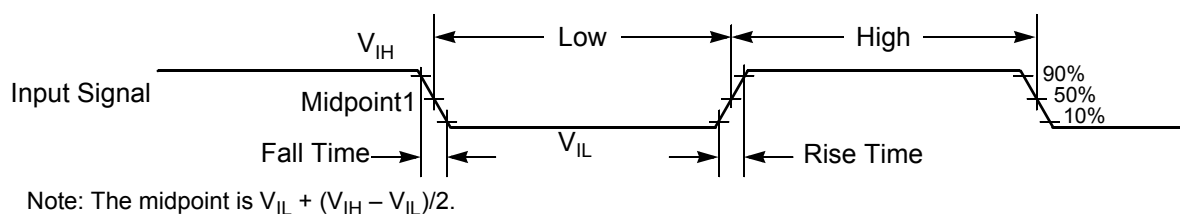


Figure 4-4 Input Signal Measurement References

Figure 4-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

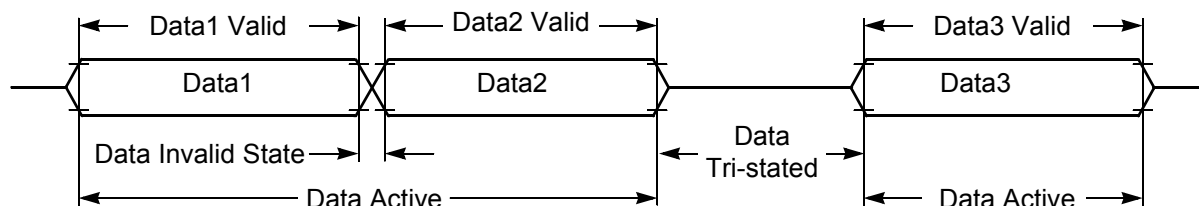


Figure 4-5 Signal States

4.5 External Clock Operation

The 56858 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

4.5.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in [Table 4-6](#). In [Figure 4-6](#) a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

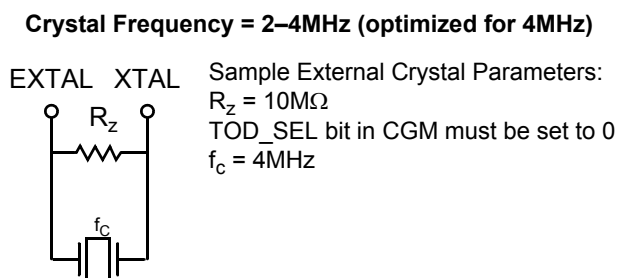


Figure 4-6 Crystal Oscillator

4.5.2 High Speed External Clock Source (> 4MHz)

The recommended method of connecting an external clock is given in [Figure 4-7](#). The external clock source is connected to XTAL and the EXTAL pin is held at ground, V_{DDA} , or $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

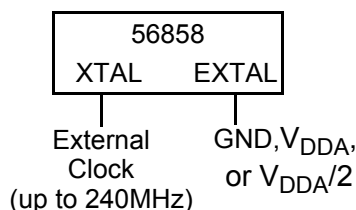


Figure 4-7 Connecting a High Speed External Clock Signal using XTAL

4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in [Figure 4-8](#). The external clock source is connected to XTAL and the EXTAL pin is held at $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

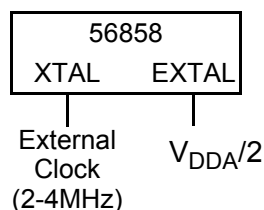


Figure 4-8 Connecting a Low Speed External Clock Signal using XTAL

Table 4-5 External Clock Operation Timing Requirements⁴

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver) ¹	f_{osc}	0	—	240	MHz
Clock Pulse Width ⁴	t_{PW}	6.25	—	—	ns
External clock input rise time ^{2, 4}	t_{rise}	—	—	TBD	ns
External clock input fall time ^{3, 4}	t_{fall}	—	—	TBD	ns

1. See [Figure 4-7](#) for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.

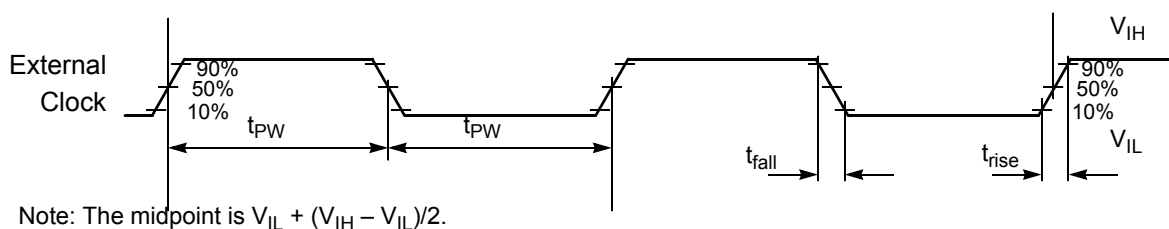


Figure 4-9 External Clock Timing

Table 4-6 PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL ¹	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time ²	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. [Figure 4-10](#) shows sample timing and parameters that are detailed in [Table 4-7](#).

The timing of each parameter consists of both a fixed delay portion and a clock related portion; as well as user controlled wait states. The equation:

$$t = D + P * (M + W)$$

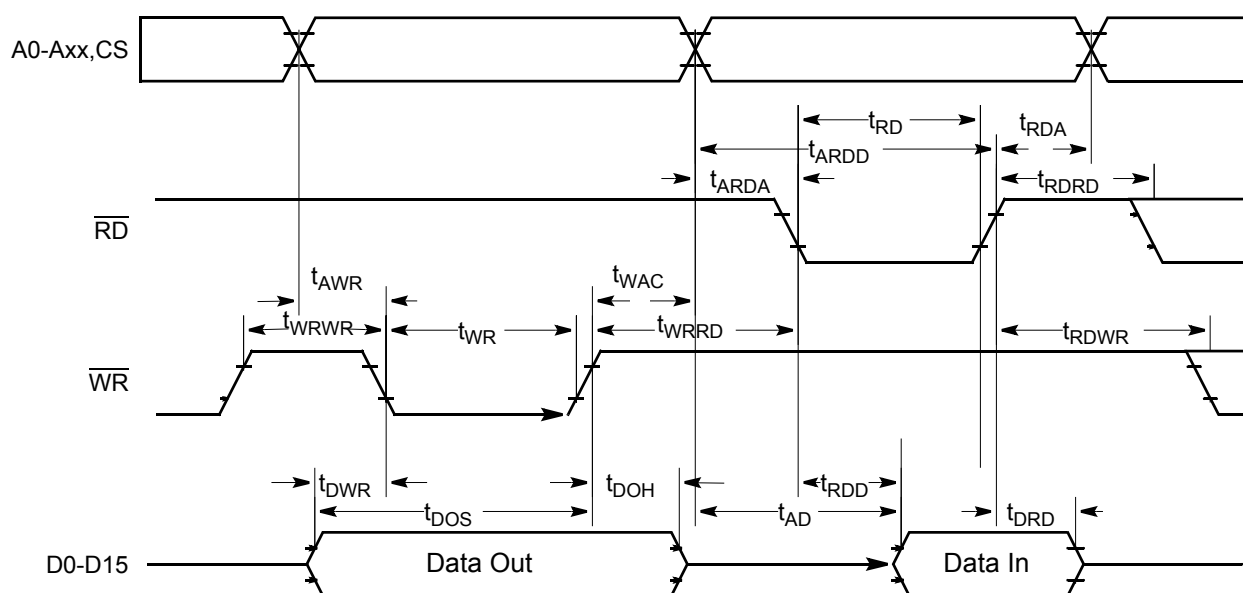
should be used to determine the actual time of each parameter. The terms in the above equation are defined as:

- t parameter delay time
- D fixed portion of the delay, due to on-chip path delays.
- P the period of the system clock, which determines the execution rate of the part (i.e. when the device is operating at 120 MHz, $P = 8.33\text{ ns}$).

- M Fixed portion of a clock period inherent in the design. This number is adjusted to account for possible clock duty cycle derating.
- W the sum of the applicable wait state controls. See the “Wait State Controls” column of [Table 4-7](#) for the applicable controls for each parameter. See the EMI chapter of the 83x Peripheral Manual for details of what each wait state field controls.

Some of the parameters contain two sets of numbers. These parameters have two different paths and clock edges that must be considered. Check both sets of numbers and use the smaller result. The appropriate entry may change if the operating frequency of the part changes.

The timing of write cycles is different when $WWS = 0$ than when $WWS > 0$. Therefore, some parameters contain two sets of numbers to account for this difference. The “Wait States Configuration” column of [Table 4-7](#) should be used to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 4-10 External Memory Interface Timing

Table 4-7 External Memory Interface Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{C}$ to $+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $P = 8.333\text{ ns}$

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-0.79	0.50	WWSS	ns
		WWS>0	-1.98	0.69		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.86	0.19	WWS	ns
		WWS>0	-0.01	0.00		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-1.52	0.00	WWSS	ns
		WWS=0	- 5.69	0.25		
		WWS>0	-2.10	0.19		
		WWS>0	-4.66	0.50		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-1.47	0.25	WWSH	ns
Valid Data Out Set Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-2.36	0.19	WWS, WWSS	ns
			-4.67	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-1.60	0.25	WWSH	
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		- 0.44	0.00	RWSH	ns
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-2.07	1.00	RWSS, RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A ¹	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		-1.34	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-10.27	1.00	RWSS, RWS	ns
			-13.5	1.19		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		- 0.94	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-9.53	1.00	RWSS, RWS	ns
			-12.64	1.19		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-0.75	0.25	WWSH, RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	$t_{RD RD}$		-0.16 ²	0.00	RWSS, RWSH	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-0.44	0.75	WWSS, WWSH	ns
		WWS>0	-0.11	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}		0.14	0.50	MDAR, BMDAR, RWSH, WWSS	ns
			-0.57	0.69		

1. N/A since device captures data before it deasserts $\overline{RD}$

2. If RWSS = RWSH = 0, RD does not deassert during back-to-back reads and D=0.00 should be used.

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 4-8 Reset, Stop, Wait, Mode Select, and Interrupt Timing^{1, 2}

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	Figure 4-11
Minimum $\overline{\text{RESET}}$ Assertion Duration ³	t_{RA}	30	—	ns	Figure 4-11
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	Figure 4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	Figure 4-12
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	Figure 4-13
	$t_{\text{IDM -FAST}}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	Figure 4-13
	$t_{\text{IG -FAST}}$	14T	—		
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State ⁴	t_{IRI}	22T	—	ns	Figure 4-14
	$t_{\text{IRI -FAST}}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Stop) to External Data Memory ⁵	t_{IW}	1.5T	—	ns	Figure 4-15
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory Fast ⁶ Normal ⁷	t_{IF}	18T	—	ns	Figure 4-15
		22ET	—	ns	
$\overline{\text{RSTO}}$ pulse width ⁸ normal operation internal reset mode	t_{RSTO}	128ET 8ET	— —	— —	Figure 4-16

1. In the formulas, T = clock cycle. For $f_{op} = 120\text{ MHz}$ operation and $f_{ipb} = 60\text{ MHz}$, $T = 8.33\text{ ns}$.

2. Parameters listed are guaranteed by design.

3. At reset, the PLL is disabled and bypassed. The part is then put into Run mode and t_{clk} assumes the period of the source clock, t_{xtal} , t_{extal} or t_{osc} .

4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.

5. The interrupt instruction fetch is visible on the pins only in Mode 3.

6. Fast stop mode:

Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue same value it had before stop mode was entered.

7. Normal stop mode:

As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.

8. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125 ns.

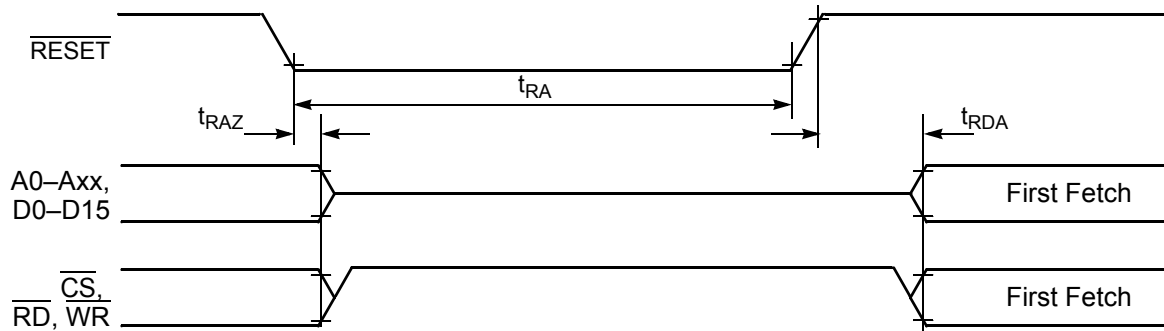


Figure 4-11 Asynchronous Reset Timing

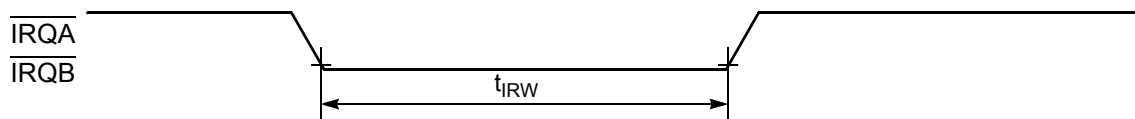


Figure 4-12 External Interrupt Timing (Negative-Edge-Sensitive)

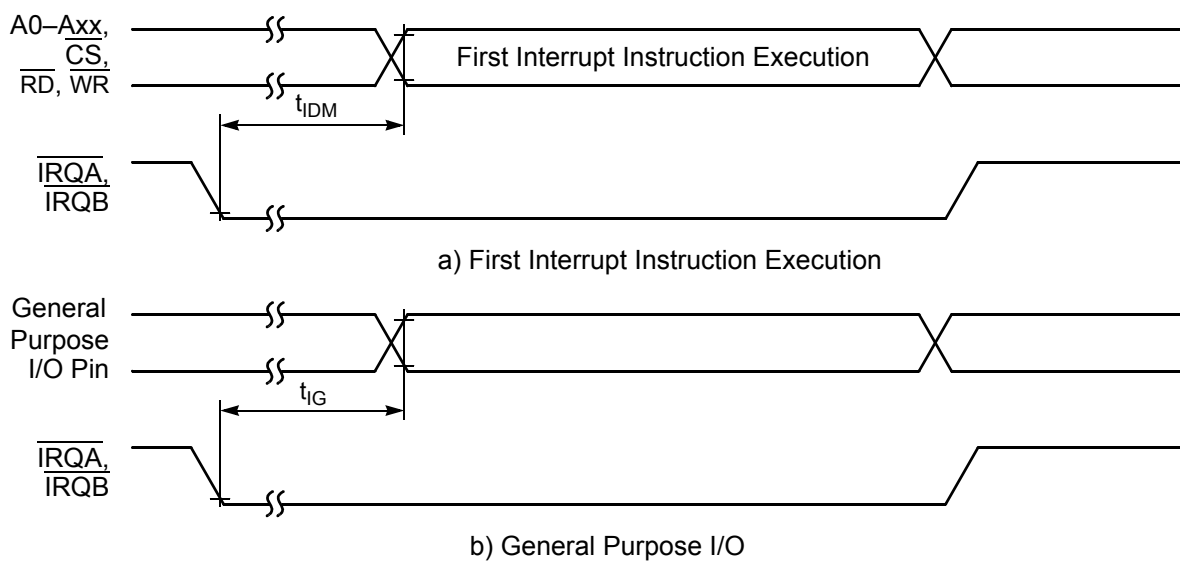


Figure 4-13 External Level-Sensitive Interrupt Timing

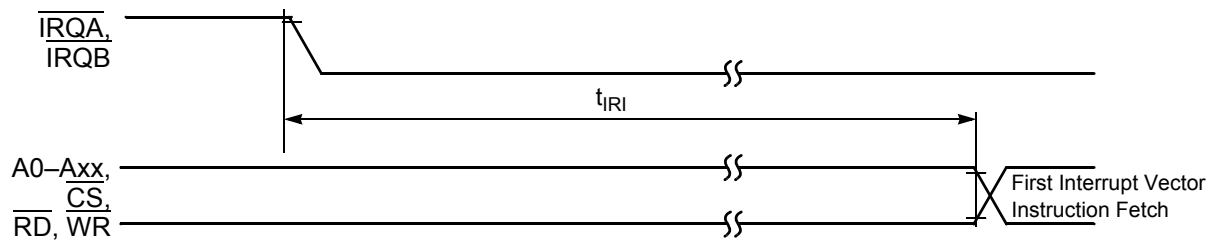


Figure 4-14 Interrupt from Wait State Timing

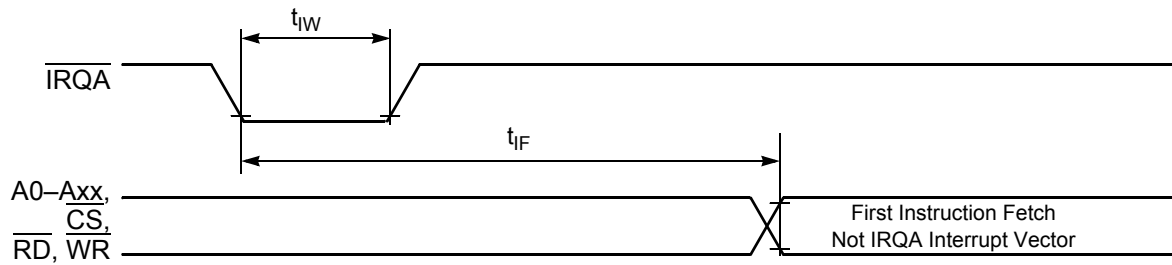


Figure 4-15 Recovery from Stop State Using Asynchronous Interrupt Timing

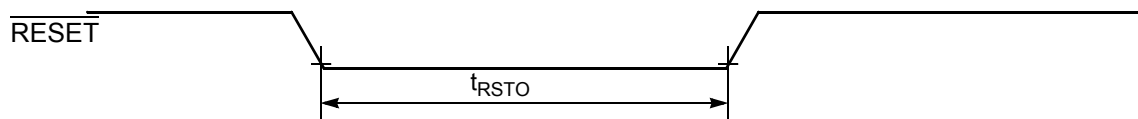


Figure 4-16 Reset Output Timing

4.8 Host Interface Port

Table 4-9 Host Interface Port Timing¹

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	4-17
Disable time	TACKDZ	3	—	ns	4-17
Time to disassert	TACKREQH	3.5	9	ns	4-17 4-20
Lead time	TREQACKL	0	—	ns	4-17 4-20
Access time	TRADV	—	13	ns	4-18 4-19
Disable time	TRADX	5	—	ns	4-18 4-19
Disable time	TRADZ	3	—	ns	4-18 4-19
Setup time	TDACKS	3	—	ns	4-20
Hold time	TACKDH	1	—	ns	4-20
Setup time	TADSS	3	—	ns	4-21 4-22
Hold time	TDSAH	1	—	ns	4-21 4-22
Pulse width	TWDS	5	—	ns	4-21 4-22
Time to re-assert 1. After second write in 16-bit mode 2. After first write in 16-bit mode or after write in 8-bit mode	TACKREQL	4T + 5 5	5T + 9 13	ns ns	4-19 4-20

1. The formulas: $T = \text{clock cycle}$. $f_{ipb} = 60\text{ MHz}$, $T = 16.7\text{ ns}$.

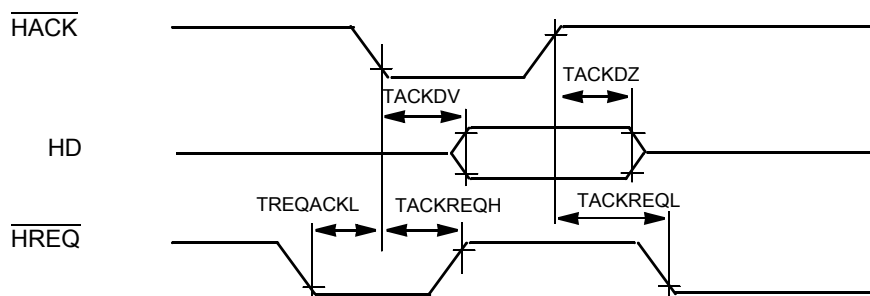


Figure 4-17 Controller-to-Host DMA Read Mode

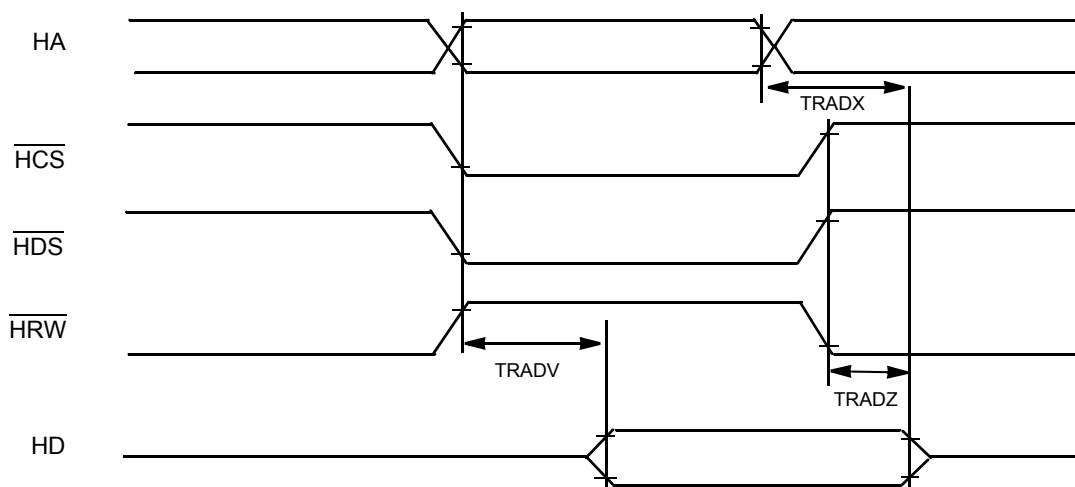


Figure 4-18 Single Strobe Read Mode

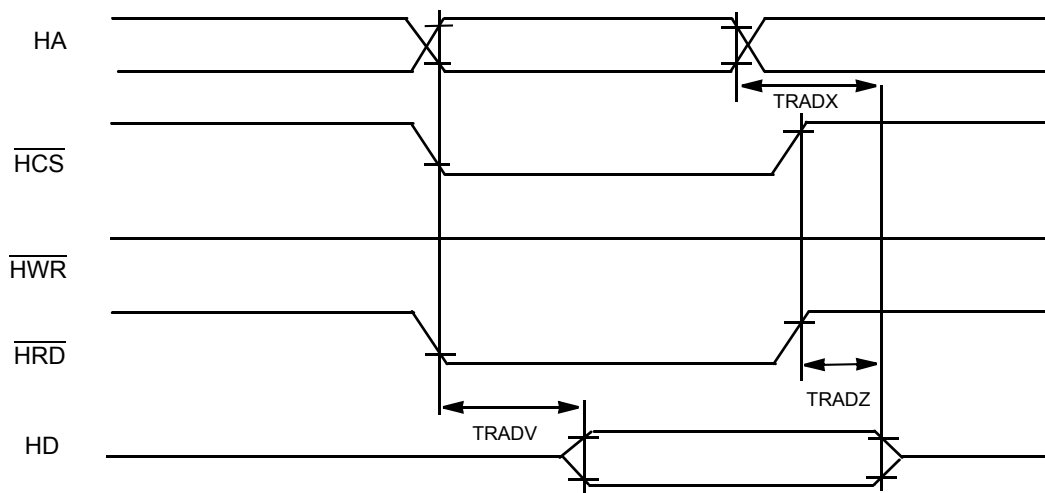


Figure 4-19 Dual Strobe Read Mode

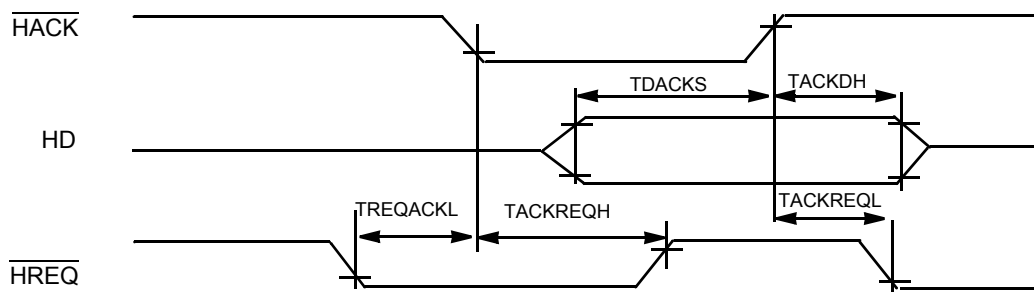


Figure 4-20 Host-to-Controller DMA Write Mode

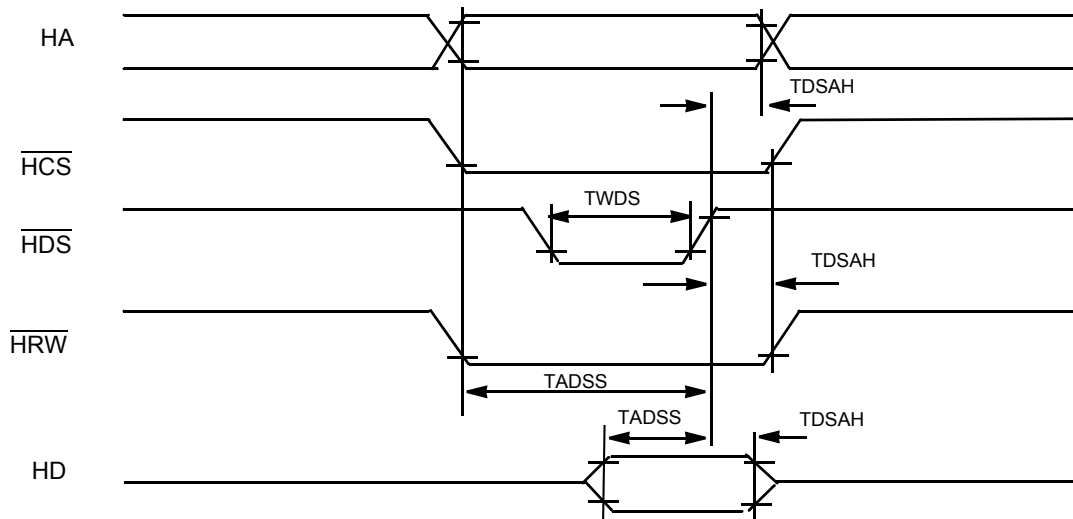


Figure 4-21 Single Strobe Write Mode

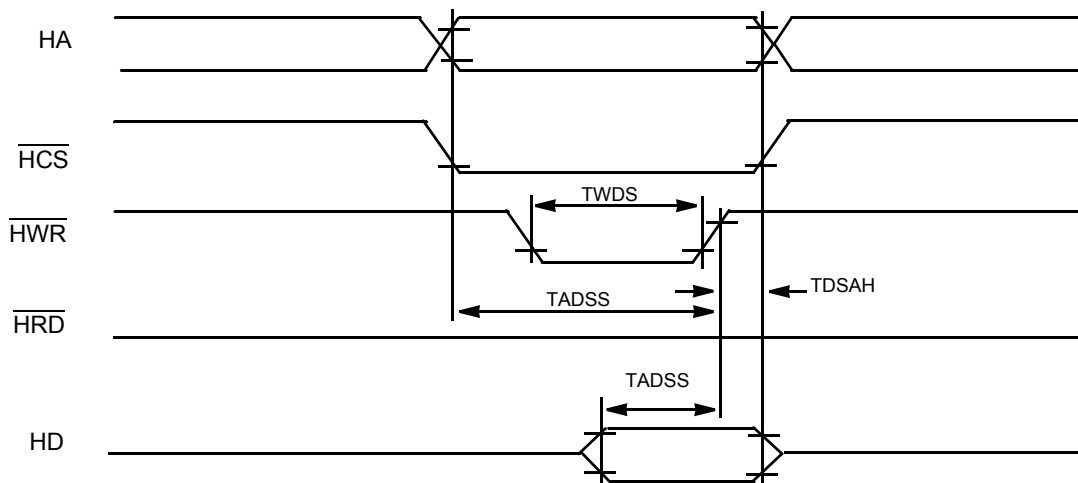


Figure 4-22 Dual Strobe Write Mode

4.9 Serial Peripheral Interface (SPI) Timing

Figure 4-23 SPI Timing ¹

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	25 25	— —	ns ns	4-24, 4-25, 4-26, 4-27
Enable lead time Master Slave	t_{ELD}	— 12.5	— —	ns ns	4-27
Enable lag time Master Slave	t_{ELG}	— 12.5	— —	ns ns	4-27
Clock (SCLK) high time Master Slave	t_{CH}	9 12.5	— —	ns ns	4-24, 4-25, 4-26, 4-27
Clock (SCLK) low time Master Slave	t_{CL}	12 12.5	— —	ns ns	4-27
Data set-up time required for inputs Master Slave	t_{DS}	10 2	— —	ns ns	4-24, 4-25, 4-26, 4-27
Data hold time required for inputs Master Slave	t_{DH}	0 2	— —	ns ns	4-24, 4-25, 4-26, 4-27
Access time (time to data active from high-impedance state) Slave	t_A	5	15	ns ns	4-27
Disable time (hold time to high-impedance state) Slave	t_D	2	9	ns ns	4-27
Data valid for outputs Master Slave (after enable edge)	t_{DV}	— —	2 14	ns ns	4-24, 4-25, 4-26, 4-27
Data invalid Master Slave	t_{DI}	0 0	— —	ns ns	4-24, 4-25, 4-26, 4-27
Rise time Master Slave	t_R	— —	11.5 10.0	ns ns	4-24, 4-25, 4-26, 4-27
Fall time Master Slave	t_F	— —	9.7 9.0	ns ns	4-24, 4-25, 4-26, 4-27

1. Parameters listed are guaranteed by design.

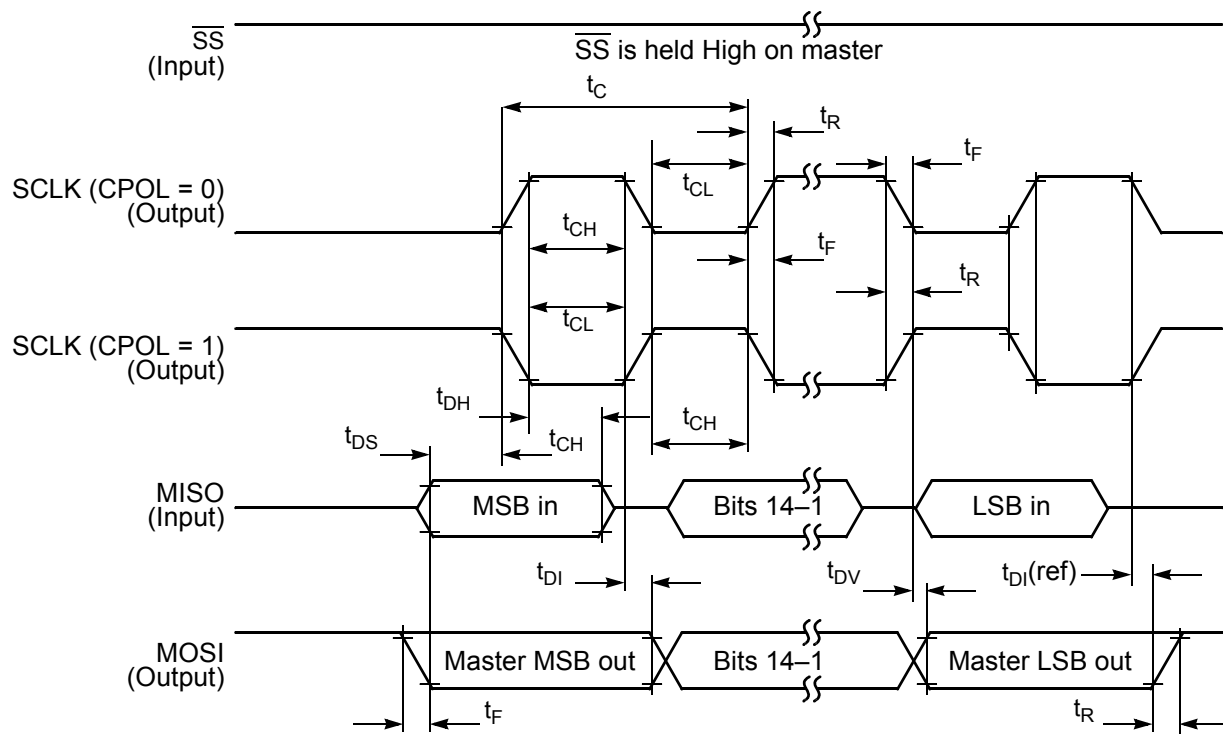


Figure 4-24 SPI Master Timing (CPHA = 0)

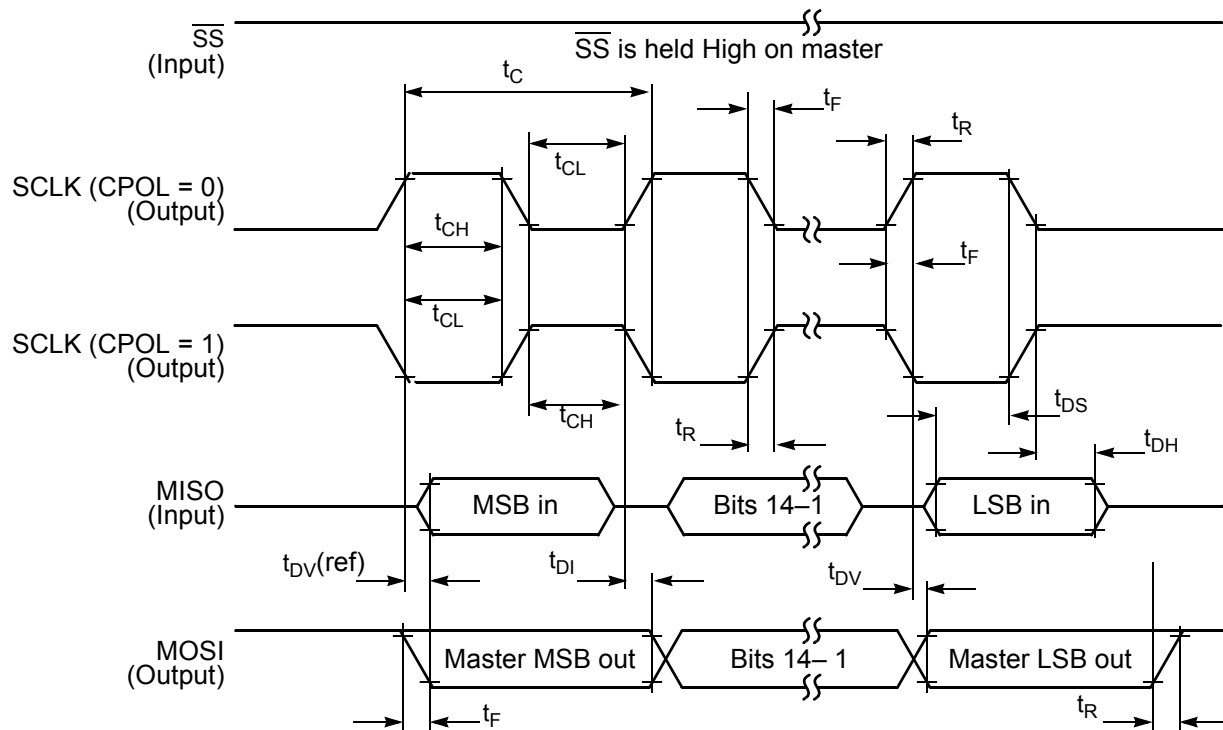


Figure 4-25 SPI Master Timing (CPHA = 1)

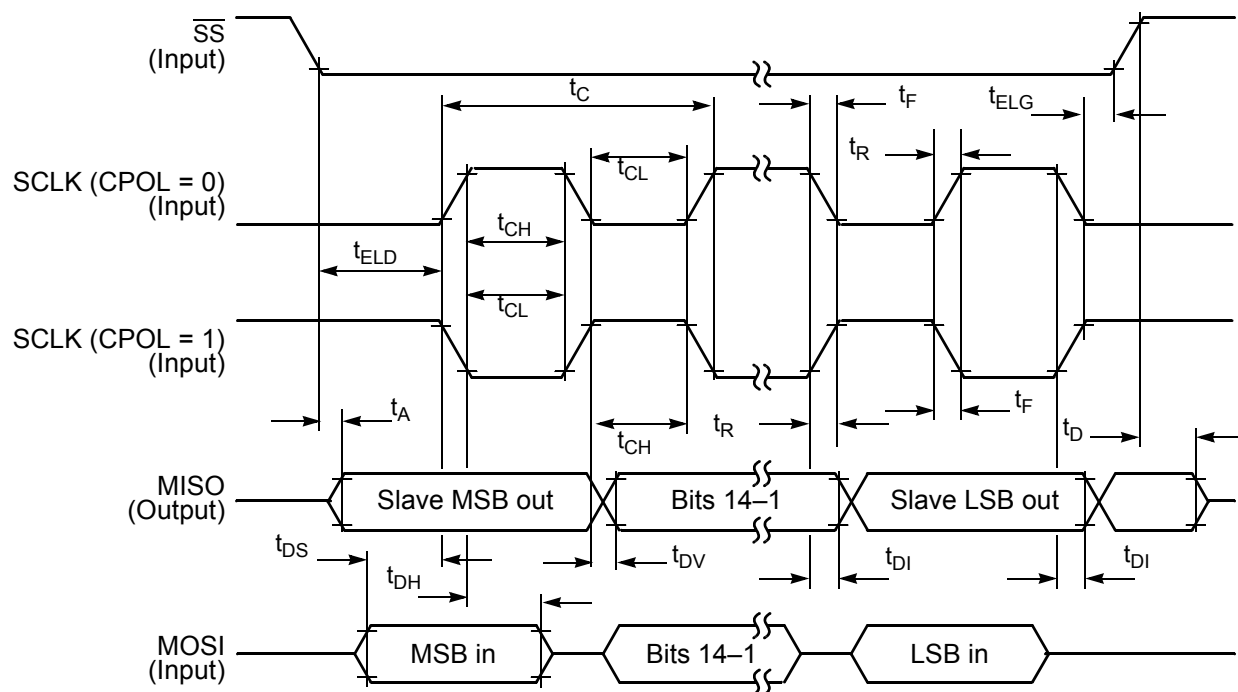


Figure 4-26 SPI Slave Timing (CPHA = 0)

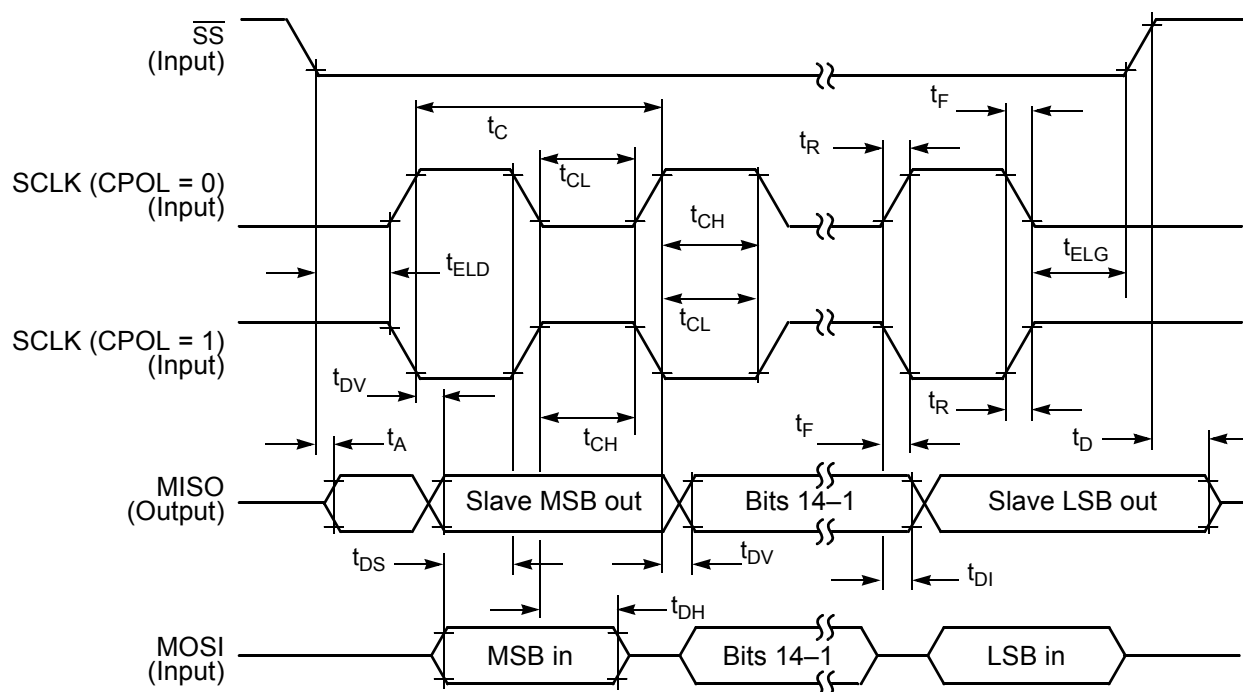


Figure 4-27 SPI Slave Timing (CPHA = 1)

4.10 Quad Timer Timing

Table 4-10 Quad Timer Timing^{1, 2}

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	$2T + 3$	—	ns
Timer input high/low period	P_{INHL}	$1T + 3$	—	ns
Timer output period	P_{OUT}	$2T - 3$	—	ns
Timer output high/low period	P_{OUTHL}	$1T - 3$	—	ns

1. In the formulas listed, T = clock cycle. For $f_{op} = 120\text{ MHz}$ operation and $f_{ipb} = 60\text{ MHz}$, $T = 8.33\text{ ns}$.
2. Parameters listed are guaranteed by design.

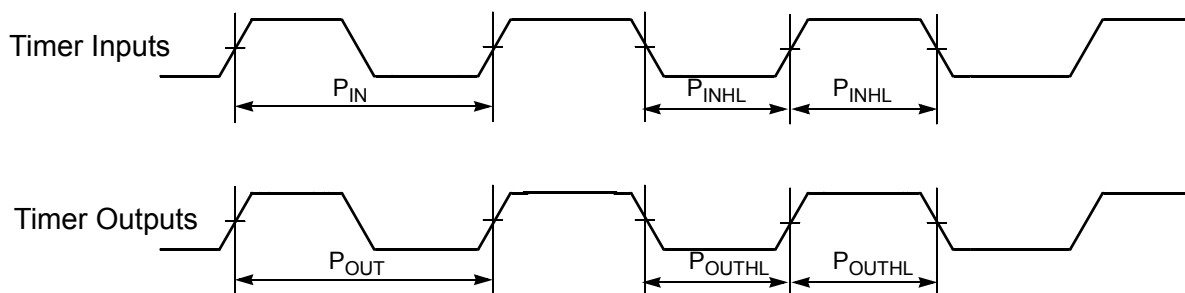


Figure 4-28 Timer Timing

4.11 Enhanced Synchronous Serial Interface (ESSI) Timing

Table 4-11 ESSI Master Mode¹ Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	f_s	—	—	15^2	MHz
SCK period ³	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4 ⁴	—	—	ns
SCK low time	t_{SCKL}	33.4 ⁴	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master ⁵	t_{TFSBHM}	-1.0	—	1.0	ns

Table 4-11 ESSI Master Mode¹ Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
Delay from SCK high to SC2 (wl) high - Master ⁵	t_{TFSWHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) high - Master ⁵	t_{RFSBHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master ⁵	t_{RFSWHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master ⁵	t_{TFSBLM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) low - Master ⁵	t_{TFSWLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master ⁵	t_{RFSBLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master ⁵	t_{RFSWLM}	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	t_{TXEM}	-0.1	—	2	ns
SCK high to STD valid - Master	t_{TXVM}	-0.1	—	2	ns
SCK high to STD not valid - Master	t_{TXNVM}	-0.1	—	—	ns
SCK high to STD high impedance - Master	t_{TXHIM}	-4	—	0	ns
SRD Setup time before SC0 low - Master	t_{SM}	4	—	—	ns
SRD Hold time after SC0 low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRD Setup time before SCK low - Master	t_{TSM}	4	—	—	ns
SRD Hold time after SCK low - Master	t_{THM}	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is $IP_clk/4 = 60\text{ MHz} / 4 = 15\text{ MHz}$ for an 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFISI=0 in SCR2 and RFISI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

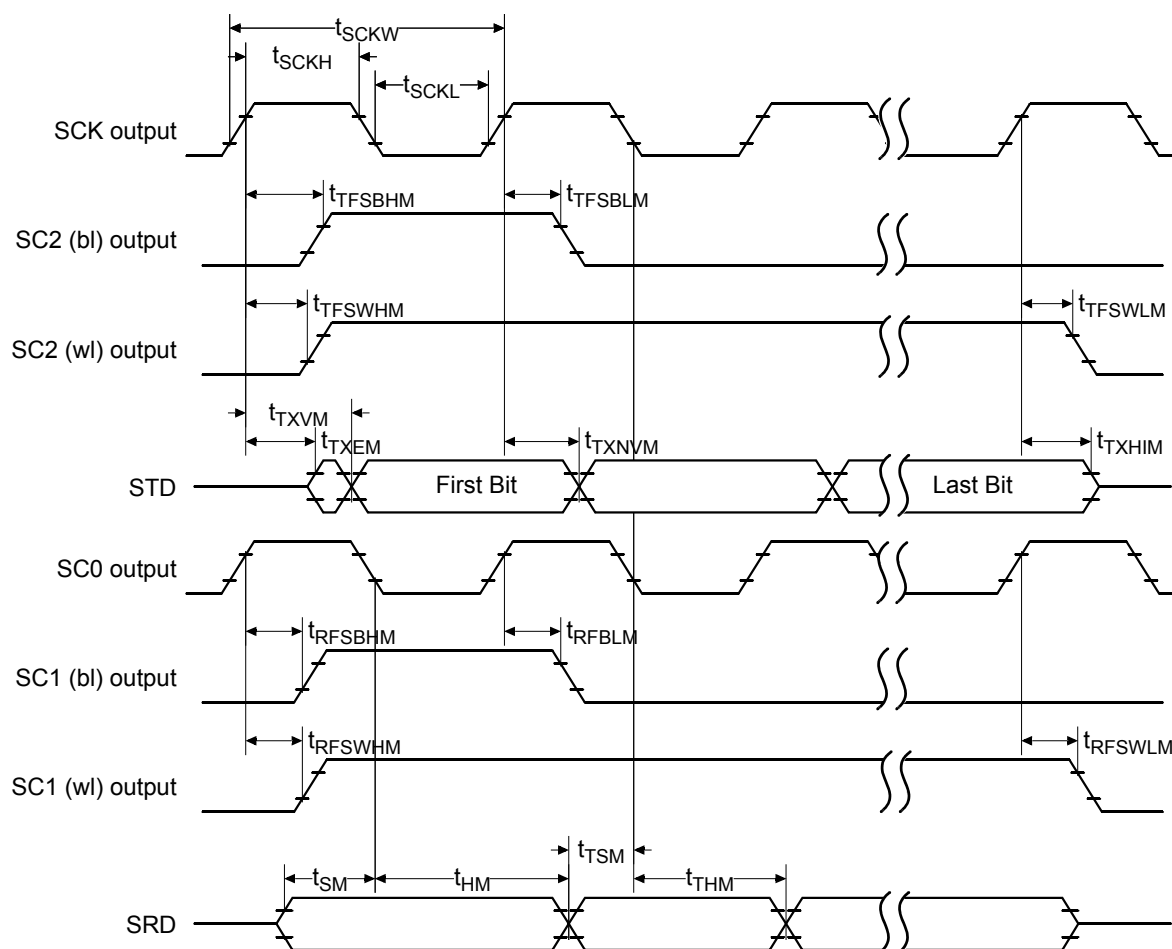


Figure 4-29 Master Mode Timing Diagram

Table 4-12 ESSI Slave Mode¹ Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{ C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	f_s	—	—	15 ²	MHz
SCK period ³	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4 ⁴	—	—	ns
SCK low time	t_{SCKL}	33.4 ⁴	—	—	ns
Output clock rise/fall time	—	—	4	—	ns

Table 4-12 ESSI Slave Mode¹ Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Parameter	Symbol	Min	Typ	Max	Units
Delay from SCK high to SC2 (bl) high - Slave ⁵	t_{TFSBHS}	-1	—	29	ns
Delay from SCK high to SC2 (wl) high - Slave ⁵	t_{TFSWHS}	-1	—	29	ns
Delay from SC0 high to SC1 (bl) high - Slave ⁵	t_{RFSBHS}	-1	—	29	ns
Delay from SC0 high to SC1 (wl) high - Slave ⁵	t_{RFSWHS}	-1	—	29	ns
Delay from SCK high to SC2 (bl) low - Slave ⁵	t_{TFSBLS}	-29	—	29	ns
Delay from SCK high to SC2 (wl) low - Slave ⁵	t_{TFSWLS}	-29	—	29	ns
Delay from SC0 high to SC1 (bl) low - Slave ⁵	t_{RFSBLS}	-29	—	29	ns
Delay from SC0 high to SC1 (wl) low - Slave ⁵	t_{RFSWLS}	-29	—	29	ns
SCK high to STD enable from high impedance - Slave	t_{TXES}	—	—	15	ns
SCK high to STD valid - Slave	t_{TXVS}	4	—	15	ns
SC2 high to STD enable from high impedance (first bit) - Slave	t_{FTXES}	4	—	15	ns
SC2 high to STD valid (first bit) - Slave	t_{FTXVS}	4	—	15	ns
SCK high to STD not valid - Slave	t_{TXNVS}	4	—	15	ns
SCK high to STD high impedance - Slave	t_{TXHIS}	4	—	15	ns
SRD Setup time before SC0 low - Slave	t_{SS}	4	—	—	ns
SRD Hold time after SC0 low - Slave	t_{HS}	4	—	—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRD Setup time before SCK low - Slave	t_{TSS}	4	—	—	ns
SRD Hold time after SCK low - Slave	t_{THS}	4	—	—	ns

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is $IP_clk/4 = 60\text{ MHz} / 4 = 15\text{ MHz}$ for a 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

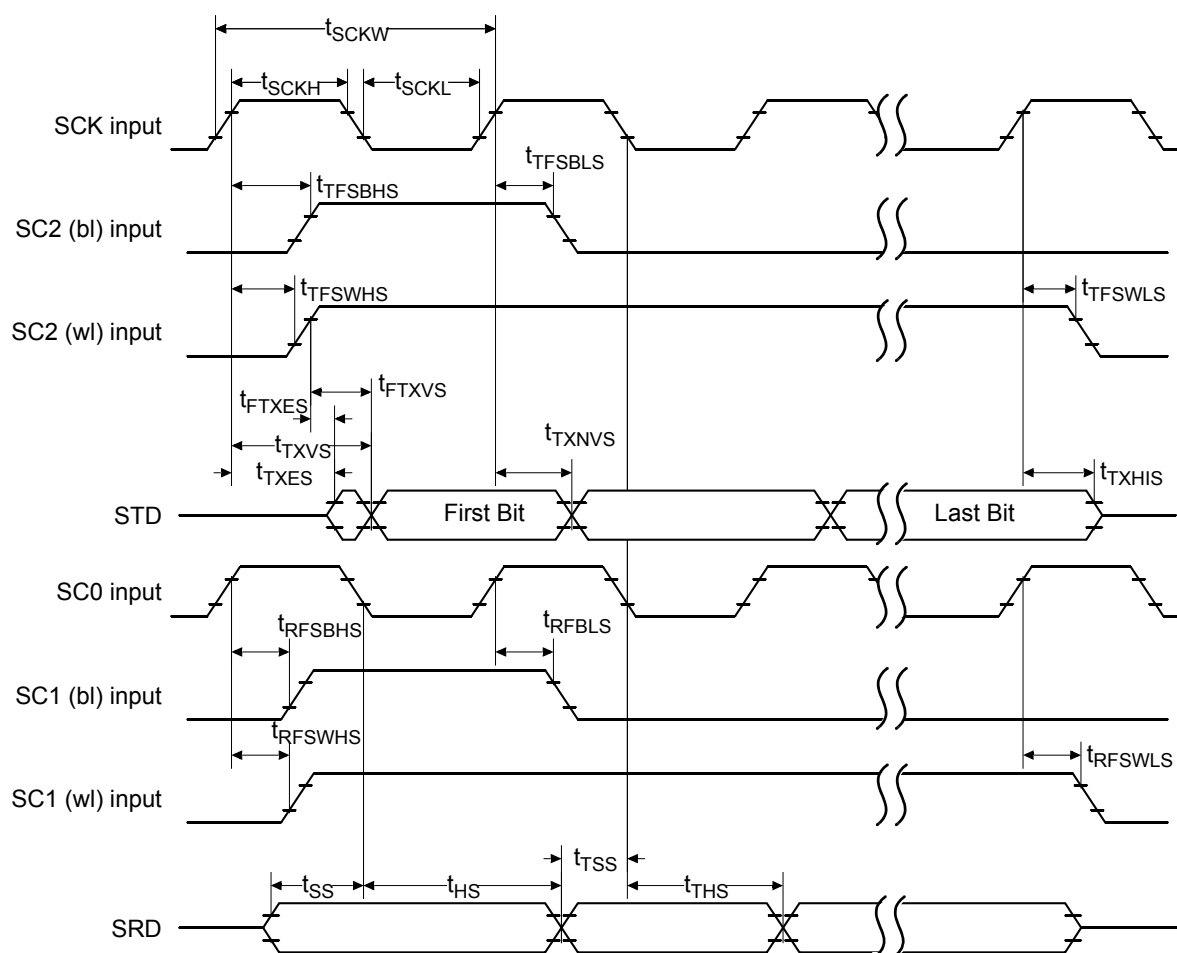


Figure 4-30 Slave Mode Clock Timing

4.12 Serial Communication Interface (SCI) Timing

Table 4-13 SCI Timing⁴

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
Baud Rate ¹	BR	—	$(f_{MAX})/(32)$	Mbps
RXD ² Pulse Width	RXD_{PW}	$0.965/BR$	$1.04/BR$	ns
TXD ³ Pulse Width	TXD_{PW}	$0.965/BR$	$1.04/BR$	ns

- f_{MAX} is the frequency of operation of the system clock in MHz.
- The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
- The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
- Parameters listed are guaranteed by design.

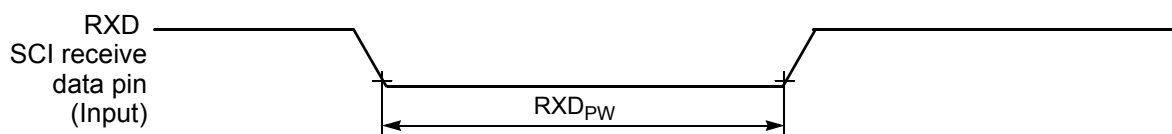


Figure 4-31 RXD Pulse Width

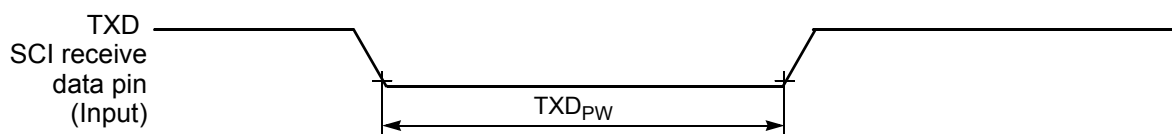


Figure 4-32 TXD Pulse Width

4.13 JTAG Timing

Table 4-14 JTAG Timing^{1, 3}

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation ²	f_{OP}	DC	30	MHz
TCK cycle time	t_{CY}	33.3	—	ns
TCK clock pulse width	t_{PW}	16.6	—	ns
TMS, TDI data setup time	t_{DS}	3	—	ns
TMS, TDI data hold time	t_{DH}	3	—	ns
TCK low to TDO data valid	t_{DV}	—	12	ns
TCK low to TDO tri-state	t_{TS}	—	10	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	35	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, $T = \text{clock cycle}$. For 120MHz operation, $T = 8.33\text{ ns}$.
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

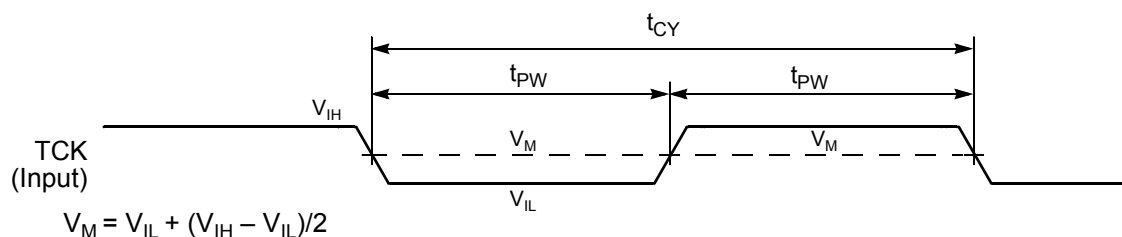


Figure 4-33 Test Clock Input Timing Diagram

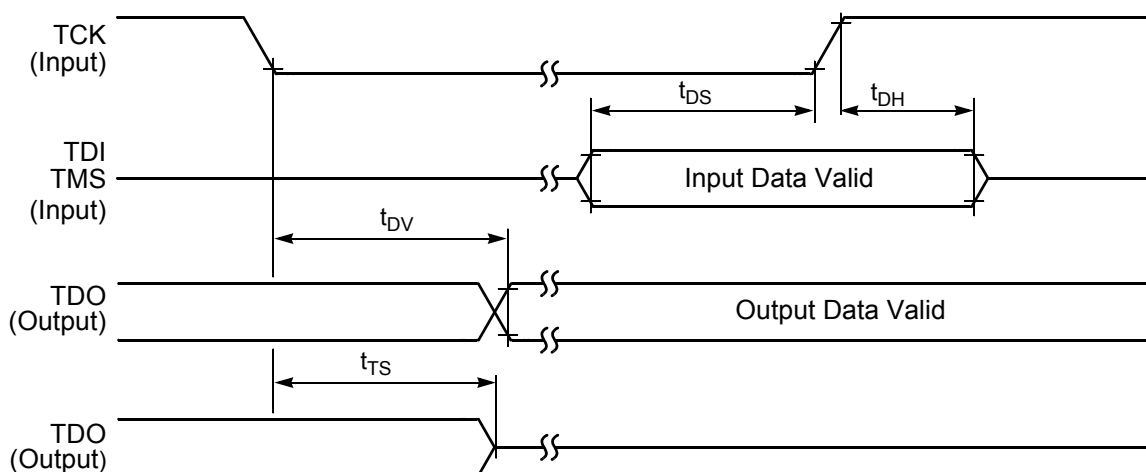


Figure 4-34 Test Access Port Timing Diagram



Figure 4-35 TRST Timing Diagram

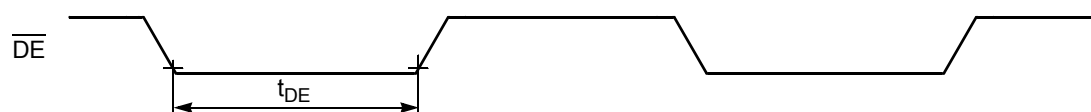


Figure 4-36 Enhanced OnCE—Debug Event

4.14 GPIO Timing

Table 4-15 GPIO Timing^{1, 2}

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0\text{ V}$, $V_{DD} = 1.62\text{--}1.98\text{ V}$, $V_{DDIO} = V_{DDA} = 3.0\text{--}3.6\text{ V}$, $T_A = -40^\circ\text{ to }+120^\circ\text{C}$, $C_L \leq 50\text{ pF}$, $f_{op} = 120\text{ MHz}$

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	$2T + 3$	—	ns
GPIO input high/low period	P_{INHL}	$1T + 3$	—	ns
GPIO output period	P_{OUT}	$2T - 3$	—	ns
GPIO output high/low period	P_{OUTHL}	$1T - 3$	—	ns

1. In the formulas listed, T = clock cycle. For $f_{op} = 120\text{ MHz}$ operation and $f_{ipb} = 60\text{ MHz}$, $T = 8.33\text{ ns}$
2. Parameters listed are guaranteed by design.

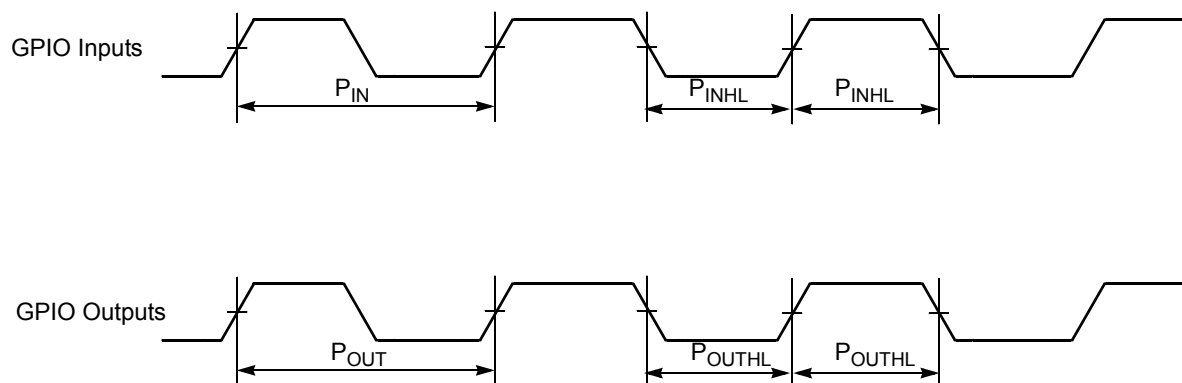


Figure 4-37 GPIO Timing

Part 5 Packaging

5.1 Package and Pin-Out Information 56853

This section contains package and pin-out information for the 144-pin LQFP configuration of the 56858.

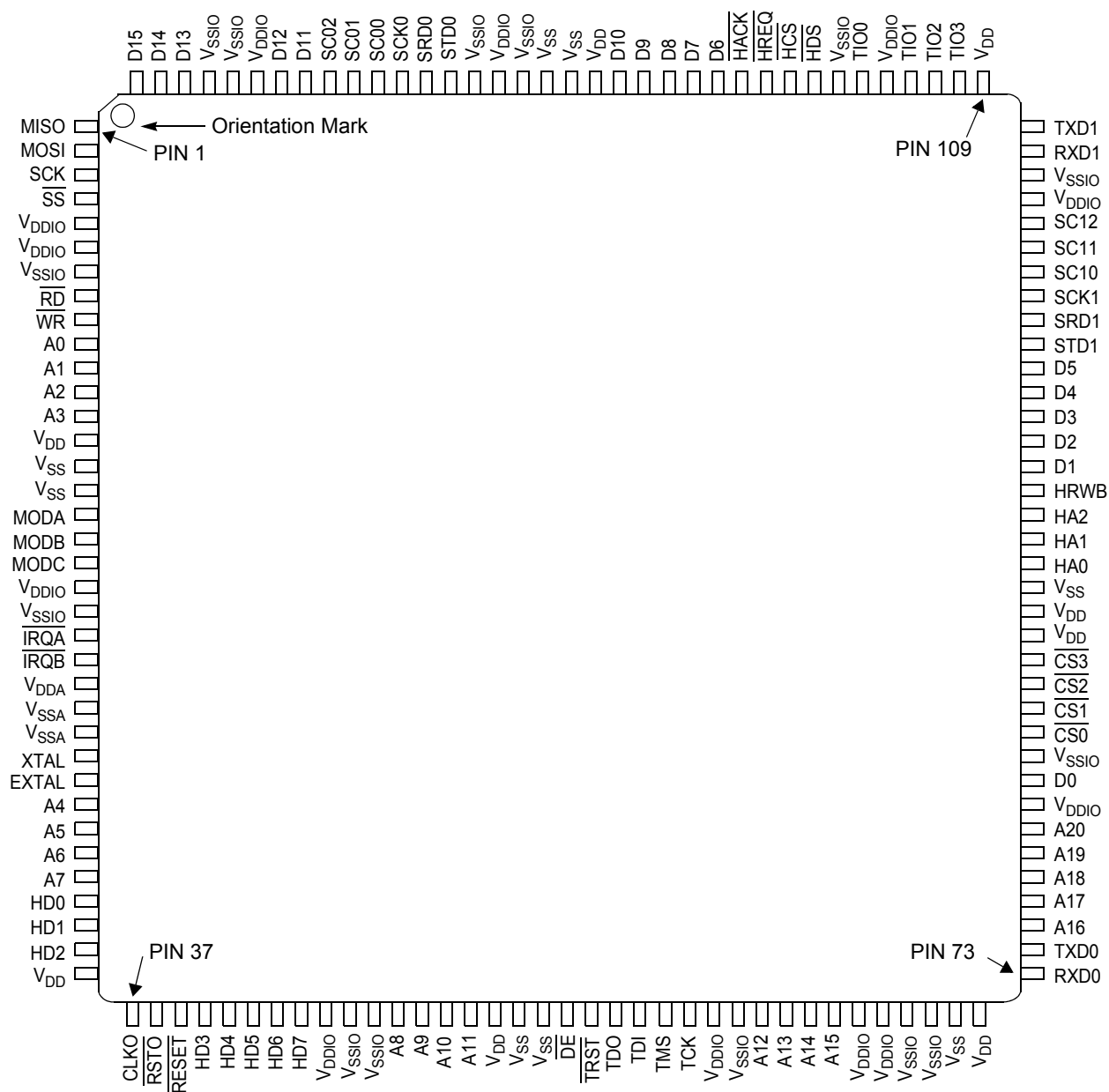


Figure 5-1 Top View, 56858 144-pin LQFP Package

Table 5-1 56858 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	MISO	37	CLKO	73	RXD0	109	V _{DD}
2	MOSI	38	$\overline{\text{RSTO}}$	74	TXD0	110	TIO3
3	SCK	39	$\overline{\text{RESET}}$	75	A16	111	TIO2
4	$\overline{\text{SS}}$	40	HD3	76	A17	112	TIO1
5	V _{DDIO}	41	HD4	77	A18	113	V _{DDIO}
6	V _{DDIO}	42	HD5	78	A19	114	TIO0
7	V _{SSIO}	43	HD6	79	A20	115	V _{SSIO}
8	$\overline{\text{RD}}$	44	HD7	80	V _{DDIO}	116	$\overline{\text{HDS}}$
9	$\overline{\text{WR}}$	45	V _{DDIO}	81	D0	117	$\overline{\text{HCS}}$
10	A0	46	V _{SSIO}	82	V _{SSIO}	118	$\overline{\text{HREQ}}$
11	A1	47	V _{SSIO}	83	$\overline{\text{CS0}}$	119	$\overline{\text{HACK}}$
12	A2	48	A8	84	$\overline{\text{CS1}}$	120	D6
13	A3	49	A9	85	$\overline{\text{CS2}}$	121	D7
14	V _{DD}	50	A10	86	$\overline{\text{CS3}}$	122	D8
15	V _{SS}	51	A11	87	V _{DD}	123	D9
16	V _{SS}	52	V _{DD}	88	V _{DD}	124	D10
17	MODA	53	V _{SS}	89	V _{SS}	125	V _{DD}
18	MODB	54	V _{SS}	90	HA0	126	V _{SS}
19	MODC	55	$\overline{\text{DE}}$	91	HA1	127	V _{SS}
20	V _{DDIO}	56	$\overline{\text{TRST}}$	92	HA2	128	V _{SSIO}
21	V _{SSIO}	57	TDO	93	HRWB	129	V _{DDIO}
22	$\overline{\text{IRQA}}$	58	TDI	94	D1	130	V _{SSIO}
23	$\overline{\text{IRQB}}$	59	TMS	95	D2	131	STD0

Table 5-1 56858 Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
24	V _{DDA}	60	TCK	96	D3	132	SRD0
25	V _{SSA}	61	V _{DDIO}	97	D4	133	SCK0
26	V _{SSA}	62	V _{SSIO}	98	D5	134	SC00
27	XTAL	63	A12	99	STD1	135	SC01
28	EXTAL	64	A13	100	SRD1	136	SC02
29	A4	65	A14	101	SCK1	137	D11
30	A5	66	A15	102	SC10	138	D12
31	A6	67	V _{DDIO}	103	SC11	139	V _{DDIO}
32	A7	68	V _{DDIO}	104	SC12	140	V _{SSIO}
33	HD0	69	V _{SSIO}	105	V _{DDIO}	141	V _{SSIO}
34	HD1	70	V _{SSIO}	106	V _{SSIO}	142	D13
35	HD2	71	V _{SS}	107	RXD1	143	D14
36	V _{DD}	72	V _{DD}	108	TXD1	144	D15

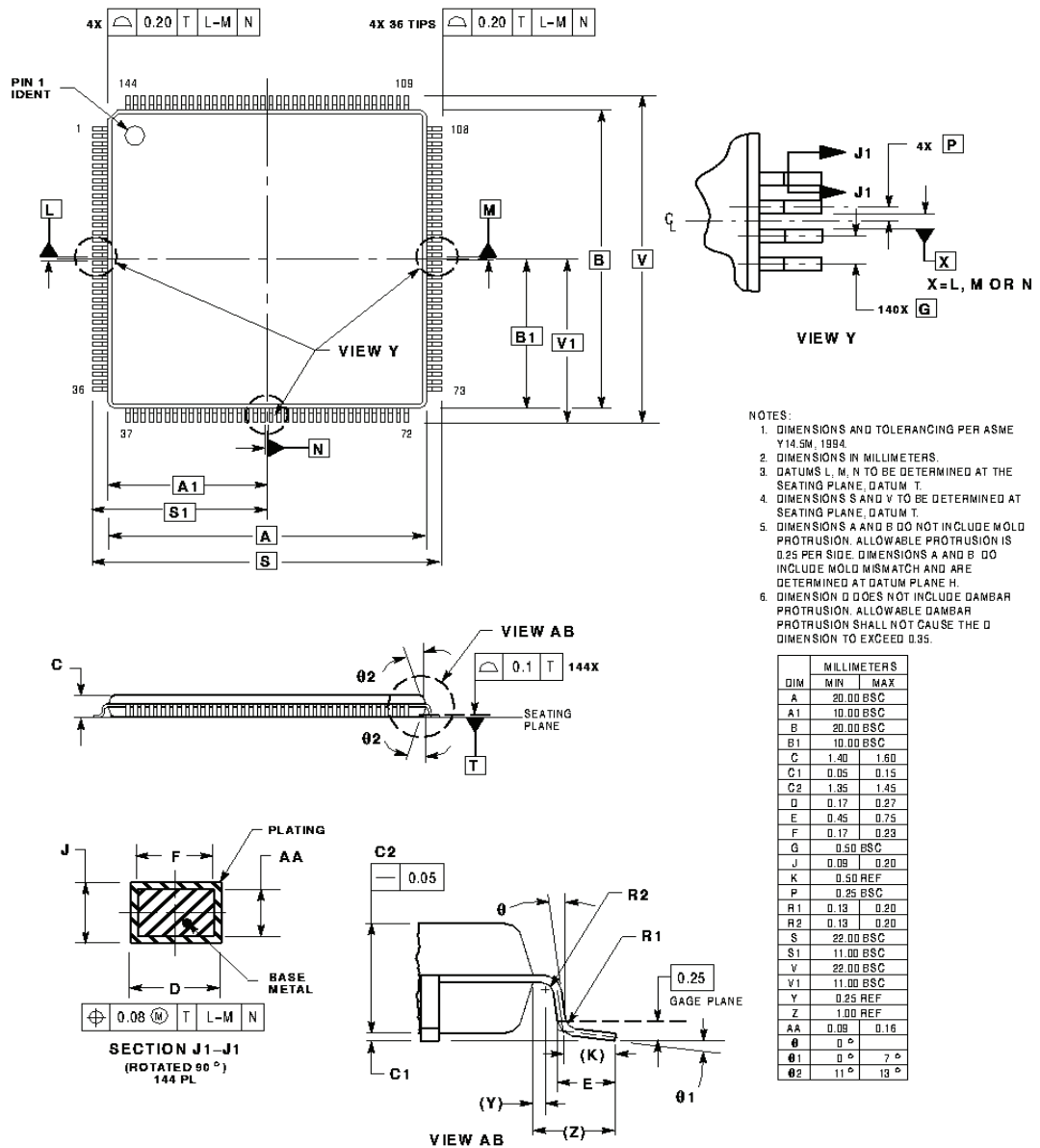


Figure 5-2 144-pin LQFP Mechanical Information

Please see www.freescale.com for the most current case outline.

This section contains package and pin-out information for the 144-pin MAPBGA configuration of the 56858.

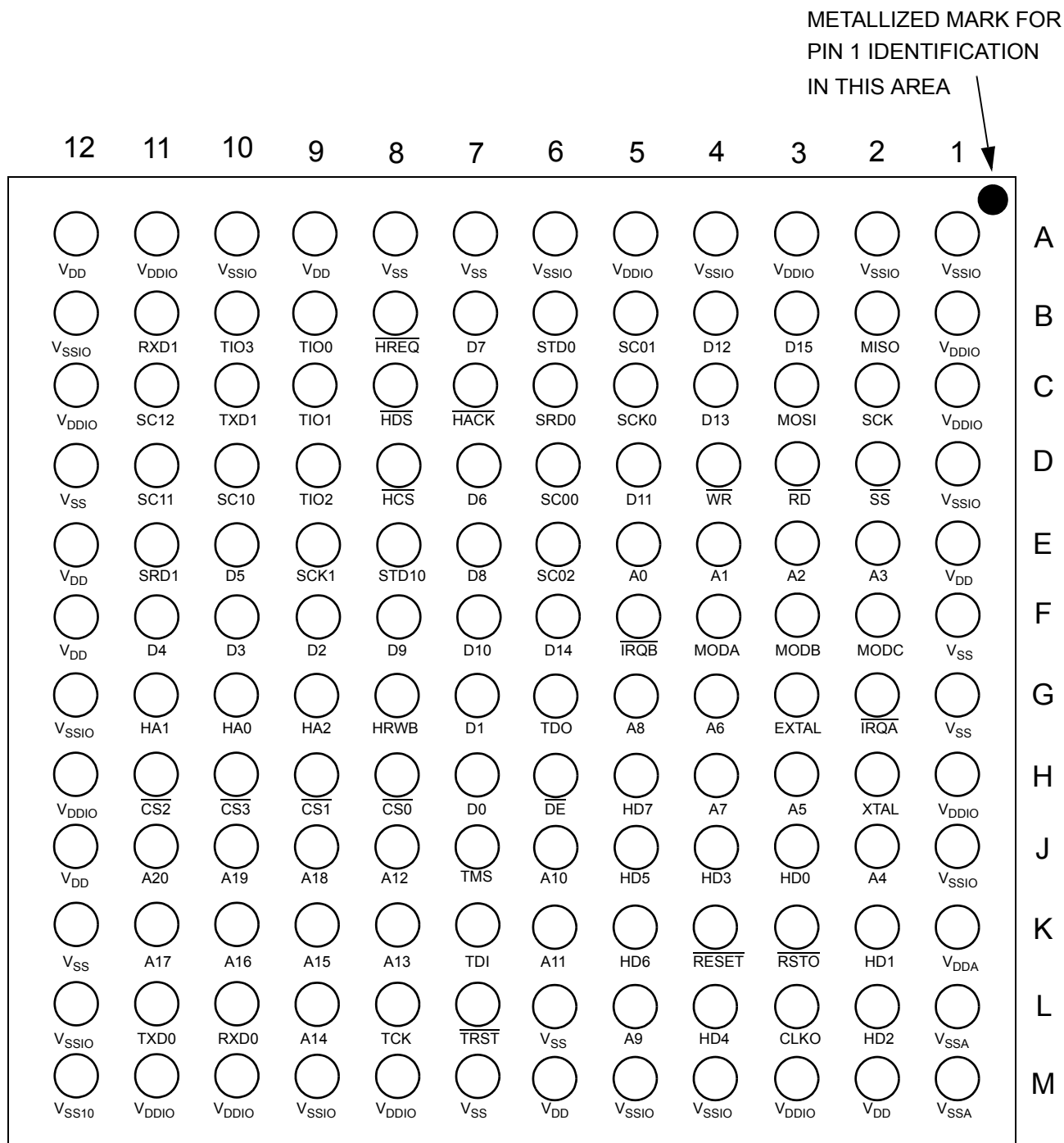


Figure 5-3 Bottom-View, 56858 144-pin MAPBGA Package

Table 5-2 56858 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E5	A0	F7	D10	D8	HCS	A5	V _{DDIO}
E4	A1	D5	D11	J3	HD0	A3	V _{DDIO}
E3	A2	B4	D12	K2	HD1	C1	V _{DDIO}
E2	A3	C4	D13	L2	HD2	M10	V _{DDIO}
J2	A4	F6	D14	J4	HD3	D3	$\overline{\text{RD}}$
H3	A5	B3	D15	L4	HD4	K4	$\overline{\text{RESET}}$
G4	A6	H6	$\overline{\text{DE}}$	J5	HD5	K3	$\overline{\text{RSTO}}$
H4	A7	G3	EXTAL	K5	HD6	L10	RXD0
G5	A8	M1	V _{SSA}	H5	HD7	B11	RXD1
L5	A9	L1	V _{SSA}	C8	$\overline{\text{HDS}}$	D6	SC00
J6	A10	G1	V _{SS}	B8	$\overline{\text{HREQ}}$	B5	SC01
K6	A11	L6	V _{SS}	G8	HRWB	E6	SC02
J8	A12	D12	V _{SS}	G2	$\overline{\text{IRQA}}$	D10	SC10
K8	A13	A7	V _{SS}	F5	$\overline{\text{IRQB}}$	D11	SC11
L9	A14	F1	V _{SS}	B2	MISO	C11	SC12
K9	A15	M7	V _{SS}	F4	MODA	C5	SCK0
K10	A16	K12	V _{SS}	F3	MODB	E9	SCK1
K11	A17	A8	V _{SS}	F2	MODC	C2	SCK
J9	A18	D1	V _{SSIO}	C3	MOSI	C6	SRD0
J10	A19	J1	V _{SSIO}	K1	V _{DDA}	E11	SRD1
J11	A20	M5	V _{SSIO}	E1	V _{DD}	D2	$\overline{\text{SS}}$
L3	CLKO	M9	V _{SSIO}	M6	V _{DD}	B6	STD0
H8	$\overline{\text{CS0}}$	L12	V _{SSIO}	F12	V _{DD}	E8	STD1
H9	$\overline{\text{CS1}}$	G12	V _{SSIO}	A9	V _{DD}	L8	TCK

Table 5-2 56858 Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
H11	$\overline{\text{CS2}}$	B12	V _{SSIO}	M2	V _{DD}	K7	TDI
H10	$\overline{\text{CS3}}$	A10	V _{SSIO}	J12	V _{DD}	G6	TDO
H7	D0	A4	V _{SSIO}	E12	V _{DD}	B9	TIO0
G7	D1	A1	V _{SSIO}	A12	V _{DD}	C9	TIO1
F9	D2	A2	V _{SSIO}	B1	V _{DDIO}	D9	TIO2
F10	D3	M4	V _{SSIO}	H1	V _{DDIO}	B10	TIO3
F11	D4	M12	V _{SSIO}	M3	V _{DDIO}	J7	TMS
E10	D5	A6	V _{SSIO}	M8	V _{DDIO}	L7	$\overline{\text{TRST}}$
D7	D6	G10	HA0	M11	V _{DDIO}	L11	TXD0
B7	D7	G11	HA1	H12	V _{DDIO}	C10	TXD1
E7	D8	G9	HA2	C12	V _{DDIO}	D4	$\overline{\text{WR}}$
F8	D9	C7	$\overline{\text{HACK}}$	A11	V _{DDIO}	H2	XTAL

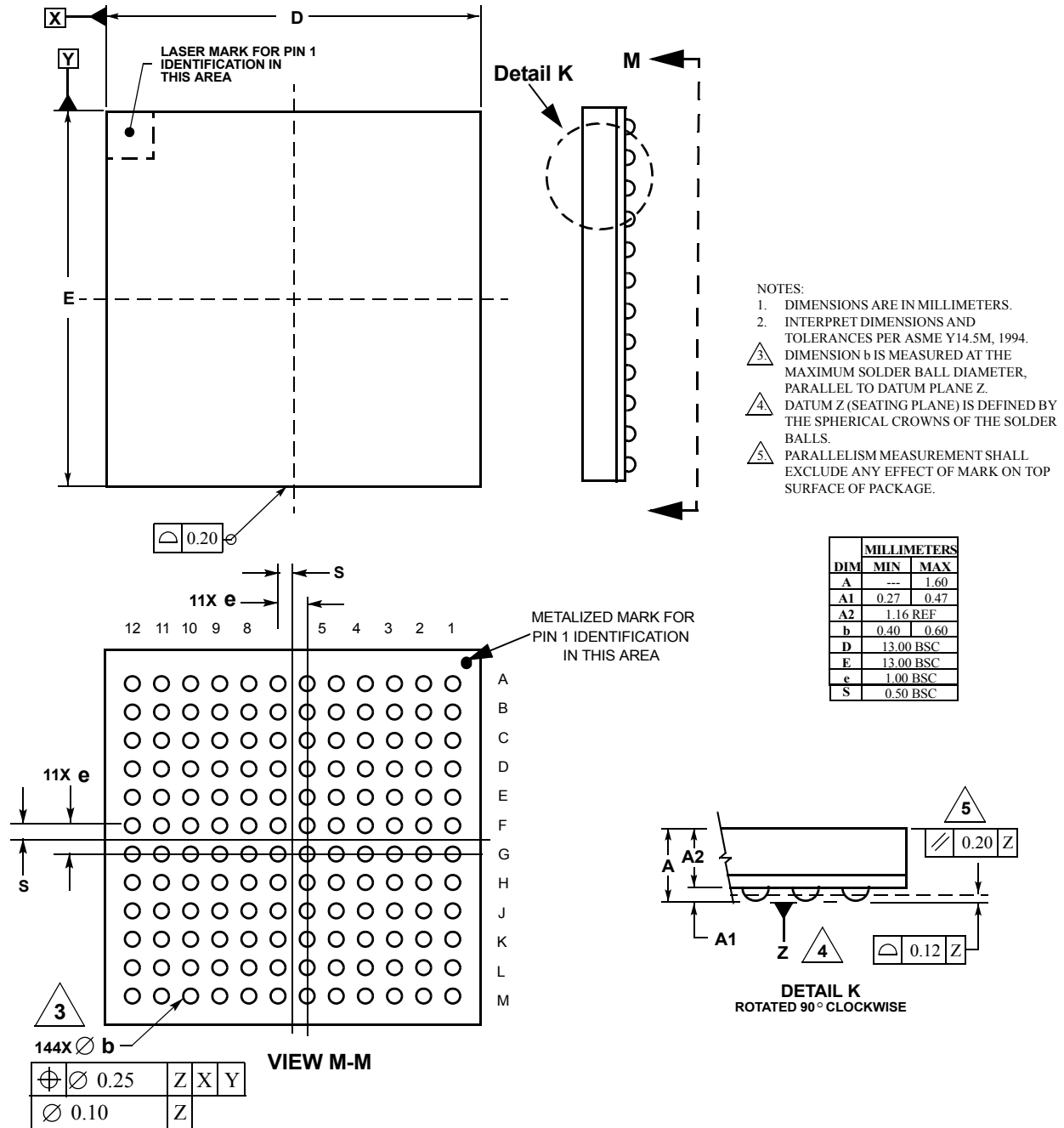


Figure 5-4 144-pin MAPBGA Mechanical Information

Please see www.freescale.com for the most current case outline.

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J , in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT} , has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 μF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA} .
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100 μF , preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.

- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{IRQx}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{TRST}$ pin for JTAG port or Enhance OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{TRST}$ whenever RESET is asserted, as well as a means to assert $\overline{TRST}$ independently of RESET. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- The internal POR (Power on Reset) will reset the part at power on with $\overline{reset}$ asserted or pulled high but requires that $\overline{TRST}$ be asserted at power on.

Part 7 Ordering Information

Table 7-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 7-1 56858 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56858	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	144	120	DSP56858FV120
DSP56858	1.8V, 3.3V	MAP Ball Grid Array (MAPBGA)	144	120	DSP56858VF120
DSP56858	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	144	120	DSP56858FVE *

*This package is RoHS compliant.

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