16 Mbps, ESD Protected, Full-Duplex RS-485 Transceivers

Data Sheet

ADM1490E/ADM1491E

FEATURES

- RS-485/RS-422 full-duplex transceiver for high speed motor control applications
- 16 Mbps data rate
- ±8 kV ESD protection on RS-485 input/output pins
- Complies with ANSI/TIA/EIA-485-A-1998
- Open circuit fail-safe
- Suitable for 5 V power supply applications
- 32 nodes on the bus (1 unit load)
- Thermal shutdown protection
- Operating temperature range: −40°C to +85°C
- ADM1490E packages
  - Narrow body, 8-lead SOIC
  - 8-lead MSOP
- ADM1491E packages
  - Narrow-body, 14-lead SOIC
  - 10-lead MSOP

APPLICATIONS

- RS-485/RS-422 interfaces
- Industrial field networks
- High data rate motor control
- Multipoint data transmission systems
- Single-ended-to-differential signal conversion

FUNCTIONAL BLOCK DIAGRAMS

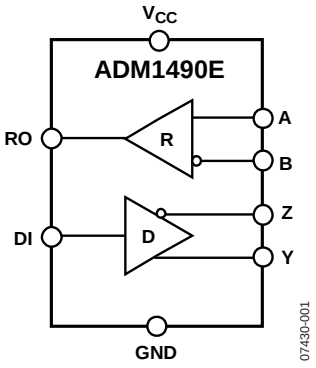


Figure 1.

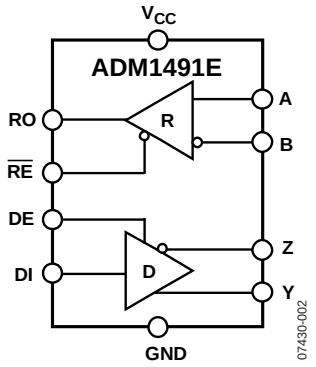


Figure 2.

GENERAL DESCRIPTION

The ADM1490E/ADM1491E are RS-485/RS-422 transceivers with ±8 kV ESD protection and are suitable for high speed, full-duplex communication on multipoint transmission lines. In particular, the ADM1490E/ADM1491E are designed for use in motor control applications requiring communications at data rates up to 16 Mbps.

The ADM1490E/ADM1491E are designed for balanced transmission lines and comply with TIA/EIA-485-A-98. The devices each have a 12 kΩ receiver input impedance for unit load RS-485 operation, allowing up to 32 nodes on the bus.

The differential transmitter outputs and receiver inputs feature electrostatic discharge circuitry that provides protection to ±8 kV using the human body model (HBM).

The ADM1490E/ADM1491E operate from a single 5 V power supply. Excessive power dissipation caused by bus contention or output shorting is prevented by short-circuit protection and thermal circuitry. Short-circuit protection circuits limit the maximum output current to ±250 mA during fault conditions. A thermal shutdown circuit senses if the die temperature rises above 150°C and forces the driver outputs into a high impedance state under this condition.

The receiver of the ADM1490E/ADM1491E contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM1490E/ADM1491E feature extremely fast and closely matched switching times. Minimal driver propagation delays permit transmission at data rates up to 16 Mbps, and low skew minimizes EMI interference.

The ADM1490E/ADM1491E are fully specified over the commercial and industrial temperature ranges. The ADM1490E is available in two packages: a narrow body, 8-lead SOIC and an 8-lead MSOP. The ADM1491E is also available in two packages: a narrow body, 14-lead SOIC and a 10-lead MSOP.

Rev. D

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagrams ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
Timing Specifications ... 4
Absolute Maximum Ratings ... 5
Thermal Resistance ... 5
ESD Caution ... 5
Pin Configurations and Function Descriptions ... 6
Typical Performance Characteristics ... 7
Test Circuits ... 9
Theory of Operation ... 10
Truth Tables ... 10
ESD Transient Protection Scheme ... 10
Applications Information ... 12
Differential Data ... 12
Cable and Data Rate ... 12
Typical Applications ... 12
Outline Dimensions ... 14
Ordering Guide ... 15

REVISION HISTORY

2/12—Rev. C to Rev. D

Changes to Figure 8 ... 6
Updated Outline Dimensions ... 14

12/10—Rev. B to Rev. C

Changes to Figure 29 ... 12
Changes to Figure 30 ... 13

7/09—Rev. A to Rev. B

Added ADM1490E, 8-Lead SOIC, and 8-Lead MSOP ... Universal
Changes to Table 4 ... 5
Added Figure 7; Renumbered Figures Sequentially ... 6
Changes to Table 5 ... 6
Changes to Typical Applications Section ... 12
Added Figure 29 ... 12
Changes to Figure 30 ... 13
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

2/09—Rev. 0 to Rev. A

Change to Table 9 ... 11
12/08—Revision 0: Initial Version

SPECIFICATIONS

4.75 V ≤ V_{CC} ≤ 5.25 V; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = 5.0 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Outputs Enabled	I_{CC1}		1.2	2.0	mA	Outputs unloaded, digital inputs = V_{CC} or GND
Outputs Disabled	I_{CC2}		0.8	1.5	mA	Outputs unloaded, digital inputs = V_{CC} or GND
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\lvert V_{OD2}\rvert$	2.0		5.0	V	R_L = 100 Ω (RS-422), see Figure 21
		1.5		5.0	V	R_L = 54 Ω (RS-485), see Figure 21
	$\lvert V_{OD3}\rvert$	1.5		5.0	V	−7 V ≤ V_{TEST} ≤ +12 V, see Figure 22
Δ$\lvert V_{OD}\rvert$ for Complementary Output States	Δ$\lvert V_{OD2}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 21
Common-Mode Output Voltage	V_{OC}			3.0	V	R_L = 54 Ω or 100 Ω, see Figure 21
Δ$\lvert V_{OC}\rvert$ for Complementary Output States	Δ$\lvert V_{OC}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 21
Output Leakage Current (Y, Z)	I_O			100	µA	DE = 0 V, V_{DD} = 0 V or 5 V, V_{IN} = 12 V
	I_O	−100			µA	DE = 0 V, V_{DD} = 0 V or 5 V, V_{IN} = −7 V
Output Short-Circuit Current	I_{OS}			250	mA	−7 V < V_{OUT} < +12 V
Logic Inputs DE, $\overline{RE}$, DI						
Input Low Voltage	V_{IL}			0.8	V	DE, $\overline{RE}$, DI
Input High Voltage	V_{IH}	2.0			V	DE, $\overline{RE}$, DI
Input Current	I_I	−1		+1	µA	DE, $\overline{RE}$, DI
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−0.2		+0.2	V	−7 V < V_{CM} < +12 V
Input Voltage Hysteresis	V_{HYS}		30		mV	V_{CM} = 0 V
Input Current (A, B)	I_I			1.0	mA	V_{CM} = 12 V
		−0.8			mA	V_{CM} = −7 V
Line Input Resistance	R_{IN}	12	30		kΩ	−7 V ≤ V_{CM} ≤ +12 V
Logic Outputs						
Output Voltage Low	V_{OL}			0.4	V	I_{OUT} = +4.0 mA, V_A − V_B = −0.2 V
Output Voltage High	V_{OH}	4.0			V	I_{OUT} = −4.0 mA, V_A − V_B = +0.2 V
Short-Circuit Current				85	mA	
Three-State Output Leakage Current	I_{OZR}			±1	µA	V_{CC} = 5.25 V, 0.4 V < V_{OUT} < 2.4 V

TIMING SPECIFICATIONS

T_A = −40°C to +85°C.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		16			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		11	17	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 23 and Figure 3
Driver Output Skew	t_{SKEW}		0.5	2	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 23 and Figure 3, $t_{SKEW} = \lvert t_{DPLH} - t_{DPHL} \rvert$
Rise Time/Fall Time	t_{DR}, t_{DF}		8	15	ns	R_L = 54 Ω, C_L = 100 pF, see Figure 23 and Figure 3
Enable Time	t_{ZH}, t_{ZL}			20	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 24 and Figure 5
Disable Time	t_{HZ}, t_{LZ}			20	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 24 and Figure 5
RECEIVER						
Propagation Delay	t_{PLH}, t_{PHL}		12	20	ns	C_L = 15 pF, see Figure 25 and Figure 4
Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKEW}		0.4	2	ns	C_L = 15 pF, see Figure 25 and Figure 4
Enable Time	t_{ZH}, t_{ZL}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 26 and Figure 6
Disable Time	t_{HZ}, t_{LZ}			13	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 26 and Figure 6

Timing Diagrams

Switching Characteristics

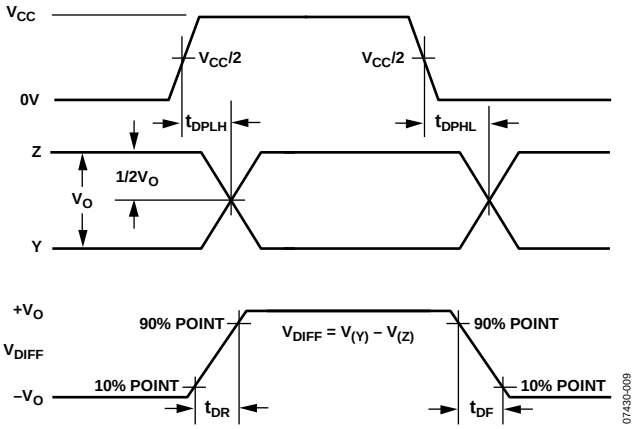


Figure 3. Driver Propagation Delay Rise/Fall Timing

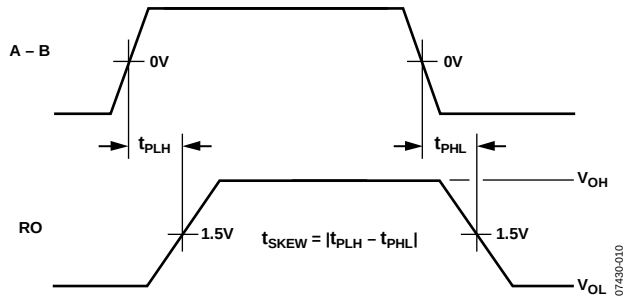


Figure 4. Receiver Propagation Delay Timing

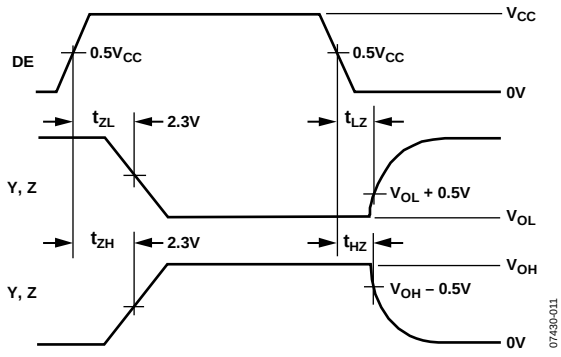


Figure 5. Driver Enable/Disable Timing

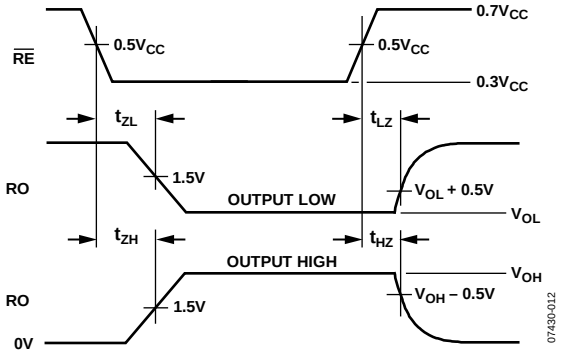


Figure 6. Receiver Enable/Disable Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +7 V
Digital I/O Voltage (DE, $\overline{RE}$)	−0.3 V to V_{CC} + 0.3 V
Driver Input Voltage (DI)	−0.3 V to V_{CC} + 0.3 V
Receiver Output Voltage (RO)	−0.3 V to V_{CC} + 0.3 V
Driver Output/Receiver Input Voltage (A, B, Y, Z)	−9 V to +14 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−55°C to +150°C
ESD (HBM) on A, B, Y, and Z	±8 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC	121	°C/W
14-Lead SOIC	86	°C/W
8-Lead MSOP	133	°C/W
10-Lead MSOP	133	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

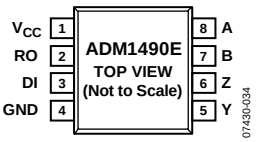
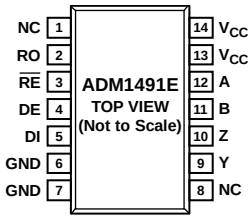


Figure 7. 8-Lead MSOP and 8-Lead SOIC Pin Configuration



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. PIN 7 IS NOT CONNECTED INTERNALLY. SHOWN AS GND TO COMPLY WITH INDUSTRY STANDARD PINOUT.
3. PIN 14 IS NOT CONNECTED INTERNALLY. SHOWN AS V_{CC} TO COMPLY WITH INDUSTRY STANDARD PINOUT.

07430-013

Figure 8. 14-Lead, Narrow Body SOIC Pin Configuration

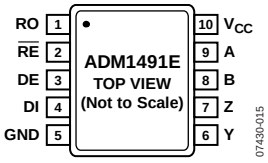


Figure 9. 10-Lead MSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.				
8-Lead SOIC, 8-Lead MSOP	**14-Lead SOIC**	**10-Lead MSOP**	**Mnemonic**	**Description**
N/A[1]	1	N/A[1]	NC	No Connect. This pin is available on the 14-lead SOIC only.
2	2	1	RO	Receiver Output.
N/A[1]	3	2	$\overline{RE}$	Receiver Output Enable. A low level enables the receiver output, whereas a high level places the receiver output in a high impedance state.
N/A[1]	4	3	DE	Driver Output Enable. A logic high enables the differential driver outputs, A and B, whereas a logic low places the differential driver outputs in a high impedance state.
3	5	4	DI	Driver Input. When the driver is enabled, a logic low on DI forces Pin A low and Pin B high, whereas a logic high on DI forces Pin A high and Pin B low.
4	6	5	GND	Ground.
N/A[1]	7	N/A[1]	GND	Ground. This pin is available on the 14-lead SOIC only.
N/A[1]	8	N/A[1]	NC	No Connect. This pin is available on the 14-lead SOIC only.
5	9	6	Y	Noninverting Driver Output Y.
6	10	7	Z	Inverting Driver Output Z.
7	11	8	B	Inverting Receiver Input B.
8	12	9	A	Noninverting Receiver Input A.
1	13	10	V_{CC}	Power Supply (5 V ± 5%).
N/A[1]	14	N/A[1]	V_{CC}	Power Supply (5 V ± 5%). This pin is available on the 14-lead SOIC only.

[1] N/A indicates not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

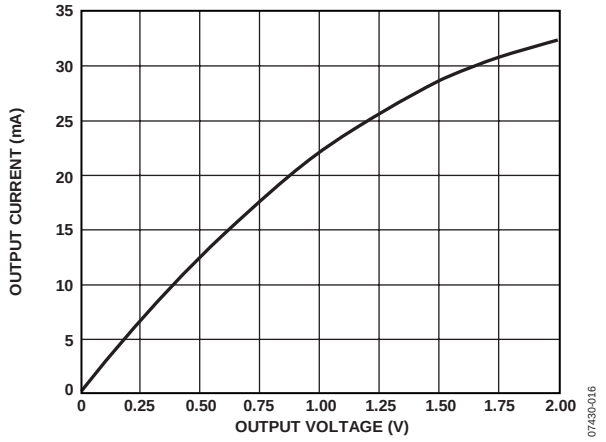


Figure 10. Output Current vs. Receiver Output Low Voltage

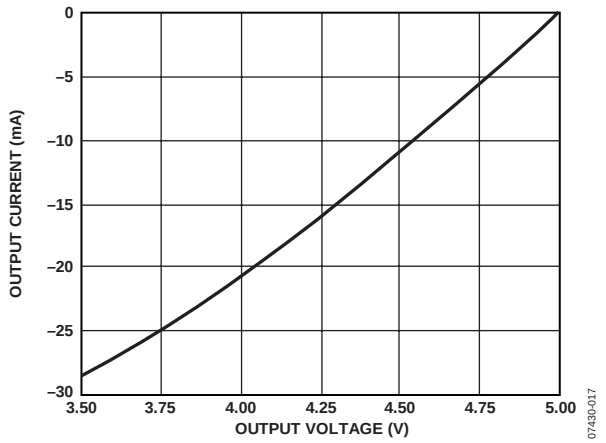


Figure 11. Output Current vs. Receiver Output High Voltage

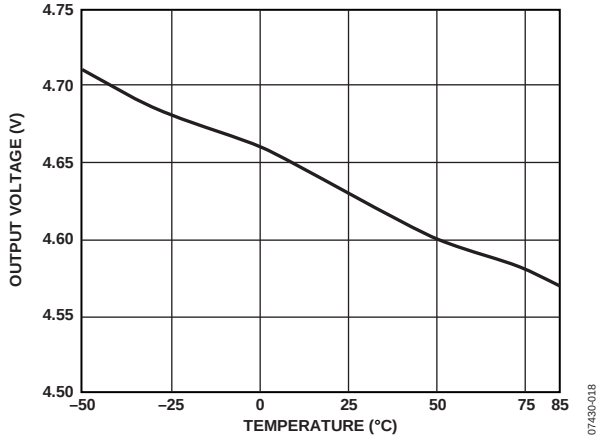


Figure 12. Receiver Output High Voltage vs. Temperature (I_{OUT} = 8 mA)

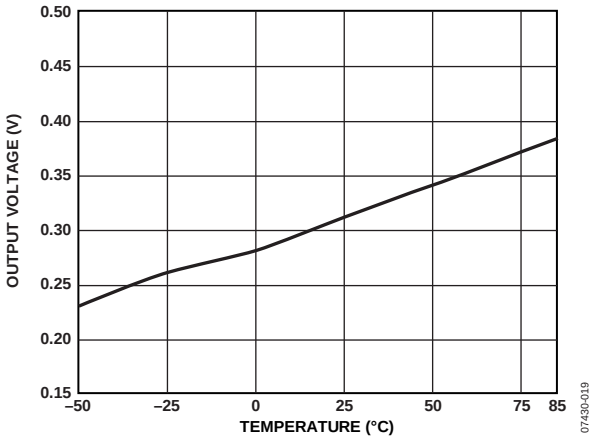


Figure 13. Receiver Output Low Voltage vs. Temperature (I_{OUT} = 8 mA)

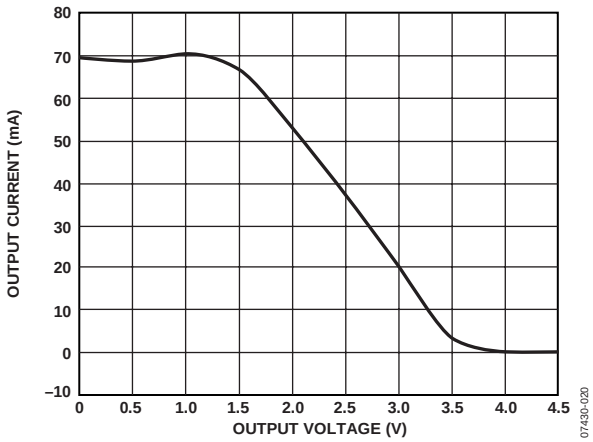


Figure 14. Output Current vs. Driver Differential Output Voltage

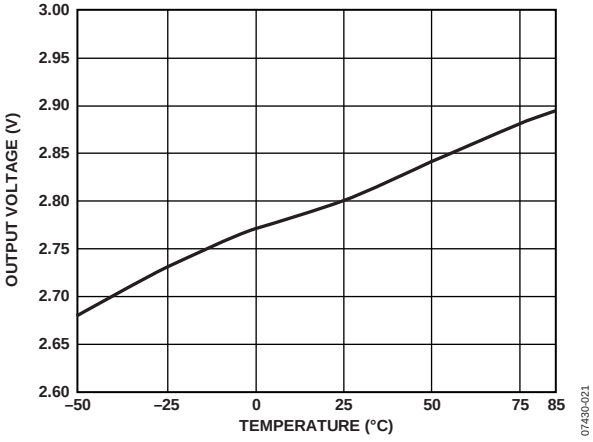


Figure 15. Driver Differential Output Voltage vs. Temperature (R_L = 56.3 Ω)

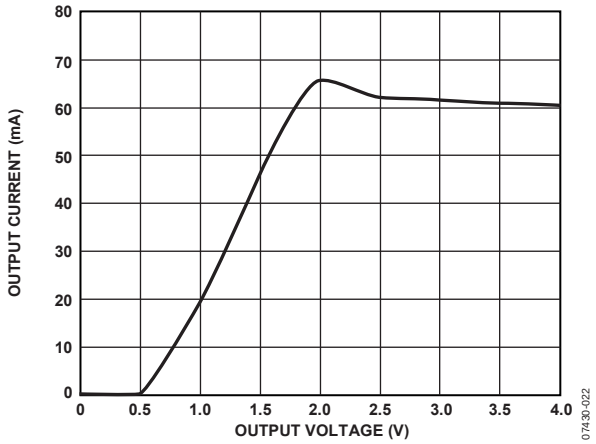


Figure 16. Output Current vs. Driver Output Low Voltage

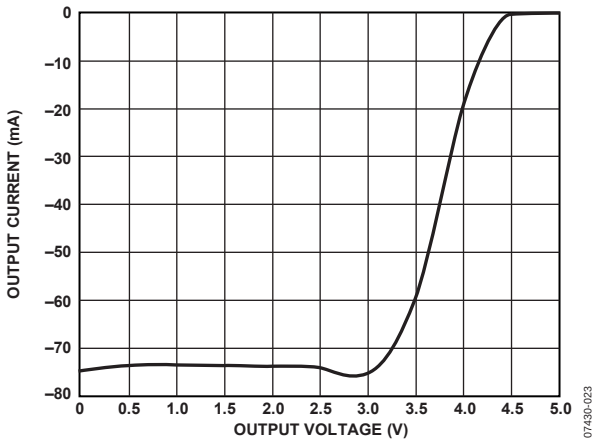


Figure 17. Output Current vs. Driver Output High Voltage

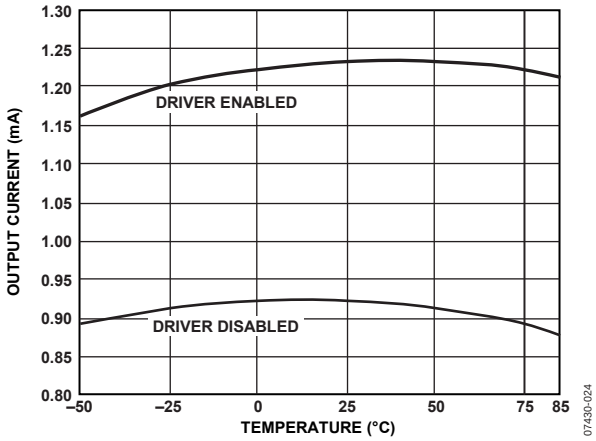


Figure 18. Output Current vs. Temperature

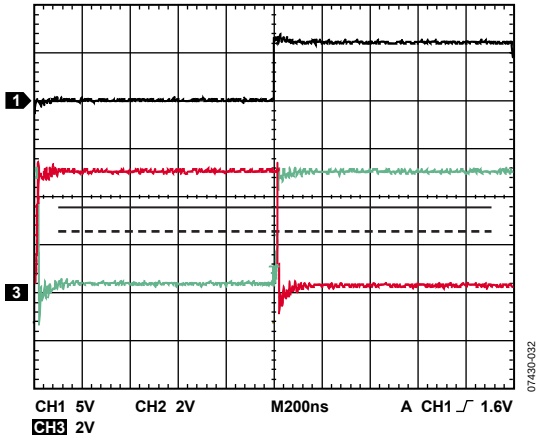


Figure 19. Unloaded Driver Differential Outputs

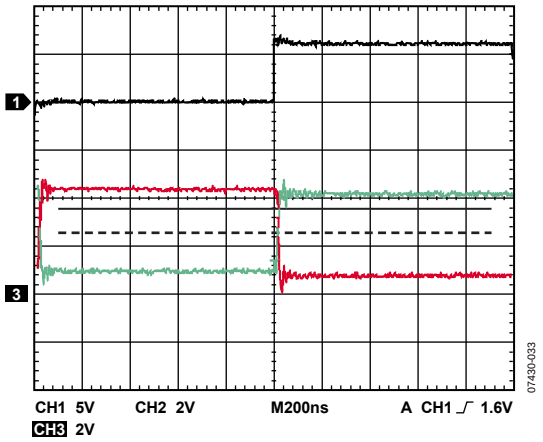


Figure 20. Loaded Driver Differential Outputs (R_L Differential = 54 Ω, C_L = 100 pF)

TEST CIRCUITS

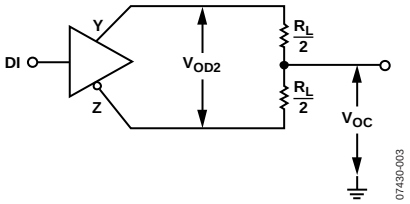


Figure 21. Driver Voltage Measurements

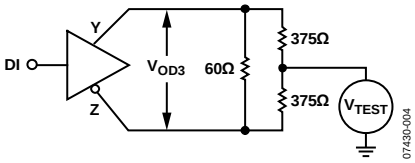


Figure 22. Driver Voltage Measurements

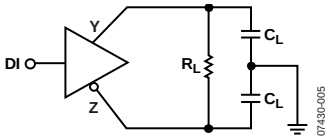


Figure 23. Driver Propagation Delay

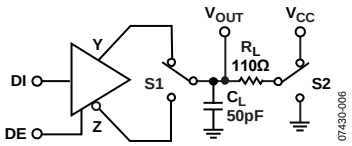


Figure 24. Driver Enable/Disable Timing

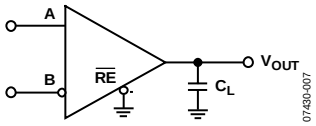


Figure 25. Receiver Propagation Delay

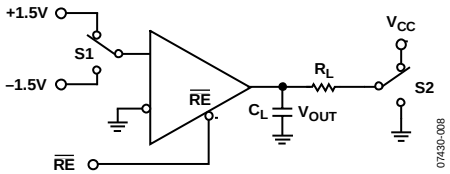


Figure 26. Receiver Enable/Disable Timing

THEORY OF OPERATION

The ADM1490E/ADM1491E are RS-422/RS-485 transceivers that operate from a single 5 V ± 5% power supply. The ADM1490E/ADM1491E are intended for balanced data transmission and comply with both TIA/EIA-485-A and TIA/EIA-422-B. Each device contains a differential line driver and a differential line receiver and is suitable for full-duplex data transmission.

The input impedance of the ADM1490E/ADM1491E is 12 kΩ, allowing up to 32 transceivers on the differential bus. A thermal shutdown circuit prevents excessive power dissipation caused by bus contention or by output shorting. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM1490E/ADM1491E feature very low propagation delay, ensuring maximum baud rate operation. The balanced driver ensures distortion-free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

TRUTH TABLES

Table 6. Abbreviations in Truth Tables

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Irrelevant
Z	High impedance (off)

Table 7. Transmitting

Inputs		Outputs	
DE	**DI**	**Z**	**Y**
H	H	L	H
H	L	H	L
L	X	Z	Z

Table 8. Receiving

Inputs		Output
$\overline{\text{RE}}$	**A – B**	**RO**
L	≥ +0.2 V	H
L	≤ −0.2 V	L
L	−0.2 V ≤ A − B ≤ +0.2 V	I
L	Inputs open	H
H	X	Z

ESD TRANSIENT PROTECTION SCHEME

The ADM1490E/ADM1491E use protective clamping structures on their inputs and outputs to clamp the voltage to a safe level and dissipate the energy present in ESD (electrostatic). The protection structure achieves ESD protection up to ±8 kV human body model (HBM).

ESD Testing

Two coupling methods are used for ESD testing: contact discharge and air gap discharge. Contact discharge calls for a direct connection to the unit being tested; air gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap; therefore, the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance, and rate of closure of the discharge gun. The contact discharge method, though less realistic, is more repeatable and is gaining acceptance and preference over the air gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately because of arcing or heating. Even if catastrophic failure does not occur immediately, the device can suffer from parametric degradation, resulting in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

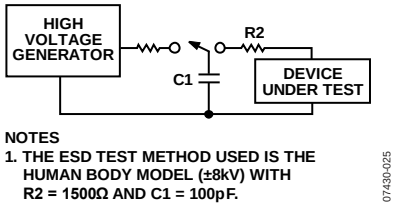


Figure 27. ESD Generator

I/O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I/O cable may result in a static discharge that can damage or destroy the interface product connected to the I/O port. It is, therefore, extremely important to have high levels of ESD protection on the I/O lines.

The ESD discharge can induce latch-up in the device under test. Therefore, it is important to conduct ESD testing on the I/O pins while power is applied to the device. This type of testing is more representative of a real-world I/O discharge in which the equipment is operating normally when the discharge occurs.

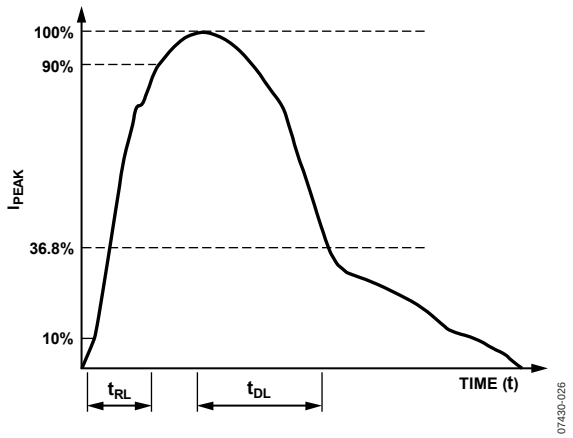


Figure 28. Human Body Model ESD Current Waveform

Table 9. ADM1490E/ADM1491E ESD Test Results

ESD Test Method	Input/Output Pins	Other Pins
Human Body Model	±8 kV	±4 kV

APPLICATIONS INFORMATION

DIFFERENTIAL DATA

Differential data transmission reliably transmits data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) that specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates of up to 10 MBaud and line lengths of up to 4000 feet. A single driver can drive a transmission line with as many as 10 receivers.

The RS-485 standard addresses true multipoint communications. This standard meets or exceeds all of the requirements of RS-422, and it allows as many as 32 drivers and 32 receivers to connect to a single bus. An extended common-mode range of −7 V to +12 V is defined. The most significant difference between the RS-422 and the RS-485 is that the drivers with RS-485 can be disabled, allowing more than one driver to be connected to a single line, with as many as 32 drivers connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

CABLE AND DATA RATE

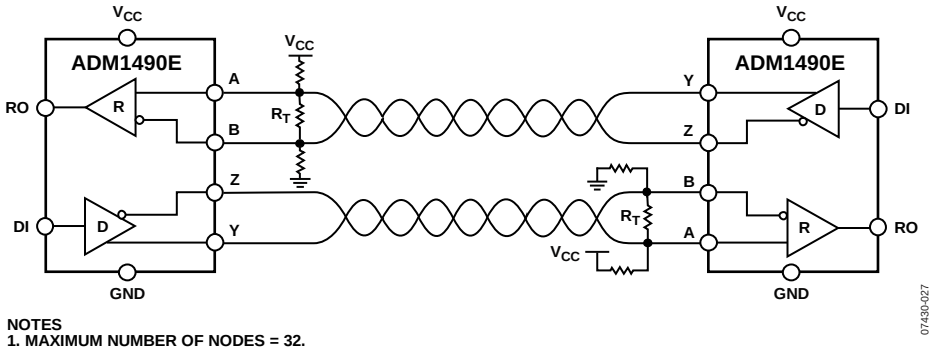
Twisted pair is the transmission line of choice for RS-485 communications. Twisted pair cable tends to cancel common-mode noise and causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important to minimize reflections. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Keep stub lengths of the main line as short as possible. A properly terminated transmission line appears purely resistive to the driver.

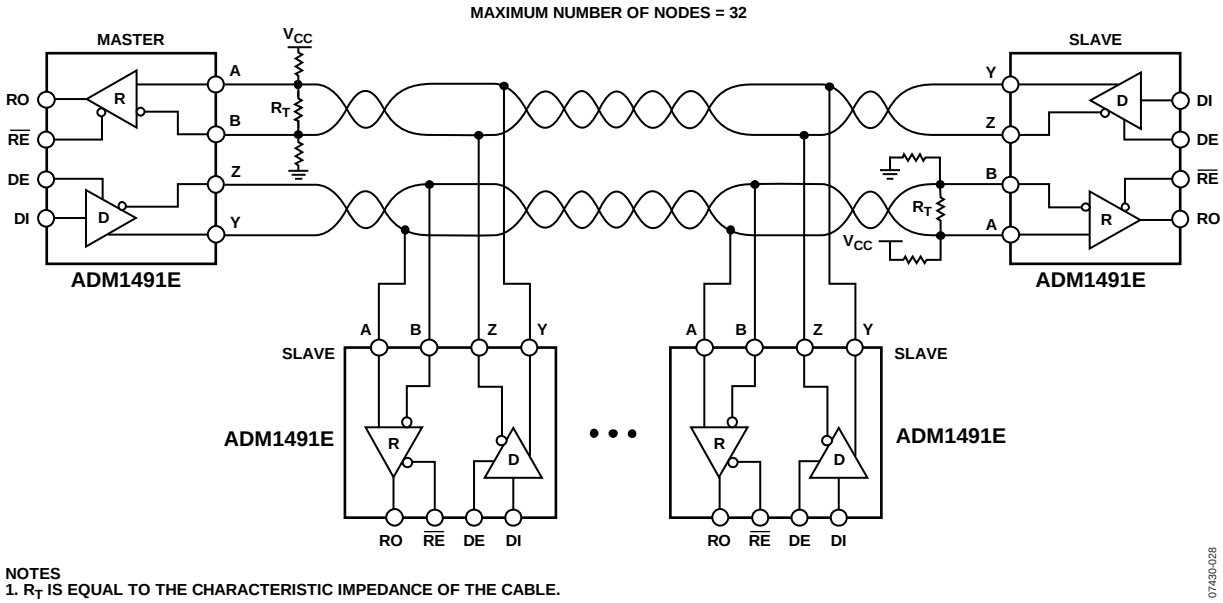
TYPICAL APPLICATIONS

Figure 29 shows a typical configuration for a full-duplex point-to-point application using the ADM1490E. Figure 30 shows a typical configuration for a full-duplex multipoint application using the ADM1491E. To minimize reflections, the lines must be terminated at the receiving end in its characteristic impedance, and stub lengths off the main line must be kept as short as possible.



NOTES
1. MAXIMUM NUMBER OF NODES = 32.

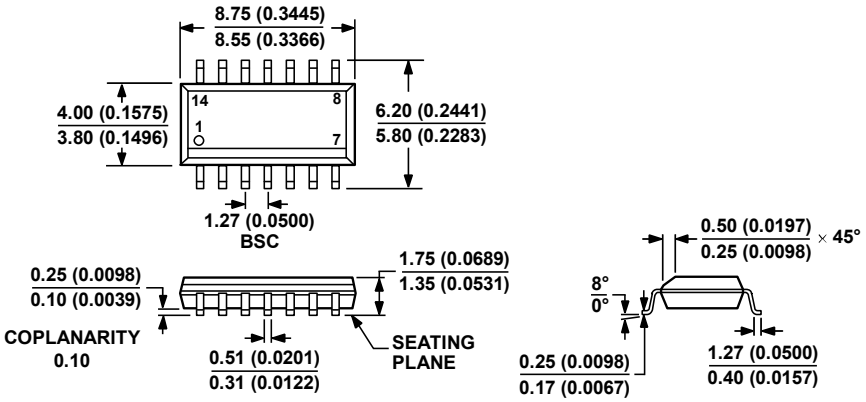
Figure 29. Typical Point-to-Point Full-Duplex Application



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE.

Figure 30. Typical RS-485 Full-Duplex Application

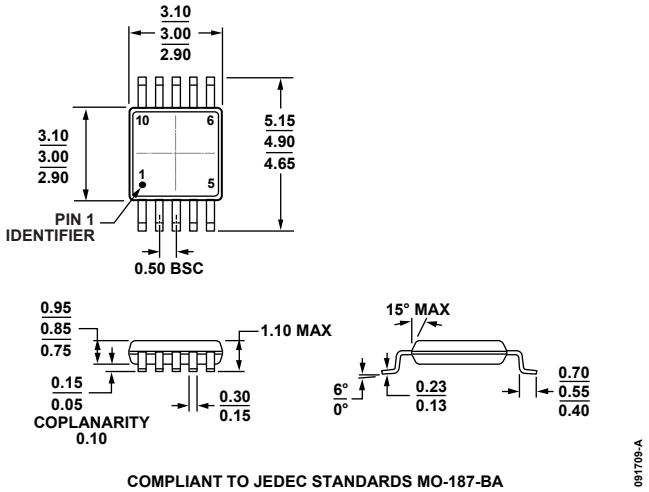
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 31. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-BA

091709-A

Figure 32. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

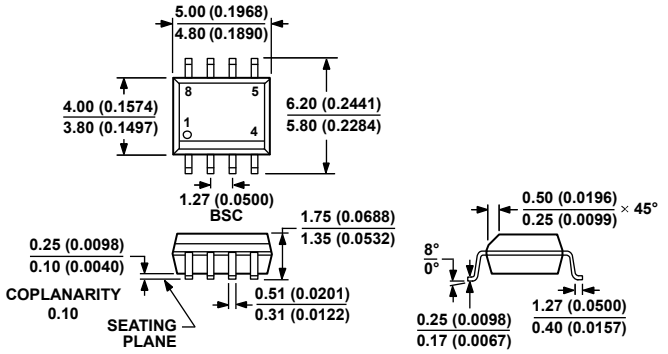


Figure 33. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

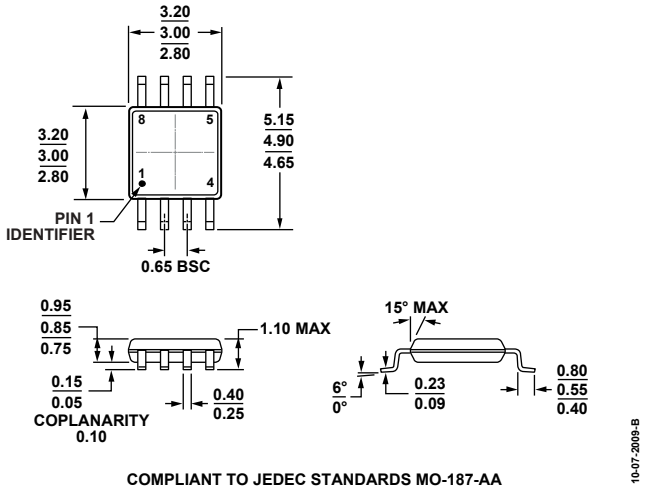


Figure 34. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADM1490EBRZ	−40°C to +85°C	8-Lead Standard Small Outline Package, Narrow Body [SOIC_N]	R-8	
ADM1490EBRZ-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package, Narrow Body [SOIC_N]	R-8	
ADM1490EBRMZ	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	F0E
ADM1490EBRMZ-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	F0E
ADM1491EBRZ	−40°C to +85°C	14-Lead Standard Small Outline Package, Narrow Body [SOIC_N]	R-14	
ADM1491EBRZ-REEL7	−40°C to +85°C	14-Lead Standard Small Outline Package, Narrow Body [SOIC_N]	R-14	
ADM1491EBRMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	F0D
ADM1491EBRMZ-REEL7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	F0D

[1] Z = RoHS Compliant Part.

NOTES

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D07430-0-2/12(D)

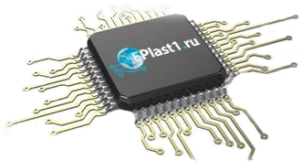
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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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