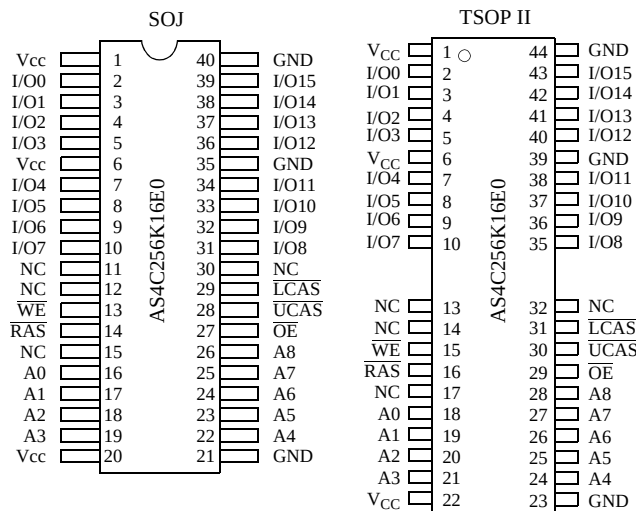


**5V 256K×16 CMOS DRAM (EDO)****Features**

- Organization: 262,144 words × 16 bits
- High speed
  - 30/35/50 ns  $\overline{\text{RAS}}$  access time
  - 16/18/25 ns column address access time
  - 7/10/10/10 ns  $\overline{\text{CAS}}$  access time
- Low power consumption
  - Active: 500 mW max (AS4C256K16E0-25)
  - Standby: 3.6 mW max, CMOS I/O (AS4C256K16E0-25)
- EDO page mode

- Refresh
  - 512 refresh cycles, 8 ms refresh interval
  - $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh or self-refresh
  - Self-refresh option is available for new generation device only. Contact Alliance for more information.
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil, 40-pin SOJ
  - 400 mil, 40/44-pin TSOP II
- 5V power supply
- Latch-up current > 200 mA

**Pin arrangement****Pin designation**

| Pin(s)                   | Description                       |
|--------------------------|-----------------------------------|
| A0 to A8                 | Address inputs                    |
| $\overline{\text{RAS}}$  | Row address strobe                |
| I/O0 to I/O15            | Input/output                      |
| $\overline{\text{OE}}$   | Output enable                     |
| $\overline{\text{UCAS}}$ | Column address strobe, upper byte |
| $\overline{\text{LCAS}}$ | Column address strobe, lower byte |
| $\overline{\text{WE}}$   | Read/write control                |
| V <sub>CC</sub>          | Power (5V ± 0.5V)                 |
| GND                      | Ground                            |

**Selection guide**

|                                                              | Symbol           | AS4C256K16E0-30 | AS4C256K16E0-35 | AS4C256K16E0-50 | Unit |
|--------------------------------------------------------------|------------------|-----------------|-----------------|-----------------|------|
| Maximum $\overline{\text{RAS}}$ access time                  | t <sub>RAC</sub> | 30              | 35              | 50              | ns   |
| Maximum column address access time                           | t <sub>CAA</sub> | 16              | 18              | 25              | ns   |
| Maximum $\overline{\text{CAS}}$ access time                  | t <sub>CAC</sub> | 10              | 10              | 10              | ns   |
| Maximum output enable ( $\overline{\text{OE}}$ ) access time | t <sub>OEA</sub> | 10              | 10              | 10              | ns   |
| Minimum read or write cycle time                             | t <sub>RC</sub>  | 65              | 70              | 85              | ns   |
| Minimum EDO page mode cycle time                             | t <sub>PC</sub>  | 12              | 14              | 25              | ns   |
| Maximum operating current                                    | I <sub>CC1</sub> | 180             | 160             | 140             | mA   |
| Maximum CMOS standby current                                 | I <sub>CC2</sub> | 2.0             | 2.0             | 2.0             | mA   |

Shaded areas contain advance information.



Functional description

The AS4C256K16E0 is a high performance 4 megabit CMOS Dynamic Random Access Memory (DRAM) organized as 262,144 words by 16 bits. The AS4C256K16E0 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

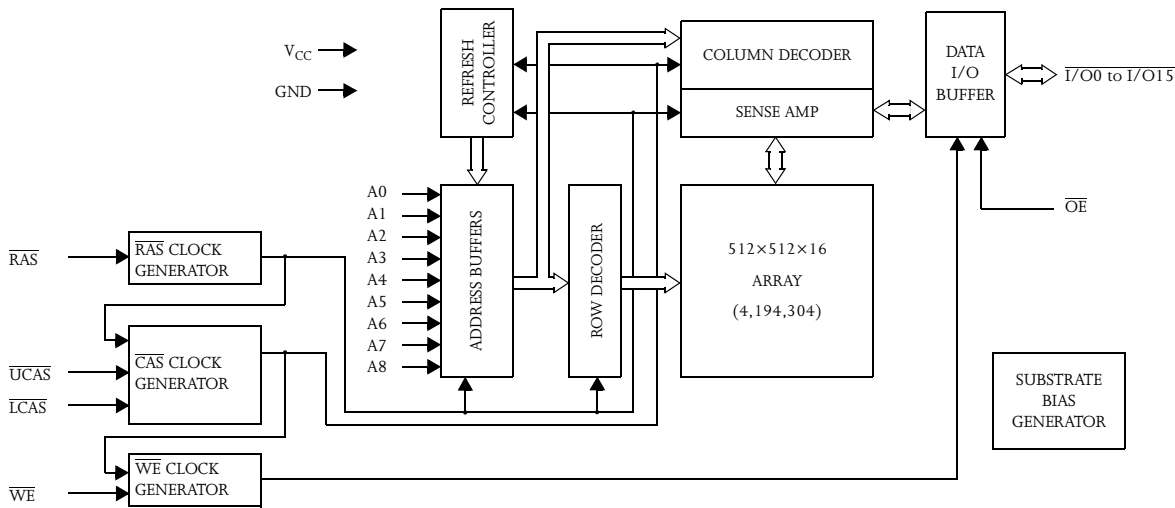
The AS4C256K16E0 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 512 × 16 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Very fast  $\overline{\text{CAS}}$  to output access time eases system design.

Refresh on the 512 address combinations of A0 to A8 during an 8 ms period is accomplished by performing any of the following:

- $\overline{\text{RAS}}$ -only refresh cycles
- Hidden refresh cycles
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles
- Normal read or write cycles
- Self-refresh cycles\*

The AS4C256K16E0 is available in standard 40-pin plastic SOJ and 40/44-pin TSOP II packages compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ± 0.5V tolerance and direct interface with TTL logic families.

Logic block diagram



Recommended operating conditions

|                |                 |      |     | (T <sub>a</sub> = 0°C to +70°C) |      |
|----------------|-----------------|------|-----|---------------------------------|------|
| Parameter      | Symbol          | Min  | Typ | Max                             | Unit |
| Supply voltage | V <sub>CC</sub> | 4.5  | 5.0 | 5.5                             | V    |
|                | GND             | 0.0  | 0.0 | 0.0                             | V    |
| Input voltage  | V <sub>IH</sub> | 2.4  | —   | V <sub>CC</sub> + 1             | V    |
|                | V <sub>IL</sub> | −1.0 | —   | 0.8                             | V    |

\*Self-refresh option is available for new generation device only. Contact Alliance for more information.



## Absolute maximum ratings

| Parameter                     | Symbol       | Min  | Max             | Unit     |
|-------------------------------|--------------|------|-----------------|----------|
| Input voltage                 | $V_{in}$     | -1.0 | +7.0            | V        |
| Output voltage                | $V_{out}$    | -1.0 | +7.0            | V        |
| Power supply voltage          | $V_{CC}$     | -1.0 | +7.0            | V        |
| Operating temperature         | $T_{OPR}$    | 0    | +70             | °C       |
| Storage temperature (plastic) | $T_{STG}$    | -55  | +150            | °C       |
| Soldering temperature × time  | $T_{SOLDER}$ | —    | $260 \times 10$ | °C × sec |
| Power dissipation             | $P_D$        | —    | 1               | W        |
| Short circuit output current  | $I_{out}$    | —    | 50              | mA       |
| Latch-up current              |              | 200  | —               | mA       |

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC electrical characteristics

| Parameter                                                               | Symbol    | Test conditions                                                                                                                                                               | -30 |     | -35 |     | -50 |     | Unit | Note |
|-------------------------------------------------------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|------|
|                                                                         |           |                                                                                                                                                                               | Min | Max | Min | Max | Min | Max |      |      |
| Input leakage current                                                   | $I_{IL}$  | $0V \leq V_{in} \leq +5.5V$<br>pins not under test = 0V                                                                                                                       | -10 | 10  | -10 | 10  | -10 | 10  | μA   |      |
| Output leakage current                                                  | $I_{OL}$  | $D_{OUT}$ disabled,<br>$0V \leq V_{out} \leq +5.5V$                                                                                                                           | -10 | 10  | -10 | 10  | -10 | 10  | μA   |      |
| Operating power supply current                                          | $I_{CC1}$ | $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , address cycling;<br>$t_{RC} = \min$                                                                                | —   | 180 | —   | 160 | —   | 140 | mA   | 1,2  |
| TTL standby power supply current                                        | $I_{CC2}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IH}$                                                                                                                 | —   | 2.0 | —   | 2.0 | —   | 2.0 | mA   |      |
| Average power supply current, $\overline{RAS}$ refresh mode             | $I_{CC3}$ | $\overline{RAS}$ cycling,<br>$\overline{UCAS} = \overline{LCAS} = V_{IH}$ ,<br>$t_{RC} = \min$                                                                                | —   | 200 | —   | 190 | —   | 140 | mA   | 1    |
| EDO page mode average power supply current                              | $I_{CC4}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IL}$ ,<br>address cycling: $t_{SC} = \min$                                                                           | —   | 190 | —   | 180 | —   | 70  | mA   | 1,2  |
| CMOS standby power supply current                                       | $I_{CC5}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{CC} - 0.2V$                                                                                                          | —   | 1.0 | —   | 1.0 | —   | 1.0 | mA   |      |
| $\overline{CAS}$ -before- $\overline{RAS}$ refresh power supply current | $I_{CC6}$ | $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{LCAS}$ , cycling;<br>$t_{RC} = \min$                                                                                        | —   | 200 | —   | 190 | —   | 140 | mA   | 1    |
| Output Voltage                                                          | $V_{OH}$  | $I_{OUT} = -5.0 \text{ mA}$                                                                                                                                                   | 2.4 | —   | 2.4 | —   | 2.4 | —   | V    |      |
|                                                                         | $V_{OL}$  | $I_{OUT} = 4.2 \text{ mA}$                                                                                                                                                    | —   | 0.4 | —   | 0.4 | —   | 0.4 | V    |      |
| Self refresh current                                                    | $I_{CC7}$ | $\overline{RAS} = \overline{UCAS} = \overline{LCAS} = V_{IL}$ ,<br>$\overline{WE} = \overline{OE} = A0-A8 = V_{CC} - 0.2V$ ,<br>$DQ0-DQ15 = V_{CC} - 0.2V$ ,<br>0.2V are open | —   | 2.0 | —   | 2.0 | —   | 2.0 | mA   |      |

Shaded areas contain advance information.



## AC parameters common to all waveforms

| Std<br>Symbol | Parameter                                                   | -30 |     | -35 |     | -50 |     | Unit | Notes |
|---------------|-------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|               |                                                             | Min | Max | Min | Max | Min | Max |      |       |
| $t_{RC}$      | Random read or write cycle time                             | 65  | —   | 70  | —   | 85  | —   | ns   |       |
| $t_{RP}$      | $\overline{RAS}$ precharge time                             | 25  | —   | 25  | —   | 25  | —   | ns   |       |
| $t_{RAS}$     | $\overline{RAS}$ pulse width                                | 30  | 75K | 35  | 75K | 50  | 75K | ns   |       |
| $t_{CAS}$     | $\overline{CAS}$ pulse width                                | 5   | —   | 6   | —   | 10  | —   | ns   |       |
| $t_{RCD}$     | $\overline{RAS}$ to $\overline{CAS}$ delay time             | 15  | 20  | 16  | 24  | 15  | 35  | ns   | 6     |
| $t_{RAD}$     | $\overline{RAS}$ to column address delay time               | 10  | 14  | 11  | 17  | 15  | 25  | ns   | 7     |
| $t_{RSH(R)}$  | $\overline{CAS}$ to $\overline{RAS}$ hold time (read cycle) | 10  | —   | 10  | —   | 10  | —   | ns   |       |
| $t_{CSH}$     | $\overline{RAS}$ to $\overline{CAS}$ hold time              | 30  | —   | 35  | —   | 50  | —   | ns   |       |
| $t_{CRP}$     | $\overline{CAS}$ to $\overline{RAS}$ precharge time         | 5   | —   | 5   | —   | 5   | —   | ns   |       |
| $t_{ASR}$     | Row address setup time                                      | 0   | —   | 0   | —   | 0   | —   | ns   |       |
| $t_{RAH}$     | Row address hold time                                       | 5   | —   | 6   | —   | 9   | —   | ns   |       |
| $t_T$         | Transition time (rise and fall)                             | 1.5 | 50  | 1.5 | 50  | 3   | 50  | ns   | 4,5   |
| $t_{REF}$     | Refresh period                                              | —   | 8   | —   | 8   | —   | 8   | ms   | 3     |
| $t_{CLZ}$     | $\overline{CAS}$ to output in low Z                         | 0   | —   | 0   | —   | 3   | —   | ns   | 8     |

Shaded areas contain advance information.

## Read cycle

| Std<br>Symbol | Parameter                                    | -30 |     | -35 |     | -50 |     | Unit | Notes |
|---------------|----------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|               |                                              | Min | Max | Min | Max | Min | Max |      |       |
| $t_{RAC}$     | Access time from $\overline{RAS}$            | —   | 30  | —   | 35  | —   | 50  | ns   | 6     |
| $t_{CAC}$     | Access time from $\overline{CAS}$            | —   | 10  | —   | 10  | —   | 10  | ns   | 6,13  |
| $t_{AA}$      | Access time from address                     | —   | 16  | —   | 18  | —   | 25  | ns   | 7,13  |
| $t_{AR(R)}$   | Column add hold from $\overline{RAS}$        | 26  | —   | 28  | —   | 30  | —   | ns   |       |
| $t_{RCS}$     | Read command setup time                      | 0   | —   | 0   | —   | 0   | —   | ns   |       |
| $t_{RCH}$     | Read command hold time to $\overline{CAS}$   | 0   | —   | 0   | —   | 0   | —   | ns   | 9     |
| $t_{RRH}$     | Read command hold time to $\overline{RAS}$   | 0   | —   | 0   | —   | 0   | —   | ns   | 9     |
| $t_{RAL}$     | Column address to $\overline{RAS}$ Lead time | 16  | —   | 18  | —   | 25  | —   | ns   |       |
| $t_{CPN}$     | $\overline{CAS}$ precharge time              | 3   | —   | 4   | —   | 5   | —   | ns   |       |
| $t_{OFF}$     | Output buffer turn-off time                  | 0   | 8   | 0   | 8   | 0   | 8   | ns   | 8,10  |

Shaded areas contain advance information.



## Write cycle

| Std<br>Symbol | Parameter                                    | -30 |     | -35 |     | -50 |     | Unit | Notes |
|---------------|----------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|               |                                              | Min | Max | Min | Max | Min | Max |      |       |
| $t_{ASC}$     | Column address setup time                    | 0   | —   | 0   | —   | 0   | —   | ns   |       |
| $t_{CAH}$     | Column address hold time                     | 5   | —   | 5   | —   | 9   | —   | ns   |       |
| $t_{AWR}$     | Column address hold time to $\overline{RAS}$ | 26  | —   | 28  | —   | 30  | —   | ns   |       |
| $t_{WCS}$     | Write command setup time                     | 0   | —   | 0   | —   | 0   | —   | ns   | 11    |
| $t_{WCH}$     | Write command hold time                      | 5   | —   | 5   | —   | 9   | —   | ns   | 11    |
| $t_{WCR}$     | Write command hold time to $\overline{RAS}$  | 26  | —   | 28  | —   | 30  | —   | ns   |       |
| $t_{WP}$      | Write command pulse width                    | 5   | —   | 5   | —   | 9   | —   | ns   |       |
| $t_{RWL}$     | Write command to $\overline{RAS}$ lead time  | 10  | —   | 11  | —   | 12  | —   | ns   |       |
| $t_{CWL}$     | Write command to $\overline{CAS}$ lead time  | 10  | —   | 11  | —   | 12  | —   | ns   |       |
| $t_{DS}$      | Data-in setup time                           | 0   | —   | 0   | —   | 0   | —   | ns   | 12    |
| $t_{DH}$      | Data-in hold time                            | 5   | —   | 5   | —   | 9   | —   | ns   | 12    |
| $t_{DHR}$     | Data-in hold time to $\overline{RAS}$        | 26  | —   | 28  | —   | 30  | —   | ns   |       |

Shaded areas contain advance information.

## Read-modify-write cycle

| Std<br>Symbol | Parameter                                              | -30 |     | -35 |     | -50 |     | Unit | Notes |
|---------------|--------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|               |                                                        | Min | Max | Min | Max | Min | Max |      |       |
| $t_{RWC}$     | Read-write cycle time                                  | 100 | —   | 105 | —   | 120 | —   | ns   |       |
| $t_{RWD}$     | $\overline{RAS}$ to $\overline{WE}$ delay time         | 50  | —   | 54  | —   | 60  | —   | ns   | 11    |
| $t_{CWD}$     | $\overline{CAS}$ to $\overline{WE}$ delay time         | 26  | —   | 28  | —   | 30  | —   | ns   | 11    |
| $t_{AWD}$     | Column address to $\overline{WE}$ delay time           | 32  | —   | 35  | —   | 40  | —   | ns   | 11    |
| $t_{RSH(W)}$  | $\overline{CAS}$ to $\overline{RAS}$ hold time (write) | 10  | —   | 10  | —   | 12  | —   | ns   |       |
| $t_{CAS(W)}$  | $\overline{CAS}$ pulse width (write)                   | 15  | —   | 15  | —   | 15  | —   | ns   |       |

Shaded areas contain advance information.



## EDO page mode cycle

| Std<br>Symbol     | Parameter                                           | -30 |     | -35 |     | -50 |     | Unit | Notes |
|-------------------|-----------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|                   |                                                     | Min | Max | Min | Max | Min | Max |      |       |
| t <sub>PC</sub>   | Read or write cycle time                            | 12  | —   | 14  | —   | 25  | —   | ns   | 14    |
| t <sub>CAP</sub>  | Access time from $\overline{\text{CAS}}$ precharge  | —   | 19  | —   | 21  | —   | 23  | ns   | 13    |
| t <sub>CP</sub>   | $\overline{\text{CAS}}$ precharge time              | 3   | —   | 4   | —   | 5   | —   | ns   |       |
| t <sub>PCM</sub>  | EDO page mode RMW cycle                             | 56  | —   | 58  | —   | 60  | —   | ns   |       |
| t <sub>CRW</sub>  | Page mode $\overline{\text{CAS}}$ pulse width (RMW) | 44  | —   | 46  | —   | 50  | —   | ns   |       |
| t <sub>RASP</sub> | $\overline{\text{RAS}}$ pulse width                 | 30  | 75K | 35  | 75K | 50  | 75K | ns   |       |

Shaded areas contain advance information.

## Refresh cycle

| Std<br>Symbol    | Parameter                                                                                                          | -30 |     | -35 |     | -50 |     | Unit | Notes |
|------------------|--------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|                  |                                                                                                                    | Min | Max | Min | Max | Min | Max |      |       |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ setup time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )                    | 10  | —   | 10  | —   | 10  | —   | ns   | 3     |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ )                     | 7   | —   | 8   | —   | 10  | —   | ns   | 3     |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time                                             | 0   | —   | 0   | —   | 0   | —   | ns   |       |
| t <sub>CPT</sub> | $\overline{\text{CAS}}$ precharge time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test) | 8   | —   | 8   | —   | 8   | —   | ns   |       |

Shaded areas contain advance information.

## Output enable

| Std<br>Symbol    | Parameter                                                              | -30 |     | -35 |     | -50 |     | Unit | Notes |
|------------------|------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|------|-------|
|                  |                                                                        | Min | Max | Min | Max | Min | Max |      |       |
| t <sub>ROH</sub> | $\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$ | 5   | —   | 5   | —   | 5   | —   | ns   |       |
| t <sub>OEA</sub> | $\overline{\text{OE}}$ access time                                     | —   | 10  | —   | 10  | —   | 10  | ns   |       |
| t <sub>OED</sub> | $\overline{\text{OE}}$ to data delay                                   | 5   | —   | 5   | —   | 8   | —   | ns   |       |
| t <sub>OEZ</sub> | Output buffer turnoff delay from $\overline{\text{OE}}$                | —   | 8   | —   | 8   | —   | 8   | ns   | 8     |
| t <sub>OEH</sub> | $\overline{\text{OE}}$ command hold time                               | 8   | —   | 8   | —   | 8   | —   | ns   |       |

Shaded areas contain advance information.

## Self refresh cycle

| Std<br>Symbol     | Parameter                                                    | -30  |     | -35  |     | -50  |     | Unit | Notes |
|-------------------|--------------------------------------------------------------|------|-----|------|-----|------|-----|------|-------|
|                   |                                                              | Min  | Max | Min  | Max | Min  | Max |      |       |
| t <sub>RASS</sub> | $\overline{\text{RAS}}$ pulse width<br>(CBR self refresh)    | 100K | —   | 100K | —   | 100K | —   | ns   |       |
| t <sub>RPS</sub>  | $\overline{\text{RAS}}$ precharge time<br>(CBR self refresh) | 85   | —   | 85   | —   | 85   | —   | ns   |       |
| t <sub>CHS</sub>  | $\overline{\text{CAS}}$ hold time<br>(CBR self refresh)      | 30   | —   | 30   | —   | 30   | —   | ns   |       |

Shaded areas contain advance information.



## Notes

- 1  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  depend on cycle rate.
- 2  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- 3 An initial pause of 200  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- 4 AC Characteristics assume  $t_T = 5$  ns. All AC parameters are measured with a load equivalent to two TTL loads and 60 pF,  $V_{IL}(\text{min}) \geq \text{GND}$  and  $V_{IH}(\text{max}) \leq V_{CC}$ .
- 5  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 6 Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
- 7 Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
- 8 Assumes three state test load (5 pF and a 380  $\Omega$  Thevenin equivalent).
- 9 Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
- 10  $t_{\text{OFF}}(\text{max})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
- 11  $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If  $t_{\text{WS}} \geq t_{\text{WS}}(\text{min})$  and  $t_{\text{WH}} \geq t_{\text{WH}}(\text{min})$ , the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- 12 These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in read-write cycles.
- 13 Access time is determined by the longest of  $t_{\text{CAA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{CAP}}$
- 14  $t_{\text{ASC}} \geq t_{\text{CP}}$  to achieve  $t_{\text{PC}}(\text{min})$  and  $t_{\text{CAP}}(\text{max})$  values.
- 15 These parameters are sampled and not 100% tested.

## Key to switching waveform



Undefined/don't care

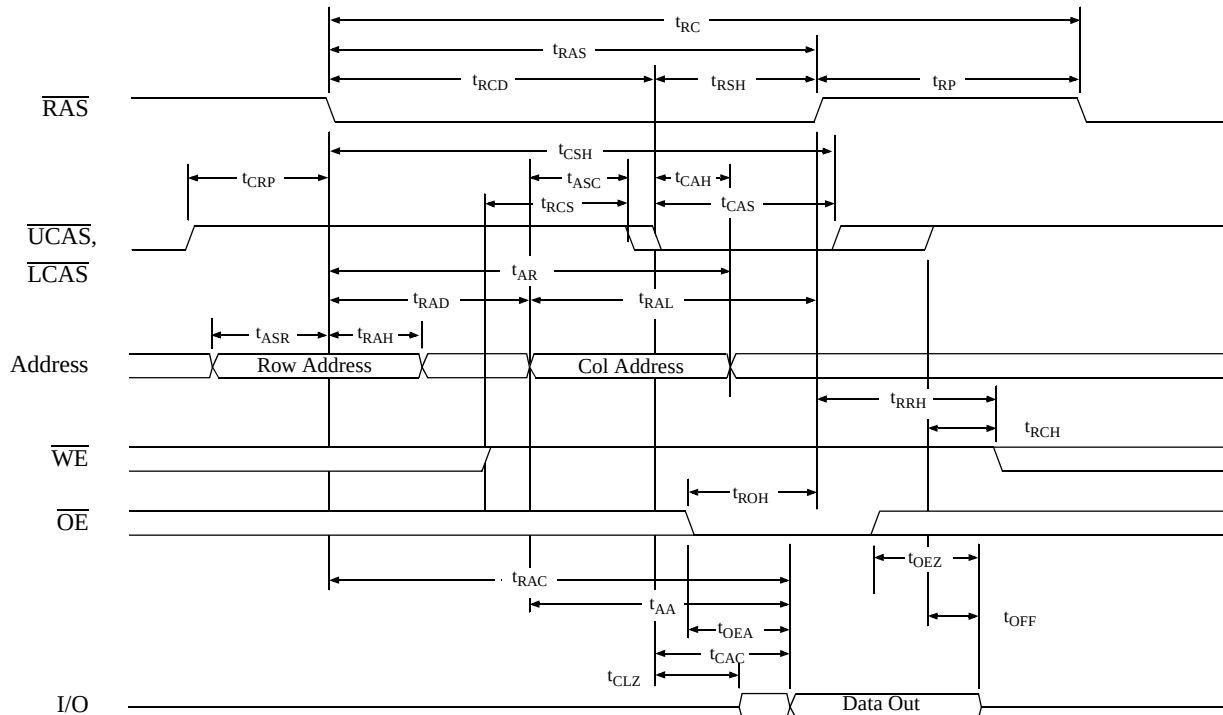


Rising input



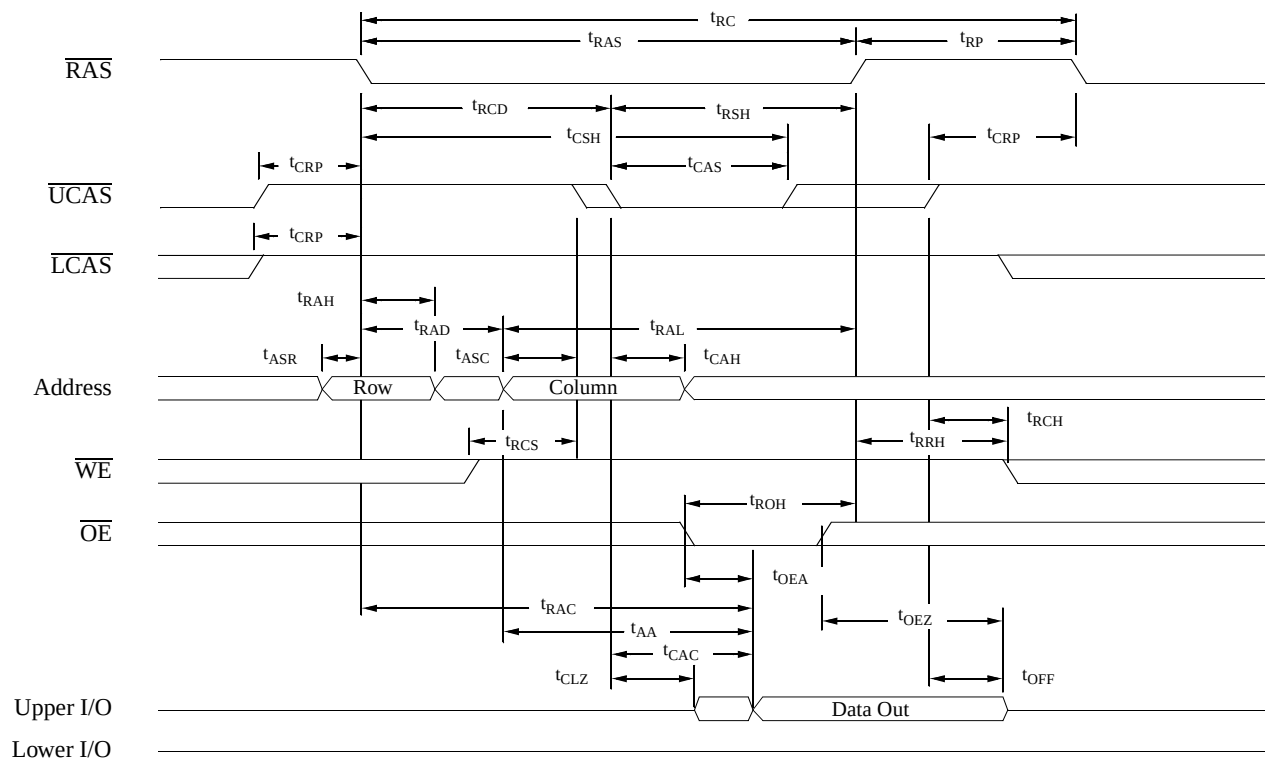
Falling input

## Read cycle waveform

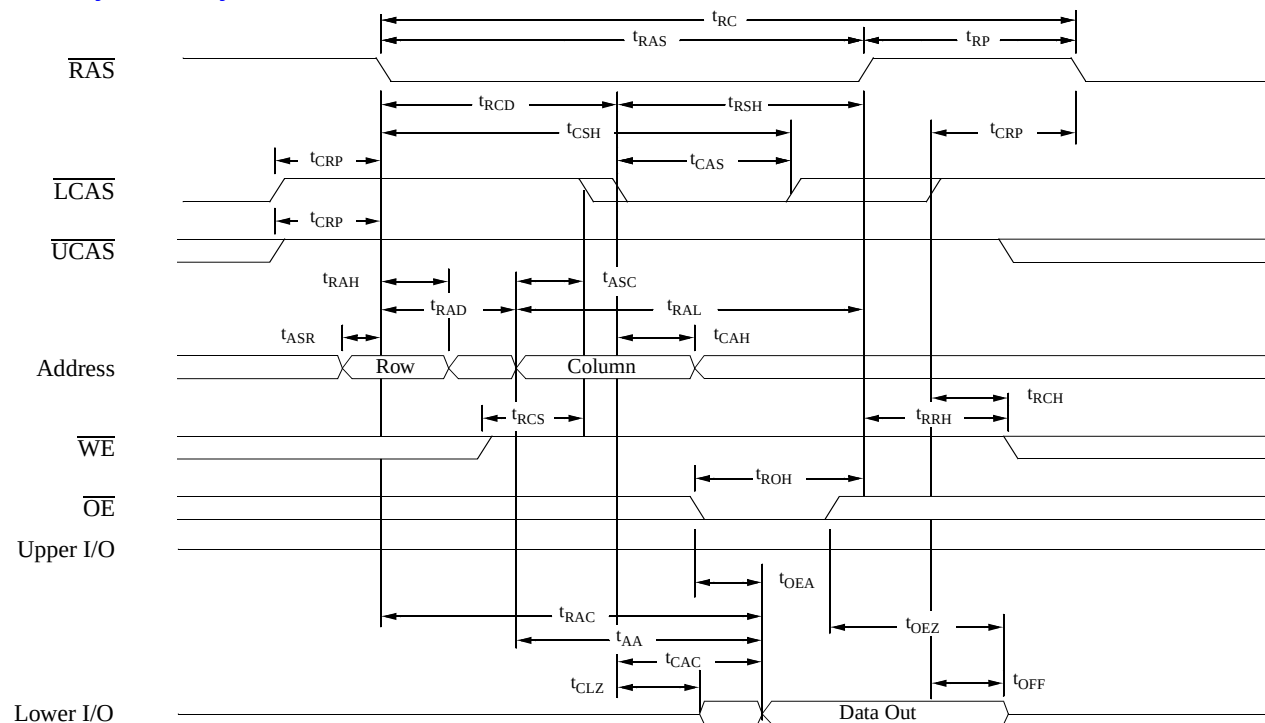




### Upper byte read cycle waveform



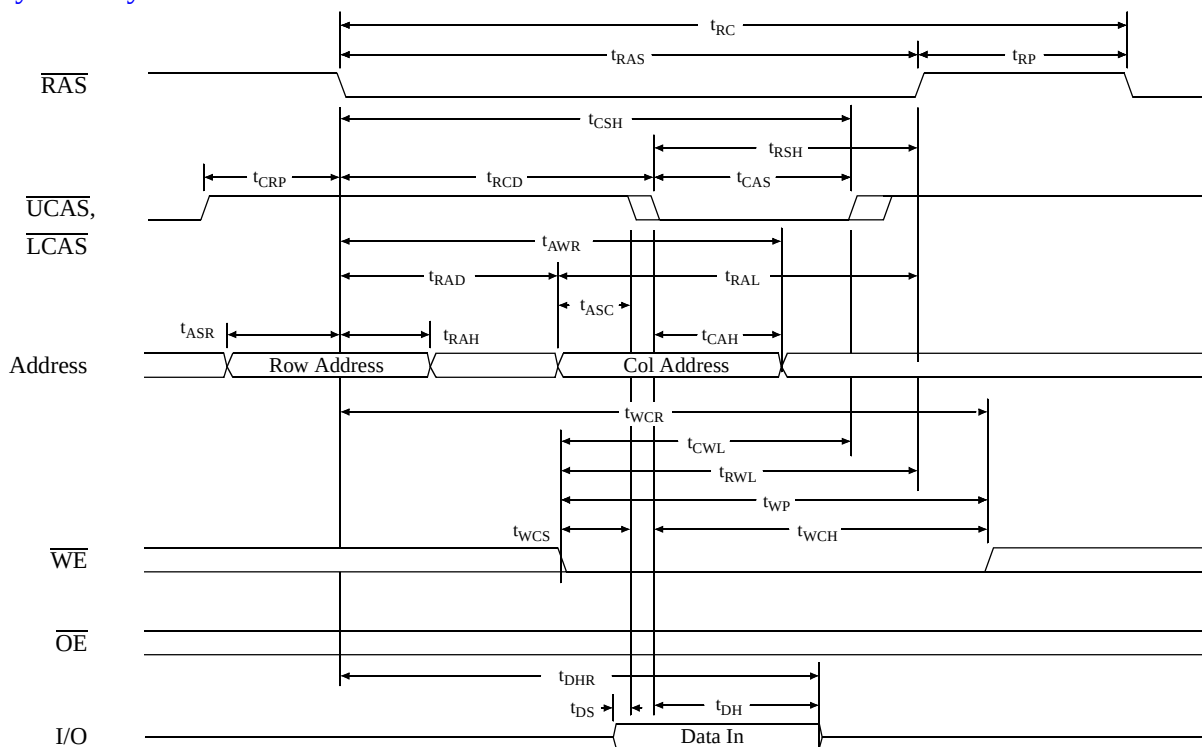
### Lower byte read cycle waveform



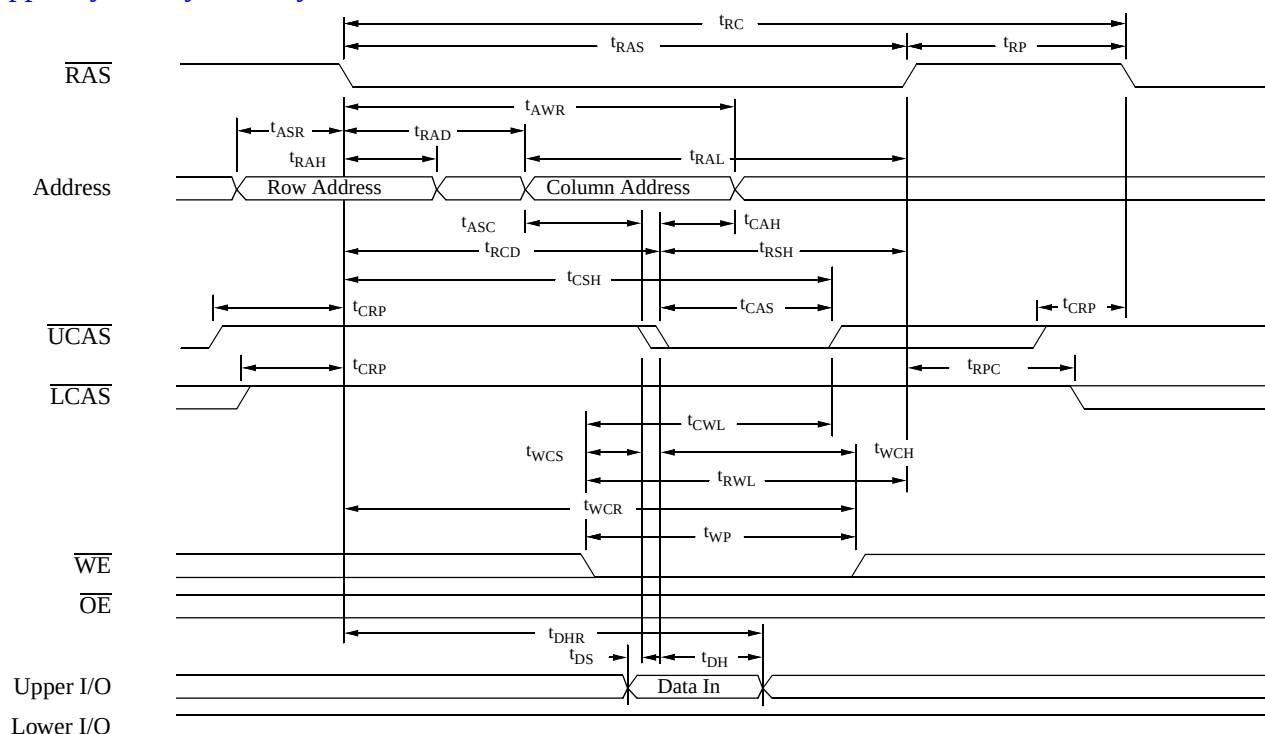




### Early write cycle waveform

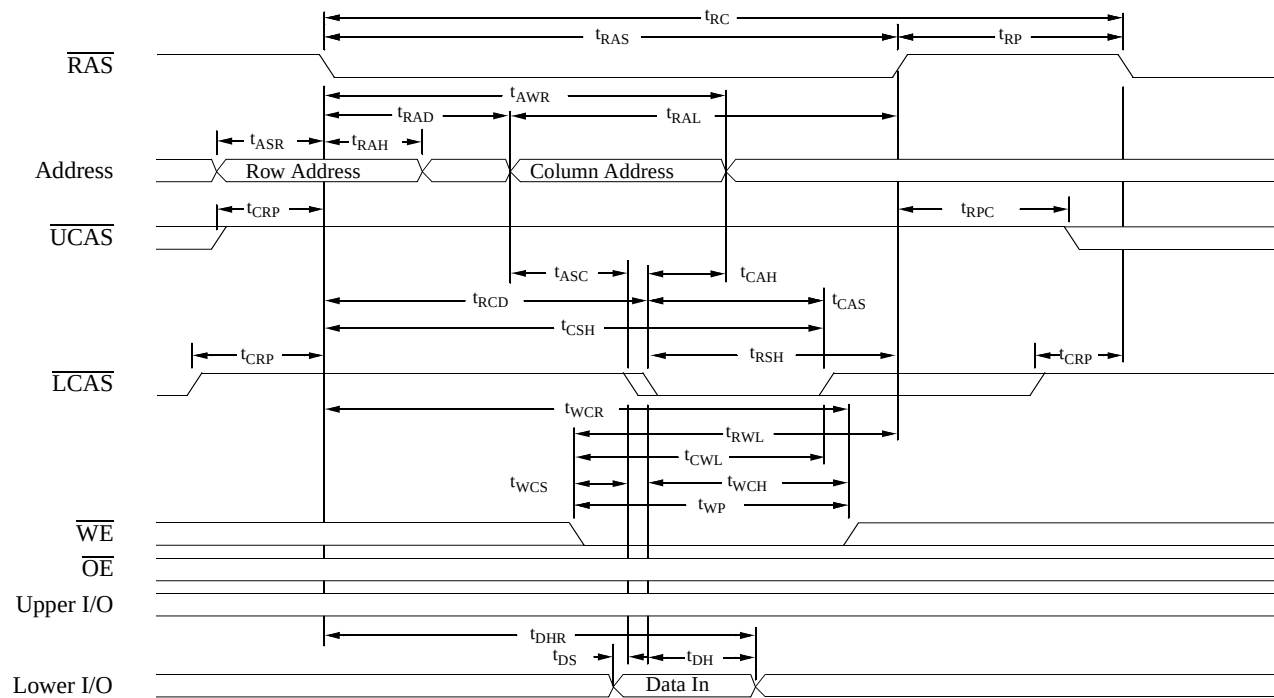


### Upper byte early write cycle waveform

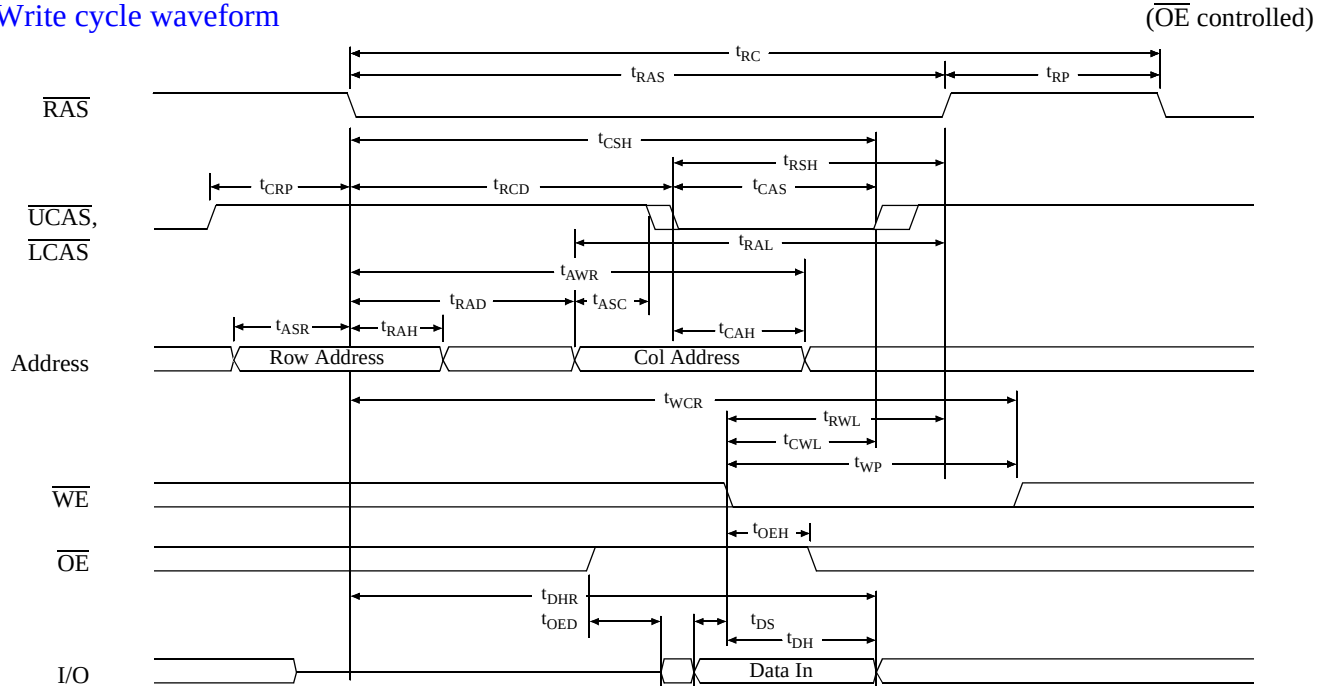




### Lower byte early write cycle waveform

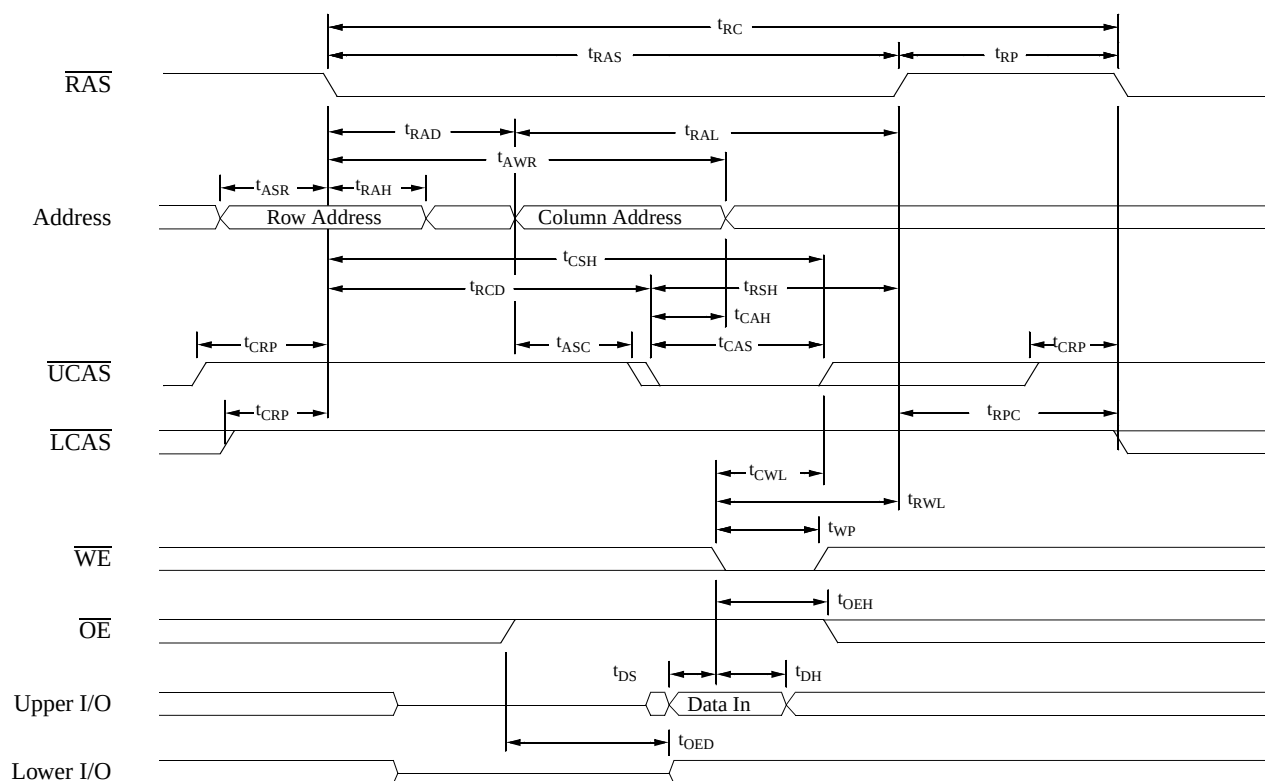


### Write cycle waveform

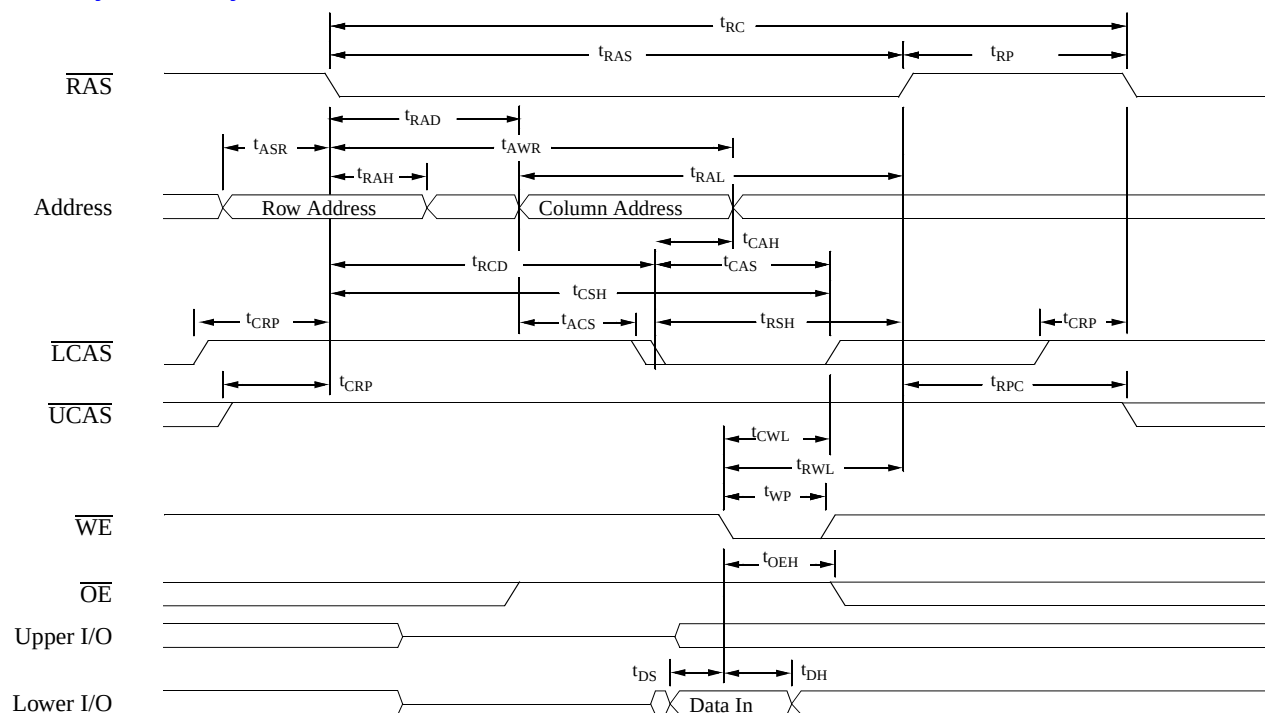




## Upper byte write cycle waveform

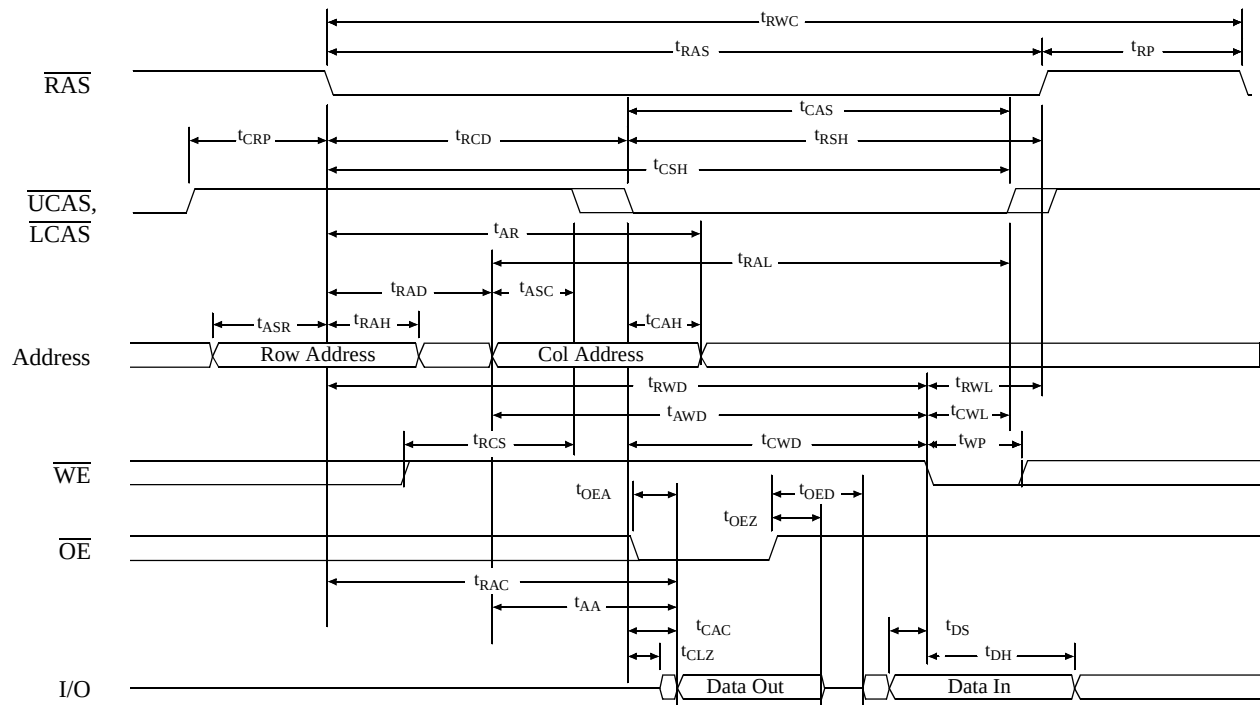
( $\overline{\text{OE}}$  controlled)

## Lower byte write cycle waveform

( $\overline{\text{OE}}$  controlled)

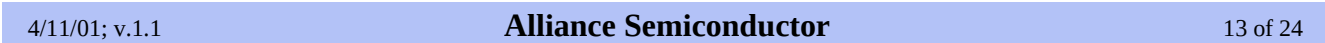


## Read-modify-write cycle waveform



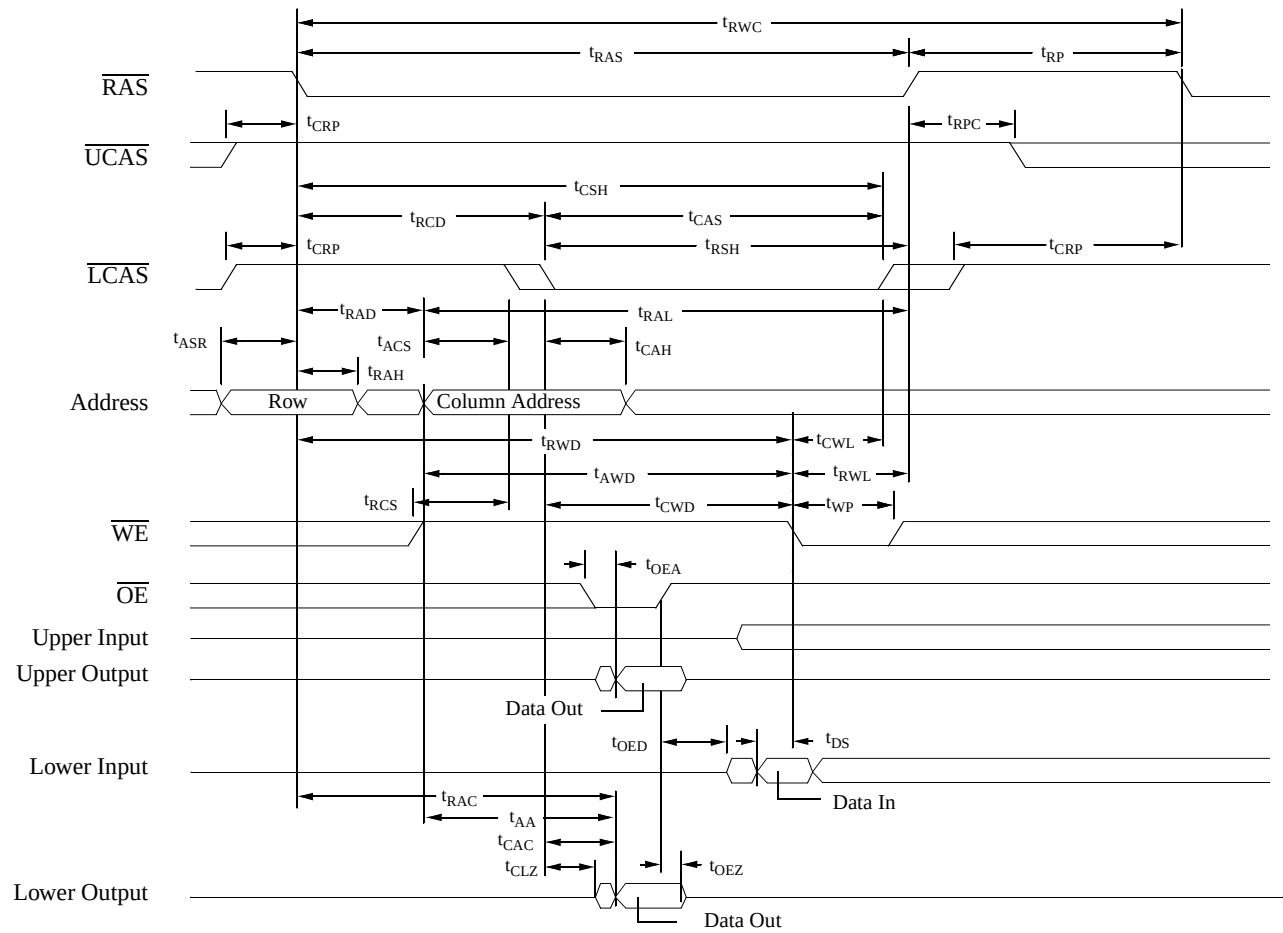
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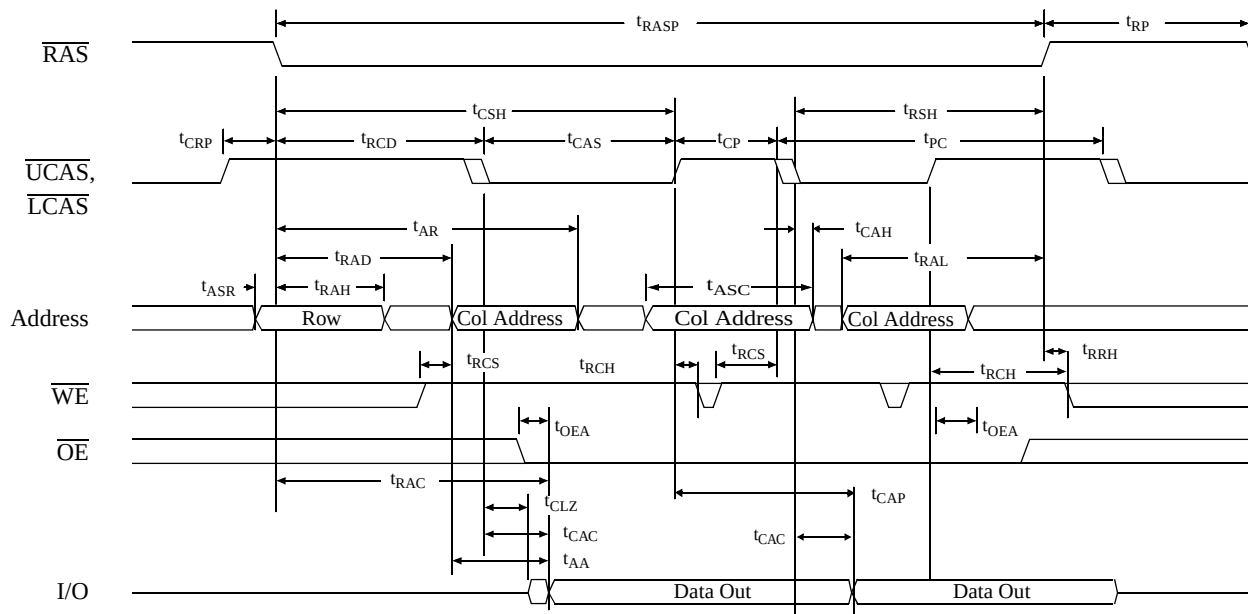


## Lower byte read-modify-write cycle waveform

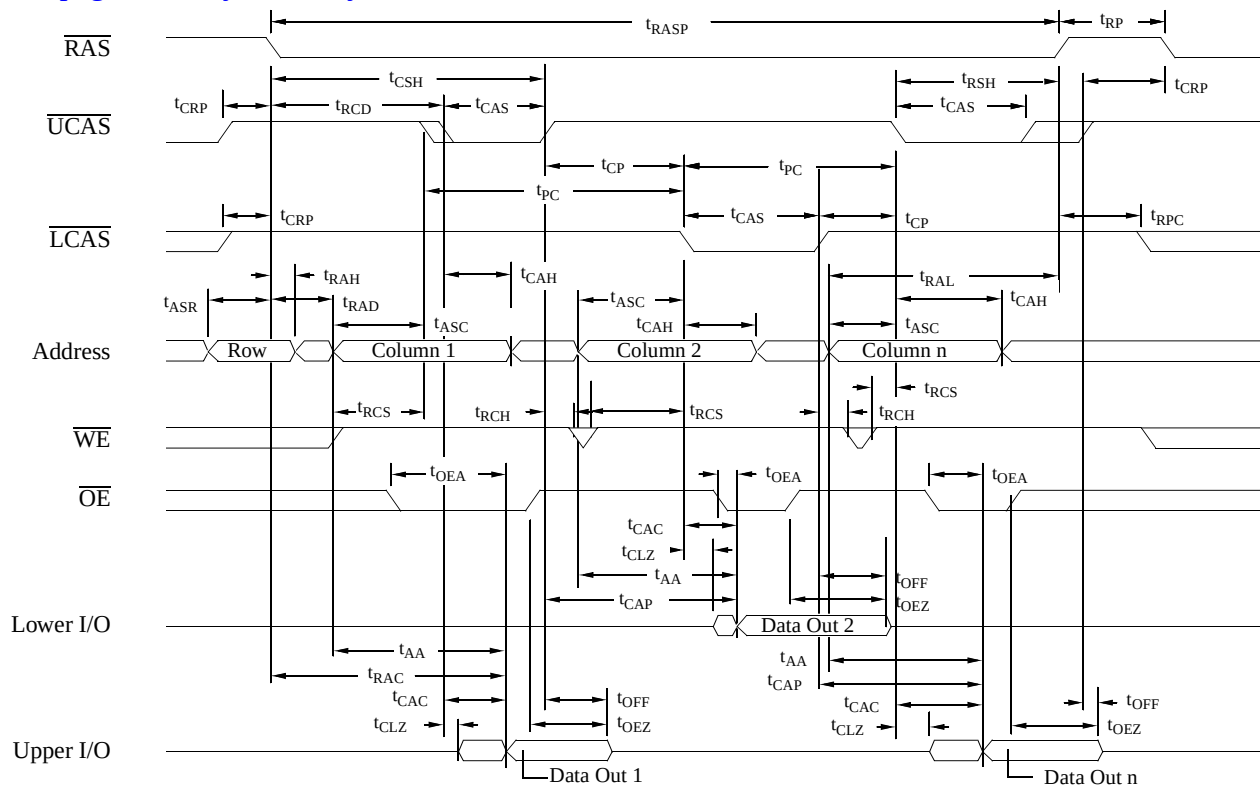




## EDO page mode read cycle waveform

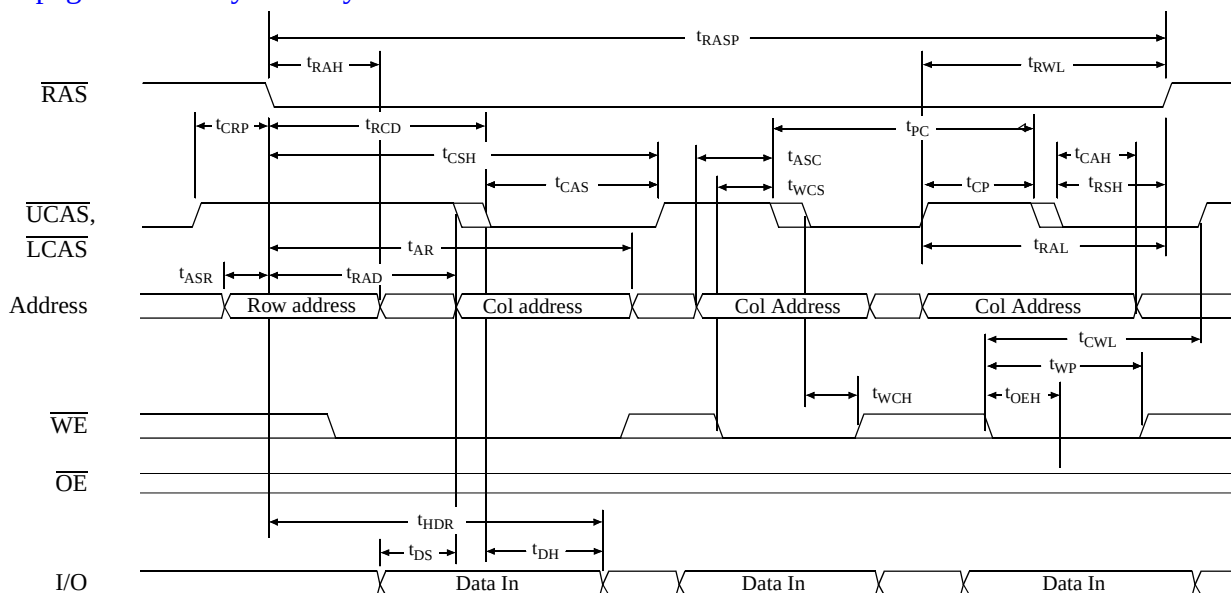


## EDO page mode byte read cycle waveform

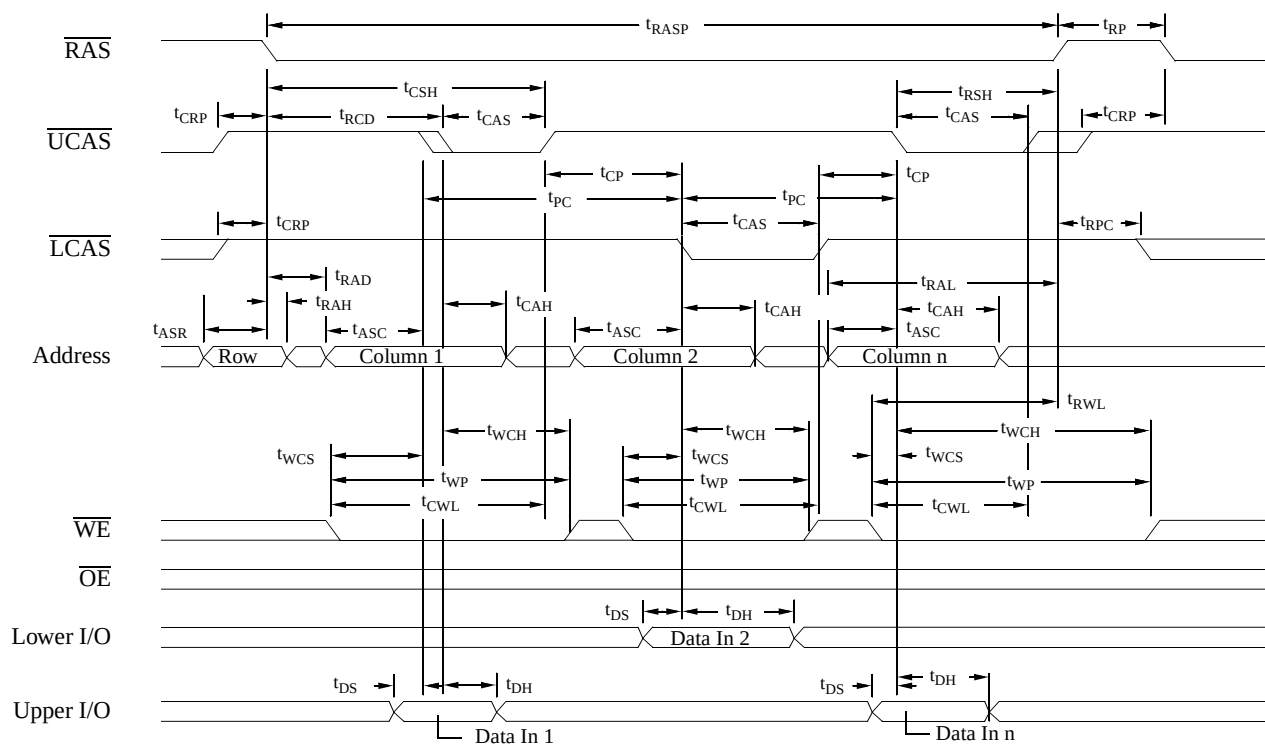




### EDO page mode early write cycle waveform



### EDO page mode byte early write cycle waveform





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$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle waveform ( $\overline{\text{WE}} = \text{V}_{\text{IH}}$ )

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle waveform ( $\overline{\text{WE}} = \text{V}_{\text{IH}}$ )



RAS only refresh cycle waveform ( $\overline{\text{WE}} = \overline{\text{OE}} = V_{\text{IH}}$  or  $V_{\text{IL}}$ )

RAS only refresh cycle waveform ( $\overline{\text{WE}} = \overline{\text{OE}} = V_{\text{IH}}$  or  $V_{\text{IL}}$ )



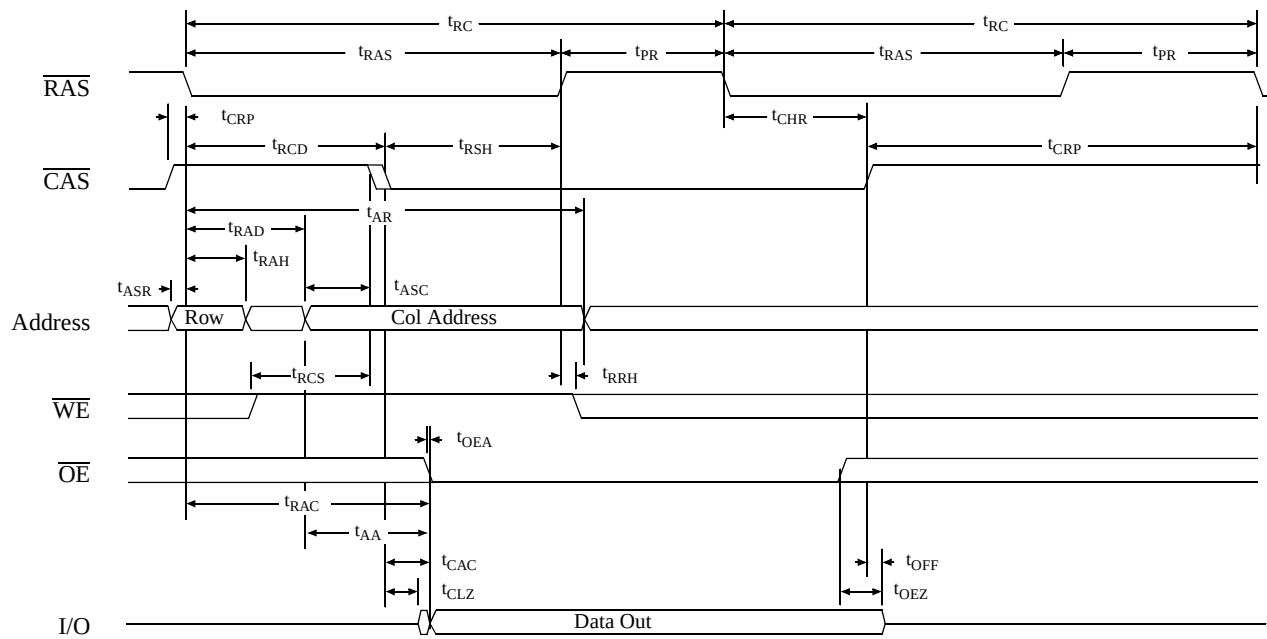
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\_\_\_\_\_

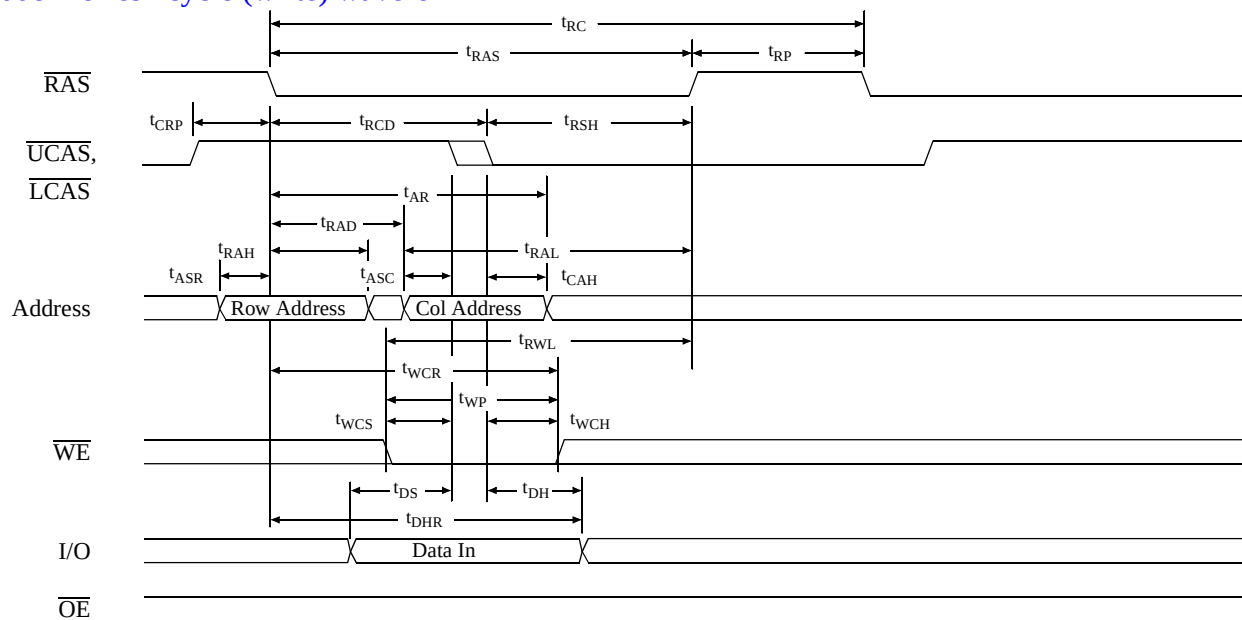




### Hidden refresh cycle (read) waveform

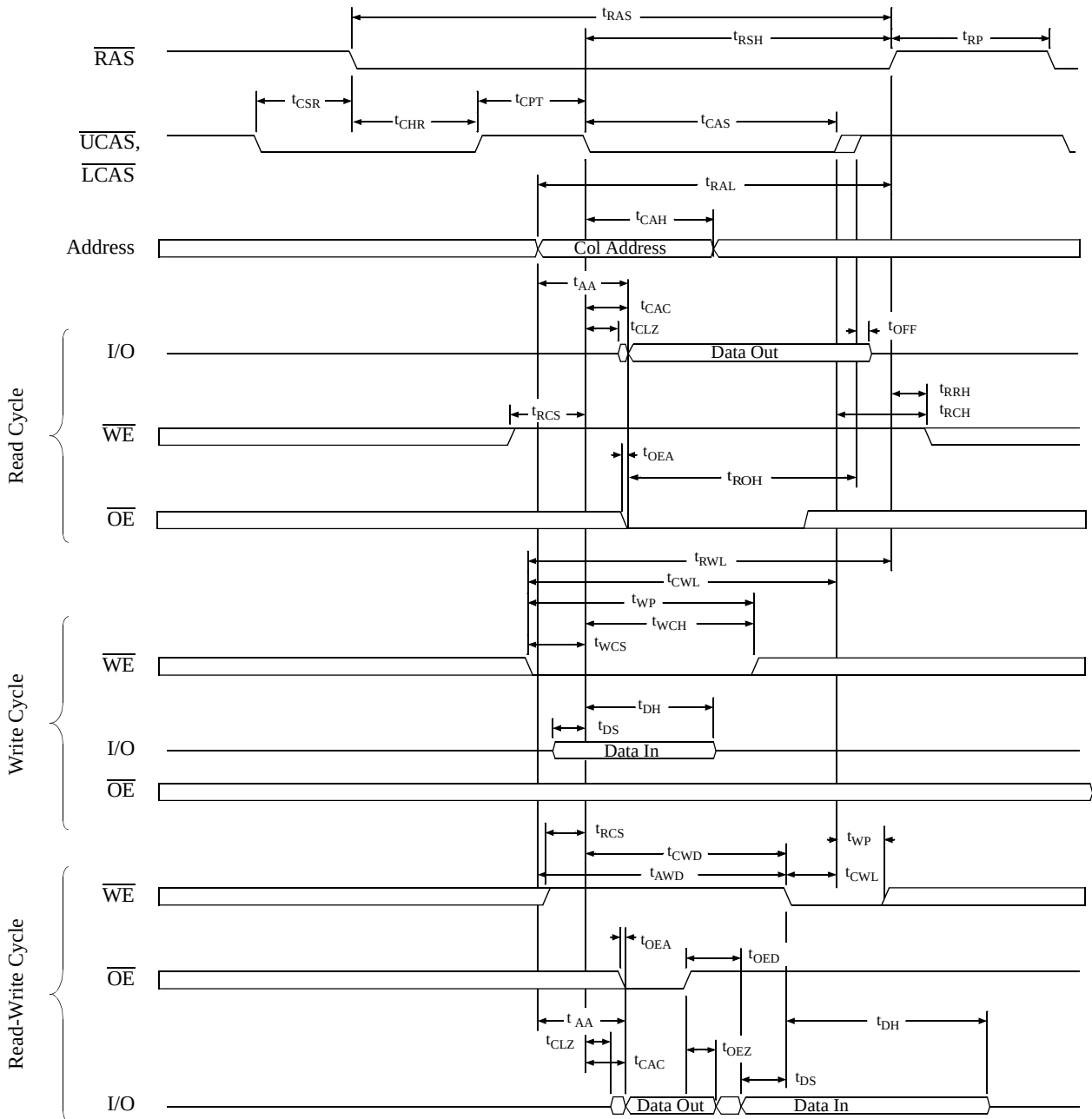


### Hidden refresh cycle (write) waveform



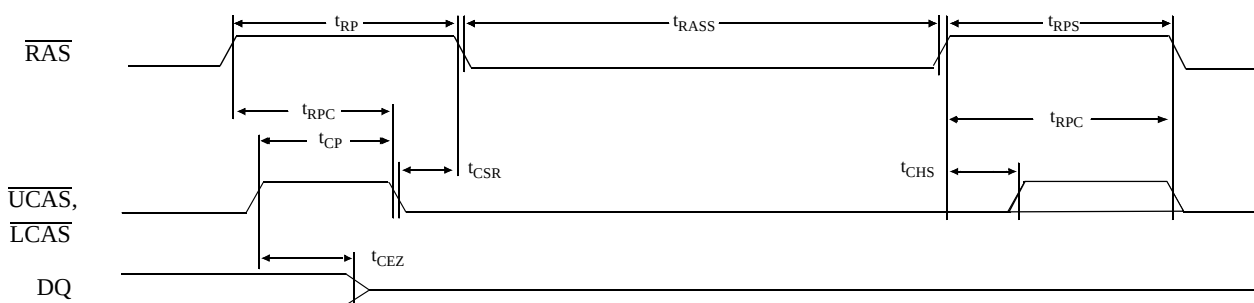


### CAS-before-RAS refresh counter test cycle waveform

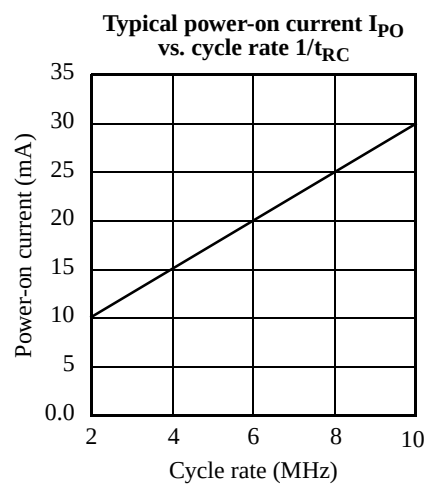
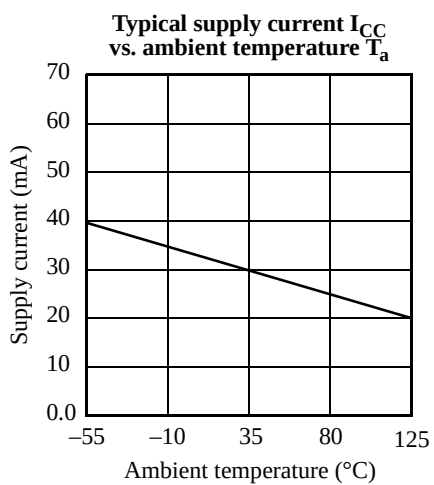
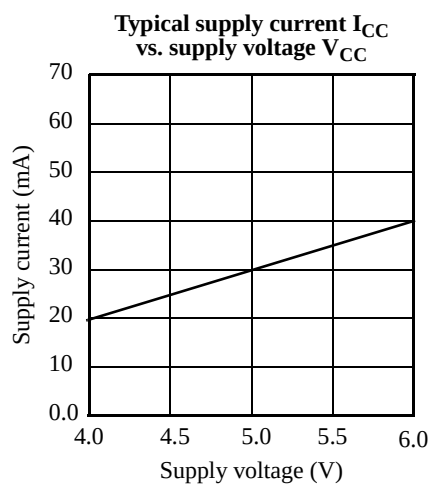
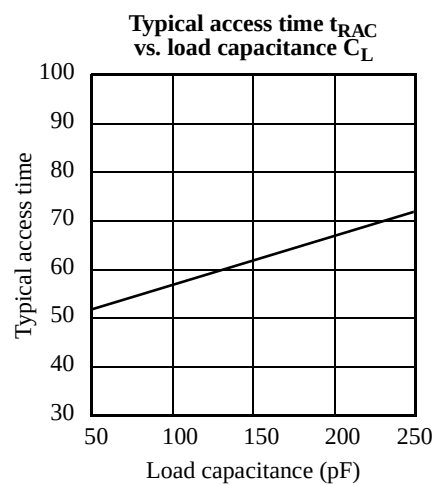
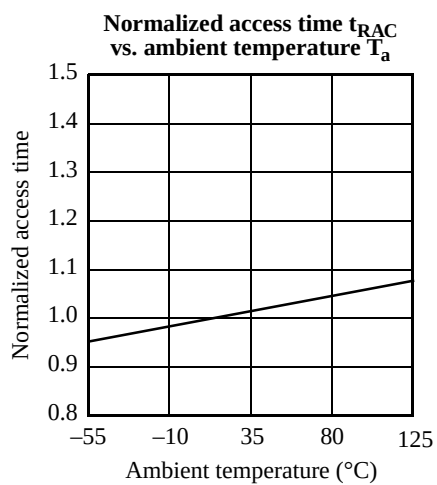
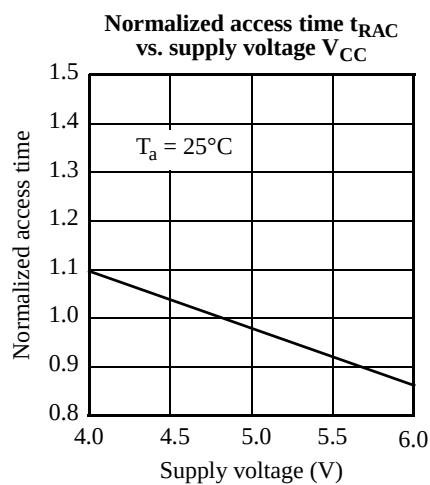


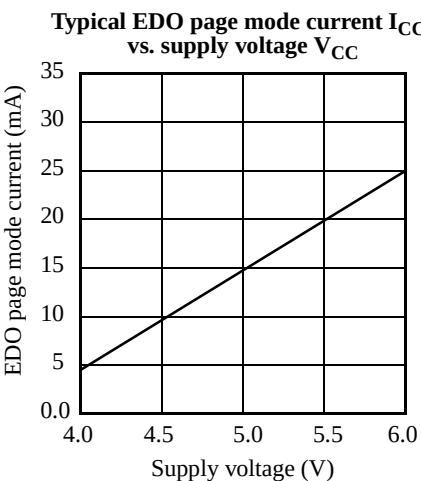
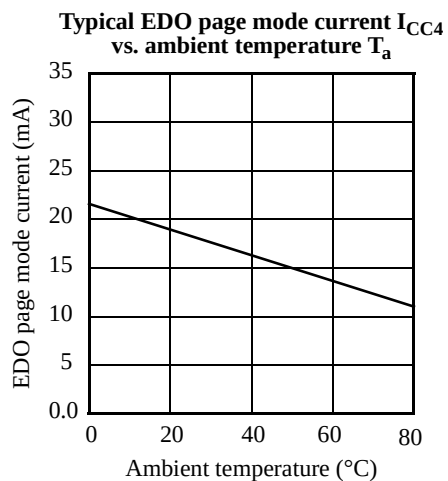
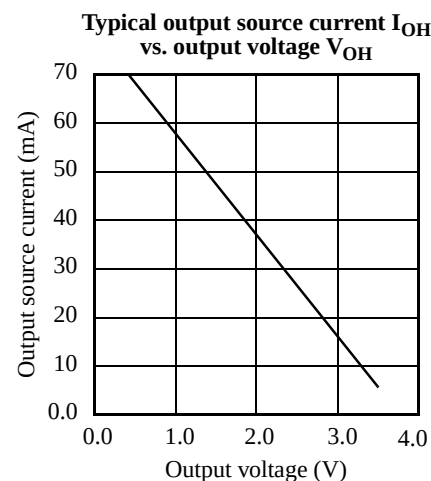
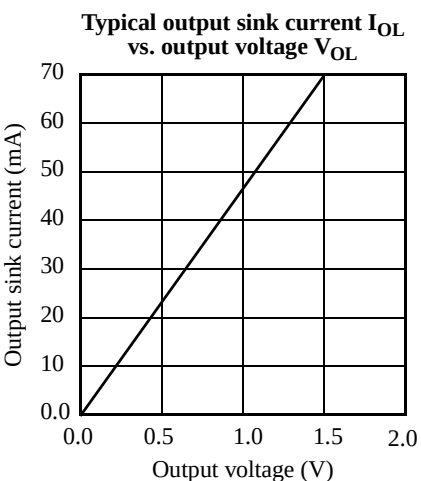
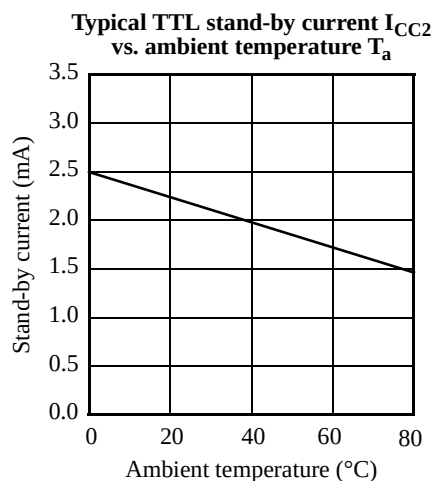
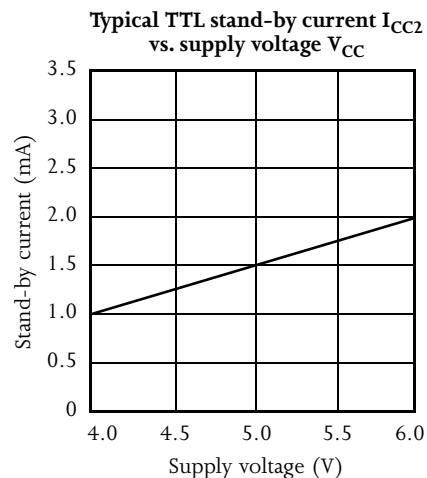
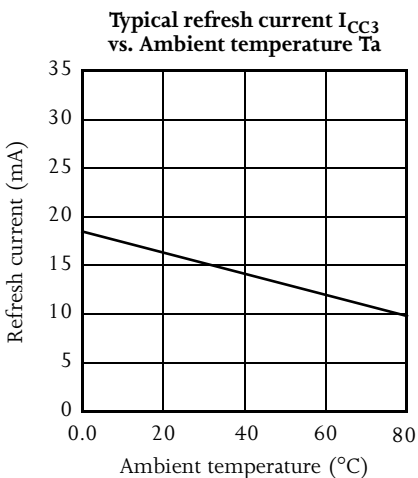
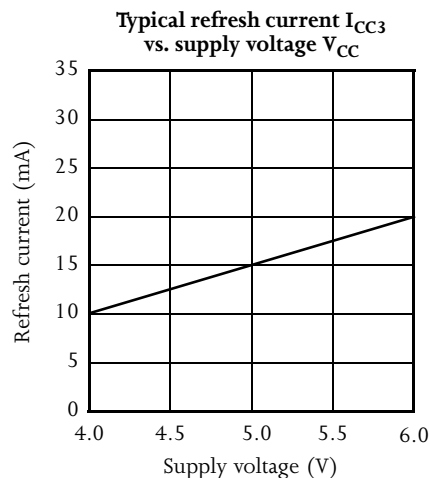


## CAS-before-RAS self refresh cycle



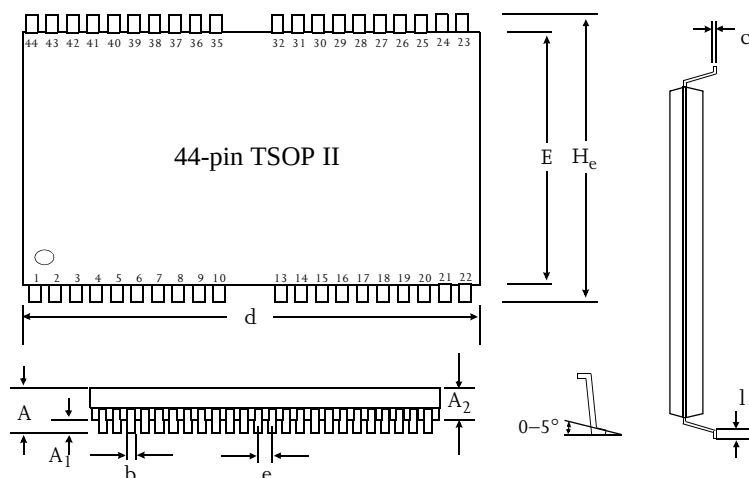
## Typical DC and AC characteristics





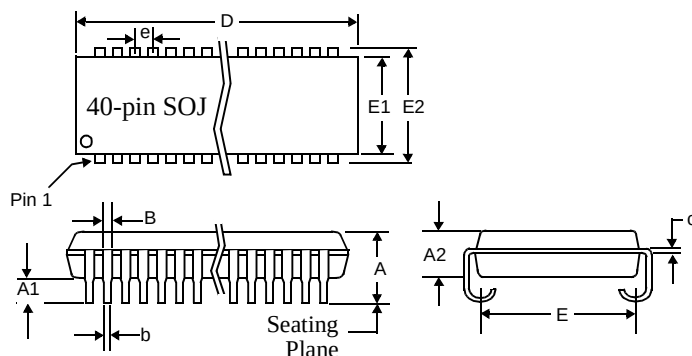


## Package dimensions



44-pin TSOP II

|                | Min<br>(mm)     | Max<br>(mm) |
|----------------|-----------------|-------------|
| A              |                 | 1.2         |
| A <sub>1</sub> | 0.05            |             |
| A <sub>2</sub> | 0.95            | 1.05        |
| b              | 0.30            | 0.45        |
| c              | 0.127 (typical) |             |
| d              | 18.28           | 18.54       |
| E              | 10.03           | 10.29       |
| H <sub>e</sub> | 11.56           | 11.96       |
| e              | 0.80 (typical)  |             |
| l              | 0.40            | 0.60        |

40-pin SOJ  
400 mil

|                | Min             | Max   |
|----------------|-----------------|-------|
| A              | 0.128           | 0.148 |
| A <sub>1</sub> | 0.025           | -     |
| A <sub>2</sub> | 1.105           | 1.115 |
| B              | 0.026           | 0.032 |
| b              | 0.015           | 0.020 |
| c              | 0.007           | 0.013 |
| D              | 1.020           | 1.035 |
| E              | 0.370 (typical) |       |
| E <sub>1</sub> | 0.390           | 0.410 |
| E <sub>2</sub> | 0.435           | 0.445 |
| e              | 0.050 (typical) |       |

## Capacitance

$f = 1 \text{ MHz}$ ,  $T_a = \text{room temperature}$ ,  $V_{CC} = 5V \pm 0.5V$

| Parameter         | Symbol    | Signals                                                                                      | Test conditions         | Max | Unit |
|-------------------|-----------|----------------------------------------------------------------------------------------------|-------------------------|-----|------|
| Input capacitance | $C_{IN1}$ | A0 to A8                                                                                     | $V_{in} = 0V$           | 5   | pF   |
|                   | $C_{IN2}$ | $\overline{RAS}$ , $\overline{UCAS}$ , $\overline{ICAS}$ , $\overline{WE}$ , $\overline{OE}$ | $V_{in} = 0V$           | 7   | pF   |
| I/O capacitance   | $C_{I/O}$ | I/O0 to I/O15                                                                                | $V_{in} = V_{out} = 0V$ | 7   | pF   |

## Ordering codes

| Package \ Access time        | 30 ns             | 35 ns             | 50 ns             |
|------------------------------|-------------------|-------------------|-------------------|
| Plastic SOJ, 400 mil, 40-pin | AS4C256K16E0-30JC | AS4C256K16E0-35JC | AS4C256K16E0-50JC |
| TSOP II, 400 mil, 40/44-pin  |                   |                   | AS4C256K16E0-50TC |

Shaded areas contain advance information.

## Part numbering system

| AS4C        | 256K16E0      | -XX                          | X                               | C                                             |
|-------------|---------------|------------------------------|---------------------------------|-----------------------------------------------|
| DRAM prefix | Device number | $\overline{RAS}$ access time | Package: J = SOJ<br>T = TSOP II | Commercial temperature range,<br>0°C to 70 °C |







Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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