Dual, Low Noise, Single-Supply Variable Gain Amplifier

AD605

FEATURES

2 independent linear-in-dB channels
Input noise at maximum gain: 1.8 nV/√Hz, 2.7 pA/√Hz
Bandwidth: 40 MHz (−3 dB)
Differential input
Absolute gain range programmable
−14 dB to +34 dB (FBK shorted to OUT) through
0 dB to 48 dB (FBK open)
Variable gain scaling: 20 dB/V through 40 dB/V
Stable gain with temperature and supply variations
Single-ended unipolar gain control
Output common mode independently set
Power shutdown at lower end of gain control
Single 5 V supply
Low power: 90 mW/channel
Drives ADCs directly

APPLICATIONS

Ultrasound and sonar time-gain controls
High performance AGC systems
Signal measurement

FUNCTIONAL BLOCK DIAGRAM

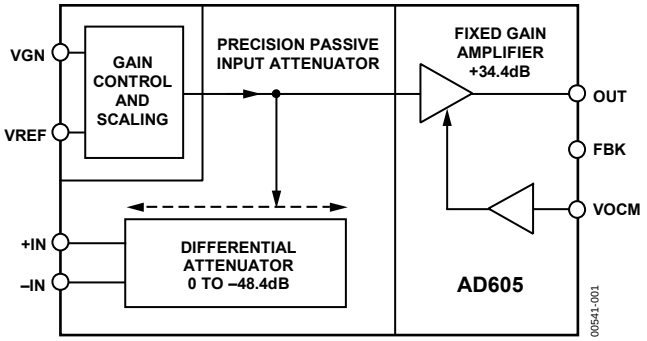


Figure 1.

GENERAL DESCRIPTION

The AD605 is a low noise, accurate, dual-channel, linear-in-dB variable gain amplifier (VGA), optimized for any application requiring high performance, wide bandwidth variable gain control. Operating from a single 5 V supply, the AD605 provides differential inputs and unipolar gain control for ease of use. Added flexibility is achieved with a user-determined gain range and an external reference input that provide user-determined gain scaling (dB/V).

The high performance linear-in-dB response of the AD605 is achieved with the differential input, single-supply, exponential amplifier (DSX-AMP) architecture. Each of the DSX-AMPs comprises a variable attenuator of 0 dB to −48.4 dB followed by a high speed, fixed-gain amplifier. The attenuator is based on a 7-stage R-1.5R ladder network. The attenuation between tap points is 6.908 dB, and 48.360 dB for the entire ladder network. The DSX-AMP architecture results in 1.8 nV/√Hz input noise spectral density and accepts a ±2.0 V input signal when VOCM is biased at VP/2.

Each independent channel of the AD605 provides a gain range of 48 dB that can be optimized for the application. Gain ranges between −14 dB to +34 dB and 0 dB to +48 dB can be selected by a single resistor between Pin FBK and Pin OUT. The lower and upper gain ranges are determined by shorting Pin FBK to Pin OUT or leaving Pin FBK unconnected, respectively. The two channels of the AD605 can be cascaded to provide 96 dB of very accurate gain range in a monolithic package.

The gain control interface provides an input resistance of approximately 2 MΩ and scale factors from 20 dB/V to 30 dB/V for a VREF input voltage of 2.5 V to 1.67 V, respectively. Note that scale factors up to 40 dB/V are achievable with reduced accuracy for scales above 30 dB/V. The gain scales linearly in dB with control voltages (VGN) of 0.4 V to 2.4 V for the 20 dB/V scale and 0.20 V to 1.20 V for the 40 dB/V scale. When VGN is <50 mV, the amplifier is powered down to draw 1.9 mA. Under normal operation, the quiescent supply current of each amplifier channel is only 18 mA.

The AD605 is available in a 16-lead PDIP and a 16-lead SOIC_N package and is guaranteed for operation over the −40°C to +85°C temperature range.

Rev. F
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REVISION HISTORY

6/08—Rev. E to Rev. F

Added Evaluation Board Section ... 18
Added Figure 42 and Table 4 ... 18
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Added Figure 45 to Figure 50 ... 20

5/07—Rev. D to Rev. E

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1/06—Rev. C to Rev. D

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7/04—Rev. B to Rev. C

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Change to TPC 22 ... 6
Updated Outline Dimensions ... 12

SPECIFICATIONS

Each channel @ T_A = 25°C, V_S = 5 V, R_S = 50 Ω, R_L = 500 Ω, C_L = 5 pF, V_{REF} = 2.5 V (scaling = 20 dB/V), −14 dB to +34 dB gain range, unless otherwise noted.

Table 1.

		AD605A			AD605B			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
Input Resistance			175 ± 40			175 ± 40		Ω
Input Capacitance			3.0			3.0		pF
Peak Input Voltage	At minimum gain		2.5 ± 2.5			2.5 ± 2.5		V
Input Voltage Noise	VGN = 2.9 V		1.8			1.8		nV/√Hz
Input Current Noise	VGN = 2.9 V		2.7			2.7		pA/√Hz
Noise Figure	R_S = 50 Ω, f = 10 MHz, VGN = 2.9 V		8.4			8.4		dB
	R_S = 200 Ω, f = 10 MHz, VGN = 2.9 V		12			12		dB
Common-Mode Rejection Ratio	f = 1 MHz, VGN = 2.65 V		−20			−20		dB
OUTPUT CHARACTERISTICS								
−3 dB Bandwidth	Constant with gain		40			40		MHz
Slew Rate	VGN = 1.5 V, output = 1 V step		170			170		V/µs
Output Signal Range	R_L ≥ 500 Ω		2.5 ± 1.5			2.5 ± 1.5		V
Output Impedance	f = 10 MHz		2			2		Ω
Output Short-Circuit Current			±40			±40		mA
Harmonic Distortion	VGN = 1 V, V_{OUT} = 1 V p-p							
HD2	f = 1 MHz		−64			−64		dBc
HD3	f = 1 MHz		−68			−68		dBc
HD2	f = 10 MHz		−51			−51		dBc
HD3	f = 10 MHz		−53			−53		dBc
Two-Tone Intermodulation Distortion (IMD)	R_S = 0 Ω, VGN = 2.9 V, V_{OUT} = 1 V p-p							
	f = 1 MHz		−72			−72		dBc
	f = 10 MHz		−60			−60		dBc
1 dB Compression Point	f = 10 MHz, VGN = 2.9 V, output referred		15			15		dBm
Third-Order Intercept	f = 10 MHz, VGN = 2.9 V, V_{OUT} = 1 V p-p, input referred		−1			−1		dBm
Channel-to-Channel Crosstalk	Ch1: VGN = 2.65 V, inputs shorted, Ch2: VGN = 1.5 V (mid gain), f = 1 MHz, V_{OUT} = 1 V p-p		−70			−70		dB
Group Delay Variation	1 MHz < f < 10 MHz, full gain range		±2.0			±2.0		ns
VOCM Input Resistance			45			45		kΩ
ACCURACY								
Absolute Gain Error								
−14 dB to −11 dB	0.25 V < VGN < 0.40 V	−1.2	+1.0	+3.0	−1.2	+0.75	+3.0	dB
−11 dB to +29 dB	0.40 V < VGN < 2.40 V	−1.0	±0.3	+1.0	−1.0	±0.2	+1.0	dB
+29 dB to +34 dB	2.40 V < VGN < 2.65 V	−3.5	−1.25	+1.2	−3.5	−1.25	+1.2	dB
Gain Scaling Error	0.4 V < VGN < 2.4 V		±0.25			±0.25		dB/V
Output Offset Voltage	V_{REF} = 2.500 V, VOCM = 2.500 V	−30	±20	+30	−30	±20	+30	mV
Output Offset Variation	V_{REF} = 2.500 V, VOCM = 2.500 V		30	57		30	50	mV

Parameter	Conditions	AD605A			AD605B			Unit
		Min	Typ	Max	Min	Typ	Max	
GAIN CONTROL INTERFACE								
Gain Scaling Factor	V_{REF} = 2.5 V, 0.4 V < VGN < 2.4 V	19	20	21	19	20	21	dB/V
	V_{REF} = 1.67 V		30			30		dB/V
Gain Range	FBK short to OUT		−14 to +34			−14 to +34		dB
	FBK open		0 to 48			0 to 48		dB
Input Voltage (VGN) Range	20 dB/V, VREF = 2.5 V		0.1 to 2.9			0.1 to 2.9		V
Input Bias Current			−0.4			−0.4		µA
Input Resistance			2			2		MΩ
Response Time	48 dB gain change		0.2			0.2		µs
POWER SUPPLY								
Supply Voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
Power Dissipation			90			90		mW
VREF Input Resistance			10			10		kΩ
Quiescent Supply Current	VPOS		18	23		18	23	mA
Power-Down	VPOS, VGN < 50 mV		1.9	3.0		1.9	3.0	mA
Power-Up Response Time	48 dB gain, V_{OUT} = 2 V p-p		0.6			0.6		µs
Power-Down Response Time			0.4			0.4		µs

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage $+V_S$	
Pin 12, Pin 13 (with Pin 4, Pin 5 = 0 V)	6.5 V
Input Voltage Pin 1 to Pin 3, Pin 6 to Pin 9, Pin 16	VPOS, 0 V
Internal Power Dissipation	
16-Lead PDIP	1.4 W
16-Lead SOIC_N	1.2 W
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering 60 sec	300°C
Thermal Resistance θ_{JA}	
16-Lead PDIP	85°C/W
16-Lead SOIC_N	100°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

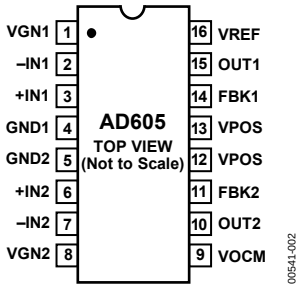


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VGN1	CH1 Gain Control Input and Power-Down Pin. If grounded, device is off; otherwise, positive voltage increases gain.
2	–IN1	CH1 Negative Input.
3	+IN1	CH1 Positive Input.
4	GND1	Ground.
5	GND2	Ground.
6	+IN2	CH2 Positive Input.
7	–IN2	CH2 Negative Input.
8	VGN2	CH2 Gain Control Input and Power-Down Pin. If grounded, device is off; otherwise, positive voltage increases gain.
9	VOCM	Input to This Pin Defines Common-Mode Voltage for OUT1 and OUT2.
10	OUT2	CH2 Output.
11	FBK2	Feedback Pin That Selects Gain Range of CH2.
12	VPOS	Positive Supply.
13	VPOS	Positive Supply.
14	FBK1	Feedback Pin That Selects Gain Range of CH1.
15	OUT1	CH1 Output.
16	VREF	Input to This Pin Sets Gain Scaling for Both Channels: 2.5 V = 20 dB/V and 1.67 V = 30 dB/V.

TYPICAL PERFORMANCE CHARACTERISTICS (PER CHANNEL)

V_{REF} = 2.5 V (20 dB/V scaling), f = 1 MHz, R_L = 500 Ω, C_L = 5 pF, T_A = 25°C, V_{SS} = 5 V.

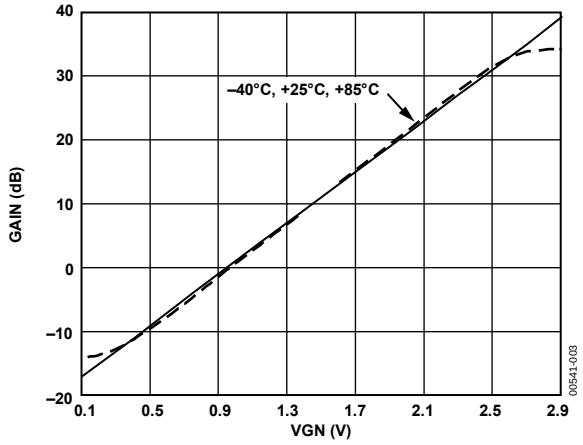


Figure 3. Gain vs. VGN

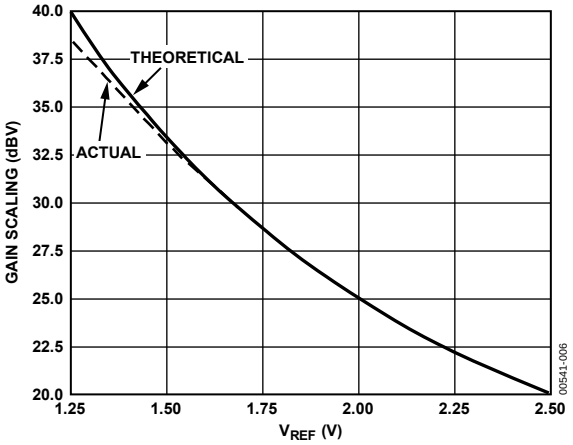


Figure 6. Gain Scaling vs. V_{REF}

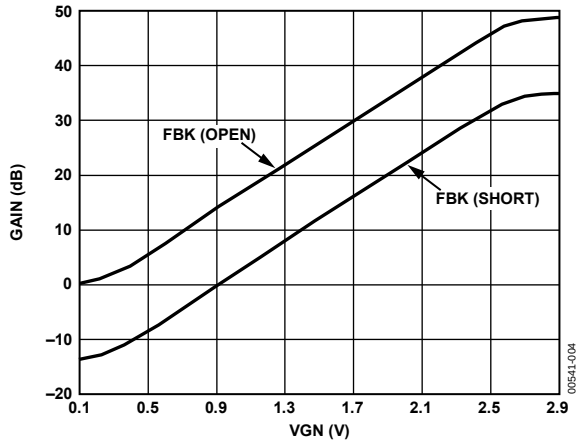


Figure 4. Gain vs. VGN for Different Gain Ranges

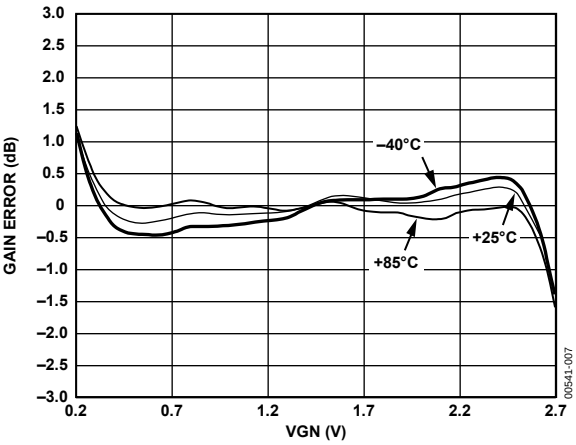


Figure 7. Gain Error vs. VGN at Three Temperatures

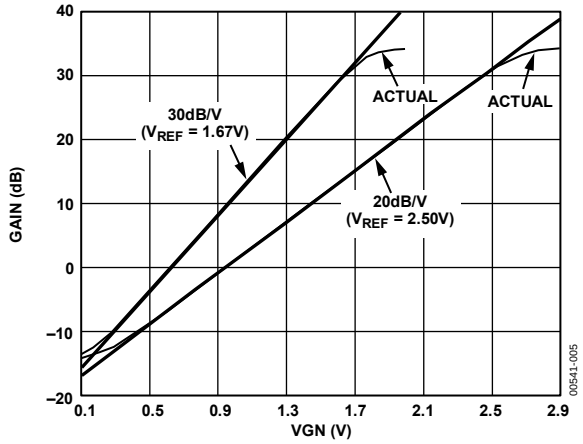


Figure 5. Gain vs. VGN for Different Gain Scalings

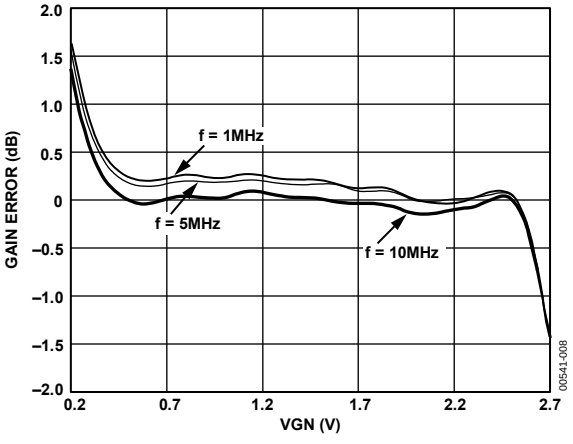


Figure 8. Gain Error vs. VGN at Three Frequencies

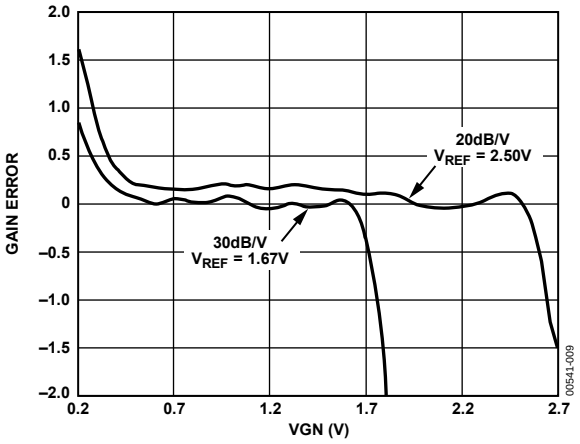


Figure 9. Gain Error vs. VGN for Two Gain Scale Values

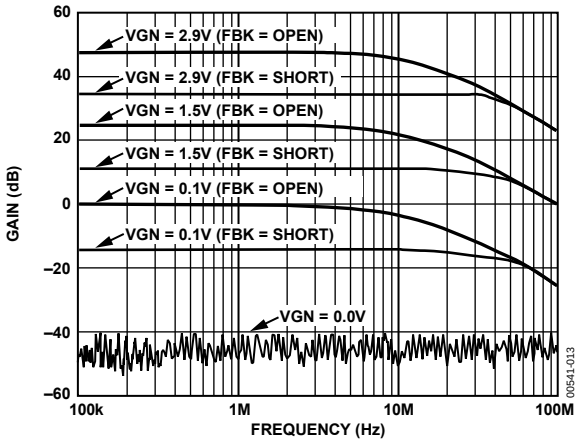


Figure 12. AC Response for Three Values of VGN

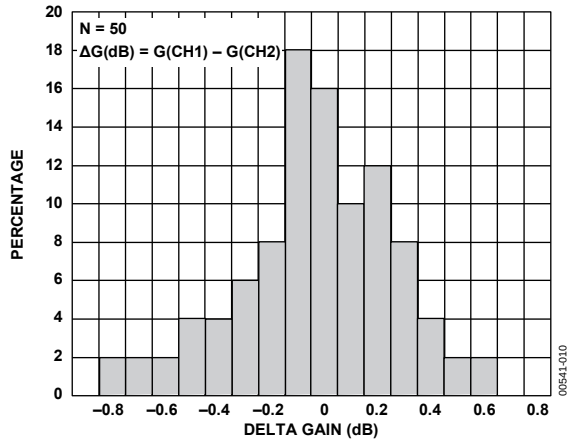


Figure 10. Gain Match, VGN1 = VGN2 = 1.0 V

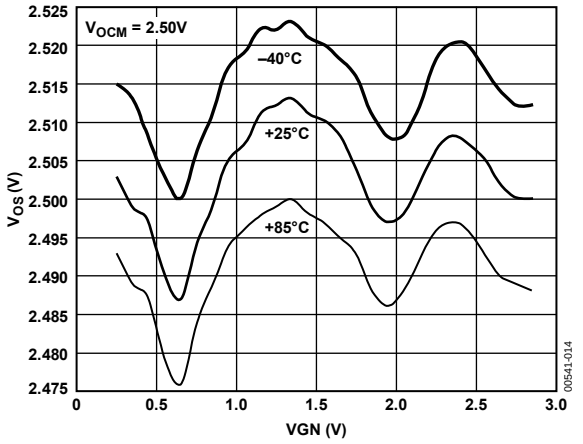


Figure 13. Output Offset vs. VGN at Three Temperatures

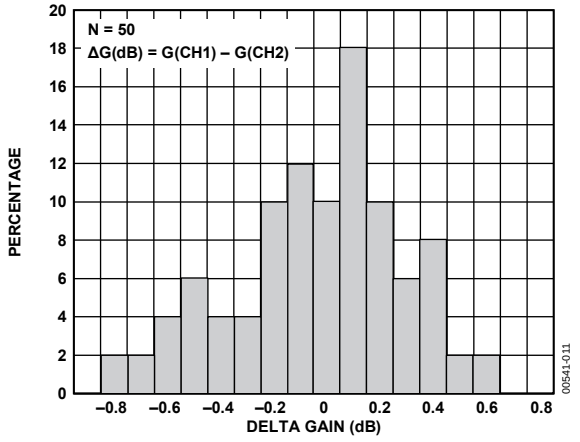


Figure 11. Gain Match, VGN1 = VGN2 = 2.50 V

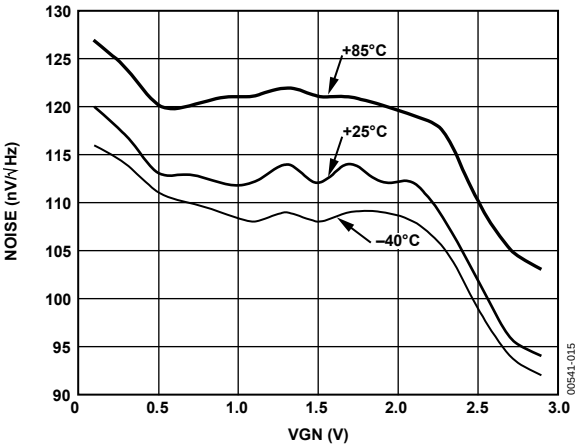


Figure 14. Output Referred Noise vs. VGN at Three Temperatures

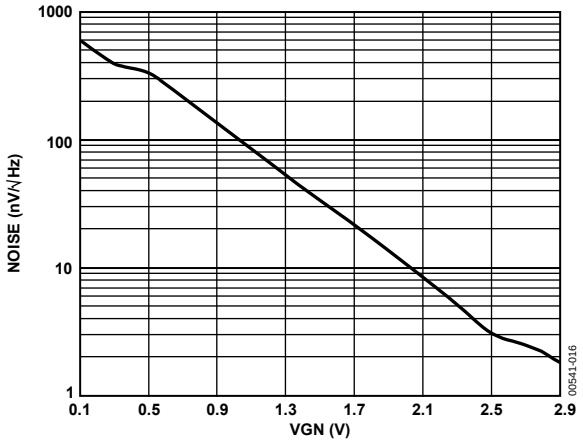


Figure 15. Input Referred Noise vs. VGN

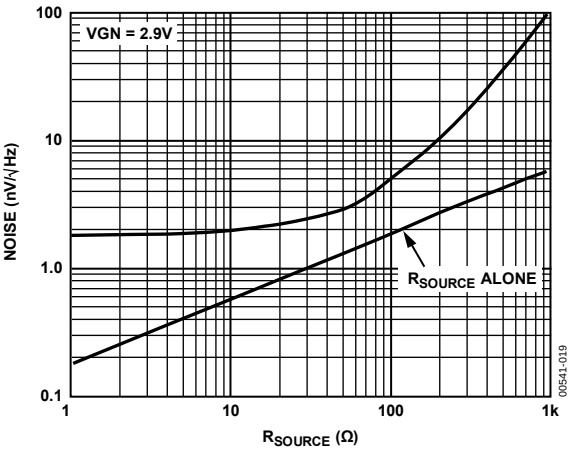


Figure 18. Input Referred Noise vs. R_{SOURCE}

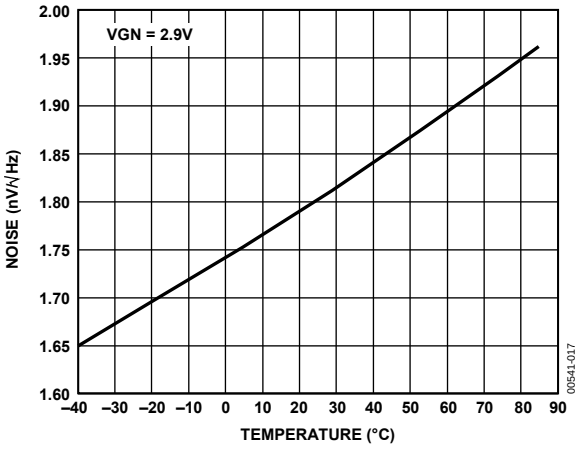


Figure 16. Input Referred Noise vs. Temperature

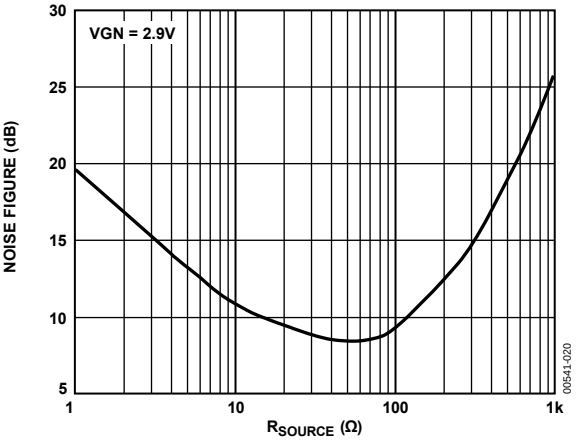


Figure 19. Noise Figure vs. R_{SOURCE}

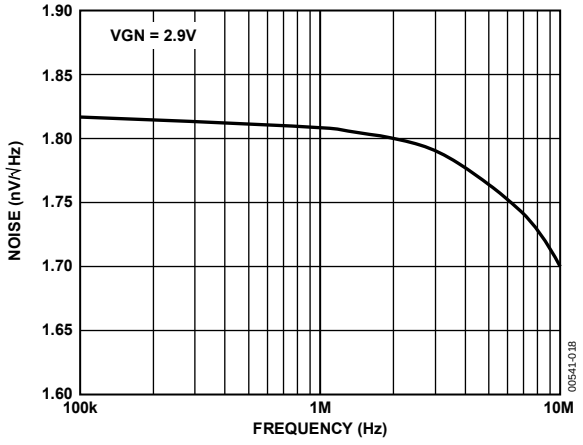


Figure 17. Input Referred Noise vs. Frequency

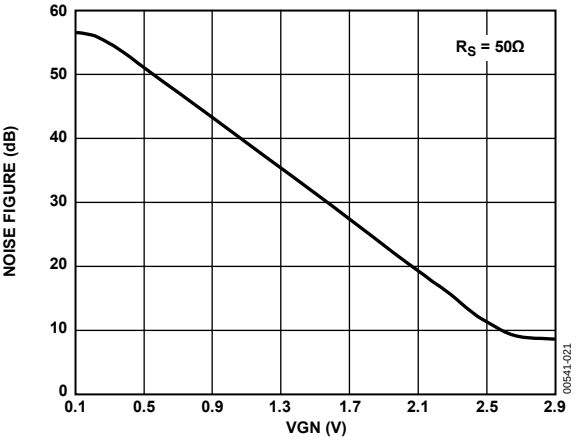


Figure 20. Noise Figure vs. VGN

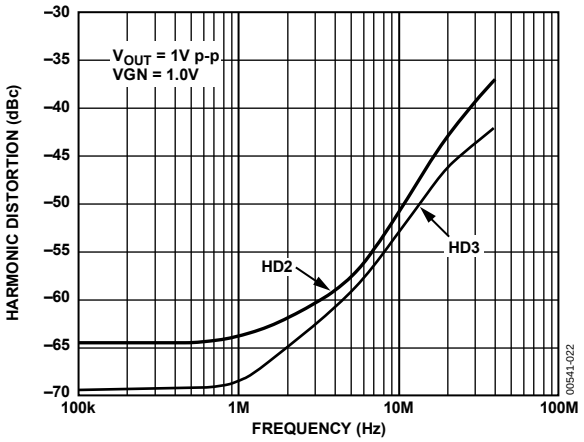


Figure 21. Harmonic Distortion vs. Frequency

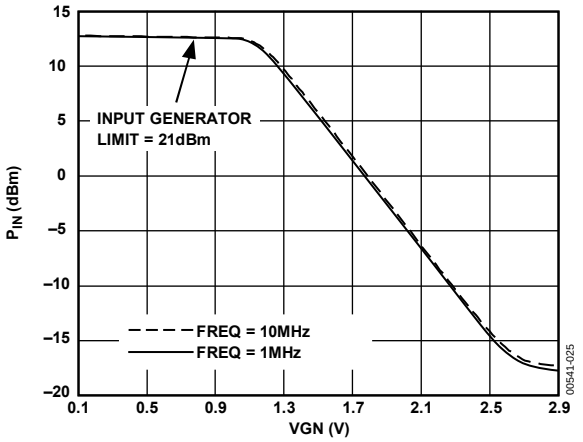


Figure 24. 1 dB Compression vs. VGN

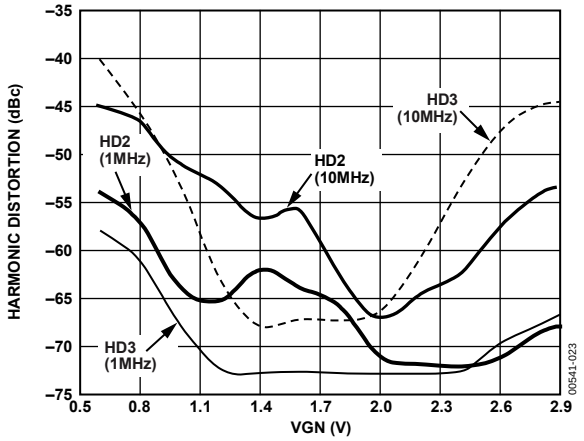


Figure 22. Harmonic Distortion vs. VGN at 1 MHz and 10 MHz

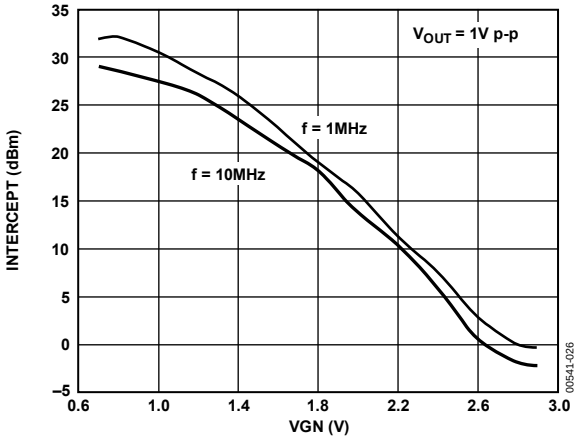


Figure 25. Third-Order Intercept vs. VGN at 1 MHz and 10 MHz

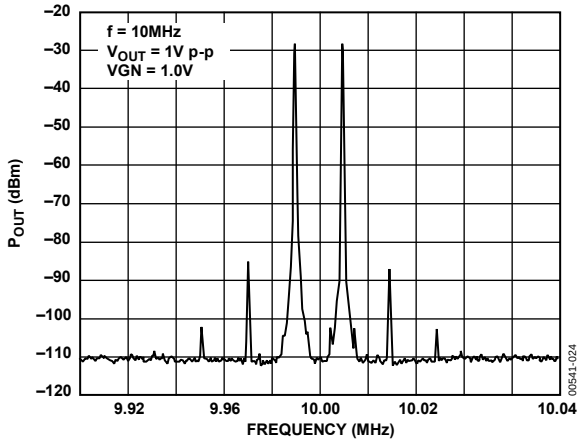


Figure 23. Intermodulation Distortion

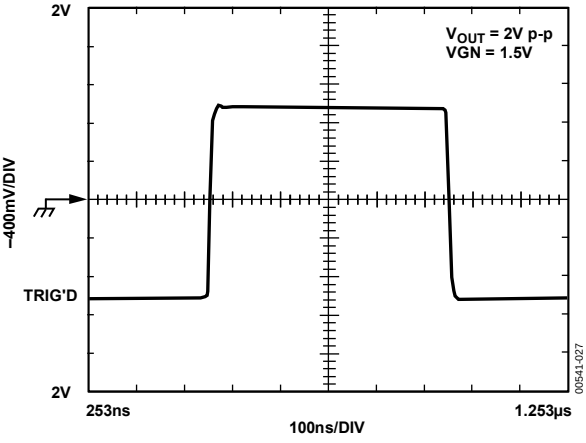


Figure 26. Large Signal Pulse Response

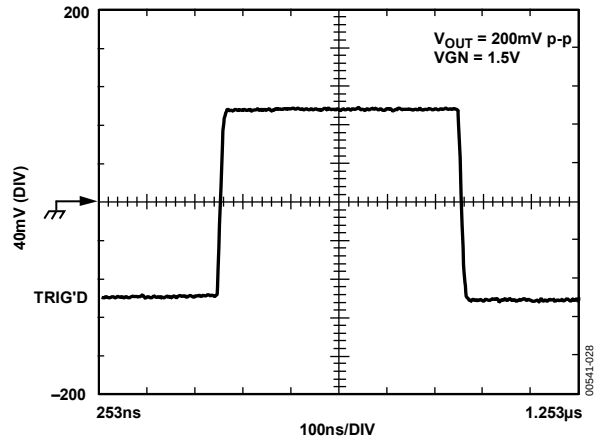


Figure 27. Small Signal Pulse Response

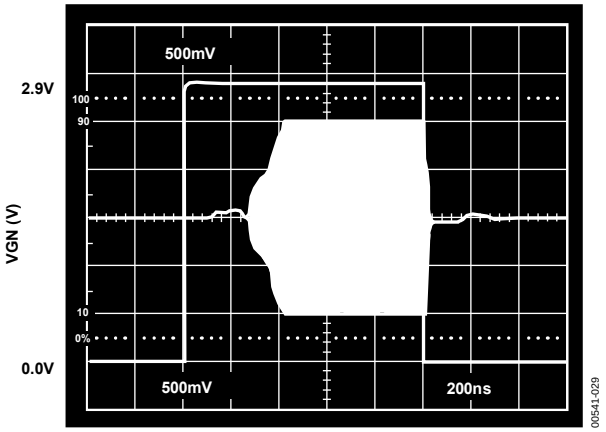


Figure 28. Power-Up/Power-Down Response

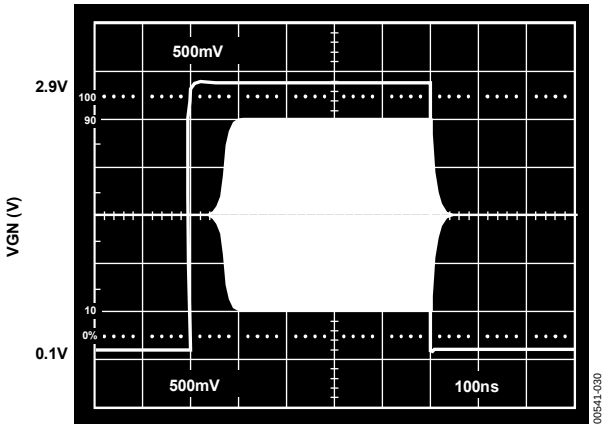


Figure 29. Gain Response

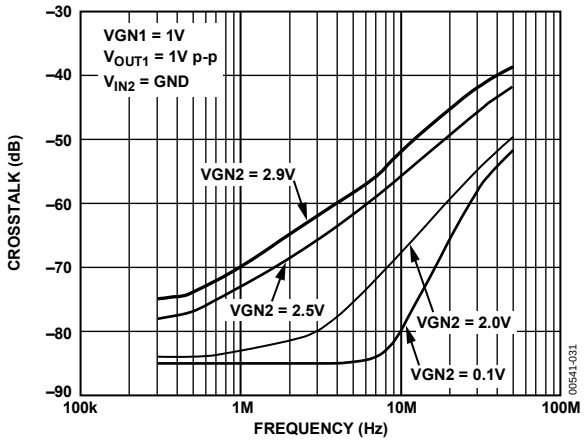


Figure 30. Crosstalk (CH1 to CH2) vs. Frequency for Four Values of VGN2

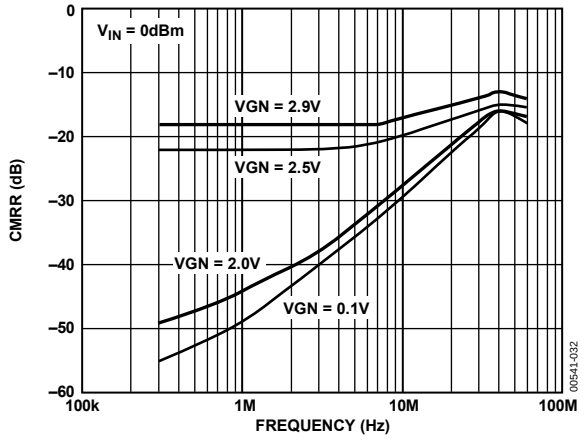


Figure 31. CMRR vs. Frequency for Four Values of VGN

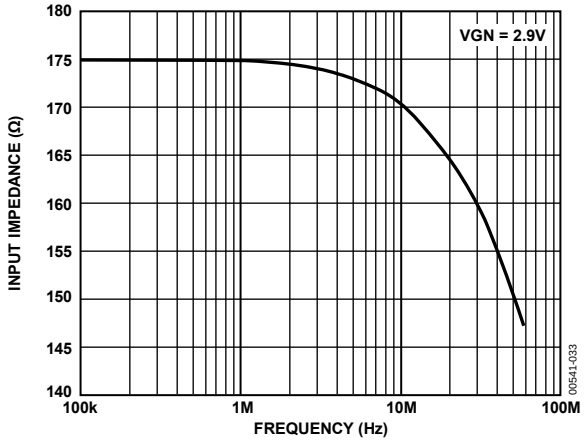


Figure 32. Input Impedance vs. Frequency

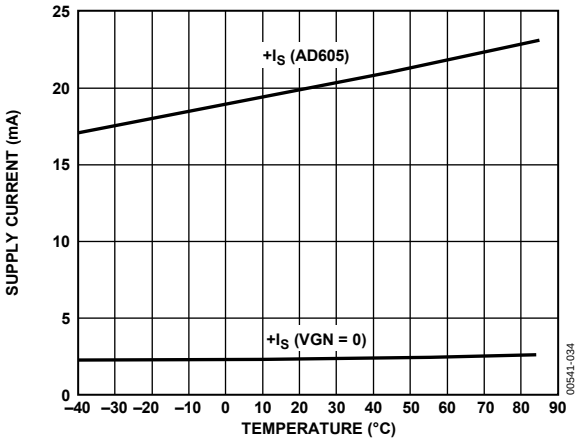


Figure 33. Supply Current (One Channel) vs. Temperature

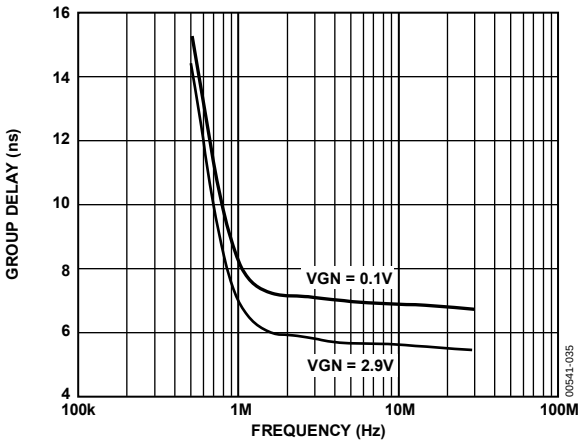


Figure 34. Group Delay vs. Frequency

THEORY OF OPERATION

The AD605 is a dual-channel, low noise VGA. Figure 35 shows the simplified block diagram of one channel. Each channel consists of a single-supply X-AMP® (hereafter called DSX, differential single-supply X-AMP) comprising the following:

- Precision passive attenuator (differential ladder)
- Gain control block
- VOCM buffer with supply splitting resistors R3 and R4
- Active feedback amplifier[1] (AFA) with gain setting resistors R1 and R2

The linear-in-dB gain response of the AD605 can generally be described by Equation 1.

$$G\ (\text{dB}) = (\textit{Gain Scaling}\ (\text{dB/V})) \times (\textit{Gain Control}\ (\text{V})) - (19\ \text{dB} - (14\ \text{dB}) \times (\textit{FB})) \quad (1)$$

where:
FB = 0, if FBK to OUT is shorted.
FB = 1, if FBK to OUT is open.

Each channel provides between −14 dB to +34.4 dB through 0 dB to +48.4 dB of gain, depending on the value of the resistance connected between Pin FBK and Pin OUT. The center 40 dB of gain is exactly linear-in-dB while the gain error increases at the top and bottom of the range. The gain is set by the gain control voltage (VGN). The VREF input establishes the gain scaling. The useful gain scaling range is between 20 dB/V and 40 dB/V for a VREF voltage of 2.5 V and 1.25 V, respectively. For example, if FBK to OUT is shorted and VREF is set to 2.50 V (to establish a gain scaling of 20 dB/V), the gain equation simplifies to

$$G\ (\text{dB}) = (20\ (\text{dB/V})) \times (\textit{VGN}\ (\text{V})) - 19\ \text{dB} \quad (2)$$

The desired gain can then be achieved by setting the unipolar gain control (VGN) to a voltage within its nominal operating range of 0.25 V to 2.65 V (for 20 dB/V gain scaling). The gain is monotonic for a complete gain control range of 0.1 V to 2.9 V. Maximum gain can be achieved at a VGN of 2.9 V.

Because the two channels are identical, only Channel 1 is used to describe their operation. VREF and VOCM are the only inputs that are shared by the two channels, and because they are normally ac grounds, crosstalk between the two channels is minimized. For the highest gain scaling accuracy, VREF should have an external low impedance voltage source. For low accuracy 20 dB/V applications, the VREF input can be decoupled with a capacitor to ground. In this mode, the gain scaling is determined by the midpoint between +VCC and GND; therefore, care should be taken to control the supply voltage to 5 V. The input resistance looking into the VREF pin is 10 kΩ ± 20%.

The AD605 is a single-supply circuit, and the VOCM pin is used to establish the dc level of the midpoint of this portion of the circuit. VOCM needs only an external decoupling capacitor to ground to center the midpoint between the supply voltages (5 V, GND). However, if the dc level of the output is important to the user (see the Applications Information section of the AD9050 data sheet for an example), VOCM can be specifically set. The input resistance looking into the VOCM pin is 45 kΩ ± 20%.

[1] To understand the active-feedback amplifier topology, refer to the AD830 data sheet. The AD830 is a practical implementation of the idea.

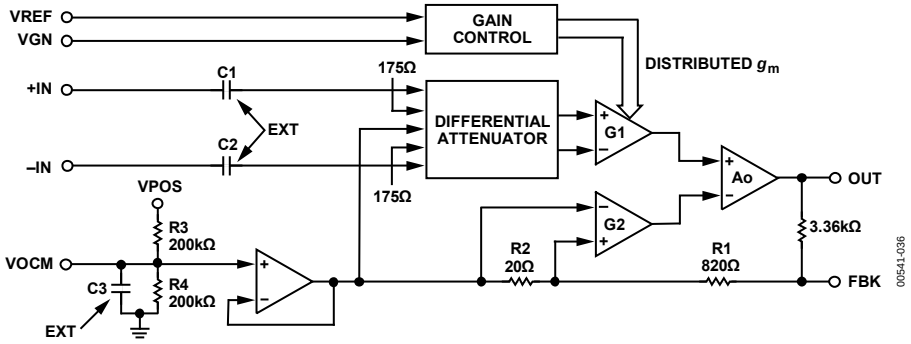


Figure 35. Simplified Block Diagram of a Single Channel of the AD605

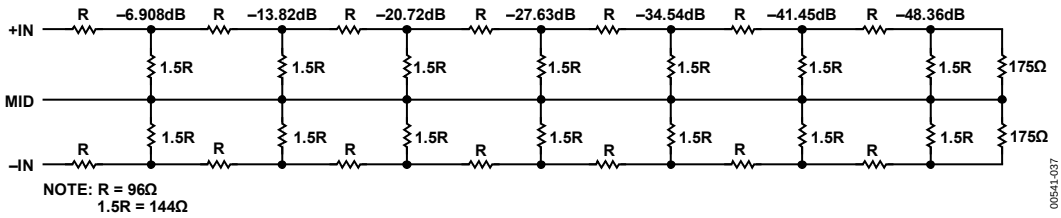


Figure 36. R-1.5R Dual Ladder Network

DIFFERENTIAL LADDER (ATTENUATOR)

The attenuator before the fixed gain amplifier is realized by a differential, 7-stage, R-1.5R resistive ladder network with an untrimmed input resistance of 175 Ω single ended or 350 Ω differentially. The signal applied at the input of the ladder network is attenuated by 6.908 dB per tap; therefore, the attenuation at the first tap is 6.908 dB, at the second, 13.816 dB, and so on all the way to the last tap where the attenuation is 48.356 dB (see Figure 36). A unique circuit technique is used to interpolate continuously between the tap points, thereby providing continuous attenuation from 0 dB to −48.36 dB. One can think of the ladder network together with the interpolation mechanism as a voltage-controlled potentiometer.

Because the DSX is a single-supply circuit, some means of biasing its inputs must be provided. Node MID together with the VOCM buffer performs this function. Without internal biasing, external biasing is required. If not done carefully, the biasing network can introduce additional noise and offsets. By providing internal biasing, the user is relieved of this task and only needs to ac couple the signal into the DSX. It should be made clear again that the input to the DSX is still fully differential if driven differentially, that is, Pin +IN and Pin −IN see the same signal but with opposite polarity. What changes is the load seen by the driver; it is 175 Ω when each input is driven single ended, but 350 Ω when driven differentially. This can be easily explained when thinking of the ladder network as two 175 Ω resistors connected back-to-back with the middle node, MID, being biased by the VOCM buffer. A differential signal applied between nodes +IN and −IN results in zero current into Node MID, but a single-ended signal applied to either input +IN or −IN, while the other input is ac grounded, causes the current delivered by the source to flow into the VOCM buffer via Node MID.

A feature of the X-AMP architecture is that the output-referred noise is constant vs. gain over most of the gain range. Referring to Figure 36, the tap resistance is approximately equal for all taps within the ladder, excluding the end sections. The resistance seen looking into each tap is 54.4 Ω, which makes 0.95 nV/√Hz of Johnson noise spectral density. Because there are two attenuators, the overall noise contribution of the ladder network is √2 times 0.95 nV/√Hz or 1.34 nV/√Hz, a large fraction of the total DSX noise. The rest of the DSX circuit components contribute another 1.20 nV/√Hz, which together with the attenuator produces 1.8 nV/√Hz of total DSX input referred noise.

AC COUPLING

The DSX is a single-supply circuit; therefore, its inputs need to be ac-coupled to accommodate ground-based signals. External Capacitor C1 and Capacitor C2 in Figure 35 level-shift the input signal from ground to the dc value established by VOCM (nominal 2.5 V). C1 and C2, together with the 175 Ω looking into each of DSX inputs (+IN and −IN), act as high-pass filters with corner frequencies depending on the values chosen for C1 and C2. For example, if C1 and C2 are 0.1 μF, together with the 175 Ω input resistance of each side of the differential ladder of the DSX, a −3 dB high-pass corner at 9.1 kHz is formed.

If the DSX output needs to be ground referenced, another ac coupling capacitor is required for level shifting. This capacitor also eliminates any dc offsets contributed by the DSX. With a nominal load of 500 Ω and a 0.1 μF coupling capacitor, this adds a high-pass filter with −3 dB corner frequency at about 3.2 kHz.

The choice for all three of these coupling capacitors depends on the application. They should allow the signals of interest to pass unattenuated, while at the same time, they can be used to limit the low frequency noise in the system.

GAIN CONTROL INTERFACE

The gain control interface provides an input resistance of approximately 2 MΩ at Pin VGN1 and gain scaling factors from 20 dB/V to 40 dB/V for VREF input voltages of 2.5 V to 1.25 V, respectively. The gain varies linearly in decibels for the center 40 dB of gain range, that is, for VGN equal to 0.4 V to 2.4 V for the 20 dB/V scale and 0.25 V to 1.25 V for the 40 dB/V scale. Figure 37 shows the ideal gain curves when the FBK-to-OUT connection is shorted as described by the following equations:

$$G\ (20\ \text{dB/V}) = 20 \times VGN - 19,\ V_{REF} = 2.500\ \text{V} \quad (3)$$

$$G\ (30\ \text{dB/V}) = 30 \times VGN - 19,\ V_{REF} = 1.6666\ \text{V} \quad (4)$$

$$\text{G}\ (40\ \text{dB/V}) = 40 \times VGN - 19,\ V_{REF} = 1.250\ \text{V} \quad (5)$$

The equations show that all gain curves intercept at the same −19 dB point; this intercept is 14 dB higher (−5 dB) if the FBK-to-OUT connection is left open. Outside the central linear range, the gain starts to deviate from the ideal control law but still provides another 8.4 dB of range. For a given gain scaling, one can calculate V_{REF} as

$$V_{REF} = \frac{2.500\ \text{V} \times 20\ \text{dB/V}}{Gain\ Scale} \quad (6)$$

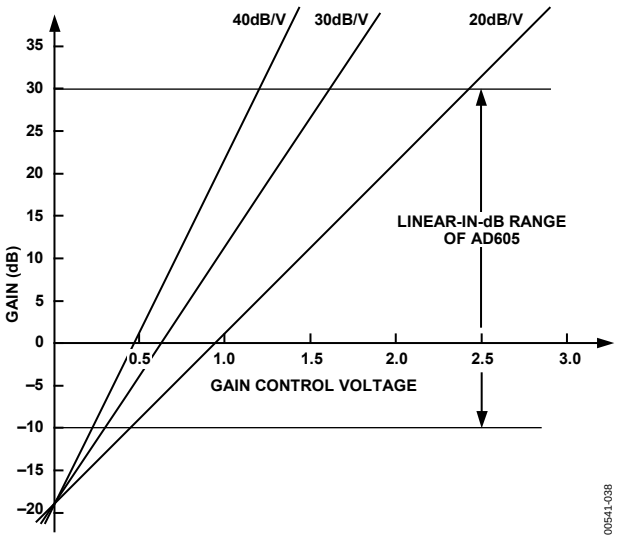


Figure 37. Ideal Gain Curves vs. V_{REF}

Usable gain control voltage ranges are 0.1 V to 2.9 V for the 20 dB/V scale and 0.1 V to 1.45 V for the 40 dB/V scale. VGN voltages of less than 0.1 V are not used for gain control because below 50 mV the channel is powered down. This can be used to conserve power and at the same time gate-off the signal. The supply current for a powered-down channel is 1.9 mA, and the response time to power the device on or off is less than 1 μs.

FIXED GAIN AMPLIFIER AND INTERPOLATOR CIRCUITS—APPLYING AN ACTIVE FEEDBACK AMPLIFIER

A typical X-amp architecture is powered by a dual polarity power supply. Because the AD605 operates from a single supply, a supply common equal to half the value of the supply voltage is required. An active feedback amplifier (AFA) is used to provide a differential input and to implement the feedback loop. The AFA in the AD605 is an op amp with two g_m stages; one is used in the feedback path, and the other is used as a highly linear differential input.

A multisection distributed g_m stage senses the voltages on the ladder network, one stage for each of the ladder nodes. Only a few of the stages are active at any time and are dependent on the gain control voltage.

The AFA makes a differential input structure possible because one of its inputs (G1) is fully differential; this input is made up of a distributed g_m stage. The second input (G2) is used for feedback. The output of G1 is some function of the voltages sensed on the attenuator taps that is applied to a high gain amplifier (A0). Because of negative feedback, the differential input to the high gain amplifier is zero; this in turn implies that the differential input voltage to G2 times g_{m2} (the transconductance of G2) is equal to the differential input voltage to G1 times g_{m1} (the transconductance of G1). Therefore, the overall gain function of the AFA is

$$\frac{V_{OUT}}{V_{ATTEN}} = \frac{g_{m1}}{g_{m2}} \times \frac{R1 \times R2}{R2} \quad (7)$$

where:

V_{OUT} is the output voltage.

V_{ATTEN} is the effective voltage sensed on the attenuator.

$(R1 + R2)/R2 = 42$.

$g_{m1}/g_{m2} = 1.25$; the overall gain is therefore 52.5 (34.4 dB).

The AFA has additional features that include the following: inverting the output signal by switching the positive and negative input to the ladder network; the possibility of using the –IN input as a second signal input; and independent control of the DSX common-mode voltage. Under normal operating conditions, it is best to connect a decoupling capacitor to Pin VOCM, in which case, the common- mode voltage of the DSX is half of the supply voltage; this allows for maximum signal swing. Nevertheless, the common-mode voltage can be shifted up or down by directly applying a voltage to VOCM. It can also be used as another signal input, the only limitation being the rather low slew rate of the VOCM buffer.

If the dc level of the output signal is not critical, another coupling capacitor is normally used at the output of the DSX; again, this is done for level shifting and to eliminate any dc offsets contributed by the DSX (see the AC Coupling section).

The gain range of the DSX is programmable by a resistor connected between Pin FBK and Pin OUT. The possible ranges are –14 dB to +34.4 dB when the pins are shorted together or 0 dB to +48.4 dB when FBK is left open. For the higher gain range, the bandwidth of the amplifier is reduced by a factor of five to about 8 MHz because the gain increased by 14 dB. This is the case for any constant gain bandwidth product amplifier that includes the active feedback amplifier.

APPLICATIONS INFORMATION

The basic circuit in Figure 38 shows the connections for one channel of the AD605 with a gain range of −14 dB to +34.4 dB. The signal is applied at +IN1. The ac coupling capacitors before Pin −IN1 and Pin +IN1 should be selected according to the required lower cutoff frequency. In this example, the 0.1 µF capacitors, together with the 175 Ω of each of the DSX input pins, provide a −3 dB high-pass corner of about 9.1 kHz. The upper cutoff frequency is determined by the amplifier and is 40 MHz.

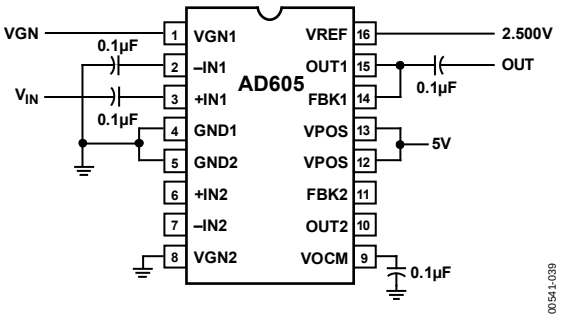


Figure 38. Basic Connections for a Single Channel

As shown in Figure 38, the output is ac-coupled for optimum performance. In the case of connecting to the 10-bit, 40 MSPS ADC, AD9050, ac coupling can be eliminated as long as Pin VOCM is biased by the same 3.3 V common-mode voltage as the AD9050.

Pin VREF requires a voltage of 1.25 V to 2.5 V, with gain scaling between 40 dB/V and 20 dB/V, respectively. Voltage VGN controls the gain; its nominal operating range is from 0.25 V to 2.65 V for 20 dB/V gain scaling and 0.125 V to 1.325 V for 40 dB/V scaling. When this pin is taken to ground, the channel powers down and disables its output.

CONNECTING TWO AMPLIFIERS TO DOUBLE THE GAIN RANGE

Figure 39 shows the two channels of the AD605 connected in series to provide a total gain range of 96.8 dB. When R1 and R2 are shorts, the gain range is from −28 dB to +68.8 dB with a slightly reduced bandwidth of about 30 MHz. The reduction in bandwidth is due to two identical low-pass circuits being connected in series; in the case of two identical single-pole, low-pass filters, the bandwidth is reduced by exactly √2. If R1 and R2 are replaced by open circuits, that is, Pin FBK1 and Pin FBK2 are left unconnected, the gain range shifts up by 28 dB to 0 dB to 96.8 dB. As previously noted, the bandwidth of each individual channel is reduced by a factor of 5 to about 8 MHz because the gain increased by 14 dB. In addition, there is still the √2 reduction because the series connection of the two channels results in a final bandwidth of the higher gain version of about 6 MHz.

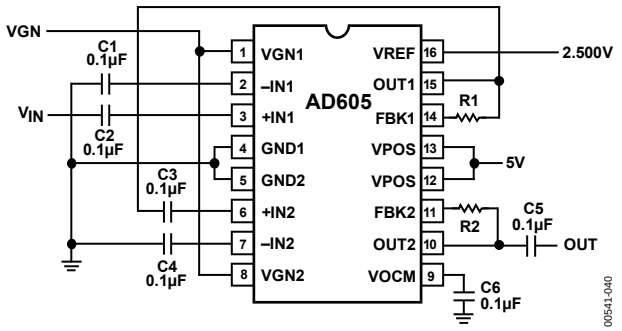


Figure 39. Doubling the Gain Range with Two Amplifiers

Two other easy combinations are possible to provide a gain range of −14 dB to +82.8 dB: make R1 a short and R2 an open, or make R1 an open and R2 a short. The bandwidth for both of these cases is dominated by the channel that is set to the higher gain and is about 8 MHz. From a noise standpoint, the second choice is the best because by increasing the gain of the first amplifier, the noise of the second amplifier has less of an impact on the total output noise. One further observation regarding noise is that by increasing the gain, the output noise increases proportionally; therefore, there is no increase in signal-to-noise ratio. It actually stays fixed.

It should be noted that by selecting the appropriate values of R1 and R2, any gain range between −28 dB to +68.8 dB and 0 dB to +96.8 dB can be achieved with the circuit in Figure 39. When using any value other than shorts and opens for R1 and R2, the final value of the gain range depends on the external resistors matching the on-chip resistors. Because the internal resistors can vary by as much as ±20%, the actual values for a particular gain have to be determined empirically. Note that the two channels within one part match quite well; therefore, R1 tracks R2 in Figure 39.

C3 is not required because the common-mode voltage at Pin OUT1 should be identical to the one at Pin +IN2 and Pin −IN2. However, because only 1 mV of offset at the output of the first DSX introduces an offset of 53 mV when the second DSX is set to the maximum gain of the lowest gain range (34.4 dB), and 263 mV when set to the maximum gain of the highest gain range (48.4 dB), it is important to include ac coupling to get the maximum dynamic range at the output of the cascaded amplifiers. C5 is necessary if the output signal needs to be referenced to any common-mode level other than half of the supply as is provided by Pin OUT2.

Figure 40 shows the gain vs. VGN for the circuit in Figure 39 at 1 MHz and the lowest gain range (−14 dB to +34.4 dB). Note that the gain scaling is 40 dB/V, double the 20 dB/V of an individual DSX; this is the result of the parallel connection of the gain control inputs, VGN1 and VGN2. The gain can also be sequentially increased by first increasing the gain of Channel 1 and then Channel 2. In this case, VGN1 and VGN2 are driven from separate voltage sources, for instance two separate DACs. Figure 41 shows the gain error of Figure 39.

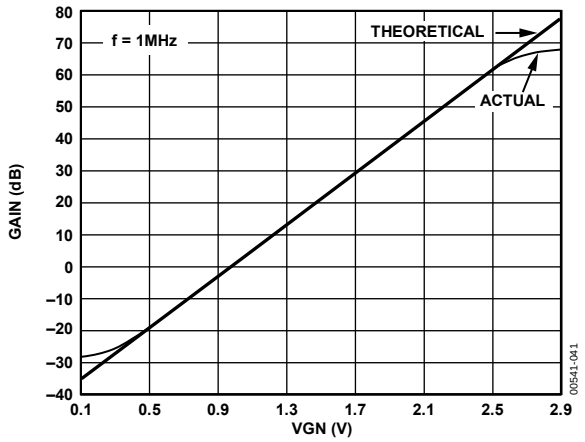


Figure 40. Gain vs. VGN for the Circuit in Figure 39

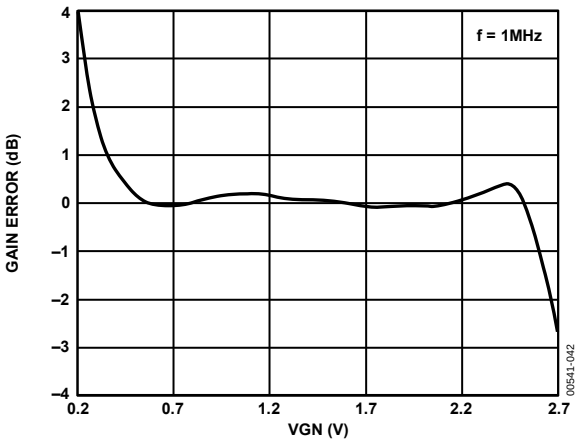


Figure 41. Gain Error vs. VGN for the Circuit in Figure 39

EVALUATION BOARD

The AD605-EVALZ provides a platform for the circuit designer to become familiar with the many operating and performance features of the AD605 variable gain amplifier. It is a factory-designed, surface-mount assembly fully tested and ready for service. Figure 42 is a photograph of the AD605-EVALZ. Multiple inputs, test points, and jumpers provide circuit configurations that support any of the operating options of the device. Figure 43 is a schematic of the board.

Power is required from only a single 5 V supply capable of supplying 55 mA to 60 mA quiescent current.

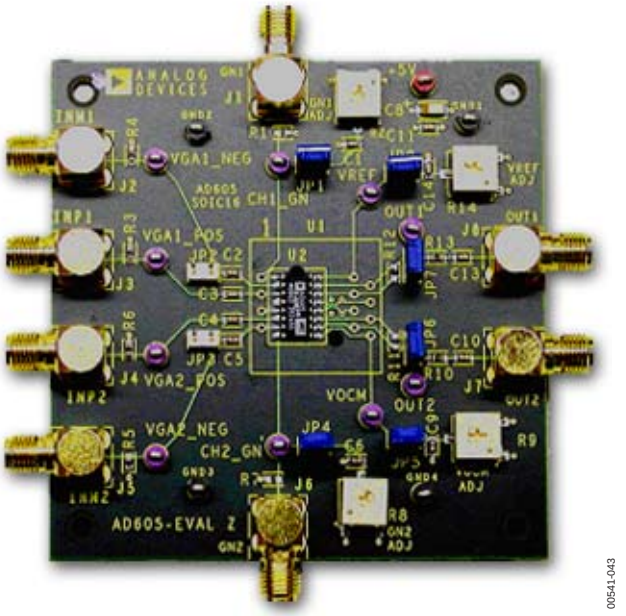


Figure 42. AD605–EVALZ Evaluation Board

INPUT CONNECTIONS

The AD605 VGA accepts differential or single-ended input signals and provides single-ended outputs. The SMA connectors enable either configuration to be used, as well as the output and gain control signals. Each of the I/O ports is also available at a test-loop labeled for easy identification.

The input resistance at each of the four input SMA connectors is 50 Ω, consisting of the 175 Ω, ±40 Ω resistance of the attenuator ladder network in parallel with the external 69.8 Ω resistors. For single-ended operation, unused inputs can be left disconnected or optional jumpers installed. Either VGA input is usable; for noninverting operation, the INPx is used, and for signal inversion, the INMx is used.

ADJUSTING GAIN, COMMON-MODE, AND REFERENCE LEVELS

The gain of each channel is adjusted with trimmers, GN1ADJ and GN2ADJ. Trimmer VREF ADJ adjusts the gain scaling in dB/V (or gain slope), and VOCM ADJ adjusts the output common-mode voltage for both channels. For dynamic gain control, JP1 and JP4 can be removed and the signal applied at the SMA connectors, GN1 and GN2.

OUTPUT CONNECTIONS

SMA connectors, OUT1 and OUT2, are the output connectors. Series resistors and capacitors are included for termination and dc blocking purposes. The output of the AD605 has a common-mode value of one-half the supply (unless amended by a voltage applied to the VCM pin).

Table 4 lists jumpers and their functions, and Figure 44 shows the evaluation board in a typical test configuration.

Table 4. Table of Jumpers

Jumper	Function	Default Configuration
JP1	Connects trimmer GN1ADJ to pin VGN1. This jumper can be removed for an ac signal at VGN1.	Installed
JP2	Grounds the IN1 pin via C2.	User supplied
JP3	Grounds the IN2 pin via C5.	User supplied
JP4	Connects trimmer GN2ADJ to Pin VGN2. This jumper can be removed for an ac signal at VGN2.	Installed
JP5	Connects trimmer VOCMADJ to the VOCM pin. This jumper can be removed for the half supply default VOCM.	Installed
JP6	Shifts the gain of Channel 2 up or down by 14 dB.	Installed
JP7	Shifts the gain of Channel 1 up or down by 14 dB.	Installed
JP8	Connects trimmer VREFADJ to the VREF pin to change the gain slope.	Installed

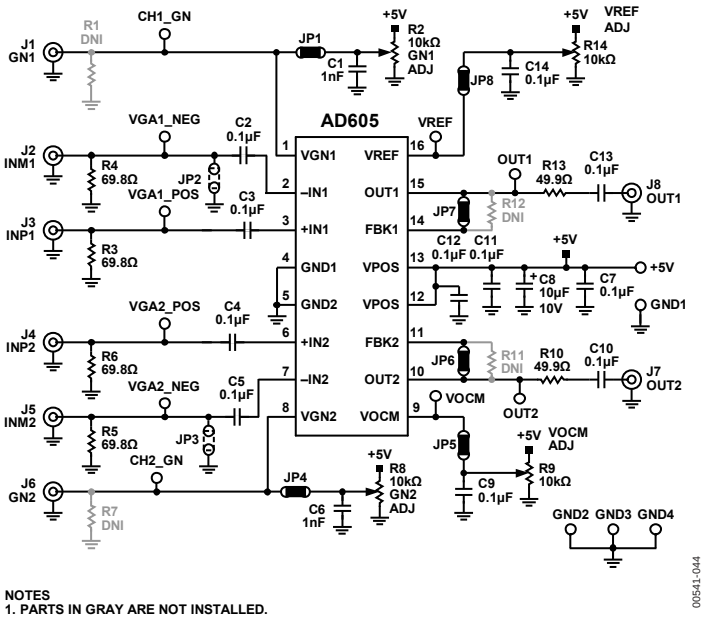


Figure 43. Schematic Diagram of the AD605-EVALZ Evaluation Board

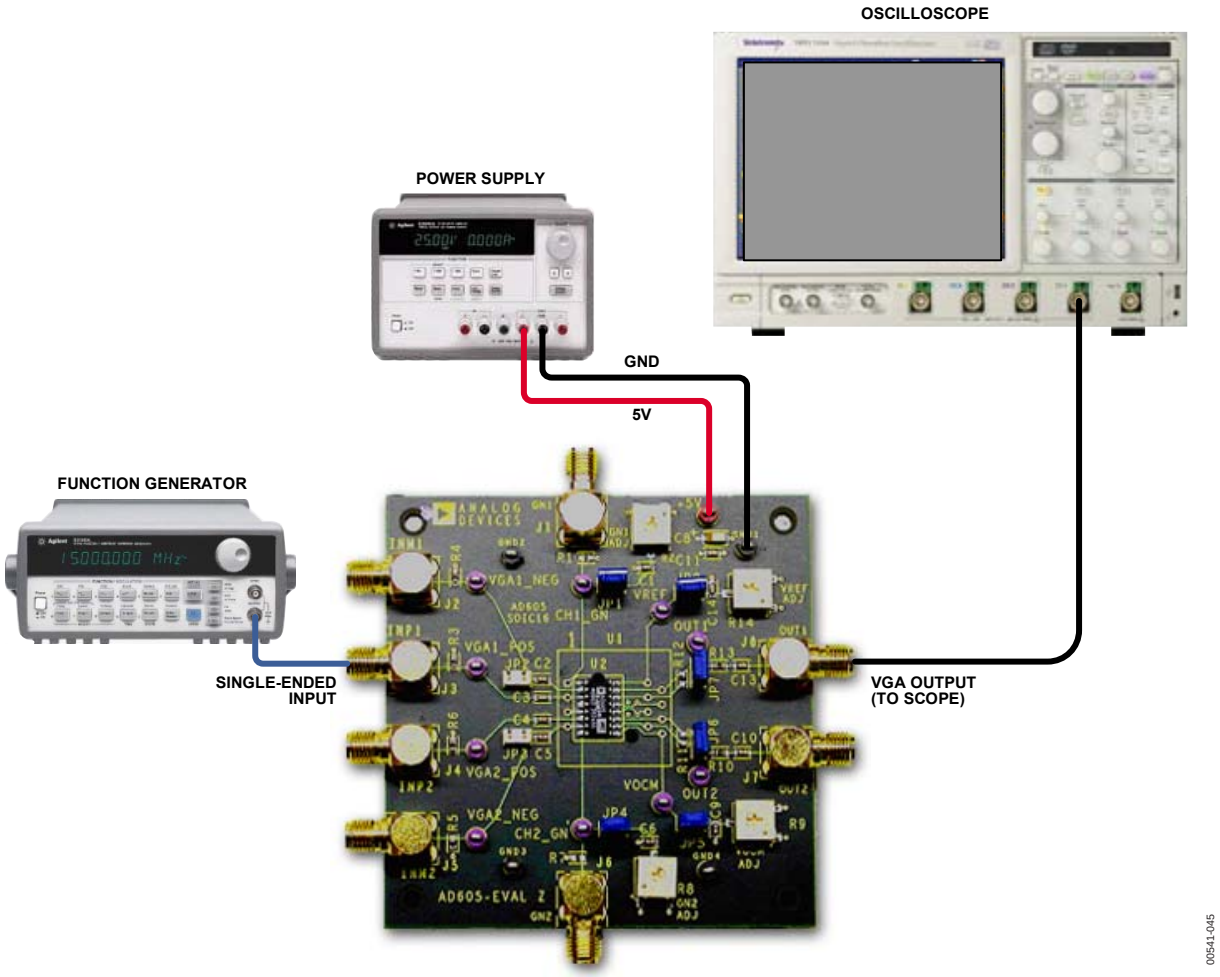


Figure 44. Typical Test Configuration of the AD605-EVALZ

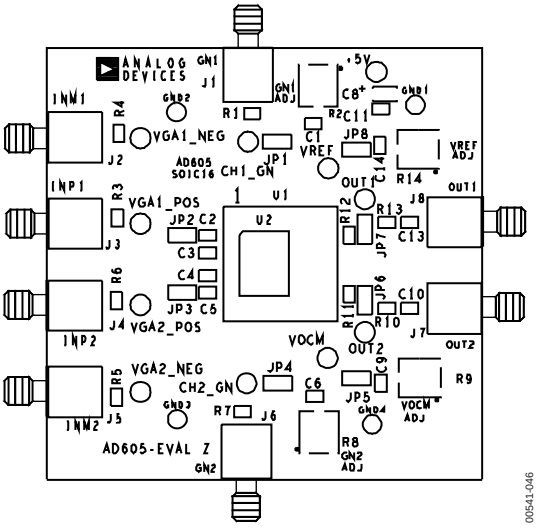


Figure 45. AD605-EVALZ Assembly

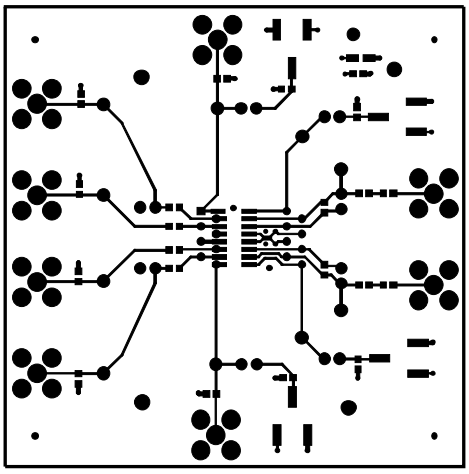


Figure 46. AD605-EVALZ Primary Side Copper

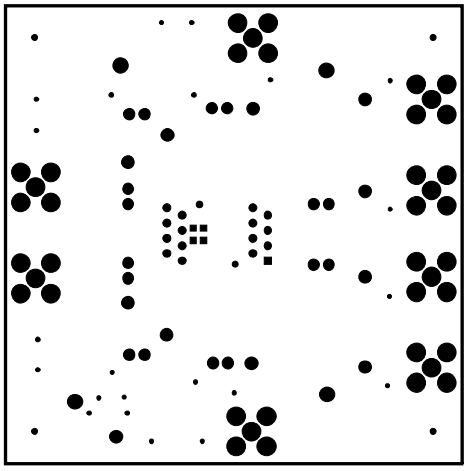


Figure 47. AD605-EVALZ Secondary Side Copper

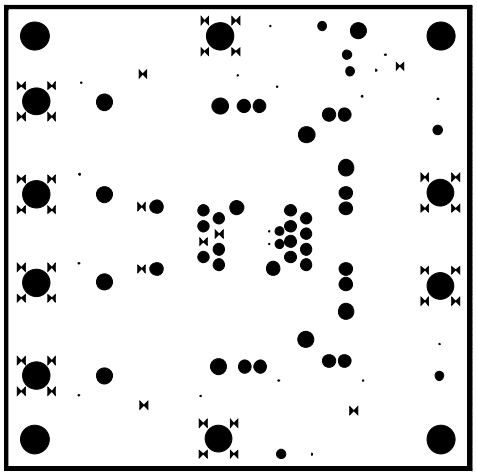


Figure 48. AD605-EVALZ Internal Ground Plane

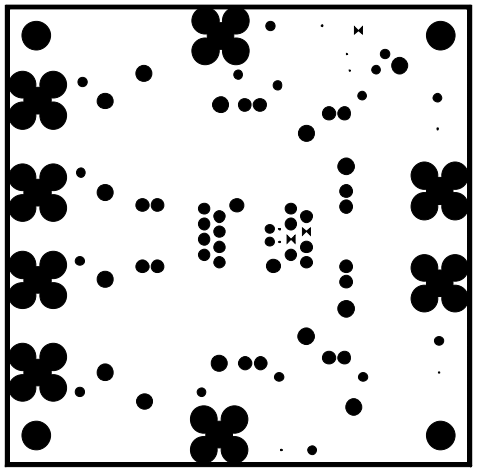


Figure 49. AD605-EVALZ Internal Power Plane

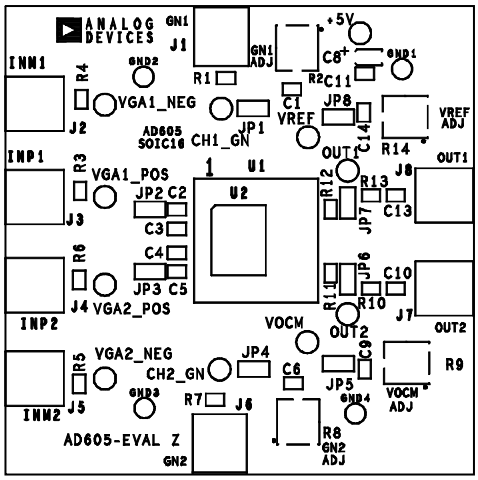
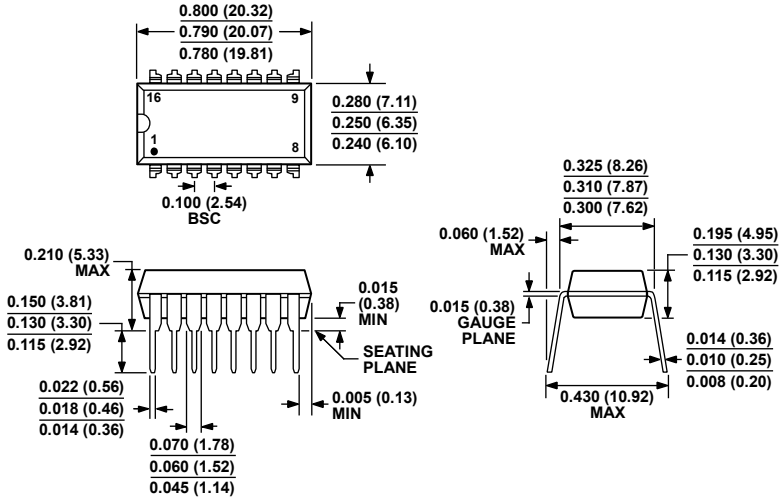


Figure 50. AD605-EVALZ Primary Side Silkscreen

OUTLINE DIMENSIONS

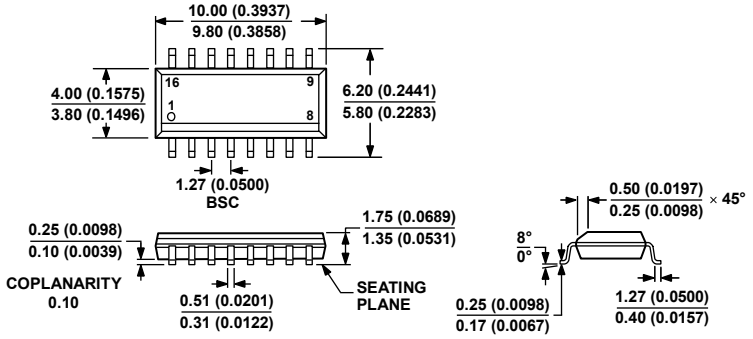


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 51. 16-Lead Plastic Dual In-Line Package [PDIP]
(N-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 52. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD605AN	−40°C to +85°C	16-Lead PDIP	N-16
AD605ANZ[1]	−40°C to +85°C	16-Lead PDIP	N-16
AD605AR	−40°C to +85°C	16-Lead SOIC_N	R-16
AD605AR-REEL	−40°C to +85°C	16-Lead SOIC_N, 13" Tape and Reel	R-16
AD605AR-REEL7	−40°C to +85°C	16-Lead SOIC_N, 7" Tape and Reel	R-16
AD605ARZ[1]	−40°C to +85°C	16-Lead SOIC_N	R-16
AD605ARZ-RL[1]	−40°C to +85°C	16-Lead SOIC_N, 13" Tape and Reel	R-16
AD605ARZ-R7[1]	−40°C to +85°C	16-Lead SOIC_N, 7" Tape and Reel	R-16
AD605BN	−40°C to +85°C	16-Lead PDIP	N-16
AD605BR	−40°C to +85°C	16-Lead SOIC_N	R-16
AD605BR-REEL	−40°C to +85°C	16-Lead SOIC_N, 13" Tape and Reel	R-16
AD605BR-REEL7	−40°C to +85°C	16-Lead SOIC_N, 7" Tape and Reel	R-16
AD605BRZ[1]	−40°C to +85°C	16-Lead SOIC_N	R-16
AD605BRZ-RL[1]	−40°C to +85°C	16-Lead SOIC_N, 13" Tape and Reel	R-16
AD605BRZ-R7[1]	−40°C to +85°C	16-Lead SOIC_N, 7" Tape and Reel	R-16
AD605-EVALZ[1]		Evaluation Board	
AD605ACHIPS		DIE	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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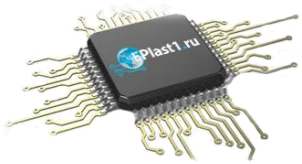
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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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