



# PMT560ENEA

100 V N-channel Trench MOSFET

14 July 2016

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power SOT223 (SC-73) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic level compatible
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

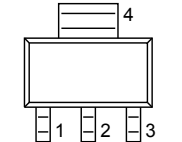
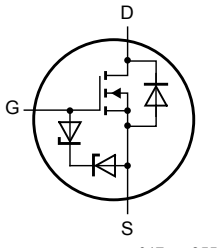
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_J = 25\text{ °C}$		-	-	100	V
$V_{GS}$	gate-source voltage			-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	1.1	A
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 1.1\text{ A}; T_J = 25\text{ °C}$		-	527	715	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-73 (SOT223)	 017aaa255
2	D	drain		
3	S	source		
4	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMT560ENEA	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMT560ENEA	56ENEA

## 8. Limiting values

**Table 5. Limiting values**

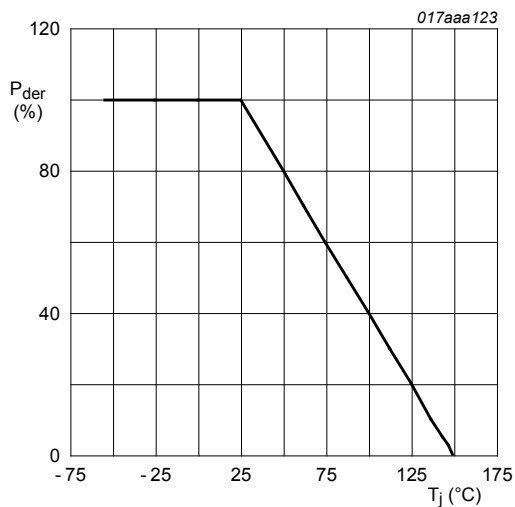
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	100	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.1	A
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	0.7	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	4.4	A
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $I_D = 0.1\text{ A}$ ; DUT in avalanche (unclamped)		-	5.3	mJ
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	750	mW
			[1]	-	1.9	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	6.25	W
$T_j$	junction temperature			-55	150	$^{\circ}\text{C}$
$T_{amb}$	ambient temperature			-55	150	$^{\circ}\text{C}$
$T_{stg}$	storage temperature			-65	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	1.1	A
<b>ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain  $6\text{ cm}^2$ .

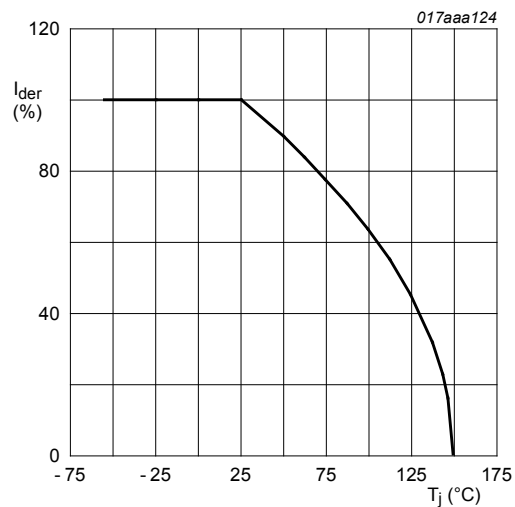
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



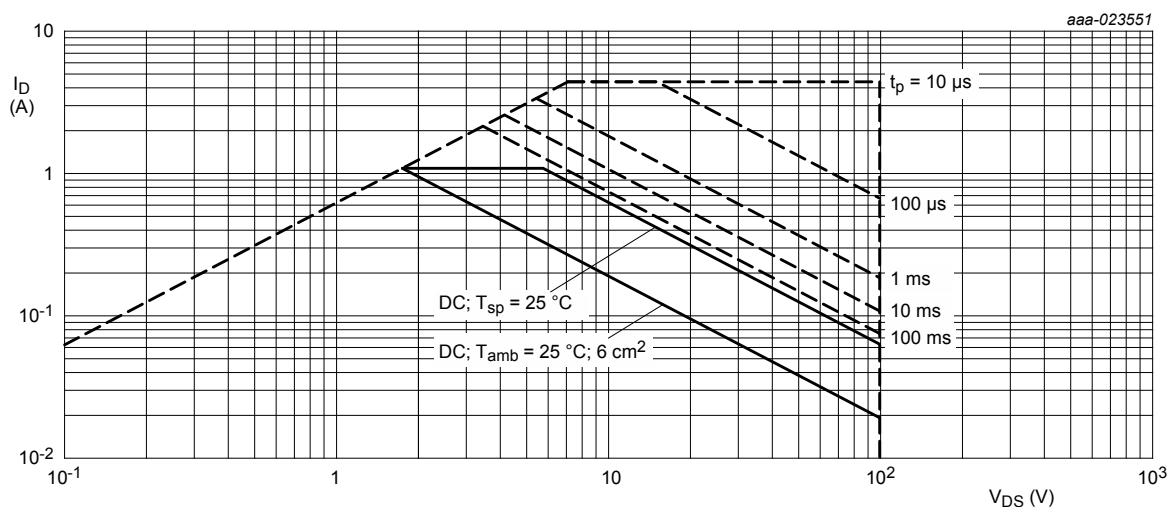
**Fig. 1. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 2. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	145	167	K/W
			[2]	-	57	66	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	13	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

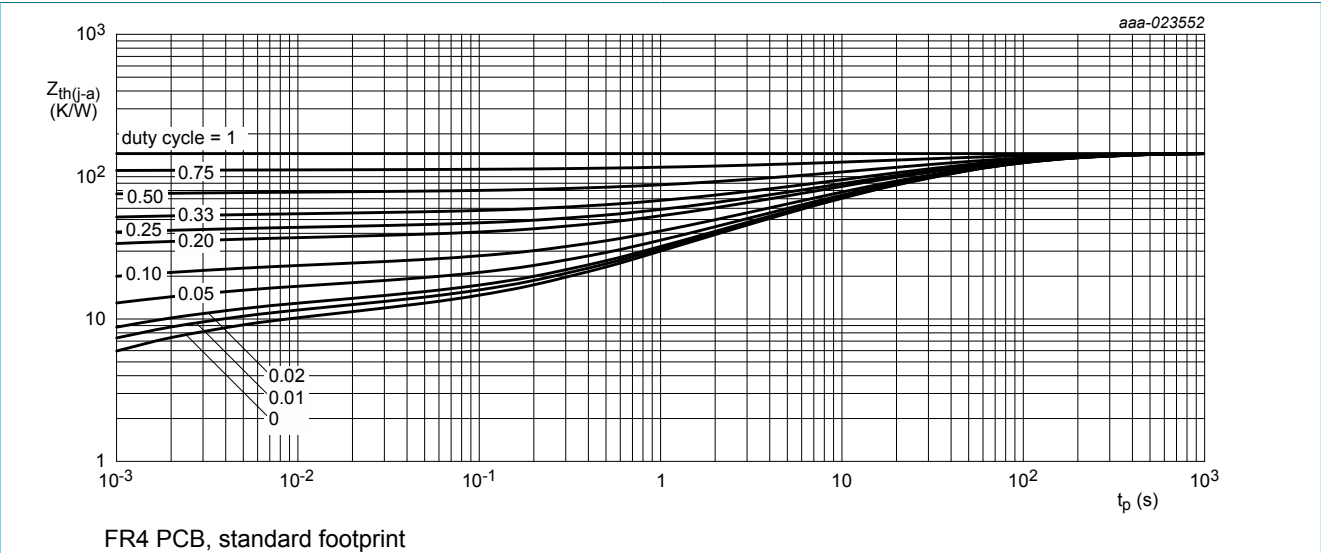


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

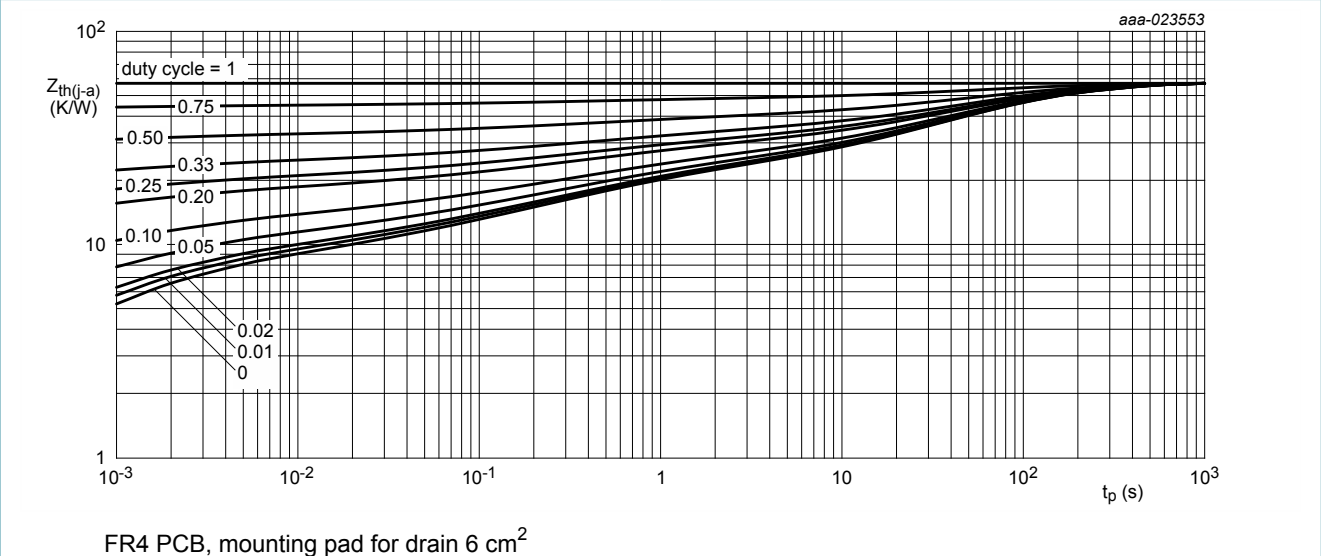


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		100	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		1.3	1.7	2.7	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	15	μA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-15	μA
		V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 1.1 A; T <sub>j</sub> = 25 °C		-	527	715	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 1.1 A; T <sub>j</sub> = 150 °C		-	1.19	1.62	Ω
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 1 A; T <sub>j</sub> = 25 °C		-	555	805	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 1.1 A; T <sub>j</sub> = 25 °C		-	3.5	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	7.6	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 1.1 A; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C		-	2.9	4.4	nC
Q <sub>GS</sub>	gate-source charge			-	0.3	-	nC
Q <sub>GD</sub>	gate-drain charge			-	0.7	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	112	-	pF
C <sub>oss</sub>	output capacitance			-	9	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	7	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 1.1 A; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	6	-	ns
t <sub>r</sub>	rise time			-	8	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	10	-	ns
t <sub>f</sub>	fall time			-	5	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.1 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.9	1.2	V

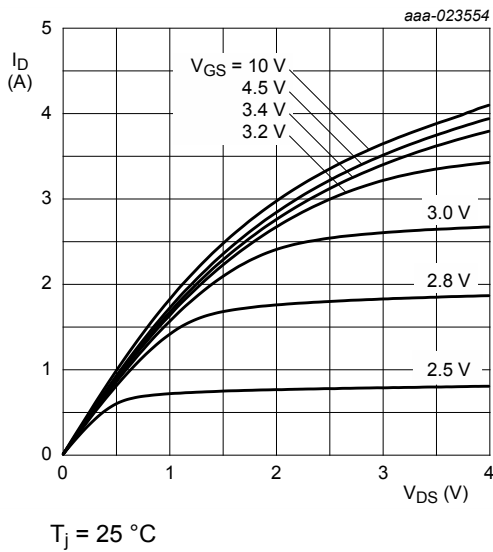


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

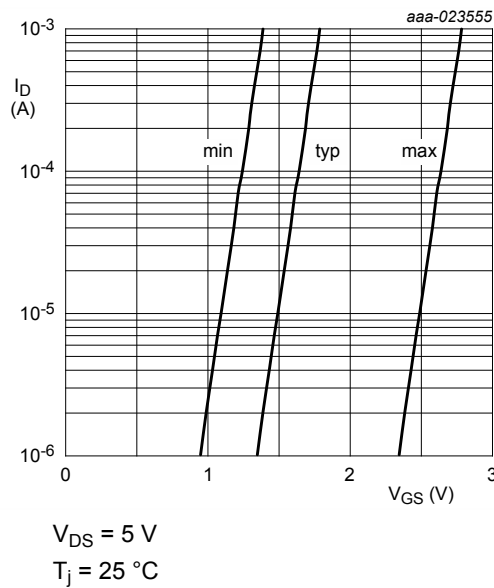


Fig. 7. Subthreshold drain current as a function of gate-source voltage

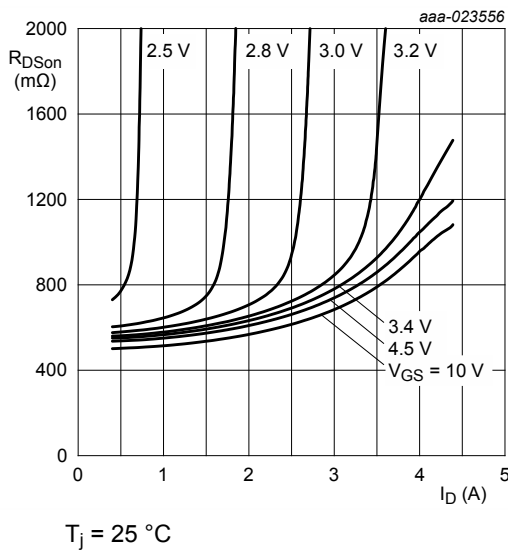


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

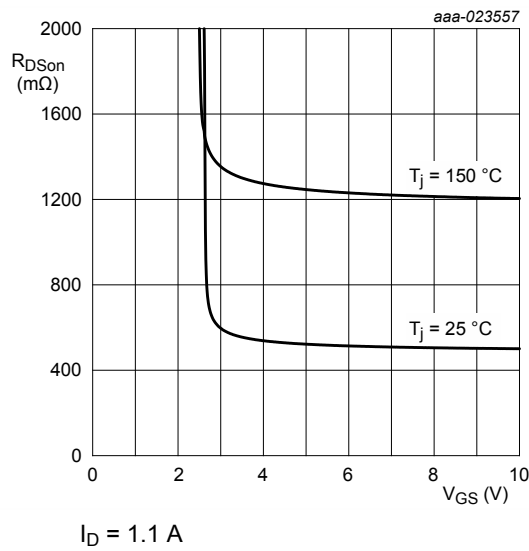


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

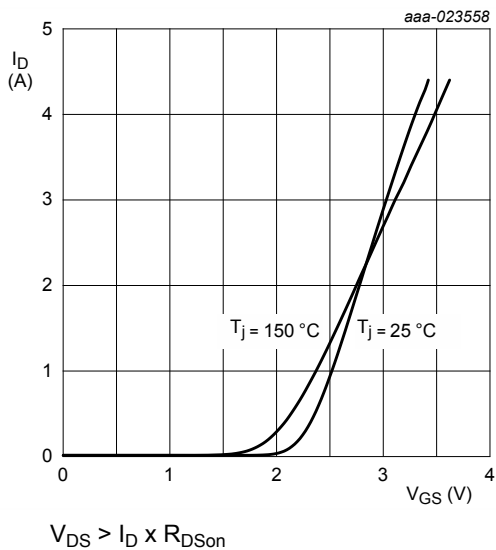


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

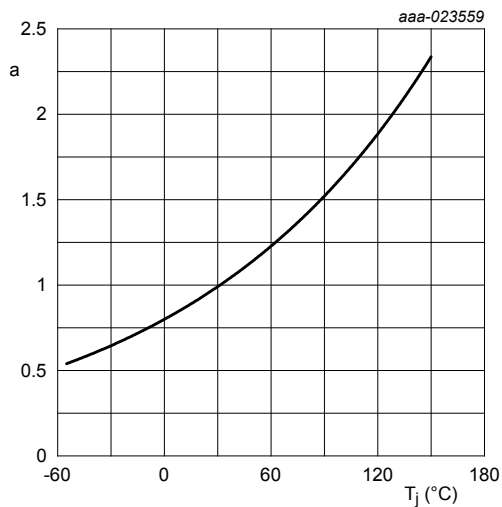


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^{\circ}\text{C})}$$

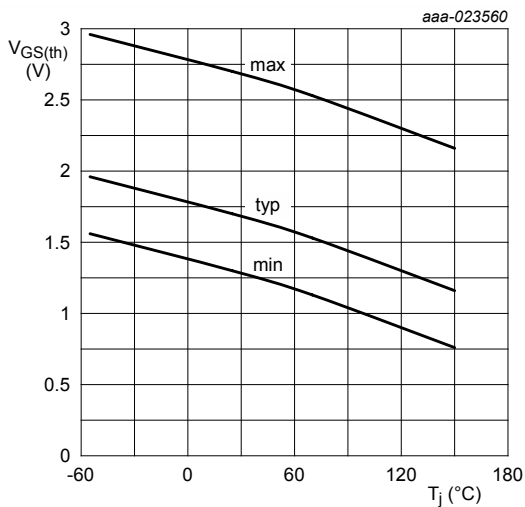


Fig. 12. Gate-source threshold voltage as a function of junction temperature

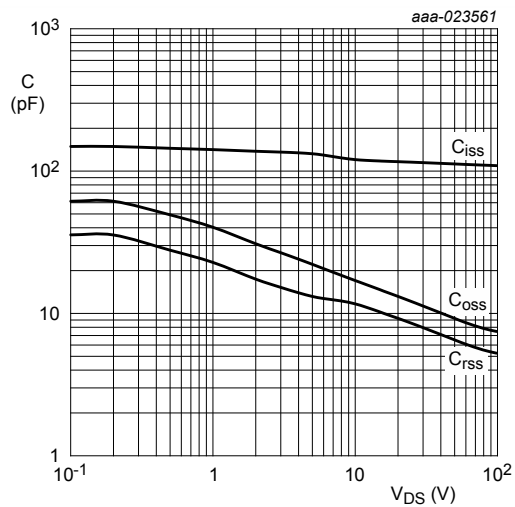


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



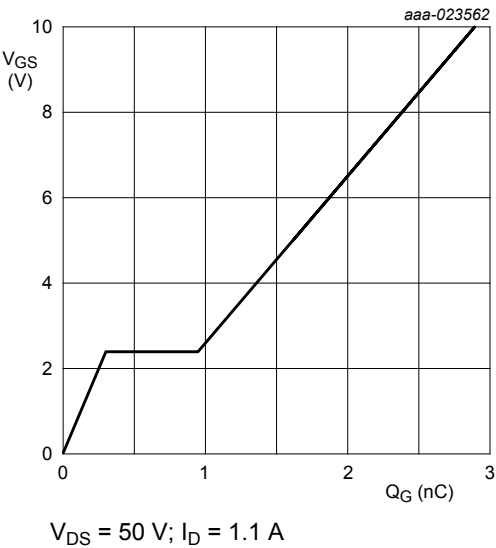


Fig. 14. Gate-source voltage as a function of gate charge; typical values

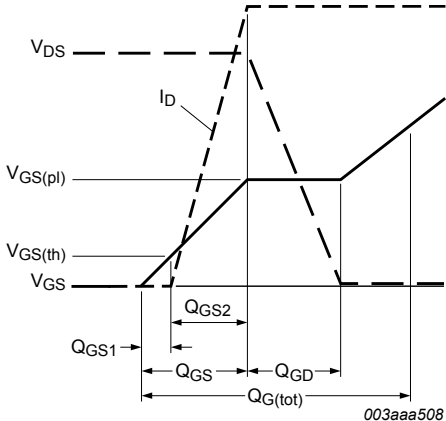
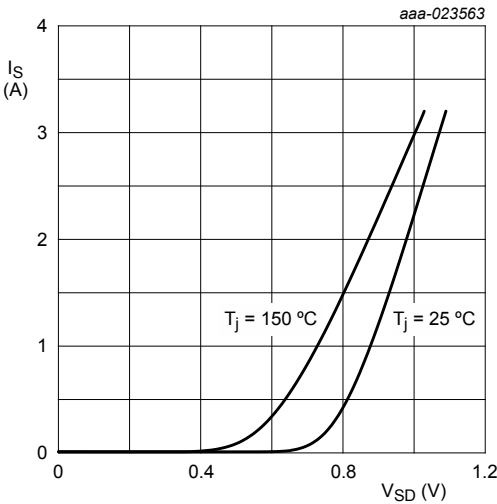


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

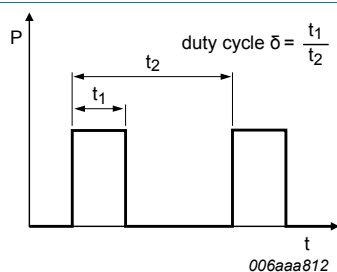


Fig. 17. Duty cycle definition

### 11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

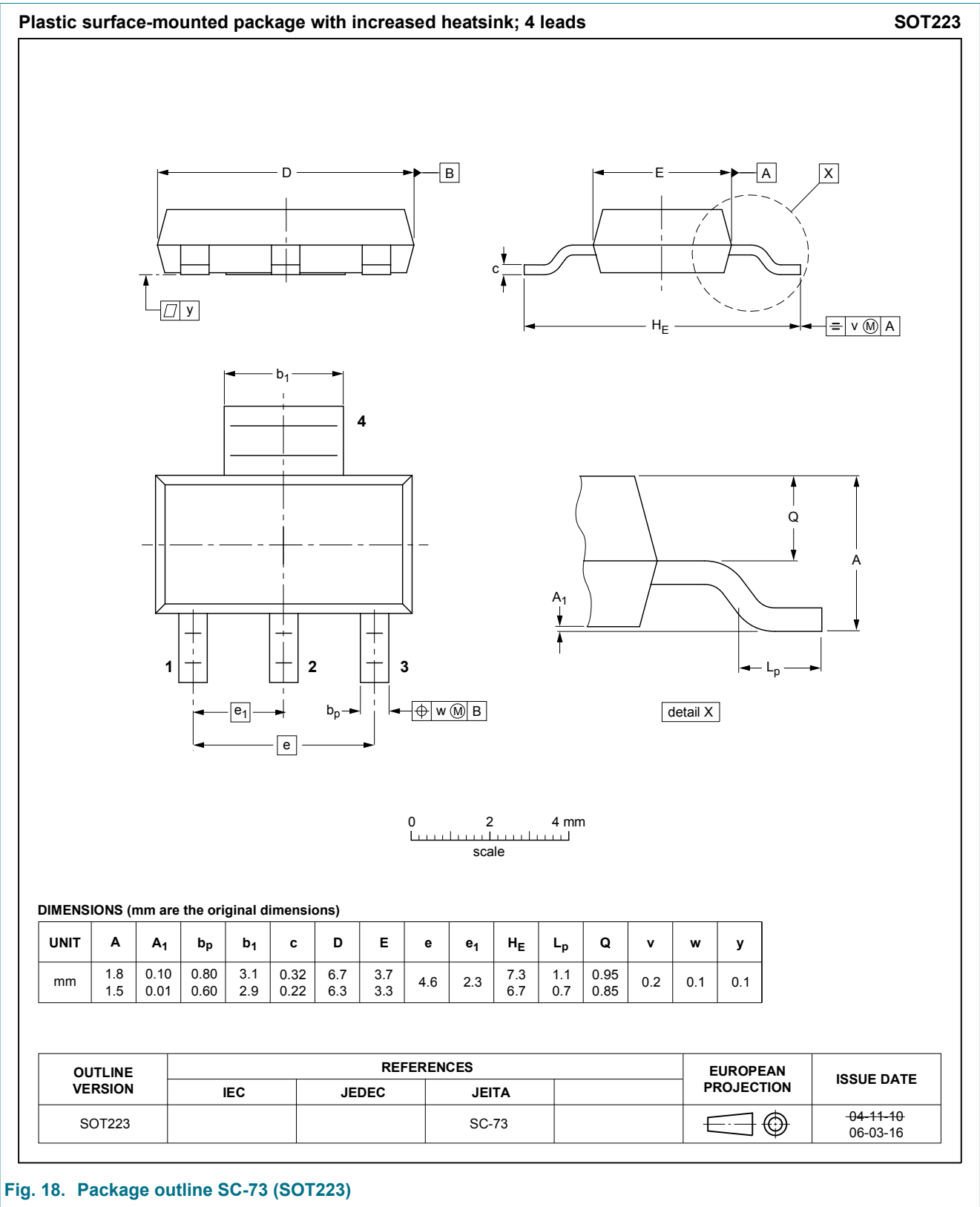


Fig. 18. Package outline SC-73 (SOT223)

13. Soldering

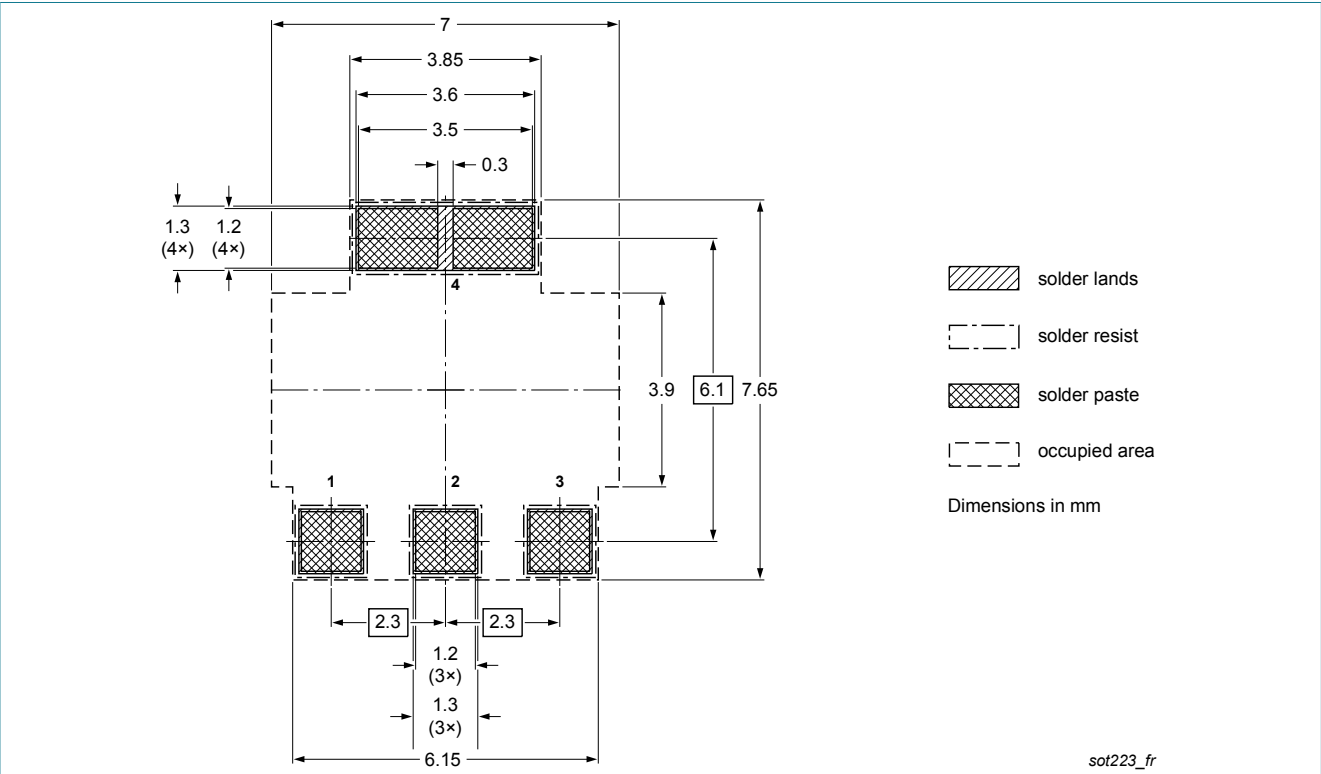


Fig. 19. Reflow soldering footprint for SC-73 (SOT223)

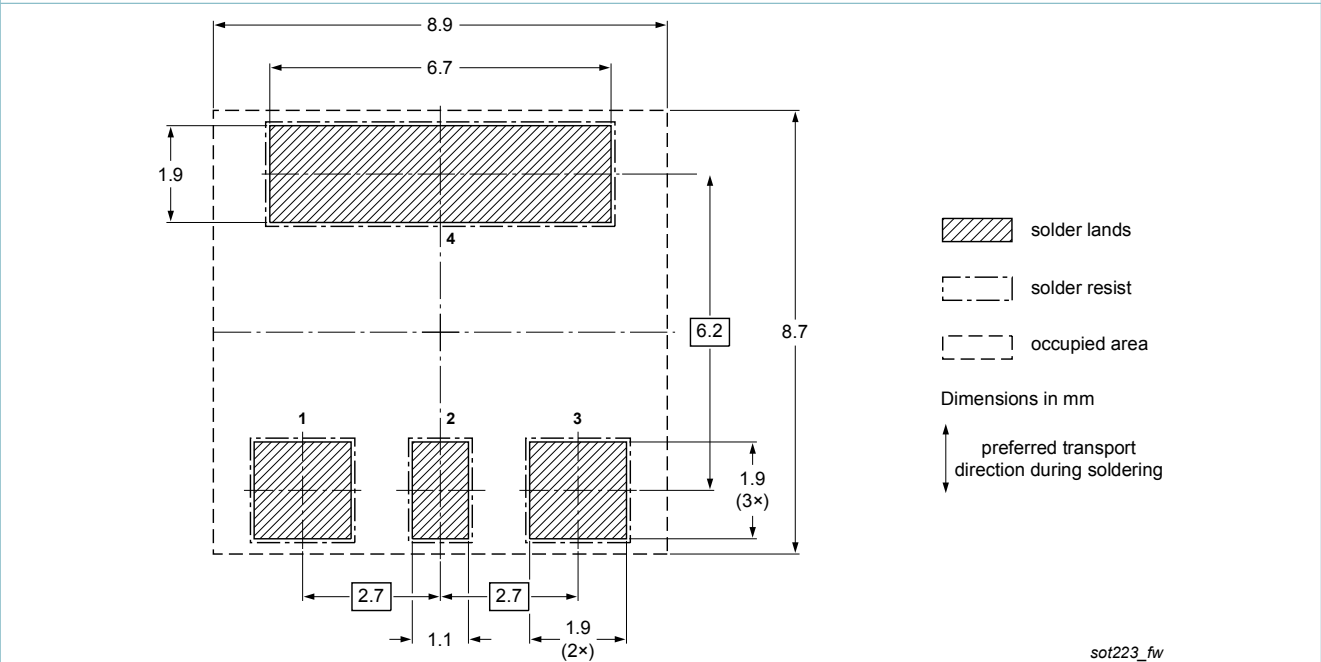


Fig. 20. Wave soldering footprint for SC-73 (SOT223)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMT560ENEA v.1	20160714	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 14 July 2016





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