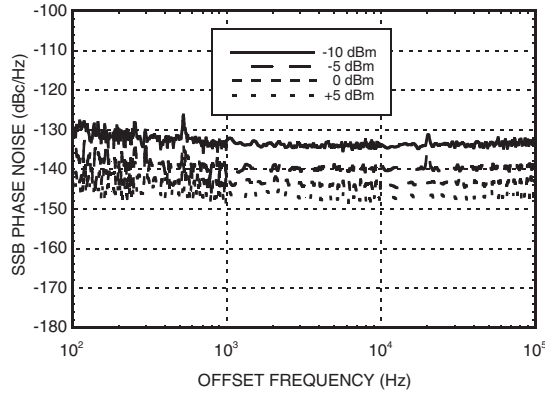




**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**

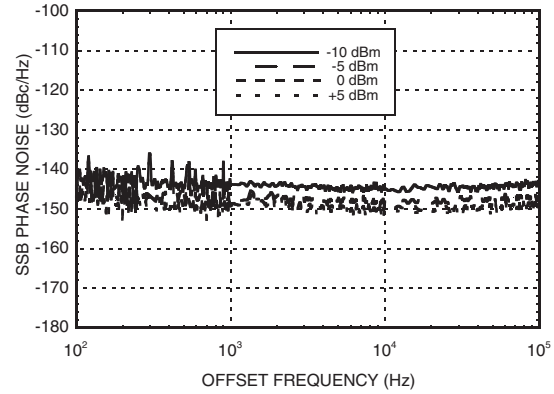
Phase Noise Floor [1][2][3]

Ref = Sine Wave, Vcc = 4.75V



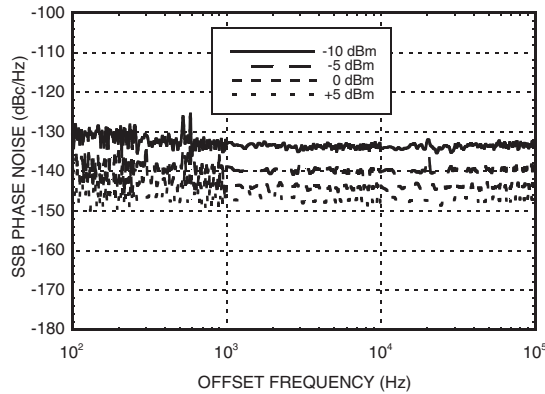
Phase Noise Floor [1][2][3]

Ref = Square Wave, Vcc = 4.75V



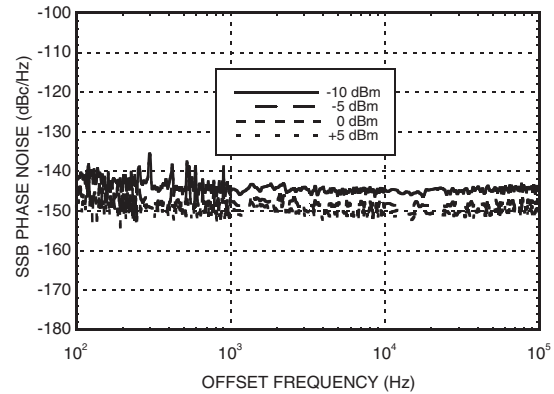
Phase Noise Floor [1][2][3]

Ref = Sine Wave, Vcc = 5V



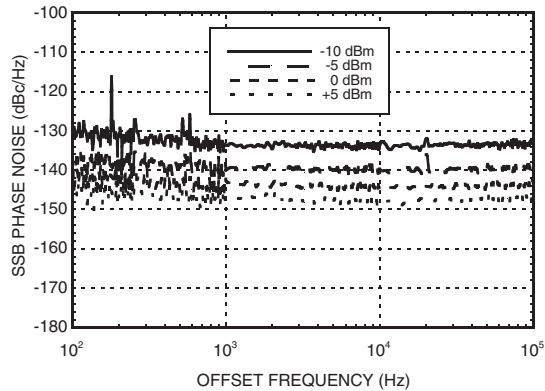
Phase Noise Floor [1][2][3]

Ref = Square Wave, Vcc = 5V



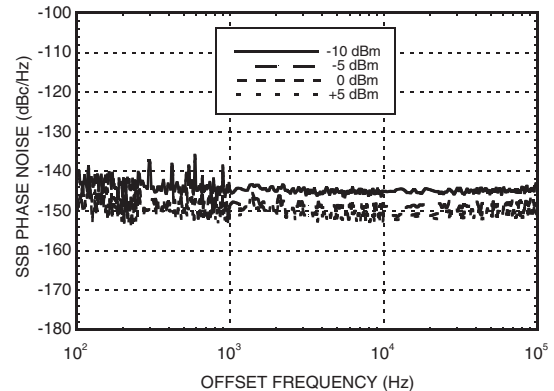
Phase Noise Floor [1][2][3]

Ref = Sine Wave, Vcc = 5.25V



Phase Noise Floor [1][2][3]

Ref = Square Wave, Vcc = 5.25V



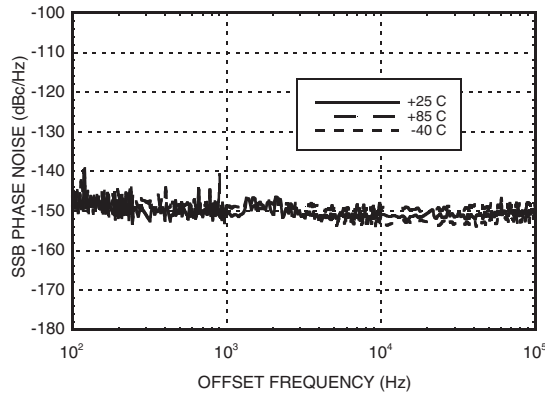
[1] Phase Noise Floor vs Offset Frequency with varying Ref Power Level
 [2] Fin = 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70
 [3] Phase Noise Floor remains constant beyond 100 kHz offset frequency



7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

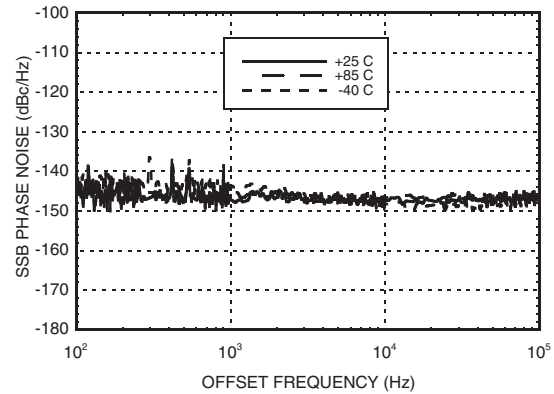
Phase Noise Floor [1][2][3]

Ref = Square Wave @ 5 dBm, Vcc = 5V

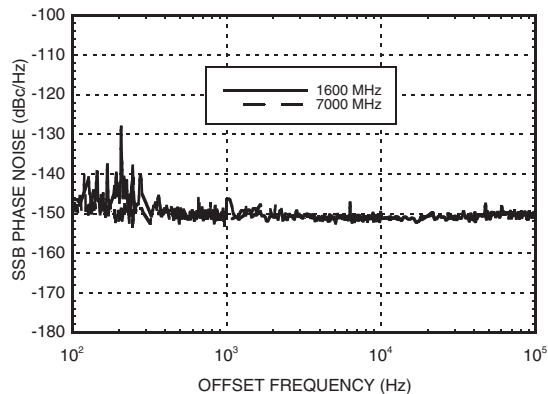


Phase Noise Floor [1][2][3]

Ref = Sine Wave @ 5 dBm, Vcc = 5V



Phase Noise Floor vs Offset Frequency with varying Fin @ 0 dBm, Ref = 100 MHz Square Wave @ 5 dBm, Vcc = 5V [3]



Absolute Maximum Ratings

RF Input (Vcc = +5V)	+10 dBm
Supply Voltage (Vcc)	+5.5V
Logic Inputs	-0.5V to (0.5V + Vcc)
Junction Temperature (Tc)	135 °C
Continuous P _{diss} (T = 85 °C) (derate 87 mW/°C above 85 °C)	4.3 W
Thermal Resistance (Junction to ground paddle)	11.60 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical DC Characteristics @ Vcc = +5V

Symbol	Characteristics	+25°C			Units
		Min.	Typ.	Max.	
I _{cc}	Power Supply Current	310	345	380	mA
V _{oh}	Output High Voltage, (NU, ND)	5	5	5	V
V _{ol}	Output Low Voltage, (NU, ND)	2.9	3.0	3.1	V

Typical Supply Current vs. Vcc

Vcc (V)	I _{cc} (mA)
4.75	318
5.00	345
5.25	369

Note: HMC669LP5(E) will work over full voltage range above.

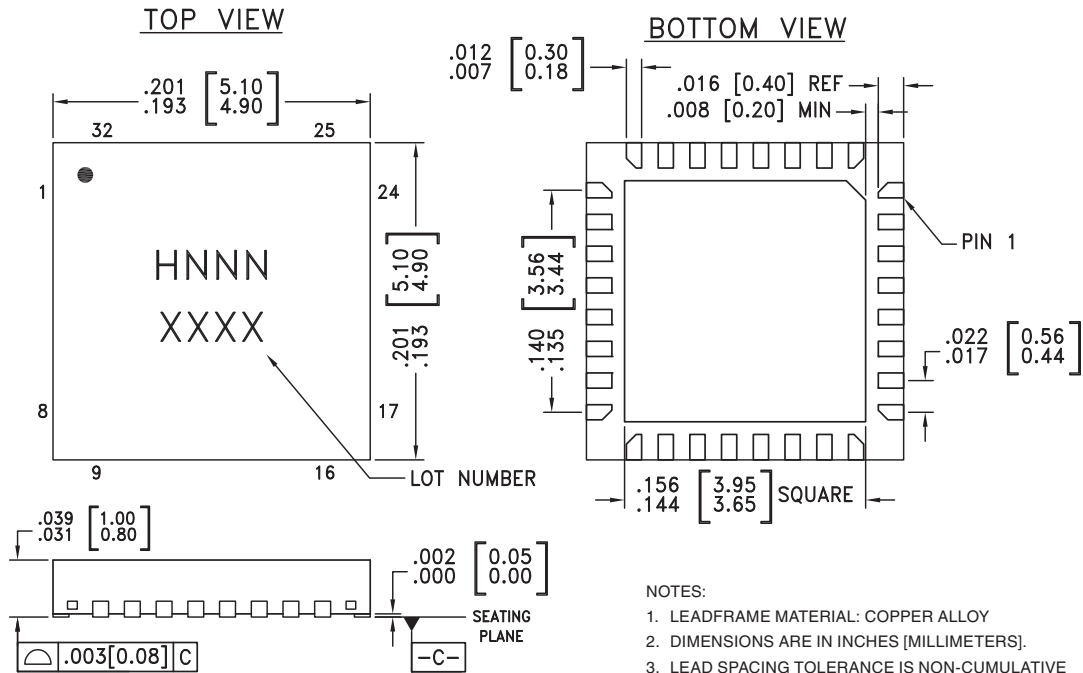


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

[1] Phase Noise Floor vs Offset Frequency over temperature

[2] Fin= 7000 MHz @ 0 dBm, Ref Frequency = 100 MHz, N = 70

[3] Phase Noise Floor remains constant beyond 100 kHz offset frequency


**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**
Outline Drawing

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC699LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 ^[1]	H699 XXXX
HMC699LP5(E)	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H699 XXXX

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX



7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

Pin Description

Pin Number	Function	Description	Interface Schematic
1	LD	Pulsed output. Average "LOW" = UNLOCKED. Average "HIGH" = LOCKED	
2	INV	PFD INVERT function CMOS compatible input control bit Logic "LOW" = NORMAL Logic "HIGH" = INVERT	
3, 6 - 8, 17, 19, 20, 24, 26, 29, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
4, 5, 18, 25	Vcc1, Vcc3, Vcc2, Vcc_pd	Supply Voltage 5V ±0.25V	
9 - 14	N0 - N5	CMOS compatible control input bit 0 (LSB) - 5	
15	FIN	(These pins are AC coupled and must be DC Blocked externally.) Frequency Input	
16	NFIN	Frequency Input Complement	
22, 23	S1, S0	CMOS compatible Control Input bit 0 (LSB) -1	

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7 GHz INTEGER N SYNTHESIZER CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)

Pin Description (Continued)

Pin Number	Function	Description	Interface Schematic
28	REF	Reference Input	
27	NREF	Reference Input Complement (These pins are AC coupled and must be DC Blocked externally.)	
30	ND	Down Output	
31	NU	Up Output	
Ground Paddle	GND	Package bottom has an exposed ground paddle that must be connected to RF/DC ground	


**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**
HMC699LP5(E) Programming

The decimal value of A counter and S counter can be defined as:

$$A = \text{int} \left(\frac{N}{8} \right) - 1$$

and $S = N - 8(A + 1)$

where $N = 16$ to 519

For a valid division ratio N, the A counter and S counter must satisfy the condition: $A + 1 \geq S$

Therefore, $N = 16$ to 54 will result into non-continuous division ratio

and $N = 56$ to 519 will be continuous division ratio.

Example: Given a reference frequency, $F_{\text{ref}} = 11$ MHz, and VCO output frequency, $F_{\text{vco}} = (198$ to $297)$ MHz, results in $N = 18$ to 27 . The decimal value of A counter and S counter for $N = 18$ will be:

$$A = \text{int} \left(\frac{18}{8} \right) - 1 = 1$$

and $S = 18 - 8(1 + 1) = 2$

Since the calculated value of A and S satisfy the condition of $A + 1 \geq S$, the $N = 18$ is usable division ratio.

The division ratio, $N = 23$, however, will result in $A = 1$ and $S = 7$. Under the condition $A + 1 \geq S$, the division ratio $N = 23$ is not usable.

In this example, the division ratio, $N = 19$ to 23 cannot be programmed and therefore, the frequency range of 209 MHz to 253 MHz cannot be used.

HMC699LP5(E) Programming Truth Table, Continuous Division Ratios

Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
56	6	0	0	1	1	0	0	0	0	0	0
57	6	1	0	1	1	0	0	0	1	0	0
58	6	2	0	1	1	0	0	0	0	1	0
59	6	3	0	1	1	0	0	0	1	1	0
60	6	4	0	1	1	0	0	0	0	0	1
61	6	5	0	1	1	0	0	0	0	0	1
62	6	6	0	1	1	0	0	0	0	1	1
63	6	7	0	1	1	0	0	0	1	1	1
64	7	0	1	1	1	0	0	0	0	0	0
65	7	1	1	1	1	0	0	0	1	0	0
66	7	2	1	1	1	0	0	0	0	1	0
67	7	3	1	1	1	0	0	0	1	1	0


**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**
HMC699LP5(E) Programming Truth Table, Continuous Division Ratios (Continued)

Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
512	63	0	1	1	1	1	1	1	0	0	0
513	63	1	1	1	1	1	1	1	1	0	0
514	63	2	1	1	1	1	1	1	0	1	0
515	63	3	1	1	1	1	1	1	1	1	0
516	63	4	1	1	1	1	1	1	0	0	1
517	63	5	1	1	1	1	1	1	1	0	1
518	63	6	1	1	1	1	1	1	0	1	1
519	63	7	1	1	1	1	1	1	1	1	1

HMC699LP5(E) Programming Truth Table, Non-Continuous Division Ratios

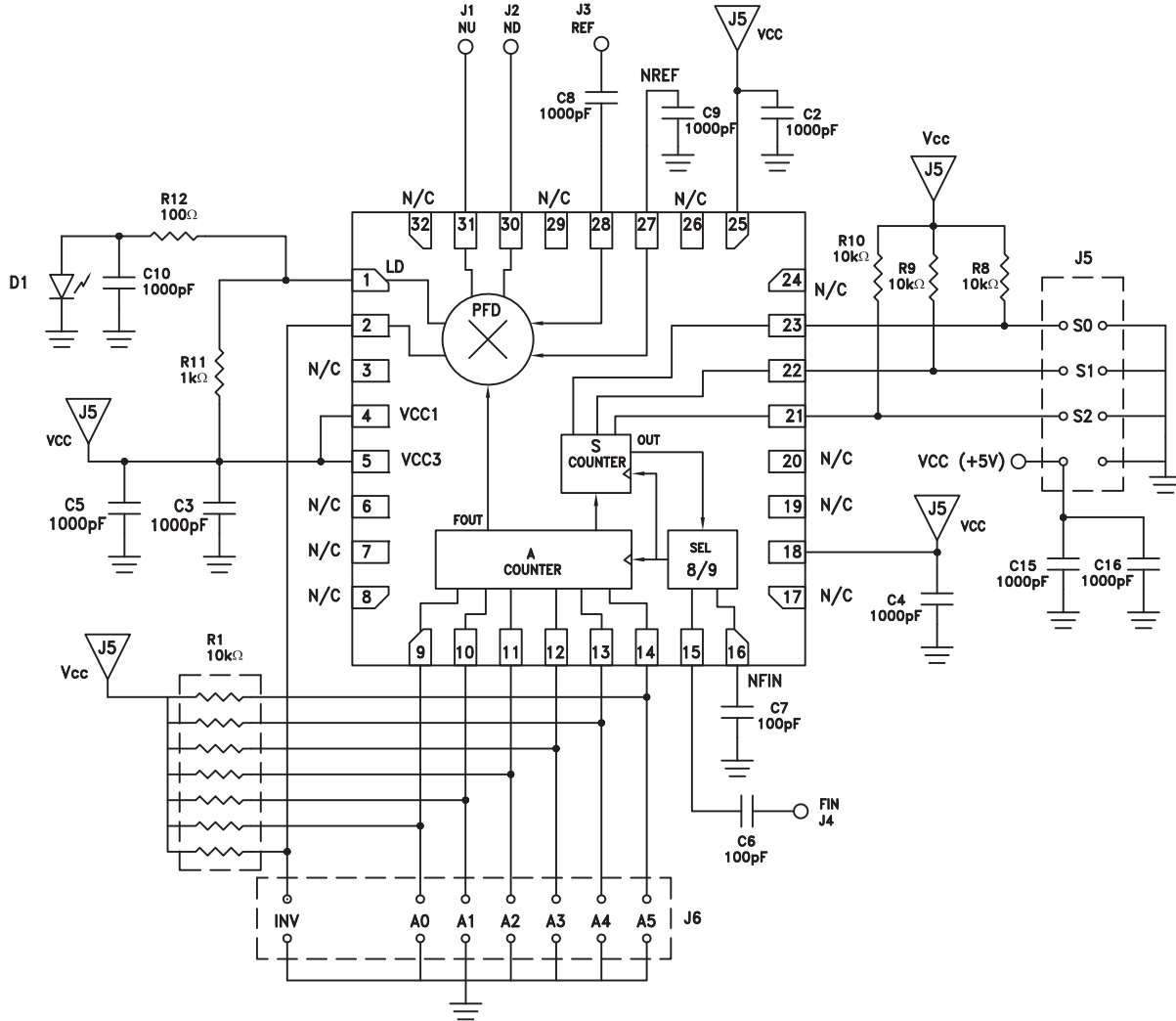
Division Ratio N	A Counter Decimal Set	Swallow S Decimal Set	(LSB) A0	A1	A2	A3	A4	A5	(LSB) S0	S1	S2
16	1	0	1	0	0	0	0	0	0	0	0
17	1	1	1	0	0	0	0	0	1	0	0
18	1	2	1	0	0	0	0	0	0	1	0
24	2	0	0	1	0	0	0	0	0	0	0
25	2	1	0	1	0	0	0	0	1	0	0
26	2	2	0	1	0	0	0	0	0	1	0
27	2	3	0	1	0	0	0	0	1	1	0
32	3	0	1	1	0	0	0	0	0	0	0
33	3	1	1	1	0	0	0	0	1	0	0
34	3	2	1	1	0	0	0	0	0	1	0
35	3	3	1	1	0	0	0	0	1	1	0
36	3	4	1	1	0	0	0	0	0	0	1
40	4	0	0	0	1	0	0	0	0	0	0
41	4	1	0	0	1	0	0	0	1	0	0
42	4	2	0	0	1	0	0	0	0	1	0
43	4	3	0	0	1	0	0	0	1	1	0
44	4	4	0	0	1	0	0	0	0	0	1
45	4	5	0	0	1	0	0	0	1	0	1
48	5	0	1	0	1	0	0	0	0	0	0
49	5	1	1	0	1	0	0	0	1	0	0
50	5	2	1	0	1	0	0	0	0	1	0
51	5	3	1	0	1	0	0	0	1	1	0
52	5	4	1	0	1	0	0	0	0	0	1
53	5	5	1	0	1	0	0	0	1	0	1
54	5	6	1	0	1	0	0	0	0	1	1

* Choose values of R2 & R4 between 4.3 and 20 Ohms for best noise performance.



**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**

Evaluation PCB Circuit



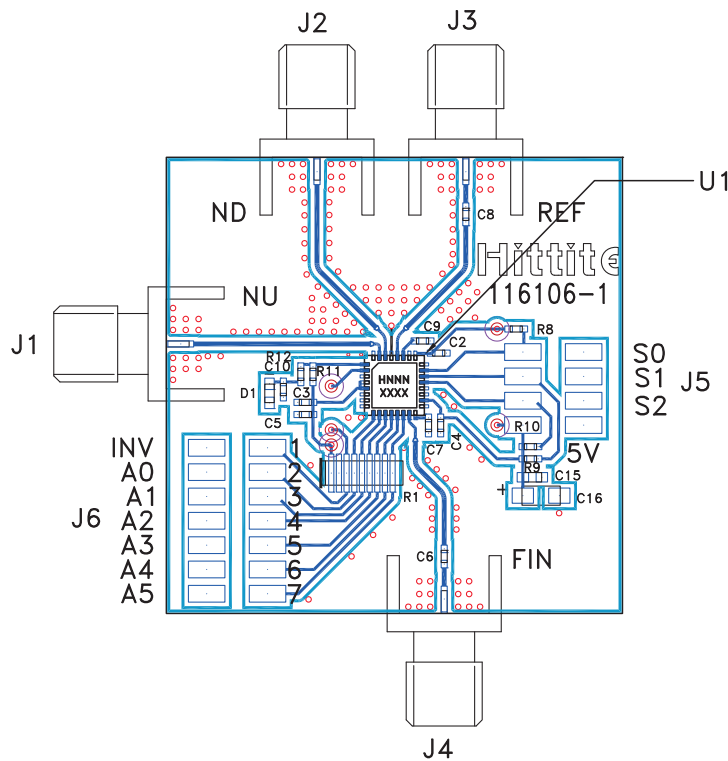
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**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

**List of Materials for
Evaluation PCB 116108 [1]**

Item	Description
J1 - J4	PC Mount SMA RF Connector
J5 - J6	2mm DC Header
C1 - C5, C8 - C10	1000 pF Capacitor, 0402 Pkg.
C6 - C7	100 pF Capacitor, 0402 Pkg.
C15	1000 pF Capacitor, 0603 Pkg.
C16	4.7 μF Tantalum Capacitor Case A
D	LED Green, 0603 Pkg., +5V
R1	10k Ohm, Resistor, Array
R8, R10	10k Ohm, Resistor, 0402 Pkg.
R11	1k Ohm, Resistor, 0402 Pkg.
R12	100 Ohm, Resistor, 0402 Pkg.
U1	HMC699LP5(E) Synthesizer
PCB [2]	116106 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

**Evaluation PCB Truth Table
(see Programming Truth Table)**

Note: 0 = Jumper Installed.
1 = Jumper Not Installed.

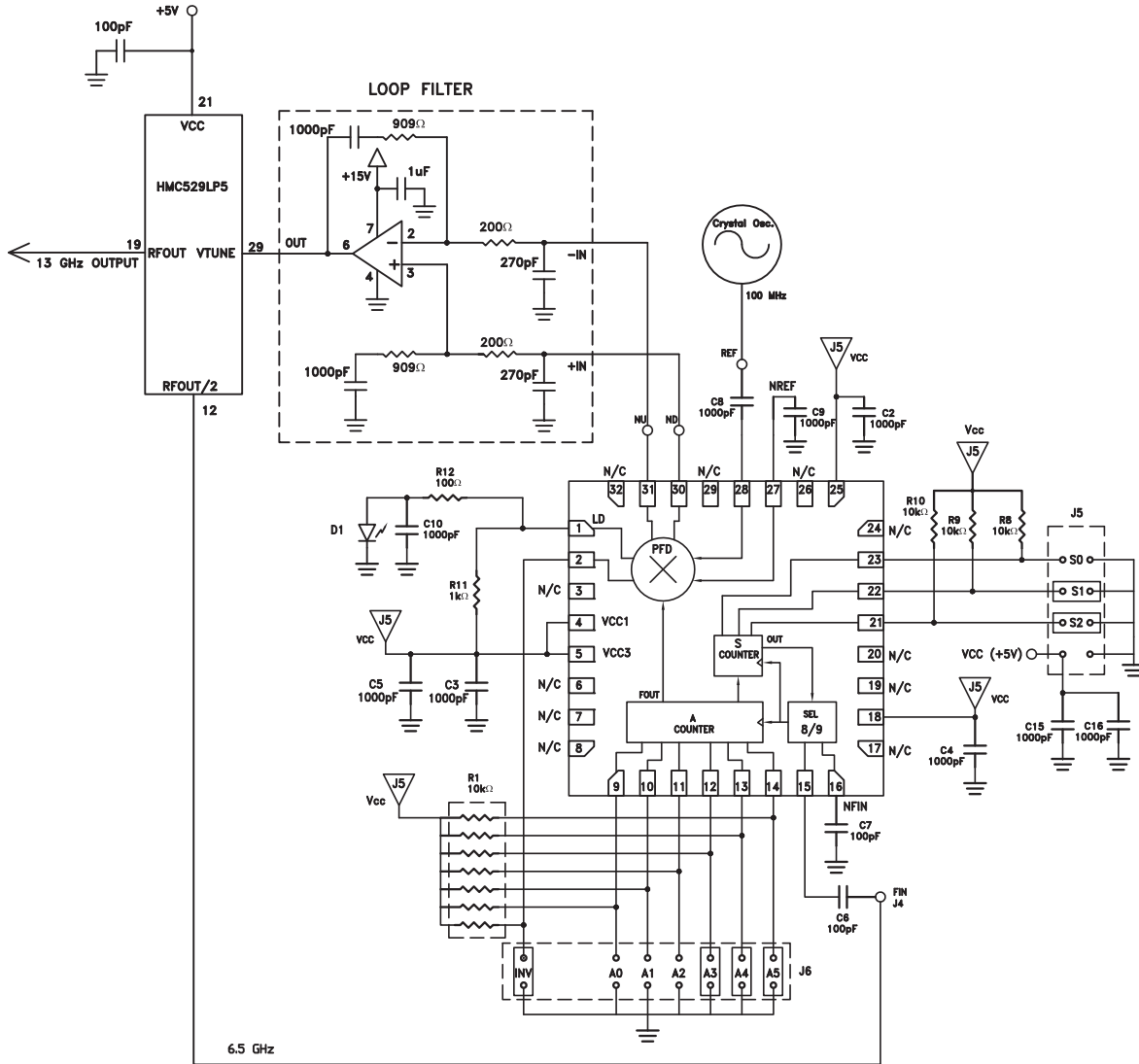
Note: The evaluation PCB for the HMC699LP5(E) contains 10 kOhm pull up resistors for each of the control inputs A0 through A5 and S0 through S2. Programming the 489 distinct division ratios consists of installing or removing jumpers A0 through A5 and S0 through S2.



**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**

Typical PLL Application Circuit using HMC699LP5

PLL application shown for a 13 GHz Fout. Contact HMC to discuss your specific application.



6

PLL - INTEGER-N SYNTHESIZER - SMT

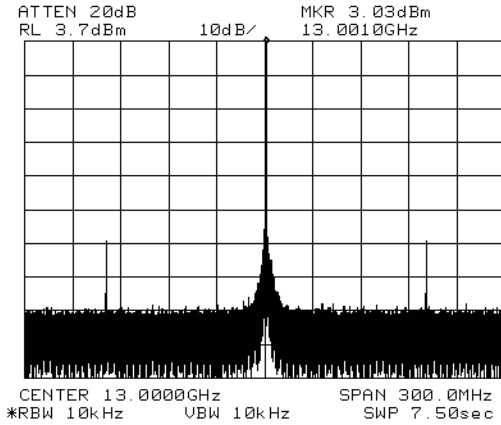
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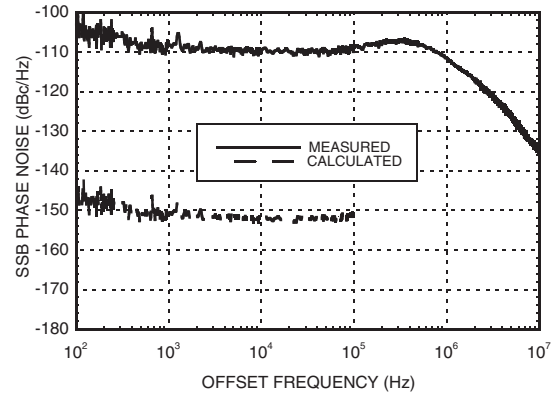


**7 GHz INTEGER N SYNTHESIZER
CONTINUOUS (N = 56 - 519), NON-CONTINUOUS (N = 16 - 54)**

**Typical Application
Showing Spurious Performance**



**Typical Application
13 GHz Measured Phase Noise [1]**



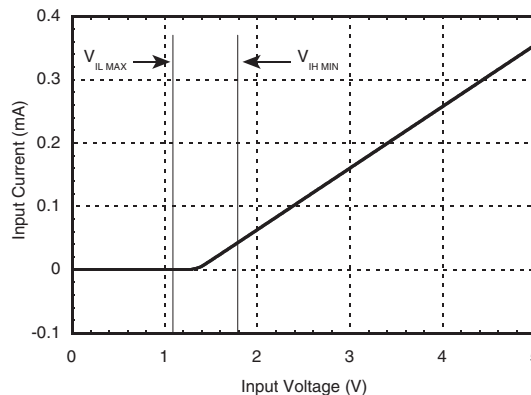
[1] Phase Noise Floor remains constant beyond 100 kHz offset frequency. Measured phase noise using Agilent 5500 with 2 unit measurement technique and corresponding calculated phase noise floor.

CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 1 μ A.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 50 μ A.

Input IV characteristics for the logic inputs (A0 - A5 and S0 - S2) are shown below:



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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.